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ASK/FSK Single Conversion Receiver

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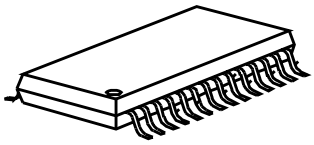
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Product Info

General Description

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for the frequency band 300 to 340 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

Package



Features

- Low supply current (Is = 6.4 mA typ. in FSK mode, Is = 5.6 mA typ. in ASK mode)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (50nA typ.)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- ASK sensitivity better than -110 dBm over specified temperature range (- 40 to +105°C)
- Selectable frequency ranges 300-320 MHz and 300-340 MHz
- Limiter with RSSI generation, operating at 10.7MHz
- Selectable reference frequency
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold
- FSK sensitivity better than -102 dBm over specified temperature range (- 40 to +105°C)

Applications

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

Ordering Information

Type	Ordering Code	Package
TDA 5221	Q67037-A1147	P-TSSOP-28-1
samples available		

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2 Product Description

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2.1 Overview

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for receive frequencies between 300 and 340 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

2.2 Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

2.3 Features

- Low supply current (I_S = 6.4 mA typ.FSK mode, 5.6 mA typ. ASK mode)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (50nA typ.)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- RF input sensitivity ASK -113dBm typ. at 25°C, better than -110dBm over complete specified operating temperature range (-40 to +105°C)
- RF input sensitivity FSK -105dBm typ. at 25°C, better than -102dBm over complete specified operating temperature range (-40 to +105°C)
- Receive frequency range between 310 and 340 MHz
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

2.4 Package Outlines

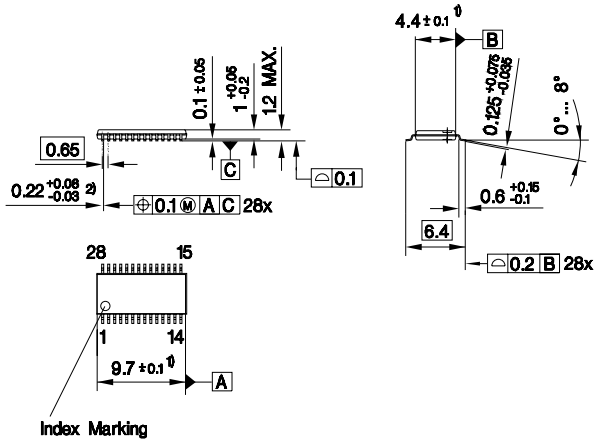


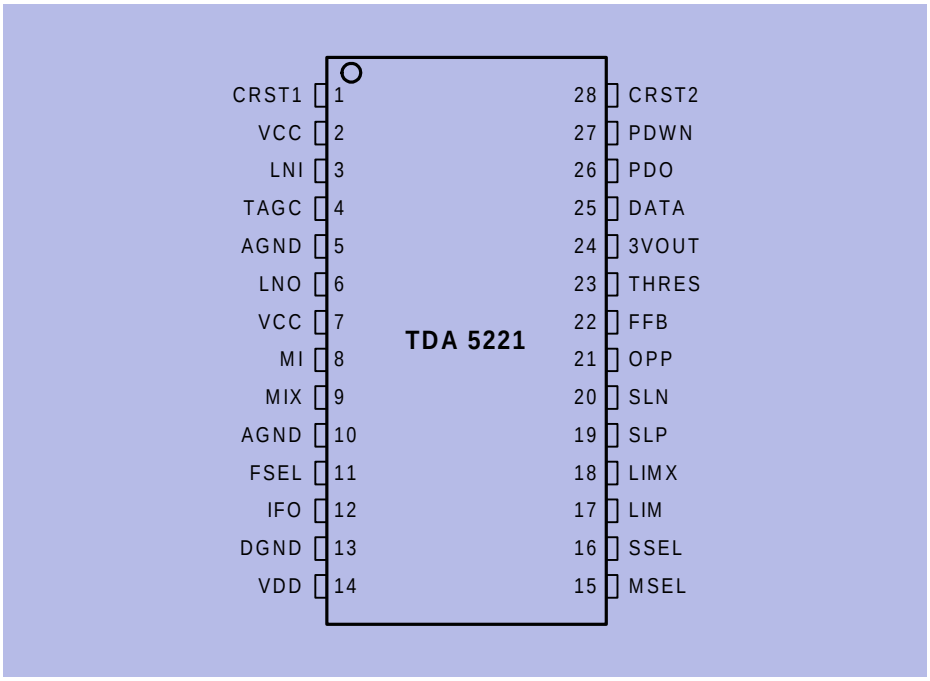
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3 Functional Description

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3.1 Pin Configuration



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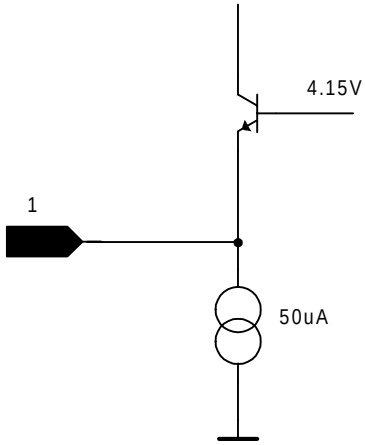
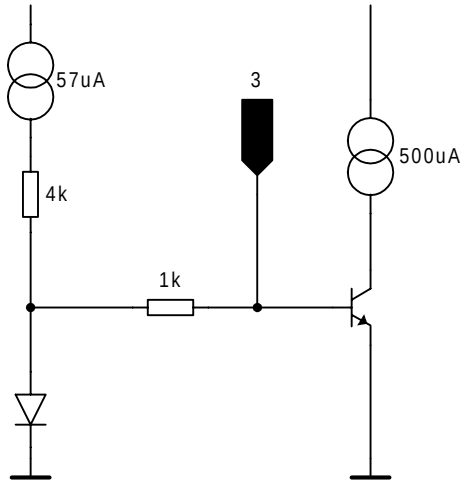
Figure 3-1 IC Pin Configuration

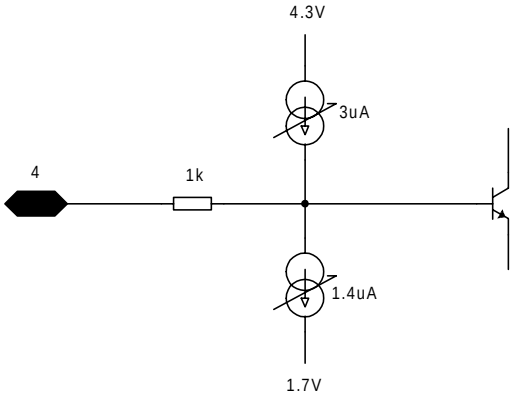
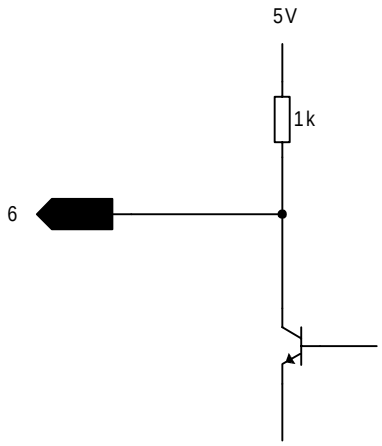
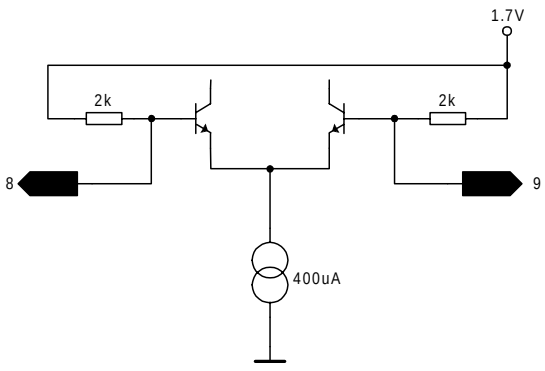
3.2 Pin Definition and Function

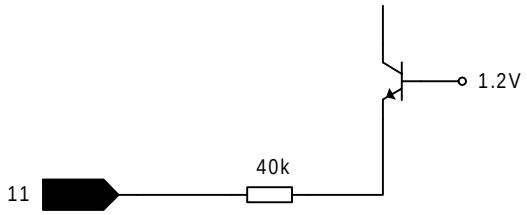
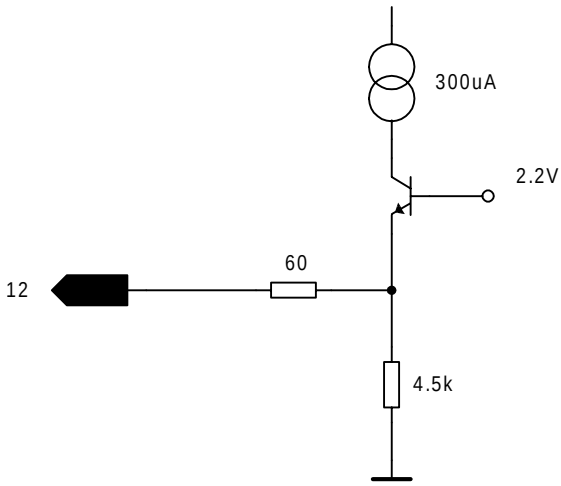
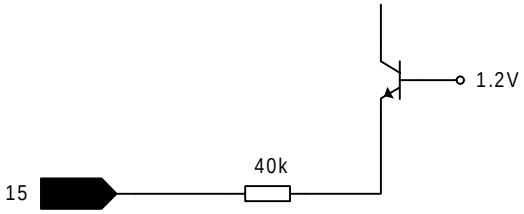
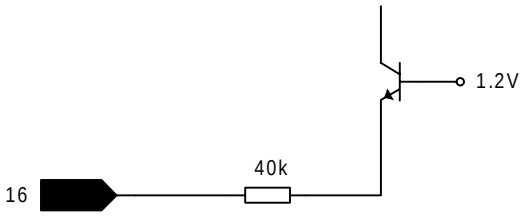
In the subsequent table the internal circuits connected to the pins of the device are shown. ESD-protection circuits are omitted to ease reading.

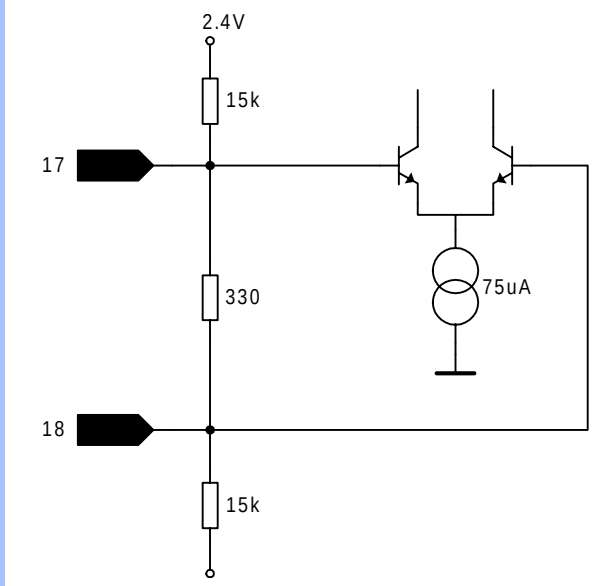
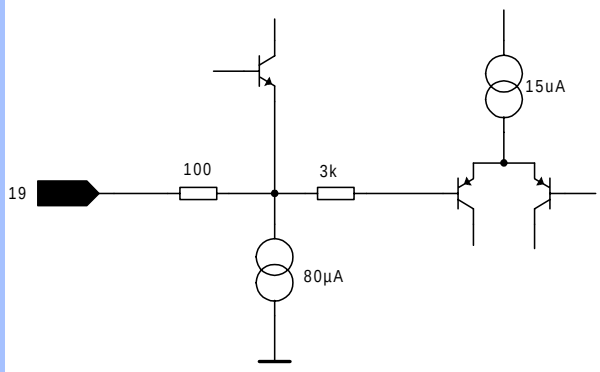
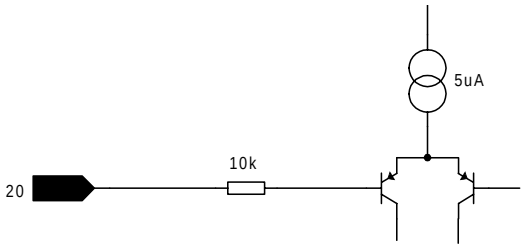
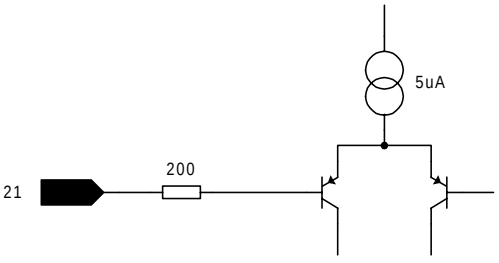
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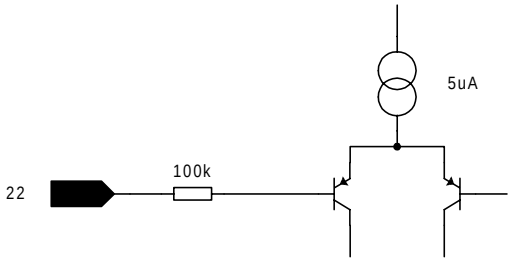
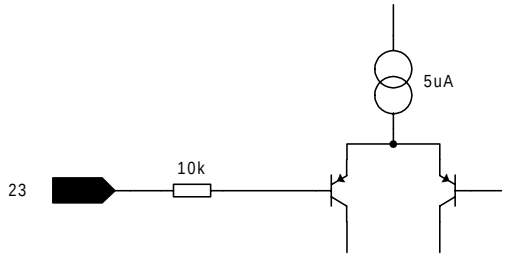
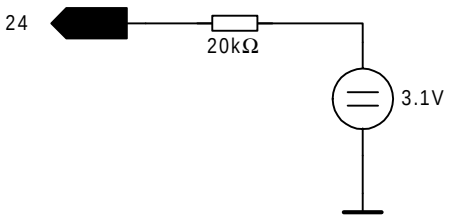
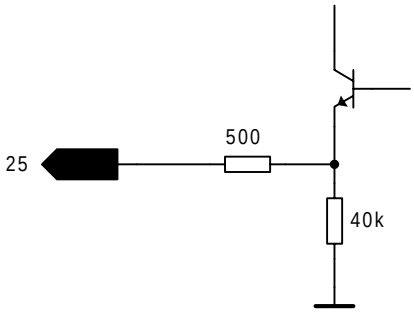
Table 3-1 Pin Definition and Function

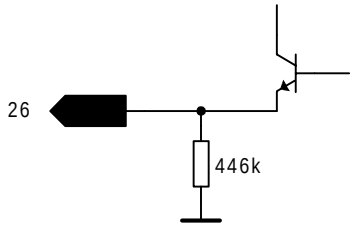
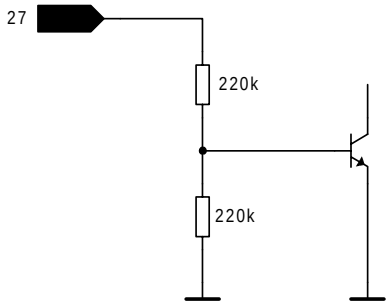
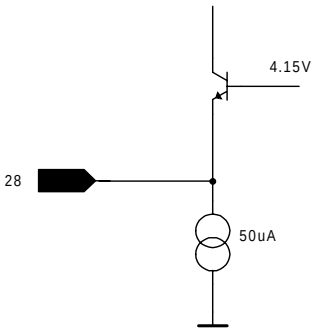
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	CRST1		External Crystal Connector 1
2	VCC		5V Supply
3	LNI		LNA Input

4	TAGC		AGC Time Constant Control
5	AGND		Analogue Ground Return
6	LNO		LNA Output
7	VCC		5V Supply
8	MI		Mixer Input
9	MIX		Complementary Mixer Input
10	AGND		Analogue Ground Return

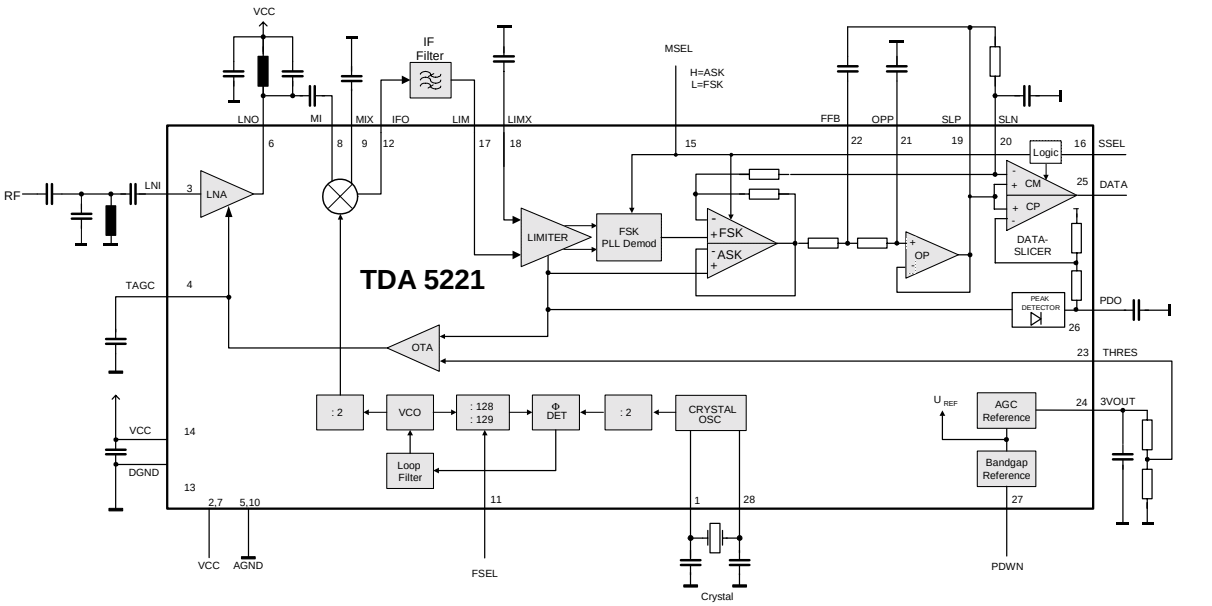
11	FSEL		Frequency Selector
12	IFO		10.7 MHz IF Mixer Output
13	DGND		Digital Ground Return
14	VDD		5V Supply (PLL Counter Circuitry)
15	MSEL		ASK/FSK Modulation Format Selector
16	SSEL		Data-Slicer Reference-Level Selector

17	LIM		Limiter Input
18	LIMX		Complementary Limiter Input
19	SLP		Data Slicer Positive Input
20	SLN		Data Slicer Negative Input
21	OPP		OpAmp Noninverting Input

22	FFB		Data Filter Feedback Pin
23	THRES		AGC Threshold Input
24	3VOUT		3V Reference Output
25	DATA		Data Output

26	PDO		Peak Detector Output
27	PDWN		Power Down Input
28	CRST2		External Crystal Connector 2

3.3 Functional Block Diagram



Functional_diagram_5221.wmf

Figure 3-2 Main Block Diagram

3.4 Functional Blocks

3.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pins 8 and 9). The noise figure of the LNA is approximately 3dB, the current consumption is 500µA. The gain can be reduced by approximately 18dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin as described in Section 4.1. The time constant of the AGC action can be determined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operat-

ing case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in Section 4.1.

3.4.2 Mixer

The Double Balanced Mixer downconverts the input frequency (RF) in the range of 310-350MHz to the intermediate frequency (IF) at 10.7MHz with a voltage gain of approximately 21dB by utilising either high- or low-side injection of the local oscillator signal. In case the mixer is interfaced only single-ended, the unused mixer input has to be tied to ground via a capacitor. The mixer is followed by a low pass filter with a corner frequency of 20MHz in order to suppress RF signals to appear at the IF output (**IFO** pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330Ω to facilitate interfacing the pin directly to a standard 10.7MHz ceramic filter without additional matching circuitry.

3.4.3 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. The **FSEL** pin (Pin11) has to be left open. The tuning range of the VCO was designed to guarantee over production spread and the specified temperature range a receive frequency range between 300 and 340 MHz depending on whether high- or low-side injection of the local oscillator is used. The oscillator signal is fed both to the synthesiser divider chain and to a divider that is dividing the signal by 2 before it is applied to the downconverting mixer. Local oscillator high side injection has to be used for receive frequencies between approximately 300 and 320 MHz, low side injection for receive frequencies between 320 and 340MHz - see also Section 4.4..

3.4.4 Crystal Oscillator

The calculation of the value of the necessary quartz load capacitance is shown in Section 4.3, the quartz frequency calculation is explained in Section 4.4.

3.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80 dB that has a bandpass-characteristic centred around 10.7 MHz. It has a typical input impedance of 330 Ω to allow for easy interfacing to a 10.7 MHz ceramic IF filter. The limiter circuit also acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is

directly proportional to the input signal level as can be seen in Figure 4-2. This signal is used to demodulate ASK-modulated receive signals in the subsequent baseband circuitry. The RSSI output is applied to the modulation format switch, to the Peak Detector input and to the AGC circuitry.

In order to demodulate ASK signals the MSEL pin has to be in its ‘High‘-state as described in the next chapter.

3.4.6 FSK Demodulator

To demodulate frequency shift keyed (FSK) signals a PLL circuit is used that is contained fully on chip. The Limiter output differential signal is fed to the linear phase detector as is the output of the 10.7 MHz center frequency VCO. The demodulator gain is typically 140µV/kHz. The passive loop filter output that is comprised fully on chip is fed to both the VCO and the modulation format switch described in more detail below. This signal is representing the demodulated signal with low frequencies applied to the demodulator demodulated to logic ones and high frequencies demodulated to logic zeroes. However this is only valid in case the local oscillator is low-side injected to the mixer which is applicable to receive frequencies above 330MHz (e.g. 345MHz). In case of receive frequencies below 330MHz (e.g.315MHz) high frequencies are demodulated as logical ones due to a sign inversion in the downconversion mixing process. See also Section 4.4.

The modulation format switch is actually a switchable amplifier with an AC gain of 11 that is controlled by the **MSEL** pin (Pin 15) as shown in the following table. This gain was chosen to facilitate detection in the subsequent circuits. The DC gain is 1 in order not to saturate the subsequent Data Filter wih the DC offset produced by the demodulator in case of large frequency offsets of the IF signal. The resulting frequency characteristic and details on the principle of operation of the switch are described in Section 4.6.

Table 3-2 MSEL Pin Operating States

MSEL	Modulation Format
Open	ASK
Shorted to ground	FSK

The demodulator circuit is switched off in case of reception of ASK signals.

3.4.7 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100kHz used as a voltage follower and two 100kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in Section 4.2.

3.4.8 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of up to 100kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for subsequent circuits. A self-adjusting slicer-threshold on pin 20 its generated by a RC-term. In ASK-mode alternatively a scaled value of the voltage at the PDO-output (approx. 87%) can be used as the slicer-threshold. The data slicer threshold generation alternatives are described in more detail in Section 4.5.

3.4.9 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. A capacitor is necessary. The input is connected to the output of the RSSI-output of the Limiter, the output is connected to the **PDO** pin (Pin 26). This output can be used as an indicator for the received signal strength to use in wake-up circuits and as a reference for the data slicer in ASK mode. Note that the RSSI level is also output in case of FSK mode.

3.4.10 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50nA.

Table 3-3 PDWN Pin Operating States

PDWN	Operating State
Open or tied to ground	Powerdown Mode
Tied to Vs	Receiver On

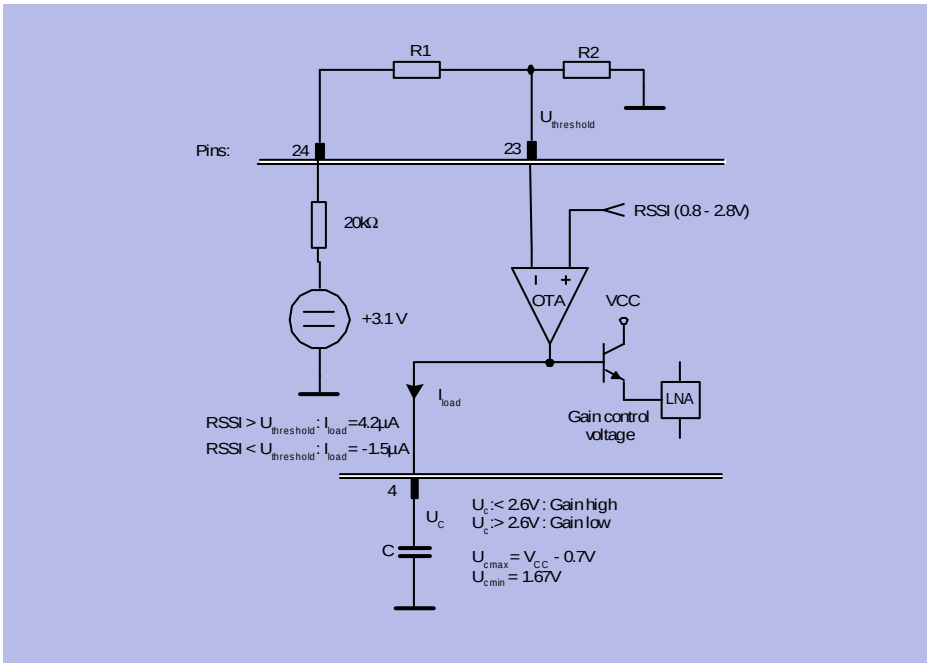
4 Applications

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4.1 Choice of LNA Threshold Voltage and Time Constant

In the following figure the internal circuitry of the LNA automatic gain control is shown.



LNA_autom.wmf

Figure 4-1 LNA Automatic Gain Control Circuitry

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage U_{thres}. As shown in the following figure the threshold voltage can have any value between approximately 0.8 and 2.8V to provide a switching point within the receive signal dynamic range.

This voltage U_{thres} is applied to the **THRES** pin (Pin 23) The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin. If the RSSI level generated by the Limiter is higher than U_{thres}, the OTA generates a positive current I_{load}. This yields a voltage rise on the **TAGC** pin (Pin 4). Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.

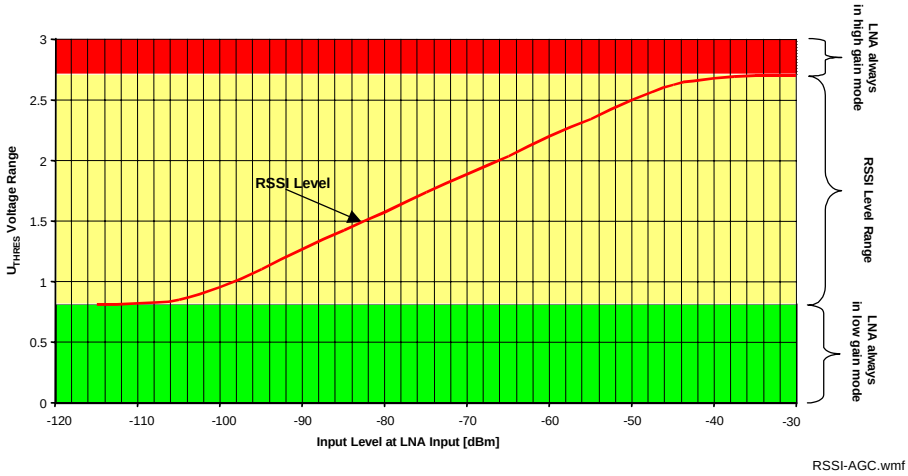


Figure 4-2 RSSI Level and Permissive AGC Threshold Levels

The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in the accompanying Application Note, a threshold voltage level of 1.8V is apparently a viable choice. It should be noted that the output of the **3VOUT** pin is capable of driving up to 50µA, but that the **THRES** pin input current is only in the region of 40nA. As the current drawn out of the **3VOUT** pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. The sum of R1 and R2 has to be 600kΩ in order to yield 3V at the **3VOUT** pin. R1 can thus be chosen as 240kΩ, R2 as 360kΩ to yield an overall **3VOUT** output current of 5µA[1] and a threshold voltage of 1.8V

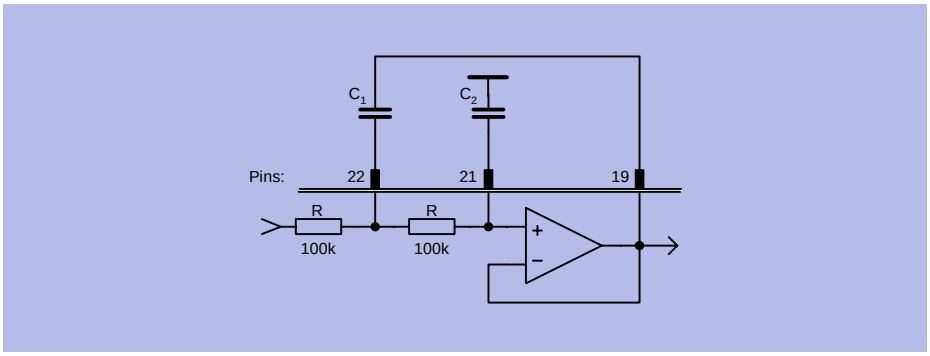
Note: If the LNA gain shall be kept in either high or low gain mode this has to be accomplished by tying the **THRES** pin to a fixed voltage. In order to achieve high gain mode operation, a voltage higher than 2.8V shall be applied to the **THRES** pin, such as a short to the **3VOLT** pin. In order to achieve low gain mode operation a voltage lower than 0.7V shall be applied to the **THRES**, such as a short to ground.

As stated above the capacitor connected to the **TAGC** pin is generating the gain control voltage of the LNA due to the charging and discharging currents of the OTA and thus is also responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Infineon the capacitor value should be greater than 47nF.

1. note the 20kΩ resistor in series with the 3.1V internal voltage source

4.2 Data Filter Design

Utilising the on-board voltage follower and the two 100kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pins 19 (SLP) and 22 (FFB) and to pin 21 (OPP) as depicted in the following figure and described in the following formulas[1].



Filter_Design.wmf

Figure 4-3 Data Filter Design

(1)(2)

$$C1 = \frac{2Q\sqrt{b}}{R2\Pi f_{3dB}} \qquad C2 = \frac{\sqrt{b}}{4QR\Pi f_{3dB}}$$

with

$$Q = \frac{\sqrt{b}}{a}$$ (3)the quality factor of the poles

where

in case of a Bessel filter a = 1.3617, b = 0.618

and thus Q = 0.577

and in case of a Butterworth filtera = 1.414, b = 1

and thus Q = 0.71

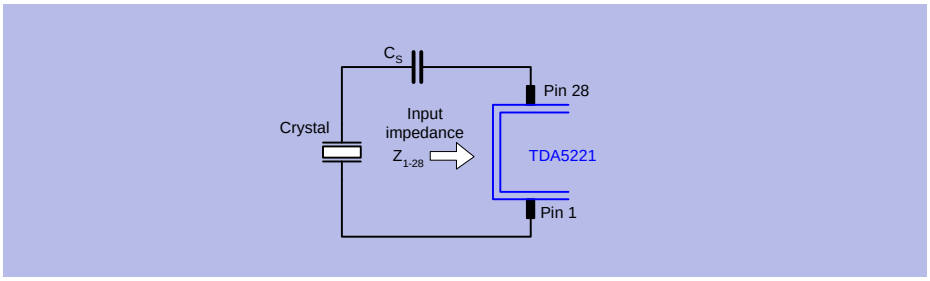
Example: Butterworth filter with f_{3dB} = 5kHz and R = 100kΩ:

C_1 = 450pF, C_2 = 225pF

1. taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999

4.3 Quartz Load Capacitance Calculation

The value of the capacitor necessary to achieve that the quartz oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in Section 5.1.3 and by the quartz specifications given by the quartz manufacturer.



Quartz_load_5221.wmf

Figure 4-4 Determination of Series Capacitance Value for the Quartz Oscillator

Crystal specified with load capacitance

$$C_S = \frac{1}{\frac{1}{C_l} + 2\pi f X_L}$$

with C_l the load capacitance (refer to the quartz crystal specification).

Example:

10.18 MHz: C_L = 12 pF X_L=870 Ω C_S = 7.2 pF

This value may be obtained by putting two capacitors in series to the quartz, such as 18pF and 22pF in the 5.1MHz case and 18pF and 12pF in the 10.2MHz case.

4.4 Quartz Frequency Calculation

As described in Section 3.4.3 the operating range of the on-chip VCO is wide enough to guarantee a receive frequency range between 300 and 340MHz. The VCO signal is divided by 2 before applied to the mixer . This local oscillator signal can be used to downconvert the RF signals both with high- or low-side injection at the mixer. High-side injection of the local oscillator has to be used for receive frequencies between 300 and 320 MHz. In this case the local oscillator frequency is calculated by adding the IF frequency (10.7 MHz) to the RF frequency. In this case the higher frequency of a FSK-modulated signal is demodulated as a logical one (high).

Low-side injection has to be used for receive frequencies between 320 and 340 MHz. The local oscillator frequency is calculated by subtracting the IF frequency (10.7 MHz) from the RF frequency then. Please note that in this case sign-inversion occurs and the higher frequency of a FSK-modulated signal is demodulated as a logical zero (low). The overall division ratios in the PLL are 32 or 32.25 depending on whether the FSEL-pin is left open or tied to ground.

Therefore the quartz frequency may be calculated by using the following formula:

$$f_{QU} = (f_{RF} \pm 10.7) / r$$

with f_{RF} receive frequency

f_{LO} local oscillator (PLL) frequency ($f_{RF} \pm 10.7$)

f_{QU} quartz oscillator frequency

r ratio of local oscillator (PLL) frequency and quartz frequency as shown in the subsequent table

Table 4-1 PLL Division Ratio Dependence on States of CSEL

FSEL	Ratio r = (f_{LO}/f_{QU})
High	32
Low	32.25

This yields the following examples:

FSEL is ‘Low‘:

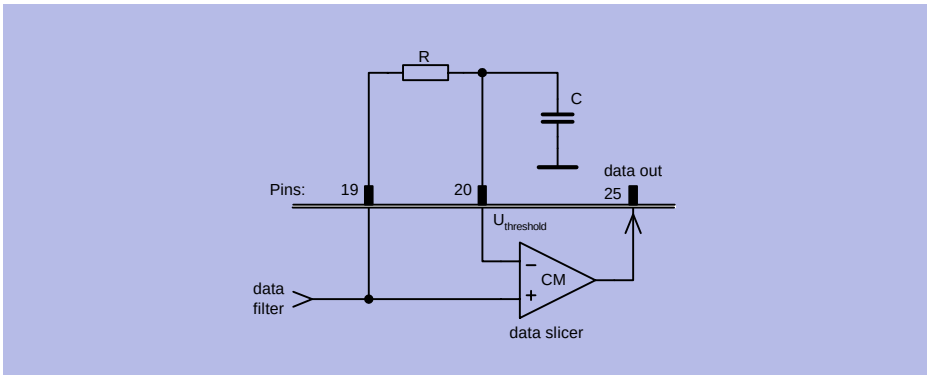
$$f_{QU} = (318.55MHz + 10.7MHz) / 32.25 = 10.209375MHz$$

FSEL is ‘High‘:

$$f_{QU} = (316MHz + 10.7MHz) / 32 = 10.209375\,MHz$$

4.5 Data Slicer Threshold Generation

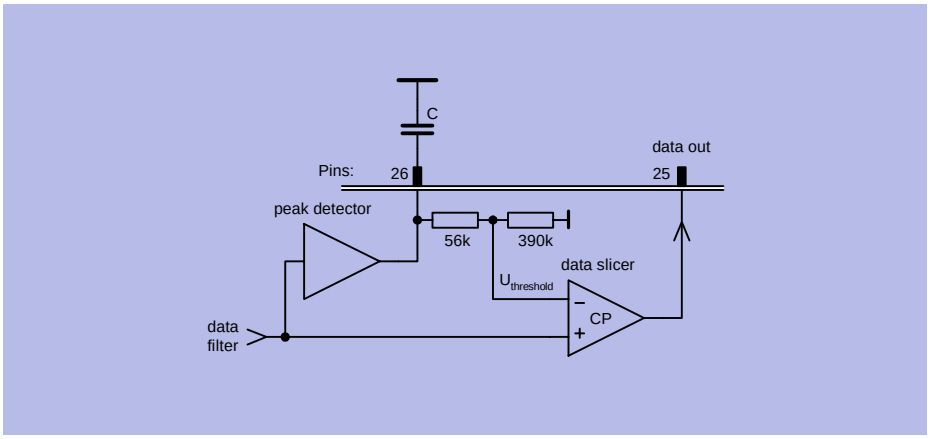
The threshold of the data slicer can be generated using an external R-C integrator as shown in Figure 4-5. The cut-off frequency of the R-C integrator has to be lower than the lowest frequency appearing in the data signal. In order to keep distortion low, the minimum value for R is 20kΩ.



Data_slice1.wmf

Figure 4-5 Data Slicer Threshold Generation with External R-C Integrator

In case of ASK operation another possibility for threshold generation is to use the peak detector in connection with an internal resistive divider and one capacitor as shown in the following figure. The component values are depending on the coding scheme and the protocol used.



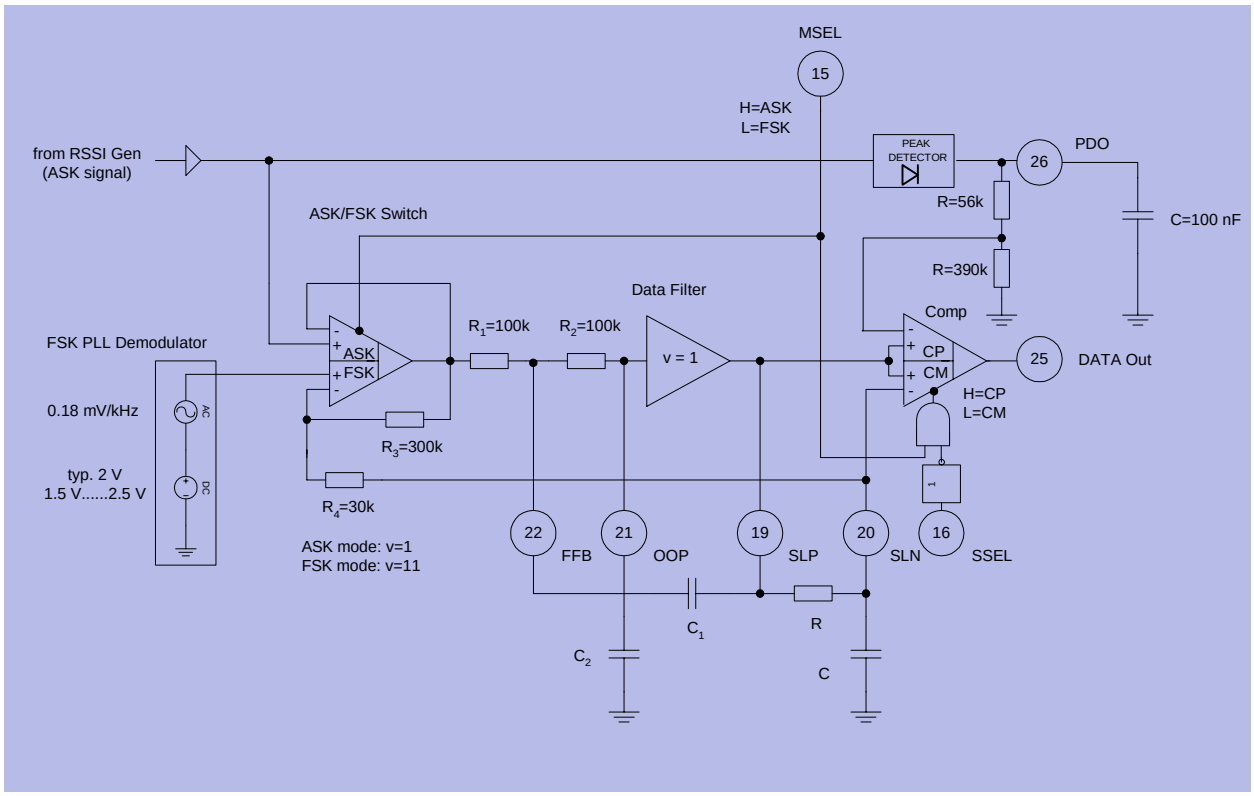
Data_slice2.wmf

Figure 4-6 Data Slicer Threshold Generation Utilising the Peak Detector

4.6 ASK/FSK Datapatch Functional Description

The TDA5221 is containing an ASK/FSK switch which can be controlled via Pin 15 (MSEL). This switch is actually consisting of 2 operational amplifiers that are having a gain of 1 in case of the ASK amplifier and a gain of 11 in case of the FSK amplifier in order to achieve an appropriate demodulation gain characteristic. In order to compensate for the DC-offset generated especially in case of the FSK PLL demodulator there is a feedback connection between the threshold voltage of the bit slicer comparator (Pin 20) to the negative input of the FSK switch amplifier.

In ASK-mode alternatively to the voltage at Pin 20 (SLN) a value of approx. 87% of the peak-detector output-voltage at Pin 26 (PDO) can be used as the slicer-reference level. The selection between these modes is controlled by Pin 16 (SSEL). This is shown in the following figure.



ask_fsk_datapath.WMF

Figure 4-7 ASK/FSK mode datapath

4.6.1 FSK Mode

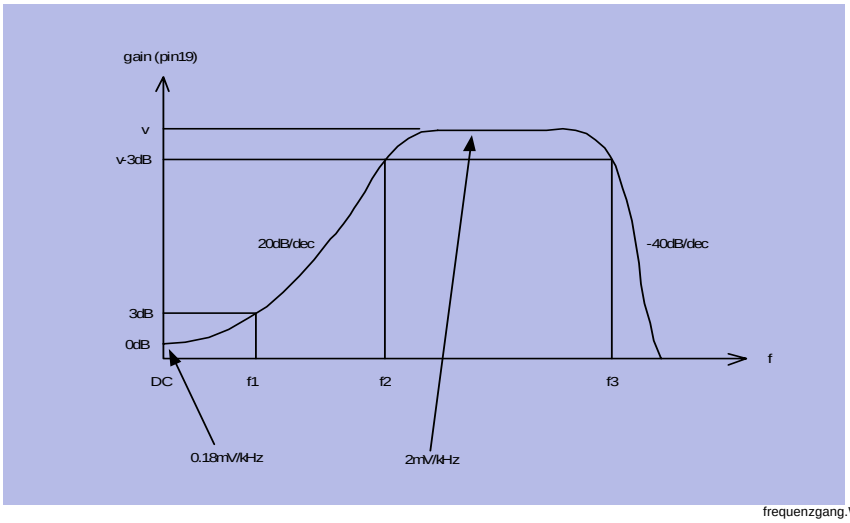
The FSK datapath has a bandpass characterisitc due to the feedback shown above (highpass) and the data filter (lowpass). The lower cutoff frequency f2 is determined by the external RC-combination. The upper cutoff frequency f3 is determined by the data filter bandwidth.

The demodulation gain of the FSK PLL demodulator is 140µV/kHz. This gain is increased by the gain v of the FSK switch, which is 11. Therefore the resulting dynamic gain of this circuit is 1.5mV/kHz within the bandpass. The gain for the DC content of FSK signal remains at 140µV/kHz. The cutoff frequencies of the bandpass have to be chosen such that the spectrum of the data signal is influenced in an acceptable amount.

In case that the user data is containing long sequences of logical zeroes the effect of the drift-off of the bit slicer threshold voltage can be lowered if the offset voltage inherent at the negative input of the slicer comparator (Pin20) is used. The comparator has no hysteresis built in.

This offset voltage is generated by the bias current of the negative input of the comparator (i.e. 20nA) running over the external resistor R. This voltage raises the voltage appearing at pin 20 (e.g. 1mV with R = 100kΩ). In order to obtain benefit of this asymmetrical offset for the demodulation of long zeros the lower of the two FSK frequencies should be chosen in the transmitter as the zero-symbol frequency.

In the following figure the shape of the above mentioned bandpass is shown.



frequenzgang.WMF

Figure 4-8 Frequency characterstic in case of FSK mode

The cutoff frequencies are calculated with the following formulas:

$$f_1 = \frac{1}{2\pi \frac{R \cdot 330k\Omega}{R + 330k\Omega} \cdot C}$$

$$f_2 = v \cdot f_1 = 11 \cdot f_1$$

$$f_3 = f_{3dB}$$

f_3 is the 3dB cutoff frequency of the data filter - see Section 4.2.

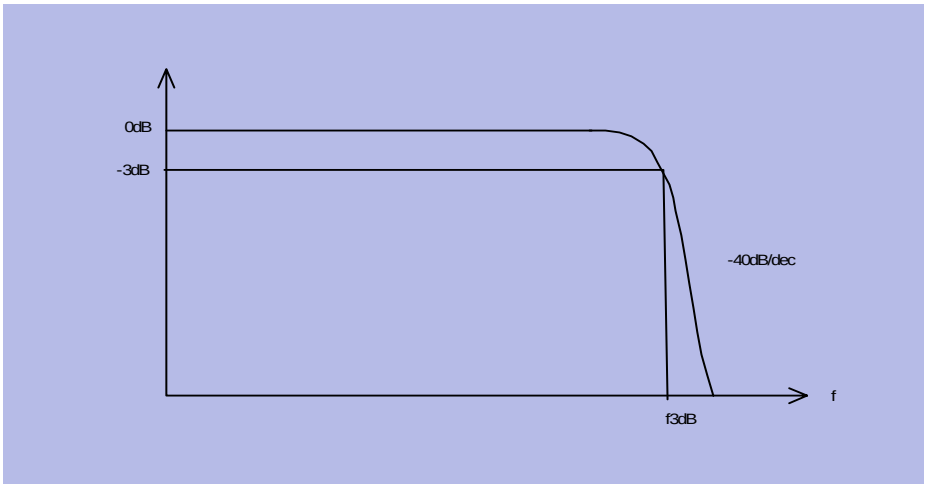
Example:

R = 100kΩ, C = 47nF

This leads tof_1 = 44Hz and f_2 = 485Hz

4.6.2 ASK Mode

In case the receiver is operated in ASK mode the datapath frequency charactersitic is dominated by the data filter alone, thus it is lowpass shaped.The cutoff frequency is determined by the external capacitors C12 and C14 and the internal 100k resistors as described in Section 4.2



freq_ask.WMF

Figure 4-9 Frequency charcteristic in case of ASK mode

4.7 Principle of the Precharge Circuit

In case the data slicer threshold shall be generated with an external RC network as described in Section 4.5 it is necessary to use large values for the capacitor C attached to the **SLN** pin (pin 20) in order to achieve long time constants. This results also from the fact that the choice of the value for R connected between the **SLP** and **SLN** pins (pins 19 and 20) is limited by the 330kΩ resistor appearing in parallel to R as can be seen in Figure 4-7. Apart from this a resistor value of 100kΩ leads to a voltage offset of 1mv at the comparator input as described in Section 4.6.1. The resulting startup time constant τ_1 can be calculated with:

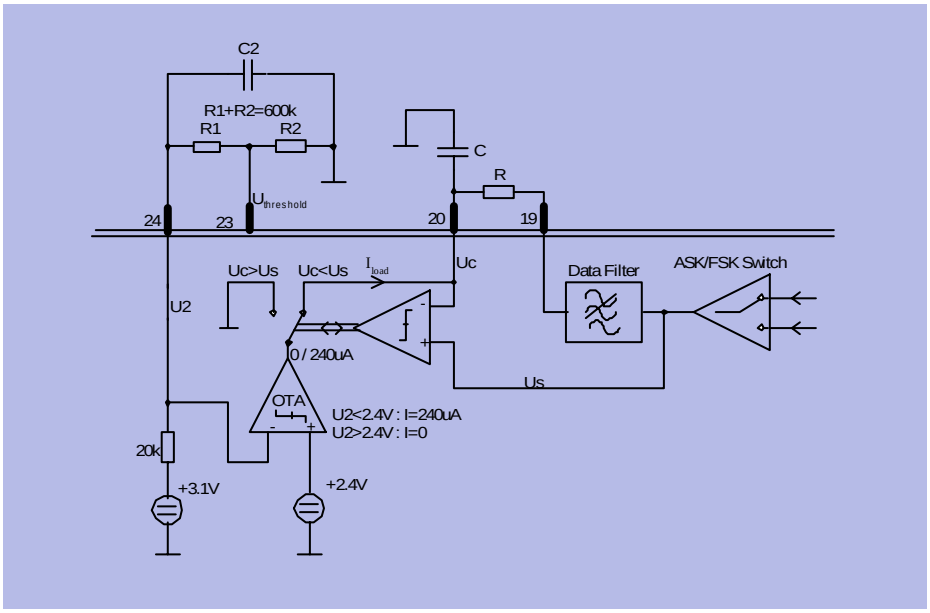
$$\tau_1 = (R \,//\, 330k\Omega) \cdot C$$

In case R is chosen to be 100kΩ and C is chosen as 47nF this leads to

$$\tau_1 = (100k\Omega \,//\, 330k\Omega) \cdot 47nF = 77k\Omega \cdot 47nF = 3.6ms$$

When the device is turned on this time constant dominates the time necessary for the device to be able to demodulate data properly. In the powerdown mode the capacitor is only discharged by leakage currents.

In order to reduce the turn-on time in the presence of large values of C a precharge circuit was included in the TDA5221 as shown in the following figure.



precharge.WMF

Figure 4-10 Principle of the precharge circuit

This circuit charges the capacitor C with an inrush current I_{load} of typically 220µA for a duration of T_2 until the voltage U_c appearing on the capacitor is equal to the voltage U_s at the input of the data filter. This voltage is limited to 2.5V. As soon as these voltages are equal or the duration T_2 is exceeded the precharge circuit is disabled.

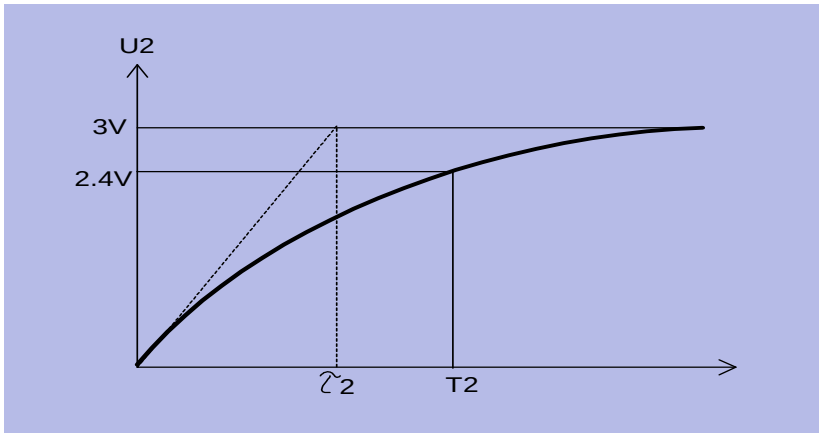
τ_2 is the time constant of the charging process of C which can be calculated as

$$\tau_2 \approx 20k\Omega \cdot C2$$

as the sum of R1 and R2 is sufficiently large and thus can be neglected. T2 can then be calculated according to the following formula:

$$T_2 = \tau_2 \ln\left(\frac{1}{1-\frac{2.4V}{3V}}\right) \approx \tau_2 \cdot 1.6$$

The voltage transient during the charging of C2 is shown in the following figure:

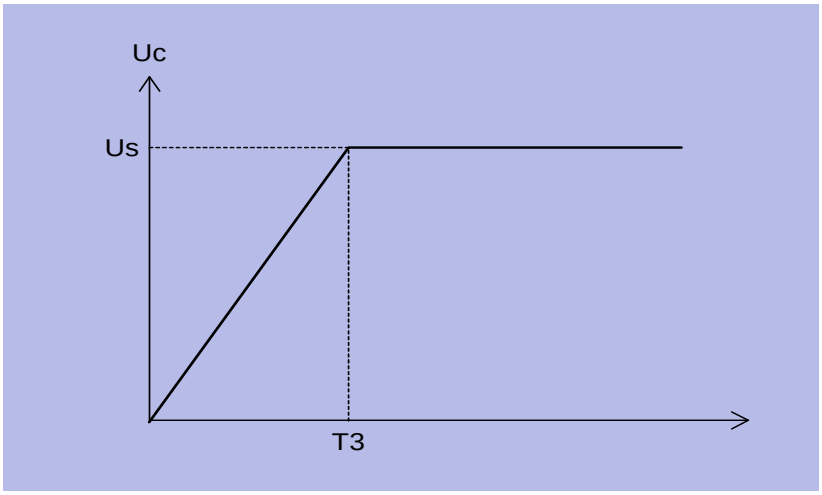


e-fkt1.WMF

Figure 4-11 Voltage appearing on C2 during precharging process

The voltage appearing on the capacitor C connected to pin 20 is shown in the following figure. It can be seen that due to the fact that it is charged by a constant current source it exhibits is a linear increase in voltage which is limited to U_{Smax} = 2.5V which is also the approximate operating point of the data filter input. The time constant appearing in this case can be denoted as T3, which can be calculated with

$$T3 = \frac{U_{Smax} \cdot C}{220\mu A} = \frac{2{,}5V}{220\mu A} \cdot C$$



e-Fkt2.WMF

Figure 4-12 Voltage transient on capacitor C attached to pin 20

As an example the choice of C2 = 22nF and C = 47nF yields

τ_2 = 0.44ms

T_2 = 0.71ms

T_3 = 0.53ms

This means that in this case the inrush current could flow for a duration of 0.64ms but stops already after 0.49ms when the U_{Smax} limit has been reached. T3 should always be chosen to be shorter than T2.

It has to be noted finally that during the turn-on duration T2 the overall device power consumption is increased by the 220µA needed to charge C.

The precharge circuit may be disabled if C2 is not equipped. This yields a T2 close to zero. Note that the sum of R4 and R5 has to be 600kΩ in order to produce 3V at the THRES pin as this voltage is internally used also as the reference for the FSK demodulator.

5 Reference

Contents of this Chapter

5.1 Electrical Data. 5-2

5.1 Electrical Data

5.1.1 Absolute Maximum Ratings



WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 5-1 Absolute Maximum Ratings, Ambient temperature T_{AMB}=-40°C ... + 105°C

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min	max		
1	Supply Voltage	V_s	-0.3	5.5	V	
2	Junction Temperature	T_j	-40	+150	°C	
3	Storage Temperature	T_s	-40	+125	°C	
4	Thermal Resistance	R_{thJA}		114	K/W	
5	ESD integrity, all pins excl. Pins 1,3, 6, 28 ESD integrity Pins 1,3,6,28	V_{ESD}		+2 +1.5	kV kV	HBM according to MIL STD 883D, method 3015.7

5.1.2 Operating Range

Within the operational range the IC operates as explained in the circuit description. The AC/DC characteristic limits are not guaranteed. Currents flowing into the device are denoted as positive currents and v.v.

Supply voltage: VCC = 4.5V .. 5.5V

Table 5-2 Operating Range, Ambient temperature T_{AMB}= -40°C ... + 105°C

#	Parameter	Symbol	Limit Values		Unit	Test Conditions	L	Item
			min	max				
1	Supply Current	I_{SF} I_{SA}	t.b.d. t.b.d.	t.b.d. t.b.d.	mA mA	f_{RF} = 315MHz, FSK Mode f_{RF} = 315MHz, ASK Mode		
2	Receiver Input Level ASK FSK, frequ. dev. ± 50kHz	RF_{in}	 -110 -102	 -13 -13	 dBm dBm	@ source impedance 50Ω, BER 2E-3, average power level, Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■	
3	LNI Input Frequency	f_{RF}	300	340	MHz			
4	MI/X Input Frequency	f_{MI}	300	340	MHz			
5	3dB IF Frequency Range ASK FSK	$f_{IF\ -3dB}$	 5 10.4	 23 11	MHz		■	
6	Powerdown Mode On	$PWDN_{ON}$	0	0.8	V			
7	Powerdown Mode Off	$PWDN_{OFF}$	2	V_S	V			
8	Gain Control Voltage, LNA high gain state	V_{THRES}	2.8	V_S	V			
9	Gain Control Voltage, LNA low gain state	V_{THRES}	0	0.7	V			

■ This value is guaranteed by design.

5.1.3 AC/DC Characteristics at T_{AMB} = 25°C

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production. Currents flowing into the device are denoted as positive currents and vice versa.

The device performance parameters marked with ■ were measured on an Infineon evaluation board as described in Section 5.2.

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
Supply									
Supply Current									
1	Supply current, standby mode	$I_{S\ PDWN}$		50	t.b.d.	nA	Pin 27 (PDWN) open or tied to 0 V		
2	Supply current, device operating in FSK mode	I_{SF}	t.b.d.	6.4	t.b.d.	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) tied to GND		
3	Supply current, device operating in ASK mode	I_{SA}	t.b.d.	5.6	t.b.d.	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) open		
LNA									
Signal Input LNI (PIN 3), V_{THRES} > 2.8V, high gain mode									
1	Average Power Level at BER = 2E-3 (Sensitivity)	RF_{in}		-113		dBm	Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■	
2	Average Power Level at BER = 2E-3 (Sensitivity) FSK	RF_{in}		-105		dBm	Manchester enc. datarate 4kBit, 280kHz IF Bandw., ± 50kHz pk. dev.	■	
3	Input impedance, f_{RF} = 315 MHz	$S_{11\ LNA}$		0.895 / -25.5 deg				■	
4	Input level @ 1dB C.P. f_{RF}=315 MHz	$P1dB_{LNA}$		-14		dBm		■	
5	Input 3rd order intercept point f_{RF} = 315 MHz	$IIP3_{LNA}$		-10		dBm	f_{in} = 315 & 317MHz	■	
6	LO signal feedthrough at antenna port	LO_{LNI}		-119		dBm		■	
Signal Output LNO (PIN 6), V_{THRES} > 2.8V, high gain mode									
1	Gain f_{RF} = 315 MHz	$S_{21\ LNA}$		1.577 / 150.3 deg				■	
2	Output impedance, f_{RF} = 315 MHz	$S_{22\ LNA}$		0.897 / -10.3 deg				■	

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
3	Voltage Gain Antenna to MI f_{RF} = 315 MHz	G_{AntMI}		21		dB		■	
4	Noise Figure	NF_{LNA}		2		dB	excluding matching network loss - see Appendix	■	
Signal Input LNI, V_{THRES} = GND, low gain mode									
1	Input impedance, f_{RF} = 315 MHz	$S_{11\ LNA}$		0.918 / -25.2 deg				■	
2	Input level @ 1dB C. P. f_{RF} = 315 MHz	$P1dB_{LNA}$		-7		dBm	matched input	■	
3	Input 3rd order intercept point f_{RF} = 315 MHz	$IIP3_{LNA}$		-13		dBm	f_{in} = 315 & 317MHz	■	
Signal Output LNO, V_{THRES} = GND, low gain mode									
1	Gain f_{RF} = 315 MHz	$S_{21\ LNA}$		0.193 / 153.7 deg				■	
2	Output impedance, f_{RF} = 315 MHz	$S_{22\ LNA}$		0.907 / -10.5 deg				■	
3	Voltage Gain Antenna to MI f_{RF} = 315 MHz	G_{AntMI}		2		dB		■	
Signal 3VOUT (PIN 24)									
1	Output voltage	V_{3VOUT}	2.9	3.1	3.3	V	3VOUT Pin open		
2	Current out	I_{3VOUT}	-3	-5	-10	µA	see Section 4.1		
Signal THRES (PIN 23)									
1	Input Voltage range	V_{THRES}	0		V_S	V	see Section 4.1		
2	LNA low gain mode	V_{THRES}	0		0.3	V			
3	LNA high gain mode	V_{THRES}	3.3		V_S	V	or shorted to VCC		
4	Current in	I_{THRES_in}		5		nA			
Signal TAGC (PIN 4)									
1	Current out, LNA low gain state	I_{TAGC_out}	-3.6	-4.2	-5	µA	RSSI > V_{THRES}		
2	Current in, LNA high gain state	I_{TAGC_in}	1	1.6	2.2	µA	RSSI < V_{THRES}		
MIXER									
Signal Input MI/MIX (PINS 8/9)									
1	Input impedance, f_{RF} = 315 MHz	$S_{11\ MIX}$		0.954 / -10.9 deg				■	
2	Input 3rd order intercept point	$IIP3_{MIX}$		-25		dBm		■	

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
Signal Output IFO (PIN 12)									
1	Output impedance	Z_{IFO}		330		Ω		■	
2	Conversion Voltage Gain f_{RF} = 315 MHz	G_{MIX}		21		dB		■	
3	Noise Figure, SSB (~DSB NF+3dB)	NF_{MIX}		13		dB		■	
4	RF to IF isolation	A_{RF-IF}		46		dB		■	
LIMITER									
Signal Input LIM/X (PINS 17/18)									
1	Input Impedance	Z_{LIM}	264	330	396	Ω		■	
2	RSSI dynamic range	DR_{RSSI}	60		80	dB			
3	RSSI linearity	LIN_{RSSI}		±1		dB		■	
4	Operating frequency (3dB points)	f_{LIM}	5	10.7	23	MHz		■	
DATA FILTER									
1	Useable bandwidth	$BW_{BB\ FILT}$			100	kHz		■	
2	RSSI Level at Data Filter Output SLP, RF_{IN}=-103dBm	$RSSI_{low}$	0.3		1	V	LNA in high gain mode		
3	RSSI Level at Data Filter Output SLP, RF_{IN}=-30dBm	$RSSI_{high}$	1.8		3	V	LNA in high gain mode		
SLICER									
Signal Output DATA (PIN 25)									
1	Maximum Datarate	DR_{max}			100	kBps	NRZ, 20pF capacitive loading	■	
2	LOW output voltage	V_{SLIC_L}	0		0.1	V			
3	HIGH output voltage	V_{SLIC_H}	V_S-1.3V	V_S-1V	V_S-0.7V	V			
Slicer, Negative Input (PIN 20)									
1	Precharge Current Out	I_{PCH_SLN}	-100	-220	-300	µA	see Section 4.7		

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
PEAK DETECTOR									
Signal Output PDO (PIN 26)									
1	Load current	I_{load}	-600	-950	-1300	µA			
2	Internal resistive load	R	t.b.d.	446	t.b.d.	kΩ			
CRYSTAL OSCILLATOR									
Signals CRSTL1, CRISTL 2, (PINS 1/28)									
1	Operating frequency	f_{CRSTL}	t.b.d.		11	MHz	fundamental mode, series resonance		
2	Input Impedance @ ~10MHz	$Z_{1\text{-}28}$		-700 + j 865		Ω		■	
3	Serial Capacity @ ~10MHz	C_{S10}=C1		7.2		pF			
ASK/FSK Signal Switch									
Signal MSEL (PIN 15)									
1	ASK Mode	V_{MSEL}	1.4		4	V	or open		
2	FSK Mode	V_{MSEL}	0		0.2	V	or tied to ground		
3	Input Bias Current MSEL	I_{MSEL}	t.b.d.	-11	t.b.d.	µA	MSEL tied to GND		
FSK DEMODULATOR									
1	Demodulation Gain	G_{FMDEM}	85	140	225	µV/ kHz			
2	Useable IF Bandwidth	BW_{IFPLL}	10.2	10.7	11.2	MHz			
POWER DOWN MODE									
Signal PDWN (PIN 27)									
1	Powerdown Mode On	$PWDN_{ON}$	0		0.8	V			
2	Powerdown Mode Off	$PWDN_{Off}$	2.8		V_S	V			
3	Input bias current PDWN	I_{PDWN}		19		µA	Power On Mode		
4	Start-up Time until valid IF signal is detected	T_{SU}			1	ms			
PLL DIVIDER									
Signal FSEL (PIN 11)									
1	Overal divison ratio 32	V_{FSEL}	1.4		4	V	or open		
2	Overal division ratio 32.25	V_{FSEL}	0		0.2	V	or tied to GND		
3	Input bias current FSEL	I_{FSEL}	t.b.d.	-11	t.b.d.	µA	FSEL tied to GND		

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
DATA-SLICER REFERENCE-LEVEL									
Signal SSEL (PIN 16), ASK-Mode									
1	Slicer-Reference is voltage at Pin 20 (SLN)	V_{SSEL}	1.4		4	V	or open		
2	Slicer-Reference is approx. 87% of the voltage at Pin 26 (PDO)	V_{SSEL}	0		0.2	V			
3	Input bias current SSEL	I_{SSEL}	-3	-5	-7	µA	SSEL tied to GND		

■ Measured only in lab.

5.1.4 AC/DC Characteristics at T_{AMB} = -40 to 105°C

Currents flowing into the device are denoted as positive currents and vice versa.

Table 5-4 AC/DC Characteristics with T_{AMB}= -40°C ... + 105°C, V_{VCC} = 4.5 ... 5.5 V

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
Supply									
Supply Current									
1	Supply current, standby mode	$I_{S\ PDWN}$		50	t.b.d.	nA	Pin 27 (PDWN) open or tied to 0 V		
2	Supply current, device operating in FSK mode	I_{SF}	t.b.d.	6.4	t.b.d.	mA	Pin 11 (FSEL) tied to GND, Pin 15 (MSEL) tied to GND		
3	Supply current, device operating in ASK mode	I_{SA}	t.b.d.	5.6	t.b.d.	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) open		
Signal 3VOUT (PIN 24)									
1	Output voltage	V_{3VOUT}	2.9	3.1	3.3	V	3VOUT Pin open		
2	Current out	I_{3VOUT}	-3	-5	-10	µA	see Section 4.1		
Signal THRES (PIN 23)									
1	Input Voltage range	V_{THRES}	0		V_S-1V	V	see Section 4.1		
2	LNA low gain mode	V_{THRES}	0		0.3	V			
3	LNA high gain mode	V_{THRES}	3		V_S	V	or shorted to Pin 24		
4	Current in	I_{THRES_in}		5		nA			
Signal TAGC (PIN 4)									
1	Current out, LNA low gain state	I_{TAGC_out}	-1	-4.2	-8	µA	RSSI > V_{THRES}		
2	Current in, LNA high gain state	V_{TAGC_in}	0.5	1.5	5	µA	RSSI < V_{THRES}		
MIXER									
1	Conversion Voltage Gain f_{RF} = 315 MHz	G_{MIX}		+19		dB			
LIMITER									
Signal Input LIM/X (PINS 17/18)									
1	RSSI dynamic range	DR_{RSSI}	60		80	dB			
2	RSSI Level at Data Filter Output SLP, RF_{IN}= -103dBm	$RSSI_{low}$	0.3		1	V	LNA in high gain mode		
3	RSSI Level at Data Filter Output SLP, RF_{IN}= -30dBm	$RSSI_{high}$	1.8		3	V	LNA in high gain mode		

Table 5-4 AC/DC Characteristics with T_{AMB}= -40°C ... + 105°C, V_{VCC} = 4.5 ... 5.5 V

	Parameter	Symbol	Limit Values			Unit	Test Conditions	L	Item
			min	typ	max				
DATA FILTER									
Slicer, Signal Output DATA (PIN 25)									
1	Maximum Datarate	DR_{max}			100	kBps	NRZ, 20pF capacitive loading	■	
2	LOW output voltage	V_{SLIC_L}	0		0.1	V			
3	HIGH output voltage	V_{SLIC_H}	V_S-1.5V	V_S-1V	V_S-0.5V	V			
Slicer, Negative Input (PIN 20)									
1	Precharge Current Out	I_{PCH_SLN}	-100	-220	-300	µA	see Section 4.7		
PEAK DETECTOR									
Signal Output PDO (PIN 26)									
1	Load current	I_{load}	-400	-850	-1400	µA			
2	Internal resistive load	R	t.b.d	446	t.b.d.	kΩ			
CRYSTAL OSCILLATOR									
Signals CRSTL1, CRSTL 2, (PINS 1/28)									
1	Operating frequency	f_{CRSTL}	t.b.d.		11	MHz	fundamental mode, series resonance		
ASK/FSK Signal Switch									
Signal MSEL (PIN 15)									
1	ASK Mode	V_{MSEL}	1.4		4	V	or open		
2	FSK Mode	V_{MSEL}	0		0.2	V			
3	Input bias current MSEL	I_{MSEL}	t.b.d.	-11	t.b.d.	µA	MSEL tied to GND		
FSK DEMODULATOR									
1	Demodulation Gain	G_{FMDEM}	105	140	245	µV/kHz			
2	Useable IF Bandwidth	BW_{IFPLL}	10.4	10.7	11	MHz			
POWER DOWN MODE									
Signal PDWN (PIN 27)									
1	Powerdown Mode On	$PWDN_{ON}$	0		0.8	V			
2	Powerdown Mode Off	$PWDN_{Off}$	2.8		V_S	V			
3	Start-up Time until valid signal is detected at IF	T_{SU}			1	ms			
PLL DIVIDER									
Signal FSEL (PIN 11)									
1	Overal divison ratio 32	V_{FSEL}	1.4		4	V	or open		
2	Overal division ratio 32.25	V_{FSEL}	0		0.2	V	or tied to GND		
3	Input bias current FSEL	I_{FSEL}	t.b.d.	-11	t.b.d.	µA	FSEL tied to GND		

DATA-SLICER REFERENCE-LEVEL

Signal SSEL (PIN 16), ASK-Mode									
1	Slicer-Reference is voltage at Pin 20 (SLN)	V_{SSEL}	1.4		4	V	or open		
2	Slicer-Reference is approx. 87% of the voltage at Pin 26 (PDO)	V_{SSEL}	0		0.2	V			
3	Input bias current SSEL	I_{SSEL}	-3	-5	-7	µA	SSEL tied to GND		