Semiconductor Corporation

CS4215

16-Bit Multimedia Audio Codec

Features

- Sample Frequencies from 4 kHz to 50 kHz
- 16-bit Linear, 8-bit Linear, μ-Law, or A-Law Audio Data Coding
- Programmable Gain for Analog Inputs
- Programmable Attenuation for Analog Outputs
- On-chip Oscillators
- +5V Power Supply
- Microphone and Line Level Analog Inputs
- Headphone, Speaker, and Line Outputs
- On-chip Anti-Aliasing/Smoothing Filters
- Serial Digital Interface

General Description

The CS4215 is an Mwave™ audio codec.

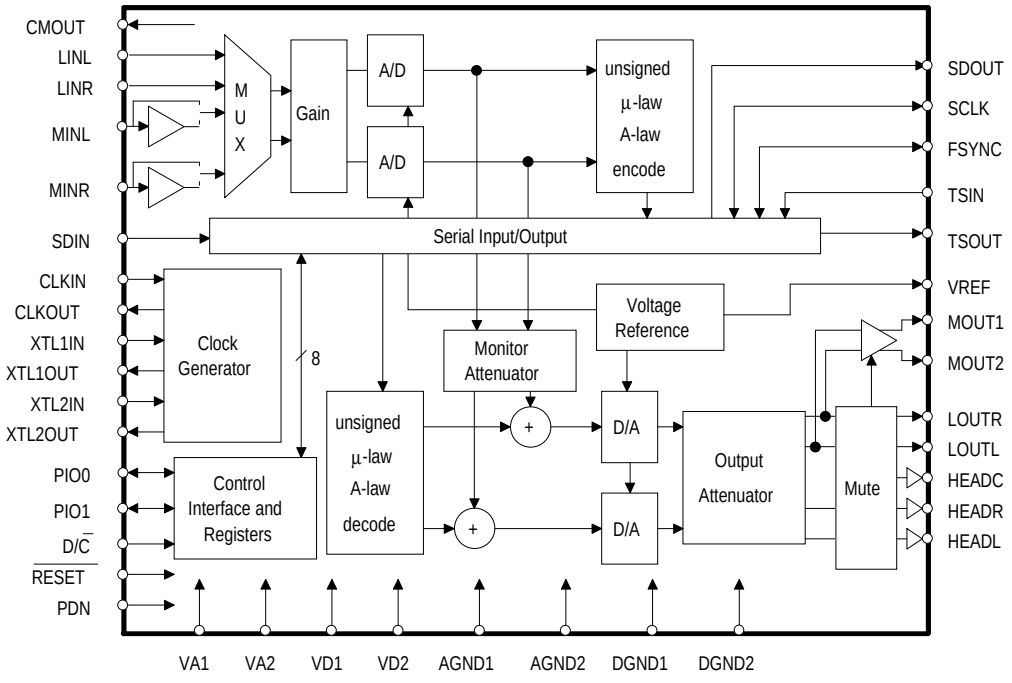
The CS4215 is a single-chip, stereo, CMOS multimedia codec that supports CD-quality music, FM radio-quality music, telephone-quality speech, and modems. The analog-to-digital and digital-to-analog converters are 64×oversampled delta-sigma converters with on-chip filters which adapt to the sample frequency selected.

The +5V only power requirement makes the CS4215 ideal for use in workstations and personal computers.

Integration of microphone and line level inputs, input and output gain setting, along with headphone and monitor speaker driver, results in a very small footprint.

Ordering Information:

CS4215-KL	0°C to 70°C	44-pin PLCC
CS4215-KQ	0°C to 70°C	100-pin TQFP
CDB4215	Evaluation Board	



This data sheet was written for Revision E CS4215 codecs and later. For differences between Revision E and previous versions, see *Appendix A*.

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ANALOG CHARACTERISTICS(T_A = 25°C; VA1, VA2, VD1, VD2 = +5V;

Input Levels: Logic 0 = 0V, Logic 1 = VD1, VD2; Full Scale Input Sine wave, No Gain, No Attenuation 1 kHz; Conversion Rate = 48 kHz; No Gain, No Attenuation, SCLK = 3.072 MHz; Measurement Bandwidth is 10 Hz to 20 kHz; Slave mode; Unless otherwise specified.)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.						
ADC Resolution			16	-	-	Bits
ADC Differential Nonlinearity			-	-	±0.9	LSB
Instantaneous Dynamic Range	Line Inputs Mic Inputs	IDR	80 72	84 78	- -	dB dB
Total Harmonic Distortion	Line Inputs Mic Inputs	THD	- -	- -	0.012 0.032	% %
Interchannel Isolation	Line to Line Inputs Line to Mic Inputs		- -	80 60	- -	dB dB
Interchannel Gain Mismatch	Line Inputs Mic Inputs		- -	- -	0.5 0.5	dB dB
Frequency Response (Note 1)	(0 to 0.45 Fs)		-0.5	-	+0.2	dB
Programmable Input Gain	Line Inputs Mic Inputs		-0.2 19.8	- -	23.5 44	dB dB
Gain Step Size			-	1.5	-	dB
Absolute Gain Step Error			-	-	0.75	dB
Offset Error with HPF = 0 (No Gain)	Line Inputs (AC Coupled) Line Inputs (DC Coupled) Mic Inputs		- - -	±150 ±10 ±400	±400 ±150 -	LSB
Offset Error with HPF = 1 (Notes 1,2) (No Gain)	Line Inputs (AC Coupled) Line Inputs (DC Coupled) Mic Inputs		- - -	0 0 0	±5 ±5 ±5	LSB
Full Scale Input Voltage:	(MLB=0) Mic Inputs (MLB=1) Mic Inputs Line Inputs		0.250 2.50 2.50	0.28 2.8 2.8	0.310 3.10 3.10	Vpp V_{pp} V_{pp}
Gain Drift			-	100	-	ppm/°C
Input Resistance	(Note 3)		20	-	-	kΩ
Input Capacitance			-	-	15	pF
CMOUT Output Voltage (Maximum output current = 400 µA)	(Note 4)		1.9	2.1	2.3	V

Notes: 1. This specification is guaranteed by characterization, not production testing.
2. Very low frequency signals will be slightly distorted when using the HPF.
3. Input resistance is for the input selected. Non-selected inputs have a very high (>1MΩ) input resistance.
4. DC current only. If dynamic loading exists, then CMOUT must be buffered or the performance of ADC's and DAC's may be degraded.

***** Parameter definitions are given at the end of this data sheet.

Mwave™ is a trademark of the IBM Corporation.

ANALOG CHARACTERISTICS (Continued)

Parameter *			Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation; Unless Otherwise Specified.							
DAC Resolution				16	-	-	Bits
DAC Differential Nonlinearity				-	-	±0.9	LSB
Total Dynamic Range			TDR	-	95	-	dB
Instantaneous Dynamic Range (OLB = 1)	(All Outputs)		IDR	80	85	-	dB
Total Harmonic Distortion (OLB = 1)	Line Out	(Note 5)	THD	-	-	0.025	%
	Headphone Out	(Note 6)		-	-	0.2	%
	Speaker Out	(Note 6)		-	-	0.32	%
Interchannel Isolation	Line Out	(Note 5)		-	80	-	dB
	Headphone Out	(Note 6)		-	40	-	dB
Interchannel Gain Mismatch		Line Out		-	-	0.5	dB
		Headphone		-	-	0.5	dB
Frequency Response (Note 1)	(0 to 0.45 Fs)			-0.5	-	+0.2	dB
Programmable Attenuation	(All Outputs)			0.2	-	-94.7	dB
Attenuation Step Size				-	1.5	-	dB
Absolute Attenuation Step Error				-	-	0.75	dB
Offset Voltage		Line Out		-	10	-	mV
Full Scale Output Voltage with OLB = 0	Line Output	(Note 5)		2.55	2.8	3.08	V_{pp}
	Headphone Output	(Note 6)		3.6	4.0	4.4	V_{pp}
	Speaker Output-Differential	(Note 6)		7.3	8.0	8.8	V_{pp}
Full Scale Output Voltage with OLB = 1	Line Output	(Note 5)		1.8	2.0	2.2	V_{pp}
	Headphone Output	(Note 6)		1.8	2.0	2.2	V_{pp}
	Speaker Output-Differential	(Note 6)		3.6	4.0	4.4	V_{pp}
Gain Drift				-	100	-	ppm/°C
Deviation from Linear Phase				-	-	1	Degree
Out of Band Energy	(22 kHz to 100 kHz)	Line Out		-	-60	-	dB
Power Supply							
Power Supply Current (Note 7)		Operating		-	110	140	mA
		Power Down		-	0.5	2	mA
Power Supply Rejection	(1 kHz)			-	40	-	dB

Notes: 5. 10 kΩ, 100 pF load. Headphone and Speaker outputs disabled.
6. 48 Ω, 100 pF load. For the headphone outputs, THD with 10kΩ, 100pF load is 0.02%.
7. Typically, 50% of the power supply current is supplied to the analog power pins (VA1, VA2) and 50% is supplied to the digital power pins (VD1, VD2). Values given are for unloaded outputs.

A/D Decimation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.0	µs

D/A Interpolation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.1/Fs	s

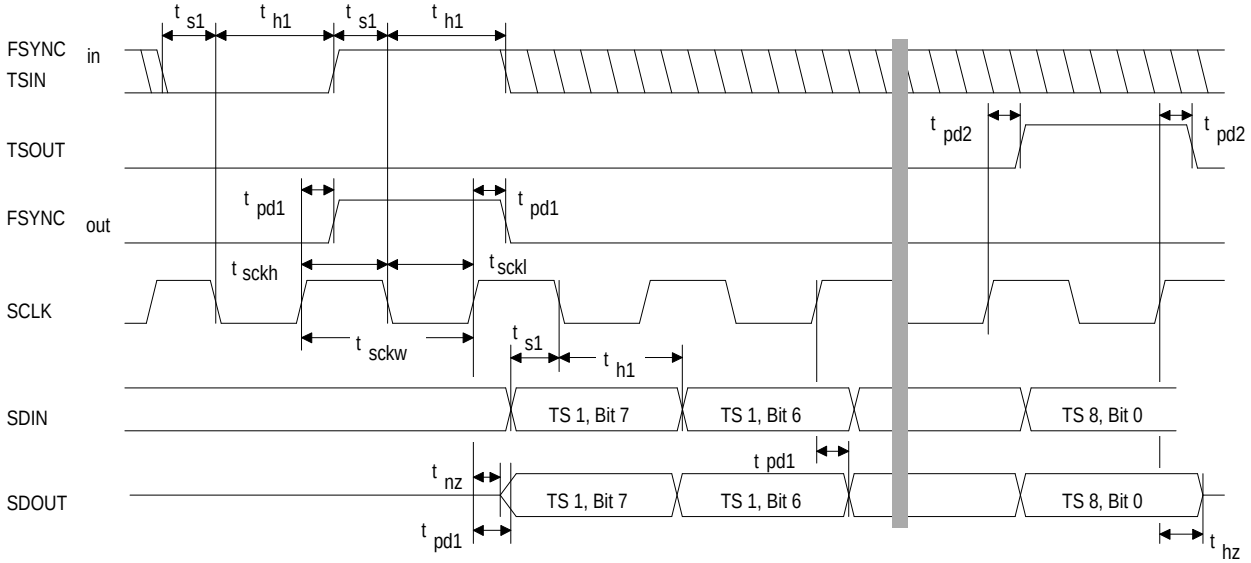
DIGITAL CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1, VD2 = 5V)

Parameter	Symbol	Min	Max	Units
High-level Input Voltage	V_{IH}	(VD1,VD2)-1.0	(VD1,VD2)+0.3	V
Low-level Input Voltage	V_{IL}	-0.3	1.0	V
High-level Output Voltage at I_0 = -2.0 mA	V_{OH}	(VD1,VD2)-0.2	-	V
Low-level Output Voltage at I_0 = 2.0 mA	V_{OL}	-	0.1	V
Input Leakage Current (Digital Inputs)		-	10	µA
Output Leakage Current (High-Z Digital Outputs)		-	10	µA

SWITCHING CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1, VD2 = +5V, outputs loaded with 30 pF; Input Levels: Logic 0 = 0V, Logic 1 = VD1, VD2)

Parameter		Symbol	Min	Typ	Max	Units
SCLK period	Master Mode, XCLK = 1 (Note 8) Slave Mode (XCLK = 0)	t_{sckw} tsckw	- 80	1/(Fs*bpf) -	- -	s ns
SCLK high time	Slave Mode, XCLK = 0 (Note 9)	tsckh	25	-	-	ns
SCLK low time	Slave Mode, XCLK = 0 (Note 9)	tsckl	25	-	-	ns
Input Setup Time		t_{s1}	15	-	-	ns
Input Hold Time		t_{h1}	10	-	-	ns
Input Transition Time	10% to 90% points		-	-	10	ns
Output delay		tpd1	-	-	28	ns
SCLK to TSOUT		tpd2	-	-	30	ns
Output to Hi-Z state	Timeslot 8, bit 0	t_{hz}	-	-	12	ns
Output to non-Hi-Z	Timeslot 1, bit 7	t_{nz}	15	-	-	ns
Input Clock Frequency	Crystals CLKIN (Note 10)		- 1.024	- -	27 13.5	MHz MHz
Input Clock (CLKIN) low time			30	-	-	ns
Input Clock (CLKIN) high time			30	-	-	ns
Sample rate		Fs	4	-	50	kHz
$\overline{\text{RESET}}$ low time	(Note 11)		500	-	-	ns

Notes:
8. In Master mode with BSEL1,0 set to 64 or 128 bits per frame (bpf), the SCLK duty cycle is 50%. When BSEL1,0 is set to 256 bpf, SCLK will have the same duty cycle as CLKOUT. See Internal Clock Generation section.
9. In Slave mode, FSYNC and SCLK must be derived from the master clock running the codec (CLKIN, XTAL1, XTAL2).
10. Sample rate specifications must not be exceeded.
11. After powering up the CS4215, RESET should be held low for 50 ms to allow the voltage reference to settle.



ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

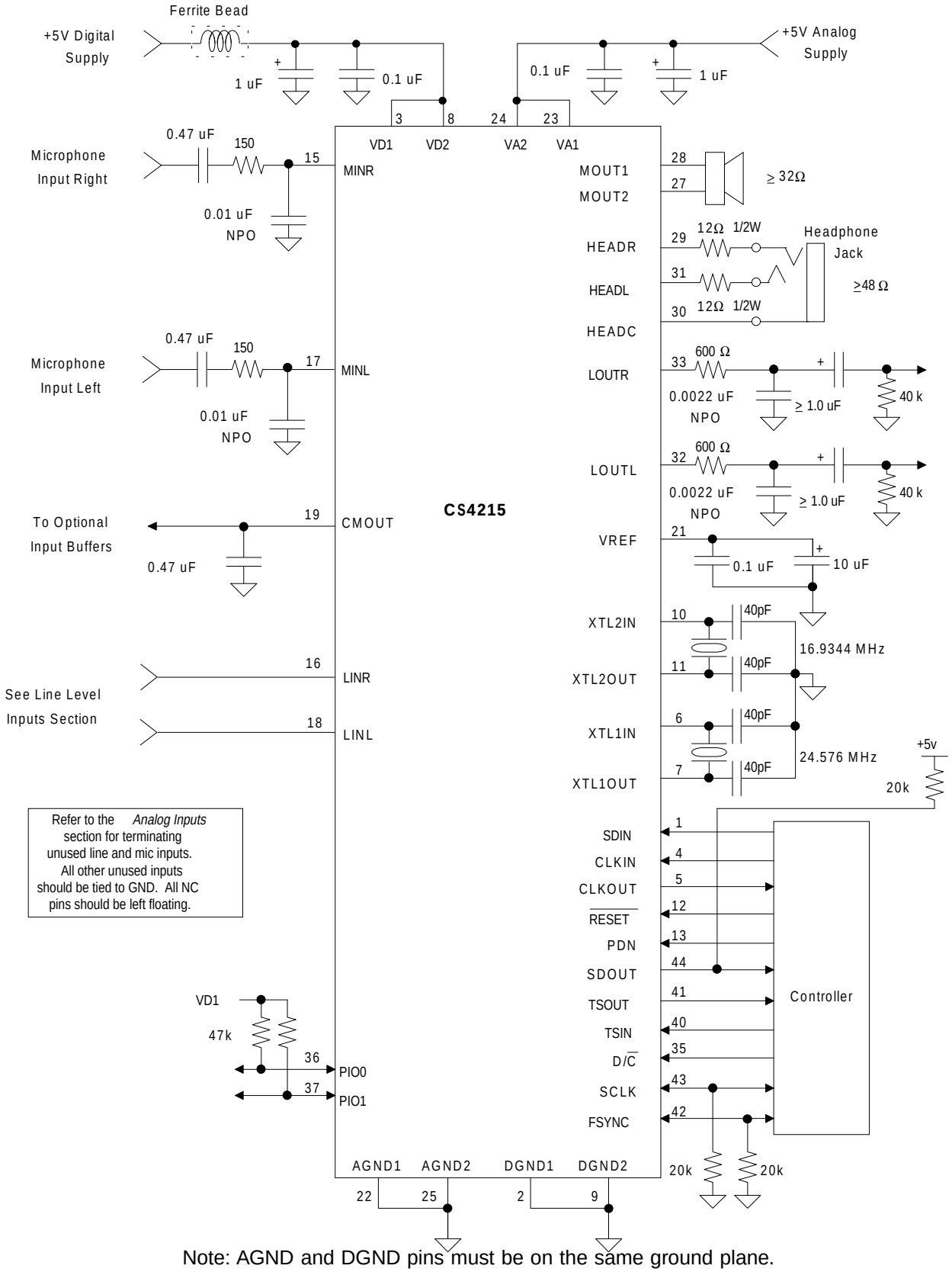
Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital Analog	VD1,VD2 VA1,VA2	-0.3 -0.3	6.0 6.0	V V
Input Current	(Except Supply Pins)		-	±10.0	mA
Analog Input Voltage			-0.3	(VA1, VA2)+0.3	V
Digital Input Voltage			-0.3	(VD1, VD2)+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital (Note 8) Analog (Note 8)	VD1,VD2 VA1,VA2	4.75 4.75	5.0 5.0	5.25 5.25	V V
Operating Ambient Temperature		T_A	0	25	70	°C

Note: 8. $|VD - VA|$ must be less than 0.5 Volts (one diode drop).



Note: AGND and DGND pins must be on the same ground plane.

Figure 1. Recommended Connection Diagram

FUNCTIONAL DESCRIPTION

Overview

The CS4215 has two channels of 16-bit analog-to-digital conversion and two channels of 16-bit digital-to-analog conversion. Both the ADCs and the DACs are delta-sigma converters. The ADC inputs have adjustable input gain, while the DAC outputs have adjustable output attenuation. Special features include a separate microphone input with a 20 dB programmable gain block, an optional 8-bit μ-law or A-law encoder/decoder, pins for two crystals to set alternative sample rates, direct headphone drive and mono speaker drive.

Control for the functions available on the CS4215, as well as the audio data, are communicated to the device over a serial interface. Separate pins for input and output data are provided, allowing concurrent writing to and reading from the device. Data must be continually written for proper operation. Multiple CS4215 devices may be attached to the same data lines.

Analog Inputs

Figure 1, the recommended connection diagram, shows examples of the external analog circuitry recommended around the CS4215. An internal multiplexer selects between line level inputs and microphone level inputs.

Input filters using a 150 Ω resistor and a .01 μF NPO capacitor to ground are required to isolate the input op-amps from, and provide a charge reserve for, the switched-capacitor input of the codec. The RC values may be safely changed by a factor of two.

The HPF bit in Control Time Slot 2 provides a high pass filter that will reduce DC offset on the analog inputs. Using the high pass filter will cause slight distortions at very low frequencies.

Unused analog inputs that are not selected have a very high input impedance, so they may be tied to AGND directly. Unused analog inputs that are selected should be tied to AGND through a 0.1uF capacitor. This prevents any DC current flow.

Line Level Inputs

LINL and LINR are the line level input pins. These pins are internally biased to the CMOUT voltage. Figure 2 shows a dual op-amp buffer which combines level shifting with a gain of 0.5 to attenuate the standard line level of 2 V_{rms} to

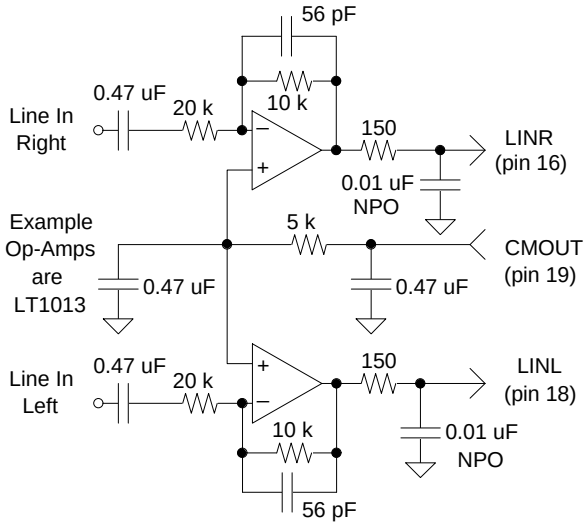


Figure 2. DC Coupled Input.

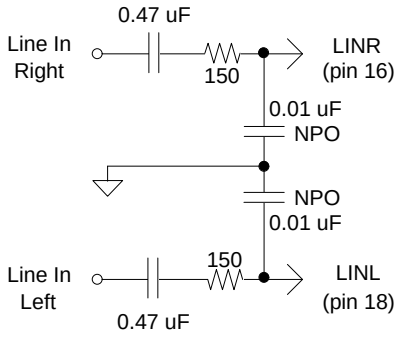


Figure 3. AC Coupled Input.

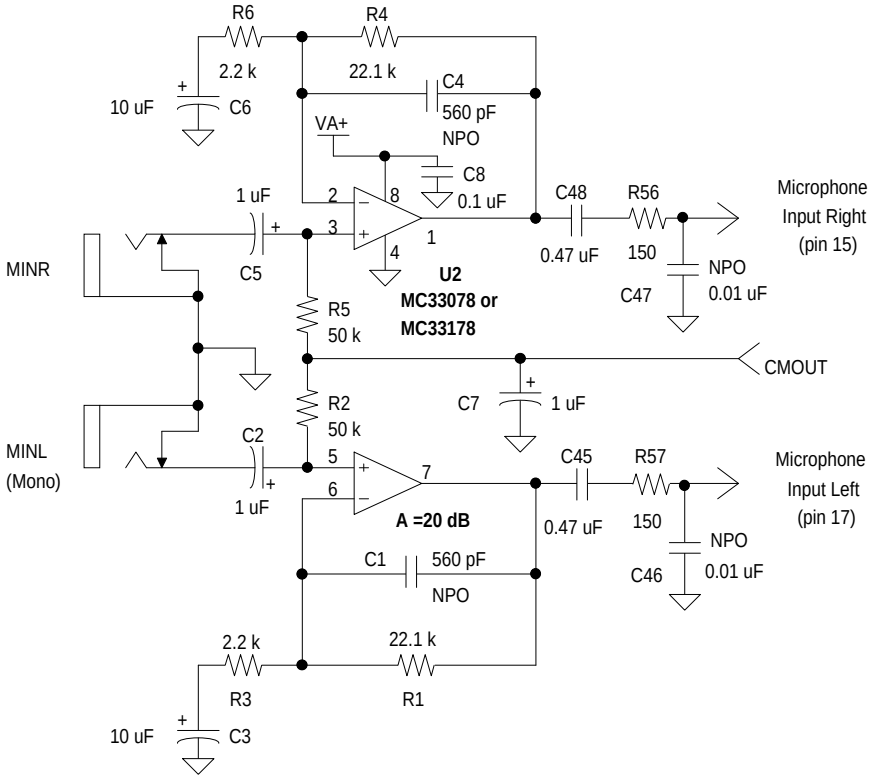


Figure 4. Optional Microphone Input Buffer

1 V_{rms}. The CMOUT reference level is used to level shift the signal. This level shifting allows the line inputs to be DC coupled into the CS4215. Minimum ADC offset results when the line inputs are DC coupled (see Analog Characteristics Table).

Figure 3 shows an AC coupled input circuit for signals centered around 0 Volts. The anti-aliasing RC filter presents a low impedance at high frequencies and should be driven by a low impedance source.

Microphone Level Inputs

Internal amplifiers with a programmable 20 dB gain block are provided for the microphone level inputs, MINR and MINL. Figure 4 shows a single-ended input microphone pre-amplifier stage with a gain of 23 dB. AC coupling is mandatory for these inputs since any DC offset on the input will be amplified by the codec.

The 20 dB gain block may be disabled using the MLB bit in Control Time Slot 1. When disabled, the inputs become line level with full scale inputs of 1 Vrms.

Adjustable Input Gain

The signals from the microphone or the line inputs are routed to a programmable gain circuit which provides up to 22.5 dB of gain in 1.5 dB steps. Level changes only take effect on zero crossings to minimize audible artifacts, often referred to as "zipper noise". The requested level change is forced if no zero crossing is found after 511 frames (10.6 ms at a 48 kHz frame rate). A separate zero crossing detector exists for each channel.

Analog Outputs

The analog outputs of the DACs are routed via an attenuator to a pair of line outputs, a pair of

headphone outputs and a mono monitor speaker output.

Output Level Attenuator

The DAC outputs are routed through an attenuator, which provides 0 dB to 94.5 dB of attenuation, adjustable in 1.5 dB steps. Level changes are implemented using both analog and digital attenuation techniques. Level changes only take effect on zero crossings to minimize audible artifacts. The requested level change is forced if an analog zero crossing does not occur within 511 frames (10.6 ms at a 48 kHz frame rate). A separate zero crossing detector exists for each channel.

Line Outputs

LOUTR and LOUTL output an analog signal, centered around the CMOUT voltage. The minimum recommended load impedance is 8 kΩ. Figure 1 shows the recommended 1.0 µF DC blocking capacitor with a 40 kΩ resistor to ground. When driving impedances greater than 10 kΩ, this provides a high pass corner of 20 Hz. These outputs may be muted.

Headphone Outputs

HEADR and HEADL output an analog signal, centered around the HEADC voltage. The default headphone output level (OLB = 0) contains an optional 3 dB gain over the line outputs which provides reasonable listening levels, even with small amplitude digital sources. These outputs have increased current drive capability and can drive a load impedance as low as 48 Ω. External 12 Ω series resistors reduce output level variations with different impedance headphones. The common return line from driving headphones should be connected to HEADC, which is biased to the CMOUT voltage. This removes the need for AC coupling, and also controls where the return currents flow. All three headphone output lines are short-circuit protected. These outputs may be muted.

Speaker Output

MOUT1 and MOUT2 differentially drive a small loudspeaker, whose impedance should be greater than 32 Ω. The signal is a summed version of the right and left line output, tapped off prior to the mute function, but after the attenuator. The speaker output may be independently muted. With OLB = 0, the speaker output also contains a 3 dB gain over the line outputs. When OLB = 1, the speaker outputs are driven at the same level as the line outputs.

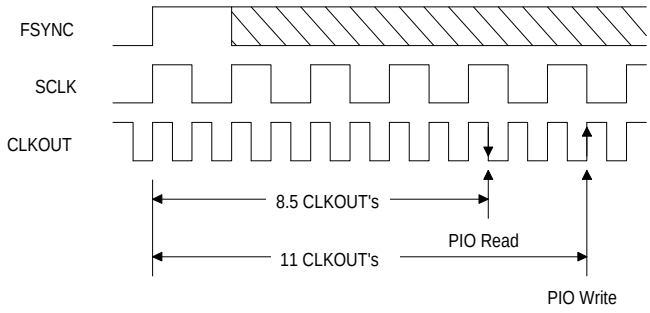
Some small speakers distort heavily when presented with low frequency energy. A high-pass filter helps eliminate the low frequency energy and can be implemented by AC coupling both speaker terminals with a resistor to ground, on the speaker side of the DC blocking capacitors. The values selected would depend on the speaker chosen, but typical values would be 22 µF for the capacitors, with the positive side connected to the codec, and 50 kΩ resistors. This circuit is contained on the CDB4215 evaluation board as shown in the end of this data sheet.

Input Monitor Function

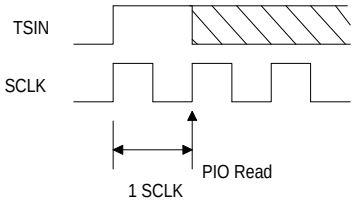
To allow monitoring of the input audio signal, the output of the ADCs can be routed through a monitor path attenuator, then digitally mixed into the input data for the DACs (see the front page block diagram). Changes in the input gain or output level settings directly affect the monitor level. If full scale data from the ADCs is added to full scale digital data from the serial interface, clipping will occur.

Calibration

Both output offset voltage and input offset error are minimized by an internal calibration cycle. At least one calibration cycle must be invoked



Data Mode -Read and Write



Control Mode - Read Only

Notes:
1. DATA MODE READ - The data is sent out via SDOUT on the next frame.
2. CONTROL MODE READ - The data is sent out, via SDOUT, the same frame.
3. DATA MODE READ, WRITE - are tied to the rising edge of FSYNC and CLKOUT. They are independent of SCLK.
4. CONTROL MODE READ - The PIO pins are sampled by a rising edge of SCLK.

Figure 5. PIO Pin Timing

after power up. A calibration cycle will occur immediately after leaving the reset state. A calibration cycle will also occur immediately after going from control mode to data mode ($D/\overline{C}$ going high). When powering up the CS4215, or exiting the power down state, a minimum of 50 ms must occur, to allow the voltage reference to settle, before initiating a calibration cycle. This is achieved by holding $\overline{RESET}$ low or staying in control mode for 50 ms after power up or exiting power down mode. The input offset error will be calibrated for whichever input channel is selected (microphone or line, using the IS bit). Therefore, the IS bit should remain steady while the codec is calibrating, although the other bits input to the codec are ignored. Calibration takes 194 FSYNC cycles and SDOUT data bits will be zero during this period. The A/D Invalid bit, ADI (bit 7 in data time slot 6), will be high during calibration and will go low when calibration is finished.

Parallel Input/Output

Two pins are provided for parallel input/output. These pins are open drain outputs and require external pull-up resistors. Writing a zero turns on the output transistor, pulling the pin to ground; writing a one turns off the output transistor, which allows an external resistor to pull the pin high. When used as an input, a one must be written to the pin, thereby allowing an external device to pull it low or leave it high. These pins can be read in control mode and their state is recorded in Control Register 5. These pins can be written to and read back in data mode using Data Register 7. Figure 5 shows the Parallel Input/Output timing.

Clock Generation

The master clock operating the CS4215 may be generated using the on-chip crystal oscillators, or by using an external clock source. In all data modes SCLK and FSYNC must be synchronous to the selected master clock.

If the master clock source stops, the digital filters will power down after 5 µs to prevent overheating. If FSYNC stops, the digital filters will power down after approximately 1 FSYNC period. The CS4215 will not enter the total power down state.

Internal Clock Generation

Two external crystals may be attached to the XTL1IN, XTL1OUT, XTL2IN and XTL2OUT pins. Use of an external crystal requires additional 40 pF loading capacitors to digital ground (see Figure 1). XTAL1 oscillator is intended for use at 24.576 MHz and XTAL2 oscillator is intended for use at 16.9344 MHz, although other frequencies may be used. The gain of the internal inverter is slightly higher for XTAL1, ensuring proper operation at >24 MHz frequencies. The crystals should be parallel resonant, fundamental mode and designed for 20 pF loading (equivalent to a 40 pF capacitor on each leg). If XTAL1 or XTAL2 is not selected as the master clock, that particular crystal oscillator is powered down to minimize interference. If a crystal is not needed, the XTL-IN pin should be grounded. An example crystal supplier is CAL Crystal, telephone number (714) 991-1580.

FSYNC and SCLK must be synchronous to the master clock. When using the codec in slave mode with one of the crystals as master clock, the controller must derive FSYNC and SCLK from the crystals, i.e. via CLKOUT. Note that CLKOUT will stop in a low condition within two periods after D/$\overline{C}$ goes low.

An internally generated clock which is 256 times the sample rate (FSYNC rate) is output (CLKOUT) for potential use with an external AES/EBU transmitter, or another CS4215. No glitch occurs on CLKOUT when selecting alternate clock sources. CLKOUT will stop in a low condition within two periods after D/$\overline{C}$ goes low, assuming one of the crystal oscillators is selected, or either CLKIN or SCLK is the master clock source and is continuous. The duty cycle of CLKOUT is 50% if the master clock is one of the crystal oscillators and the DFR bits are 0, 1, 2, 6 or 7. If the DFR bits are 3 or 5, the duty cycle is 33% (high time). If the DFR bits are 4 then CLKOUT has the timing shown in Figure 6. If the master clock is SCLK or CLKIN, the duty cycle of CLKOUT will be the same as the master clock source.

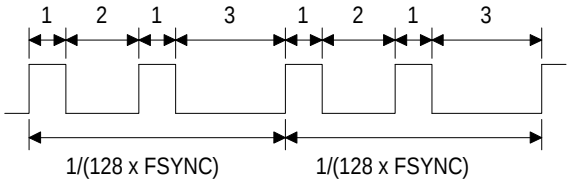


Figure 6. CLKOUT duty cycle using the on-chip crystal oscillator when DFR = 4 (typically FSYNC = 37.8 kHz)

External Clock

An external clock input pin (CLKIN) is provided for potential use with an external AES/EBU receiver, or an already existing system clock. When MCK2 = 0, the input clock must be exactly 256 times the sample rate, and FSYNC and SCLK must be synchronous to CLKIN. When MCK2 = 1 the DFR bits allow various divide ratios off the CLKIN frequency.

Alternatively, an external high frequency clock may be driven into XTL1IN or XTL2IN. The correct clock source must be selected using the MCK bits. Manipulating DFR bits will allow various divide ratios from the clock to be se-

lected. SCLK and FSYNC must be synchronous to the external clock.

As a third alternative, SCLK may be programmed to be the master clock input. In this case, it must be 256 times Fs.

Serial Interface

The serial interface of the CS4215 transfers digital audio data and control data into and out of the device. Multiple CS4215 devices may share the same data lines. DSP's supported include the Motorola 56001 in network mode and a subset of the 'CHI' bus from AT&T/Intel.

Serial Interface Signals

Figure 7 shows an example of two CS4215 devices connected to a common controller. The Serial Data Out (SDOUT) and Serial Data In (SDIN) lines are time division multiplexed between the CS4215s.

The serial interface clock, SCLK, is used for transmitting and receiving data. SCLK can be generated by one of the CS4215s, or it can be input from an external SCLK source. When generated by an external source, SCLK must be synchronous to the master clock. Data is transmitted on the rising edge of SCLK and is received on the falling edge of SCLK. The SCLK frequency is always equal to the bit rate.

The Frame Synchronizing signal (FSYNC) is used to indicate the start of a frame. It may be output from one of the CS4215s, or it may be generated from an external controller. If FSYNC is generated externally, it must be high for at least 1 SCLK period, and it must fall at least 2 SCLKs before the start of a new frame (see Figure 8). It must also be synchronous to the master clock. The frequency of FSYNC is equal to the system sample rate (see Figure 8). Each CS4215 requires 64 SCLKs to transfer all the data. The SCLK frequency can be set to 64, 128, or 256 bits per frame, thereby allowing for 1, 2 or 4 CS4215s connected to the same bus.

In a typical multi-part scenario, one CS4215 (the master) would generate FSYNC and SCLK, while the other CS4215s (the slaves) would receive FSYNC and SCLK. The CLKOUT of the master would be connected to the CLKIN of each slave device as shown in Figure 7. Then, the master device would be programmed for the desired sample frequency (assuming one of the crystals is selected as the clock source), the number of bits per frame, and for SCLK and FSYNC to be outputs. The slave devices would be programmed to use CLKIN as the clock source, the same number of bits per frame, and for SCLK and FSYNC to be inputs. Since CLKOUT is al-

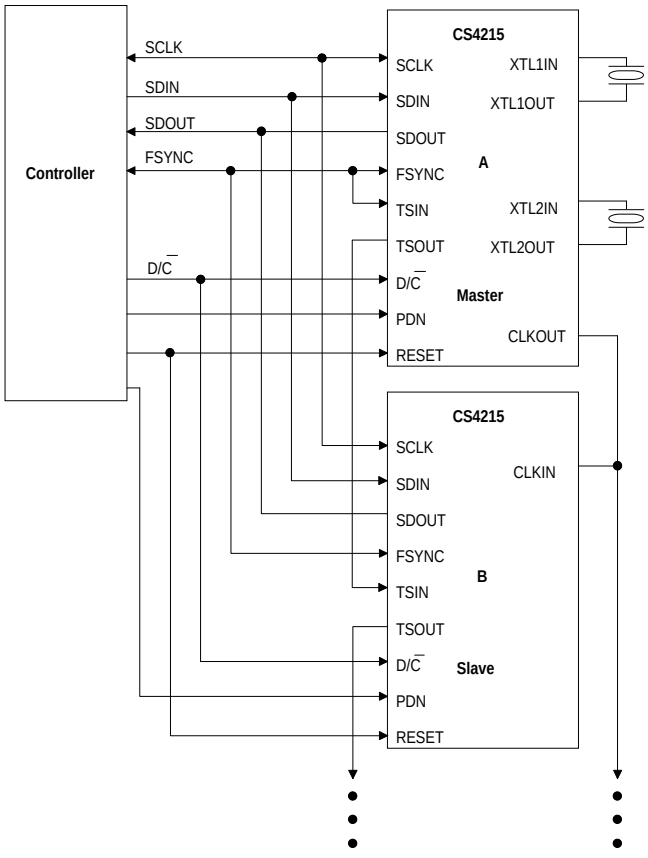


Figure 7. Multiple CS4215's

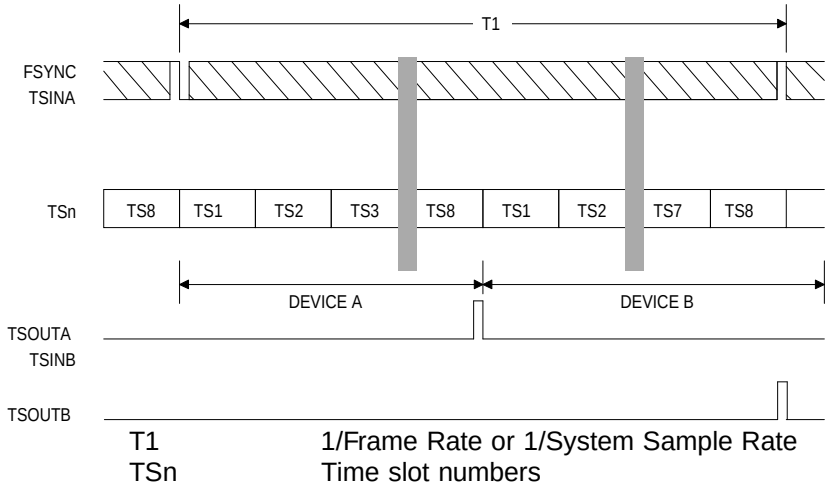


Figure 8. Serial Interface Timing for 2 CS4215's

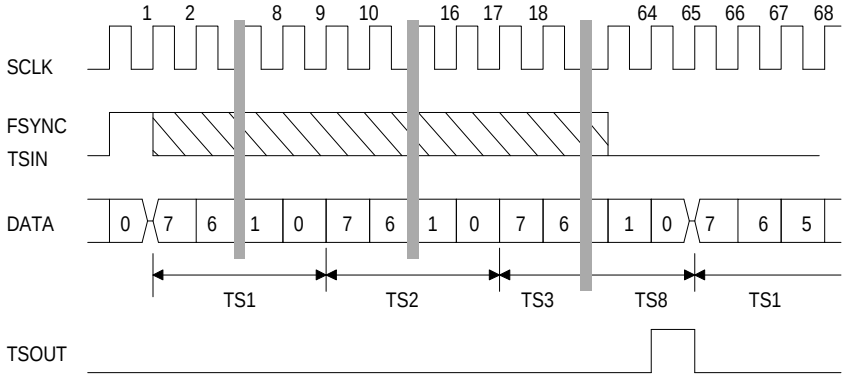


Figure 9. Frame Sync and Bit Offset Timing

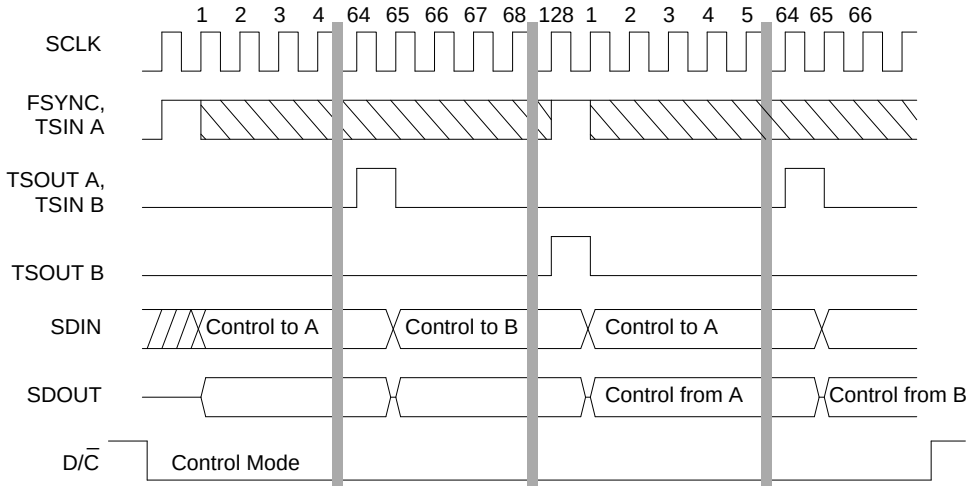


Figure 10. Control Mode Timing for 2 CS4215's

ways 256 times the sample frequency and scales with the selected sample frequency on the master, the slave devices will automatically scale with changes in the master codec's sample frequency.

CS4215s are time division multiplexed onto the bus using the Time Slot Out (TSOUT) and Time Slot In (TSIN) signals. TSOUT is an output signal that is high for one SCLK bit time, and indicates that the CS4215 is about to release the bus. TSIN is an input signal that informs the CS4215 that the next time slot is available for it to use. The first device in the chain uses FSYNC as its TSIN signal. All subsequent devices use the TSOUT of the previous device as its TSIN input. TSIN must be high for at least 1 SCLK period and fall at least 2 SCLKs before start of a new frame.

Serial Interface Operation

The serial interface format has a variable number of time slots, depending on the number of CS4215s attached to the bus. All time slots have 8 bits. Each CS4215 requires 8 time slots (64 bits) to communicate all data (see Figure 9).

CONTROL MODE

The Control Mode is used to set up the CS4215 for subsequent operation in Data Mode by loading the internal control registers. Control mode is asserted by bringing D/$\overline{C}$ low. If D/$\overline{C}$ is low during power up, then the CS4215 will enter control mode immediately. The SCLK and FSYNC pins are tri-stated, and the CS4215 will receive SCLK and FSYNC from an external source. If the CS4215 is in master mode (SCLK and FSYNC are outputs) and D/$\overline{C}$ is brought low, then SCLK & FSYNC will continue to be driven for a minimum of 4 and a maximum of 12 SCLKs, if the ITS bit = 0. If ITS is 1, SCLK and FSYNC will three-state immediately after D/$\overline{C}$ goes low. If D/$\overline{C}$ is brought low when the codec is programmed as master with ITS=0, the codec will timeout and release FSYNC and SCLK within 100µs. The values in the control registers for control of the serial ports are ignored in control mode. The data received on SDIN is stored into the control registers which have addresses matching their time slots. The data in the registers is transmitted on SDOUT with the time slot equal to the register number (see Figure 10).

The steps involved when going from data mode to control mode and back are shown in the flow chart in Figure 11.

Control Formats

The CS4215 control registers have the functions and time slot assignments shown in Table 1. The register address is the time slot number when D/$\overline{C}$ is 0. Reserved bits should be written as 0 and could be read back as 0 or 1. When comparing data read back, reserved bits should be masked. The SDOUT pin goes into a high-impedance state prior to Time Slot 1 and after Time Slot 8. The data listed below the register is its reset state.

The parallel port register is used to read and write the two open-drain input/output pins. The outputs are all set to 1 on RESET. PIO bits are read only in control mode. Note that, since PIO signals are open drain signals, an external device

Time slot	Description
1	Status
2	Data Format
3	Serial Port Control
4	Test
5	Parallel Port
6	RESERVED
7	Revision
8	RESERVED

Table 1. Control Registers

may drive them low even when they have been programmed as highs. Therefore, the value read back may differ from the value written. In the data mode, (D/$\overline{C}$=1), this register can be read and written to through the serial port as part of the Input Settings Registers. In control mode, (D/$\overline{C}$=0) these bits can only be read.

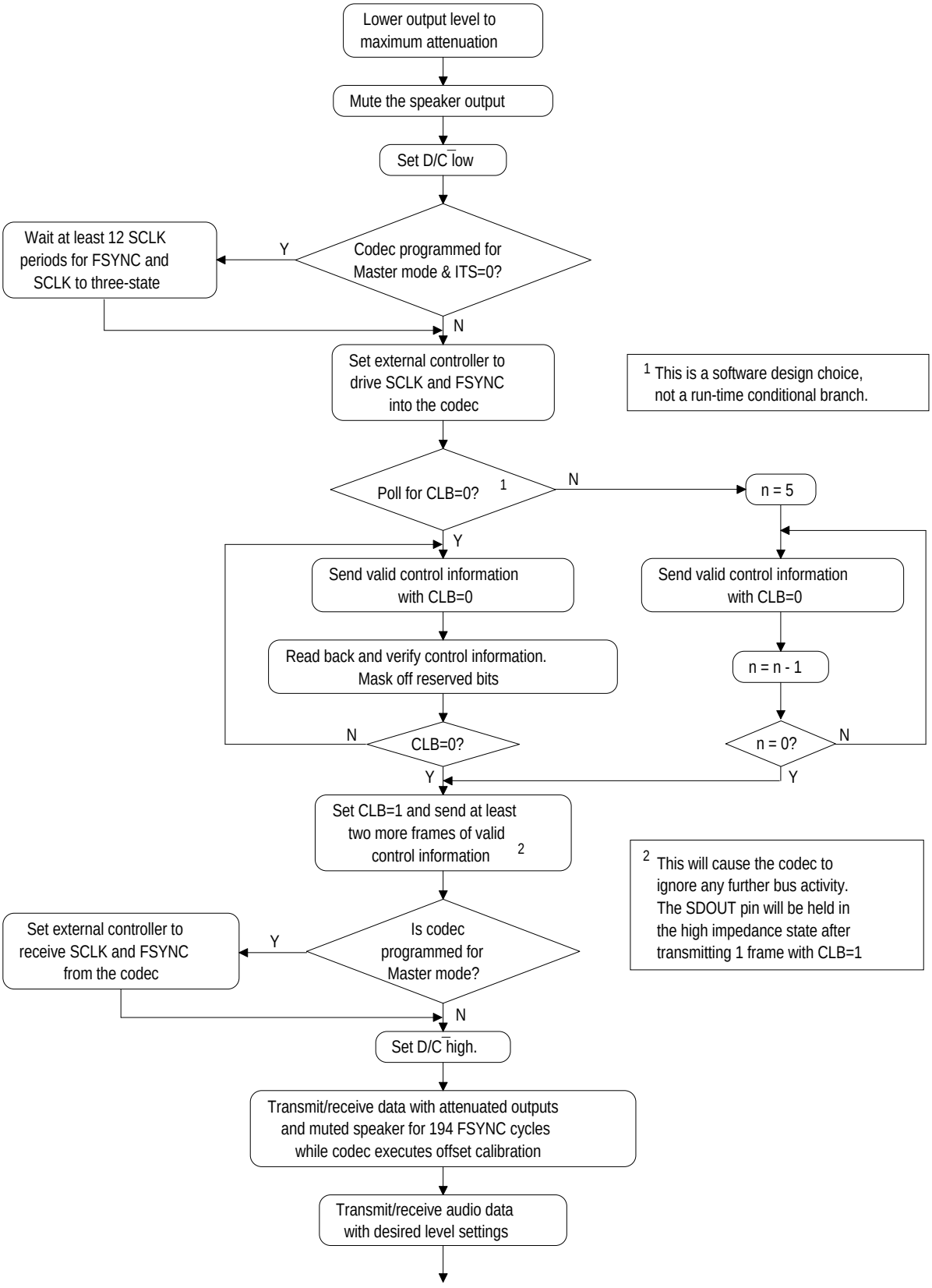


Figure 11. Control Mode Flow Chart

Control Time Slot 1, Status Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**0**	**0**	**1**	**MLB**	**OLB**	**CLB**	**RSRV**	
Reset (R)	0	0	1	0	0	1	X	X

BIT	NAME	VALUE		FUNCTION
RSRV	Reserved Bits			Must be written as 0.
CLB	Control Latch Bit	1	*R*	Ensures proper transition between control and data mode.
OLB	Output Level Bit	0	*R*	Line full scale outputs are 2.8 Vpp (1Vrms) Headphone full scale output is 4.0 Vpp. Speaker full scale output is 8.0 Vpp.
		1		Line and Headphone full scale outputs are 2.0 Vpp. Speaker full scale output is 4.0 Vpp.
MLB	Microphone Level	0	*R*	20 dB Fixed Gain Enabled Full scale microphone inputs are 0.288 Vpp.
		1		20 dB Fixed Gain Disabled Full scale inputs are 2.88 Vpp.

Control Time Slot 2, Data Format Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**HPF**	**RSRV**	**DFR2**	**DFR1**	**DFR0**	**ST**	**DF1**	**DF0**
Reset (R)	0	X	0	0	0	0	0	1

BIT	NAME	VALUE		FUNCTION
DF1-0	Data Format Selection	0 0	0	16-bit $2^{'s}$-complement linear.
		0 1	1 *R*	8-bit μ–Law.
		1 0	2	8-bit A-Law.
		1 1	3	8-bit unsigned linear.
ST	Stereo Bit	0	*R*	Mono Mode.
		1		Stereo Mode.
DFR2-0	Data Conversion Frequency Selection			

			CLKIN (÷)	XTAL1(kHz) 24.576 MHz	XTAL2 (kHz) 16.9344 MHz
0 0 0	0	*R*	3072	8	5.5125
0 0 1	1		1536	16	11.025
0 1 0	2		896	27.42857	18.9
0 1 1	3		768	32	22.05
1 0 0	4		448	NA	37.8
1 0 1	5		384	NA	44.1
1 1 0	6		512	48	33.075
1 1 1	7		2560	9.6	6.615

RSRV	Reserved Bit		Must be written as 0
HPF	High Pass Filter	0 *R*	Disabled.
		1	Enabled. A Digital High Pass Filter is used to force the ADC DC offset to zero.

Control Time Slot 3, Serial Port Control Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**ITS**	**MCK2**	**MCK1**	**MCK0**	**BSEL1**	**BSEL0**	**XCLK**	**XEN**
Reset (R)	0	0	0	0	1	0	0	1

BIT	NAME	VALUE			FUNCTION
XEN	Transmitter Enable	0 1		 *R*	Enable the serial data output. Disable (high-impedance state) serial data output.
XCLK	Transmit Clock	0 1		*R* 	Receive SCLK and FSYNC from external source SLAVE Mode Generate SCLK and FSYNC MASTER Mode
BSEL1-0	Select Bit Rate	0 0 0 1 1 0 1 1	0 1 2 3	 *R* 	64 bits per frame. 128 bits per frame. 256 bits per frame. Reserved.
MCK2-0	Clock Source Select	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0	0 1 2 3 4	*R* 	SCLK is master clock, 256 bits per frame. BSEL must equal 2, and XCLK must equal 0. XTAL1, 24.576 MHz, is clock source. XTAL2, 16.9344 MHz, is clock source. CLKIN is clock source, and must be 256xFs. CLKIN is clock source, DFR2-0 select sample frequency.
ITS	Immediate Three-State	0 1		*R* 	SCLK and FSYNC three-state up to 12 clocks after D/C goes low. SCLK and FSYNC three-state immediately after D/C goes low.

Control Time Slot 4, Test Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**TEST**						**ENL**	**DAD**
Reset (R)	0	0	0	0	0	0	0	0

BIT	NAME	VALUE		FUNCTION
DAD	Loopback Mode	0 1	*R*	Digital-Digital Loopback. Digital-Analog-Digital Loopback.
ENL	Enable Loopback Testing	0 1	*R*	Disable. Enable.
TEST	Test bits			The TEST bits must be written as zero, otherwise special factory test modes may be invoked.

Control Time Slot 5, Parallel Port Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**PIO1**	**PIO0**	**RSRV**					
Reset (R)	1	1	X	X	X	X	X	X

BIT	NAME	VALUE	FUNCTION
RSRV	Reserved Bits		Must be written as 0.
PIO1-0	Parallel I/O Bits	1 1 3 *R*	See the Parallel Input/Output Section.

Control Time Slot 6, Reserved Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**RSRV**							
Reset (R)	X	X	X	X	X	X	X	X

BIT	NAME	VALUE	FUNCTION
RSRV	Reserved Bits		Must be written as 0.

Control Time Slot 7, Version Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**RSRV**				**VER3**	**VER2**	**VER1**	**VER0**
Reset (R)	X	X	X	X	0	0	1	0

BIT	NAME	VALUE	FUNCTION
VER3-0	Device Version Number	0 0 0 0 0 0 0 0 1 1 0 0 1 0 2 *R*	"C". See *Appendix A.* "D". See *Appendix A.* "E". This Data Sheet
RSRV	Reserved Bits		Must be written as 0.

Control Time Slot 8, Reserved Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**RSRV**							
Reset (R)	X	X	X	X	X	X	X	X

BIT	NAME	VALUE	FUNCTION
RSRV	Reserved Bits		Must be written as 0.

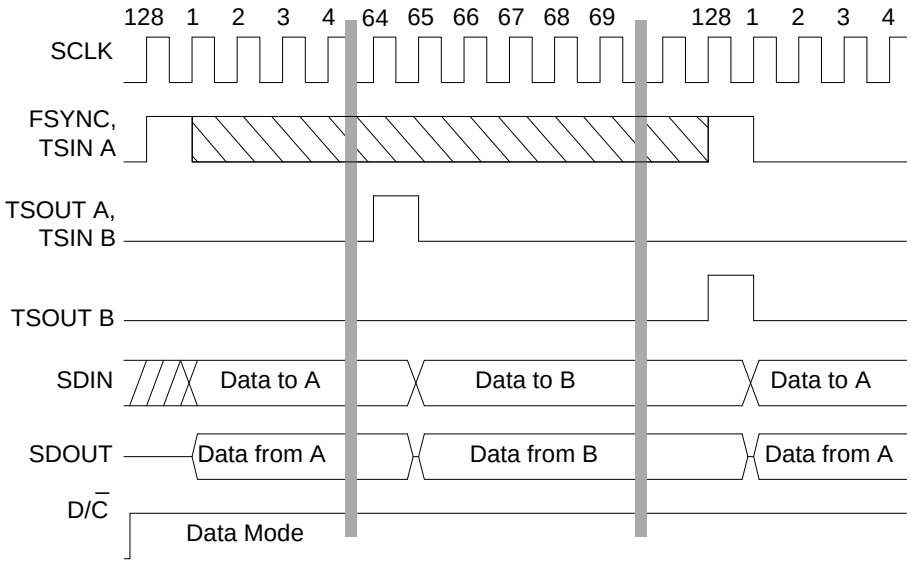


Figure 12. Data Mode Timing for 2 CS4215's

DATA MODE

The data mode is used during conversions to pass digital data between the CS4215 and external devices. The frame sync rate is equal to the value of the conversion frequency set by the DFR2-DFR0 bits of the Data Format register. Each frame has either 64, 128, or 256 bit times depending on the BSEL bits in the Serial Control register. Control of gain, attenuation, input selection and output muting are embedded in the data stream.

Time slot	Description
1	Left Audio MS8 bits
2	Left Audio LS8 bits
3	Right Audio MS8 bits
4	Right Audio LS8 bits
5	Output Setting
6	Output Setting
7	Input Setting
8	Input Setting

Table 2. Data Registers

Data Formats

All time slots contain 8 bits. The MSB of the data is transmitted/received first. The CS4215 data registers have the functions and time slot assignments shown in Table 2. The register address is the time slot number when D/$\overline{C}$ is 1. The SDOUT pin goes into a high-impedance state prior to time slot 1 and after Time Slot 8 (see Figure 12).

The CS4215 supports four audio data formats: 16-bit 2's-complement linear, 8-bit unsigned linear, 8-bit A-Law, and 8-bit μ-Law. Figure 13 illustrates the transfer characteristic for 16-bit and 8-bit linear formats. Note that a digital code

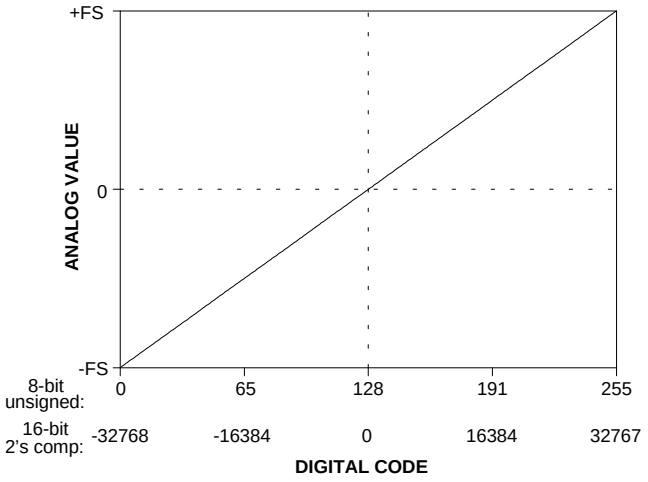


Figure 13. Linear Data Formats

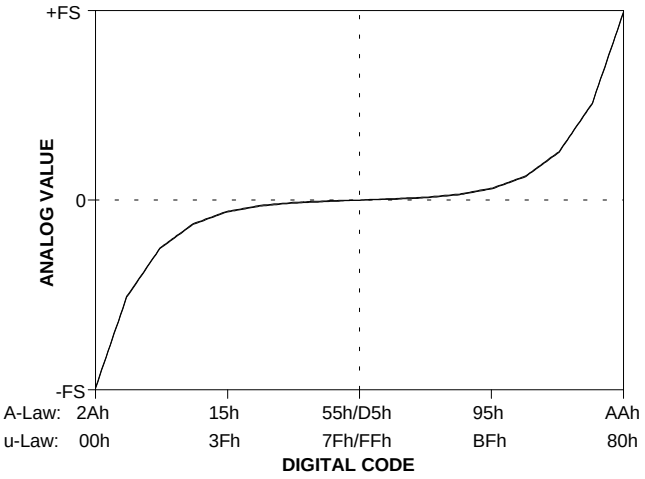


Figure 14. Companded Data Formats

of 128 (80 Hex) is considered analog zero for the 8-bit unsigned format.

A non-linear coding scheme is used for the companded formats as shown in Figure 14. This scheme is compatible with CCITT G.711. Companding uses more precision at lower amplitudes at the expense of less precision at higher amplitudes. µ-Law is equivalent to 13 bits at low signal levels and A-Law is equivalent to 12 bits. This low-level dynamic range is obtained at the expense of large-signal dynamic range which, for both µ-Law and A-Law, is equivalent to 6 bits. The CS4215 internally operates at 16 bits. The companded data is expanded to the upper 13 (12) bits for the DACs and compressed from the upper 13 (12) bits to 8 bits for the ADCs.

Data Time Slot 1&2, Left Channel Audio Data

Time slot 1 and 2 contain audio data for the left channel. In mono modes, only the left channel data is used, however both the right and left output DACs are driven. In 8-bit modes, only time slot 1 is used for the data.

Data Time Slot 3&4, Right Channel Audio Data

Time slot 3 and 4 contains audio data for the right channel. In mono modes, the right ADC outputs zero and the right DAC uses the left digital data. In 8-bit modes, only time slot 3 is used for the data.

Figure 15 summarizes all the time slot bit allocations for the 4 data modes and for control mode.

Reset

$\overline{\text{RESET}}$ going low causes all the internal control registers to be set to the states shown with each register description. $\overline{\text{RESET}}$ must be brought low and high at least once after power up. $\overline{\text{RESET}}$ returning high causes the CS4215 to execute an offset calibration cycle. $\overline{\text{RESET}}$ or D/$\overline{\text{C}}$ returning high should occur at least 50 ms after the power supply has stabilized to allow the voltage reference to settle.

Data Time Slot 5, Output Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**HE**	**LE**	**LO5**	**LO4**	**LO3**	**LO2**	**LO1**	**LO0**
Reset (R)	0	0	1	1	1	1	1	1

BIT	NAME	VALUE		FUNCTION
LO5-0	Left Channel Output Attenuation Setting	1 1 1 1 1 1 63	*R*	1.5dB attenuation steps. LO5 is the MSB. 0 = no attenuation. 111111 = -94.5dB
LE	Line Output Enable	0 1	*R*	Analog line outputs off (muted). Analog line outputs on.
HE	Headphone Output Enable	0 1	*R*	Headphone output off (muted). Headphone output on.

Data Time Slot 6, Output Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**ADI**	**SE**	**RO5**	**RO4**	**RO3**	**RO2**	**RO1**	**RO0**
Reset (R)	1	0	1	1	1	1	1	1

BIT	NAME	VALUE	FUNCTION
RO5-0	Right Channel Output Attenuation Setting	1 1 1 1 1 1 63 *R*	1.5dB attenuation steps. RO5 is the MSB. 0 = no attenuation. 111111 = -94.5dB Not used in mono modes.
SE	Speaker Enable	0 *R* 1	Speaker off (muted). Speaker on.
ADI	A/D Data Invalid	0 1 *R*	A/D data valid. A/D data invalid. Busy in calibration.

Data Time Slot 7, Input Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**PIO1**	**PIO0**	**OVR**	**IS**	**LG3**	**LG2**	**LG1**	**LG0**
Reset (R)	1	1	0	0	0	0	0	0

BIT	NAME	VALUE	FUNCTION
LG3-0	Left Channel Input Gain Setting	0 0 0 0 *R*	1.5dB gain steps. LG3 is the MSB. 0 = no gain, 1111 = 22.5dB gain.
IS	Input Select	0 *R* 1	Line level inputs (LINL, LINR). Microphone level inputs (MINL, MINR).
OVR	Overrange	0 *R*	When read as 1, this bit indicates that an input over-range condition has occurred. The bit remains set until cleared by writing 0 into the register. Writing a 1 enables the overrange detection. The bit will remain 0 until an over-range occurs. Serial port clear has priority over internal settings.
PIO1-0	Parallel I/O	1 1 3 *R*	Parallel input/output bits.

Data Time Slot 8, Input Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**MA3**	**MA2**	**MA1**	**MA0**	**RG3**	**RG2**	**RG1**	**RG0**
Reset (R)	1	1	1	1	0	0	0	0

BIT	NAME	VALUE	FUNCTION
RG3-0	Right Channel Input Gain Setting	0 0 0 0 *R*	1.5dB gain steps. RG3 is the MSB. 0 = no gain, 1111 = 22.5dB gain.
MA3-0	Monitor Path Attenuation	1 1 1 1 15 *R*	6dB attenuation steps. MA3 is the MSB. 0 = no attenuation, 1111 = mute.

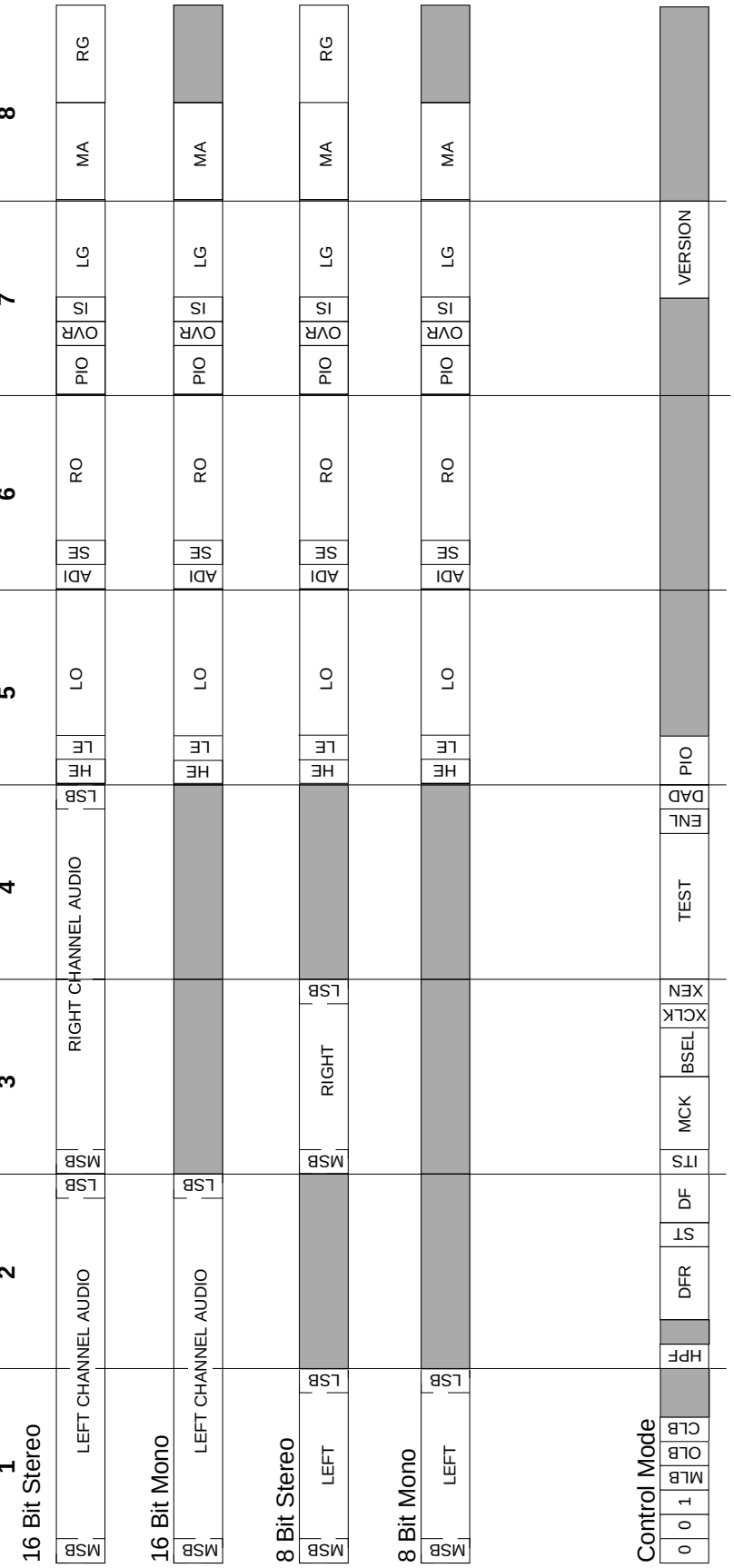


Figure 15. Time Slot/Register Overview

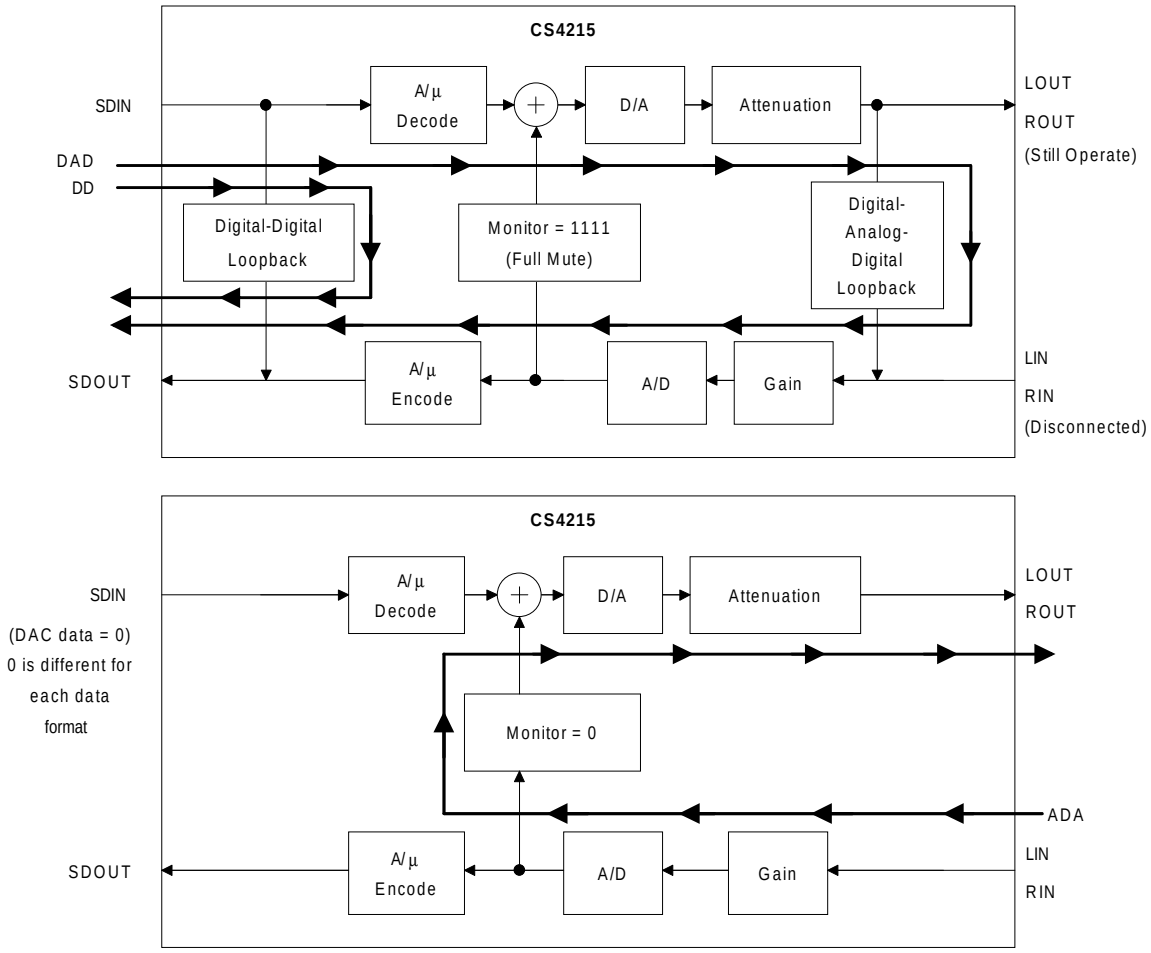


Figure 16. DD, DAD & ADA Loopback Paths

Power Down Mode

Bringing the PDN pin high puts the CS4215 into the power down mode. In this mode HEADC and CMOUT will not supply current. Power down will change all the control registers to the reset state shown under each Control Time Slot register. In the power down mode, the TSOUT pin will follow the TSIN state with less than 10 ns delay.

After returning to normal operation from power down, an offset calibration cycle must be executed. Either bringing $\overline{\text{RESET}}$ low then high, or updating the control registers, will cause an offset calibration cycle. In either case, a delay of 50 ms must occur after PDN goes low before executing the offset calibration. This allows the internal voltage reference time to settle.

LOOPBACK TEST MODES

The CS4215 contains three loopback modes that may be used to test the codec. Two of the loopback test modes are designed to allow the host to perform a self-test on the CS4215. The third mode allows laboratory testing using external equipment.

Host Self-Test Loopback Modes

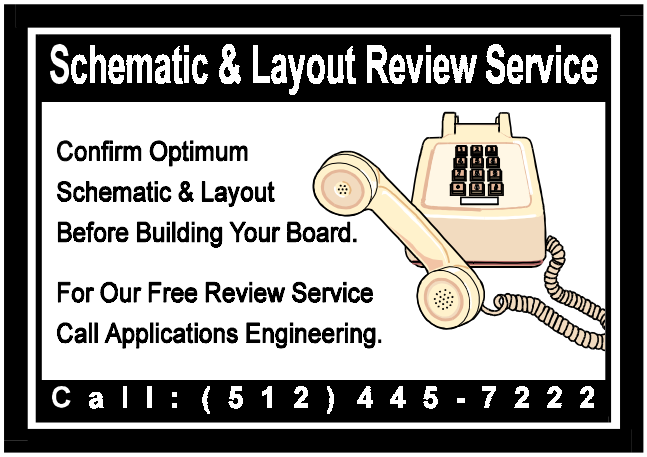
Since the CS4215 is a mixed-signal device, it is equipped with an internal register that will enable the host to perform a two-tiered test on power-up or as needed. The loopback test is enabled by setting the Enable Loopback bit, ENL, in control register 4. The first tier of loopback is a digital-digital loopback, DD, which is selected by clearing the DAD bit in control register 4 (see

Figure 16). DD loopback checks the interface between the host and the CS4215 by taking the data on SDIN and looping it back onto SDOUT, with the data on SDOUT being one frame delayed from the data on SDIN. The host can verify that the data received is exactly the same as the data sent, thereby indicating the interface between the two devices and the digital interface on the CS4215 are operating properly. The output DAC's are functional in DD loopback. Now that the interface has been verified, the rest of the CS4215 can be tested using the second tier of loopback.

The second tier of loopback is a digital-analog-digital loopback, DAD, which is selected by setting the DAD bit in control register 4. DAD loopback checks the analog section of the CS4215 by connecting the right and left analog outputs, after the output attenuator, to the analog inputs of the gain stage. This allows testing of most of the CS4215 from the host by sending a known digital signal to the DACs and monitoring the digital signal from the ADCs. During DAD loopback, the monitor attenuator must be set at maximum (full mute), and the analog outputs may be individually muted. The analog inputs are disconnected internally. The flow of test data for both DD and DAD loopback modes is illustrated in the top portion of Figure 16.

Analog-to-Analog Loopback Mode

A third loopback mode is achieved by setting the monitor attenuator to zero attenuation and sending the DACs digital zero via SDIN. This loopback is termed analog-digital-analog, ADA, since the selected analog input will now appear on the enabled analog outputs. Since this test is controlled by external stimulus and the host is not involved (except to send the DACs zeros), it is generally considered a laboratory test as opposed to a self test. The bottom portion of Figure 16 illustrates the ADA signal flow through the CS4215. Note that this test requires the host send analog zeros to the DAC. Each data format has a different code for zero. See Figures 13 and 14.



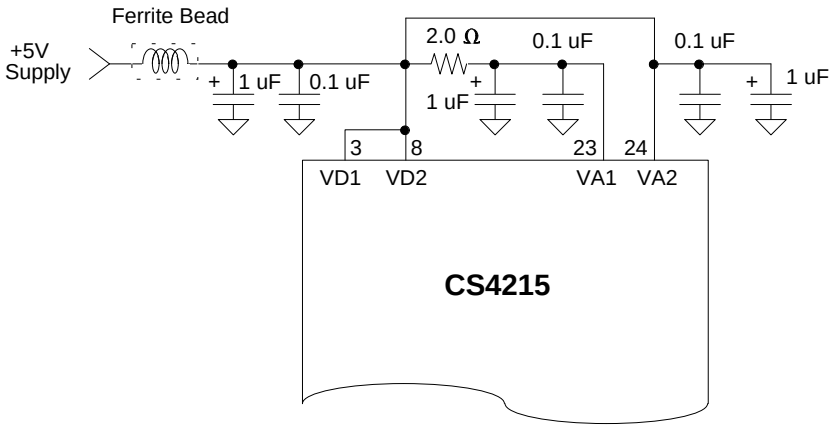


Figure 17. Optional Power Supply Arrangement

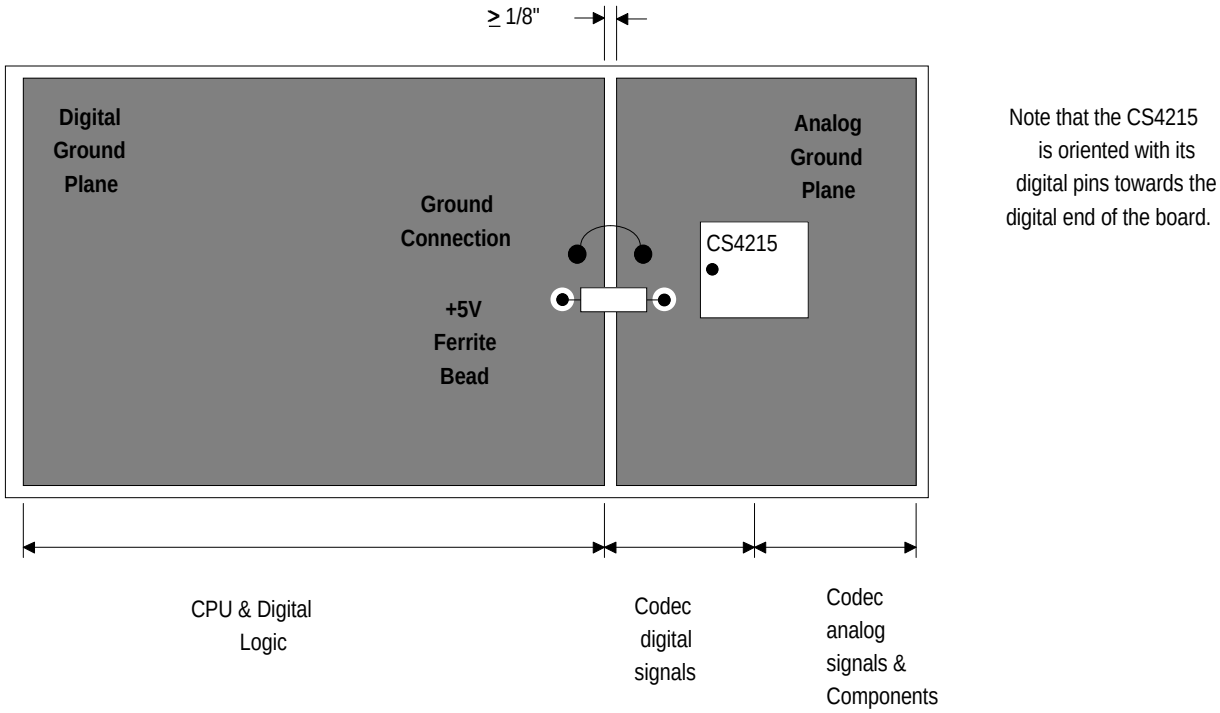


Figure 18. Suggested Layout Guideline

POWER SUPPLY AND GROUNDING

When using separate supplies, the digital power should be connected to the CS4215 via a ferrite bead, positioned closer than 1" to the device (see Figure 1). The codec VA1, VA2 pins should be derived from the cleanest power source available. If only one supply is available, use the suggested arrangement in Figure 17. VA1 supplies analog power to the ADCs and DACs while VA2 supplies power to the output power drivers (headphones and speaker). The large currents necessary for VA2 are not flowing through the 2.0 Ω resistor, and therefore do not corrupt the VA1 converter supply.

The CS4215 along with associated analog circuitry, should be positioned near to the edge of the circuit board, and have its own, separate, ground plane. On the CS4215, the analog and digital grounds are internally connected; therefore, the four ground pins must be externally connected with zero impedance between ground pins. The best solution is to place the entire chip on a solid ground plane as shown in Figure 18. Preferably, it should also have its own power plane. A single connection between the CS4215 ground and the board ground should be positioned as shown in Figure 18.

Figure 19 illustrates the optimum ground and decoupling layout for the CS4215 assuming a surface-mount socket and leaded decoupling capacitors. Surface-mount sockets are useful since the pad locations are exactly the same as the actual chip; therefore, given that space for the socket is left on the board, the socket can be optional for production. Figure 19 depicts the top layer containing signal traces and assumes the bottom or inter-layer contains a solid analog ground plane. The important points with regards to this diagram are that the ground plane is SOLID under the codec and connects all codec ground pins with thick traces providing the absolute lowest impedance between ground pins. The decoupling capacitors are placed as close as possible to the device which, in this case, is the socket boundary. The lowest value capacitor is

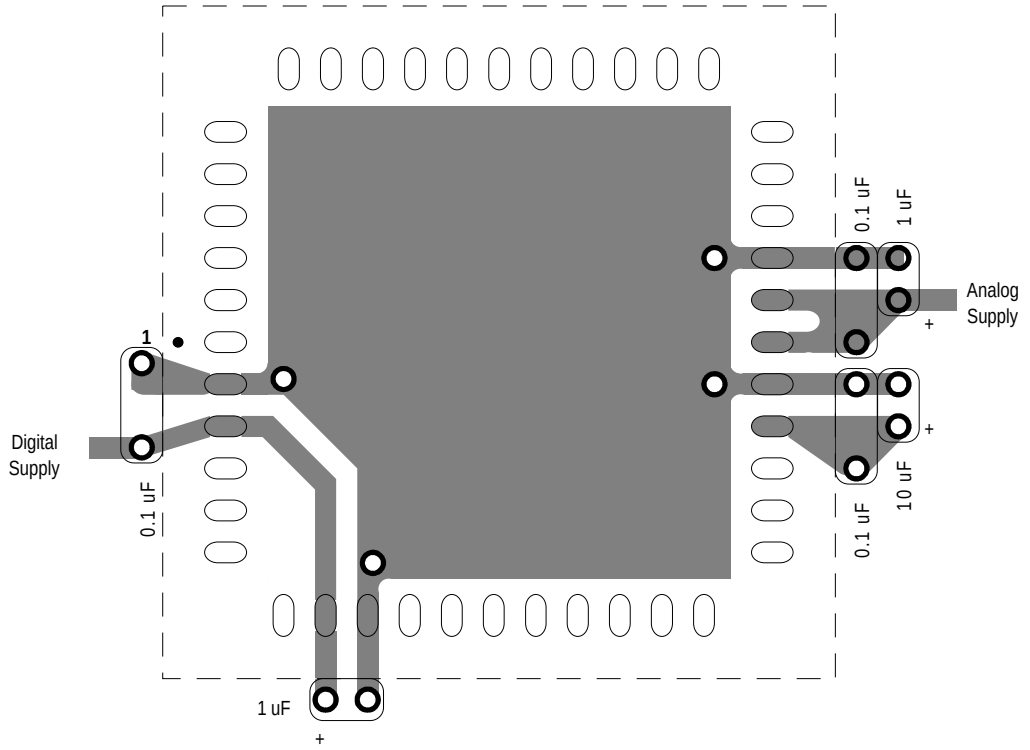


Figure 19. CS4215 Decoupling Layout Guideline

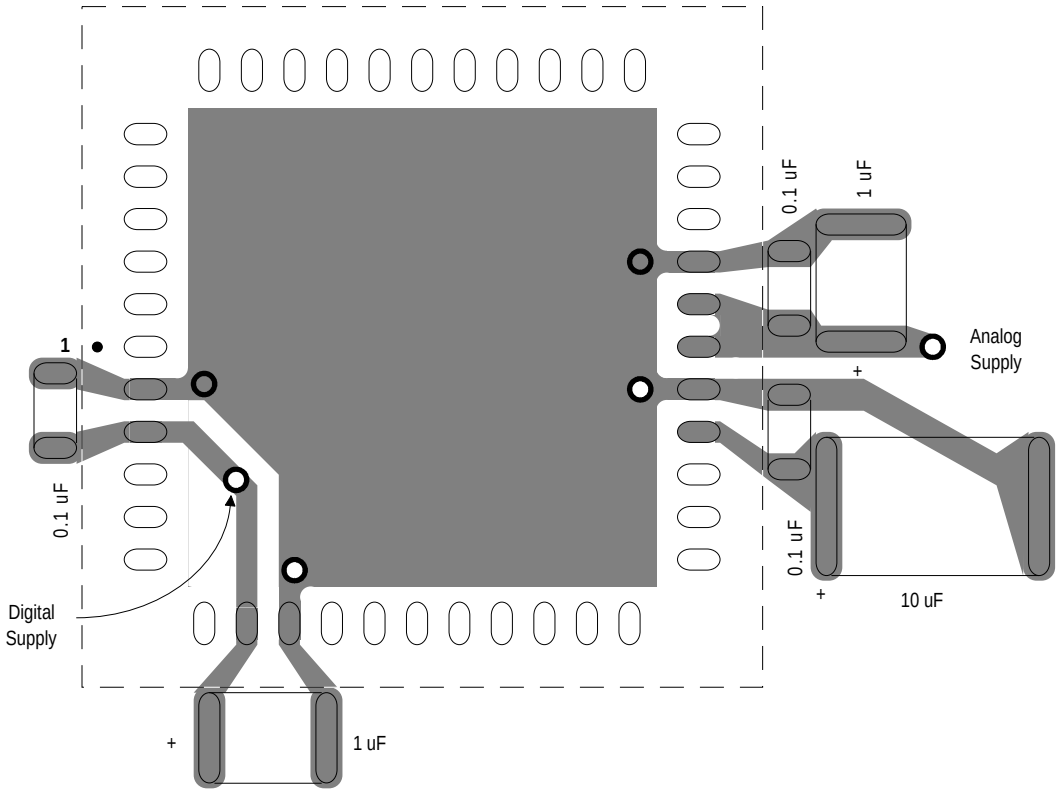


Figure 20. CS4215 Surface Mount Decoupling Layout

placed closest to the codec. Vias are placed near the AGND and DGND pins, under the IC, and should be attached to the solid analog ground plane on another layer. The negative side of the decoupling capacitors should also attach to the same solid ground plane. Traces bringing the power to the codec should be wide thereby keeping the impedance low.

Although not shown in the figures, the trace layers (top layer in the figures) should have ground plane fill in-between the traces to minimize coupling into the analog section. See the CDB4215 evaluation board data sheet for an example layout.

If using all surface-mount components, the decoupling capacitors should still be placed on the layer with the codec and in the positions shown in Figure 20. The vias shown are assumed to attach to the appropriate power and analog ground layers. Traces bringing power to the codec should be as wide as possible to keep the impedance low. For the same reason, vias should be large for power and ground runs.

If using through-hole sockets, effort should be made to find a socket with the minimum height which will minimize the socket impedance. When using a through-hole socket, the vias under the codec in Figure 19 are not needed since the pins serve the same function.

ADC and DAC Filter Response Plots

Figures 21 through 27 show the overall frequency response, passband ripple and transition band for the CS4215 ADCs and DACs. Figure 27 shows the DACs' deviation from linear phase. Fs is the selected sample frequency. Since the sample frequency is programmable, the filters will adjust to the selected sample frequency. Fs is also the FSYNC frequency.

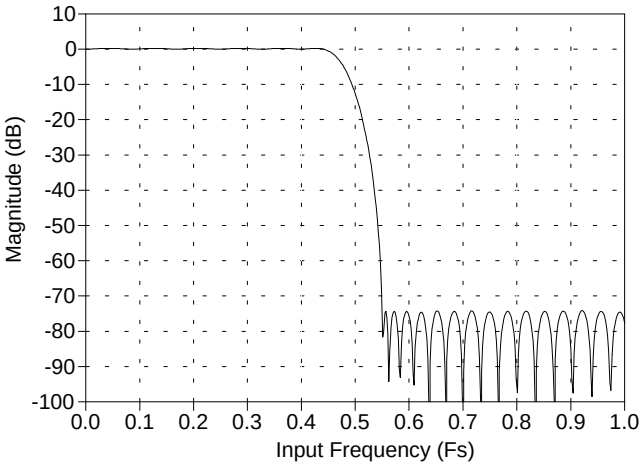


Figure 21. ADC Frequency Response

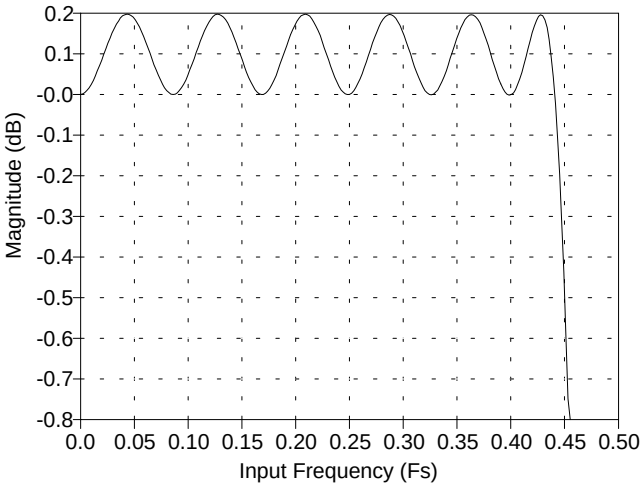


Figure 22. ADC Passband Ripple

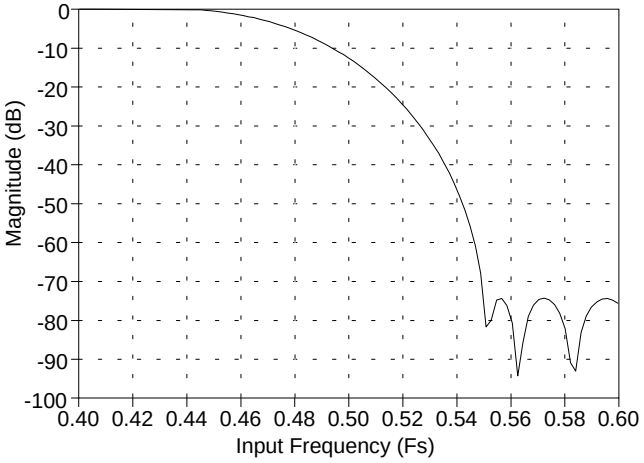


Figure 23. ADC Transition Band

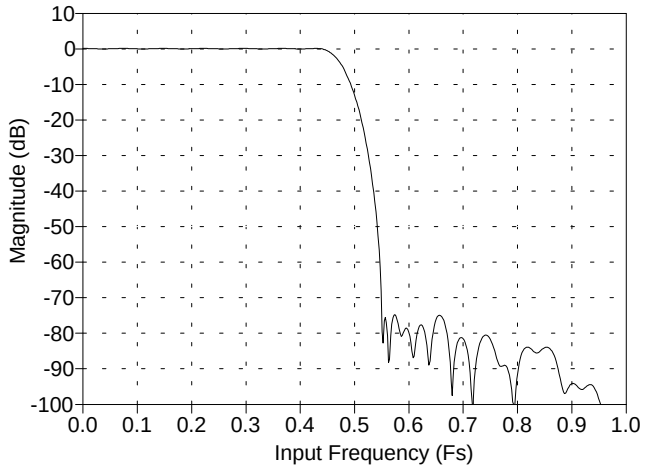


Figure 24. DAC Frequency Response

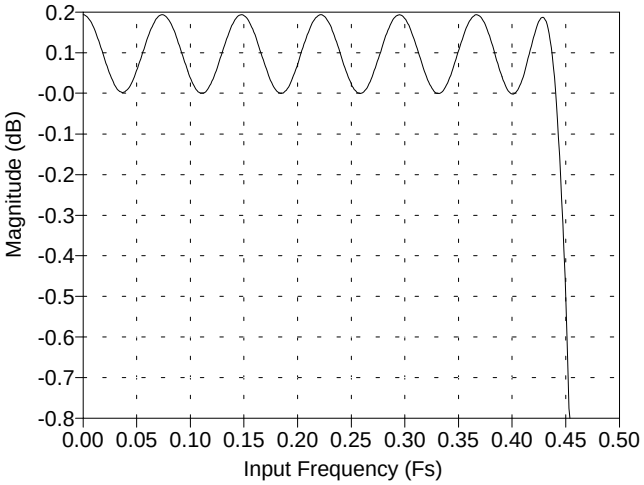


Figure 25. DAC Passband Ripple

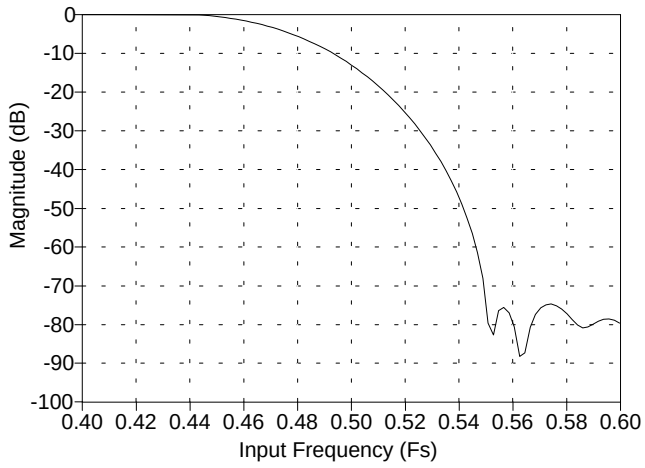


Figure 26. DAC Transition Band

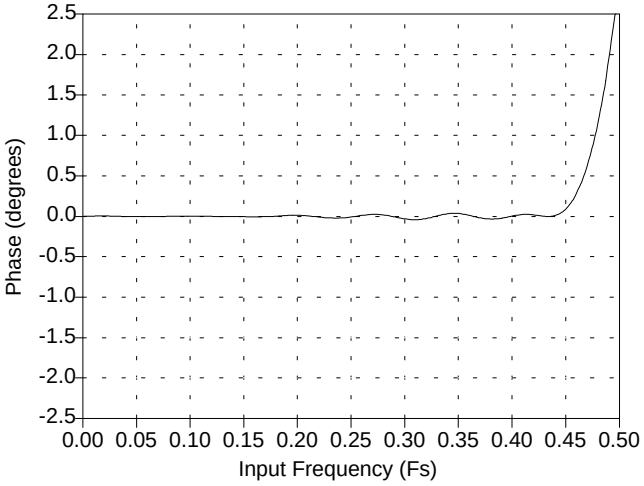
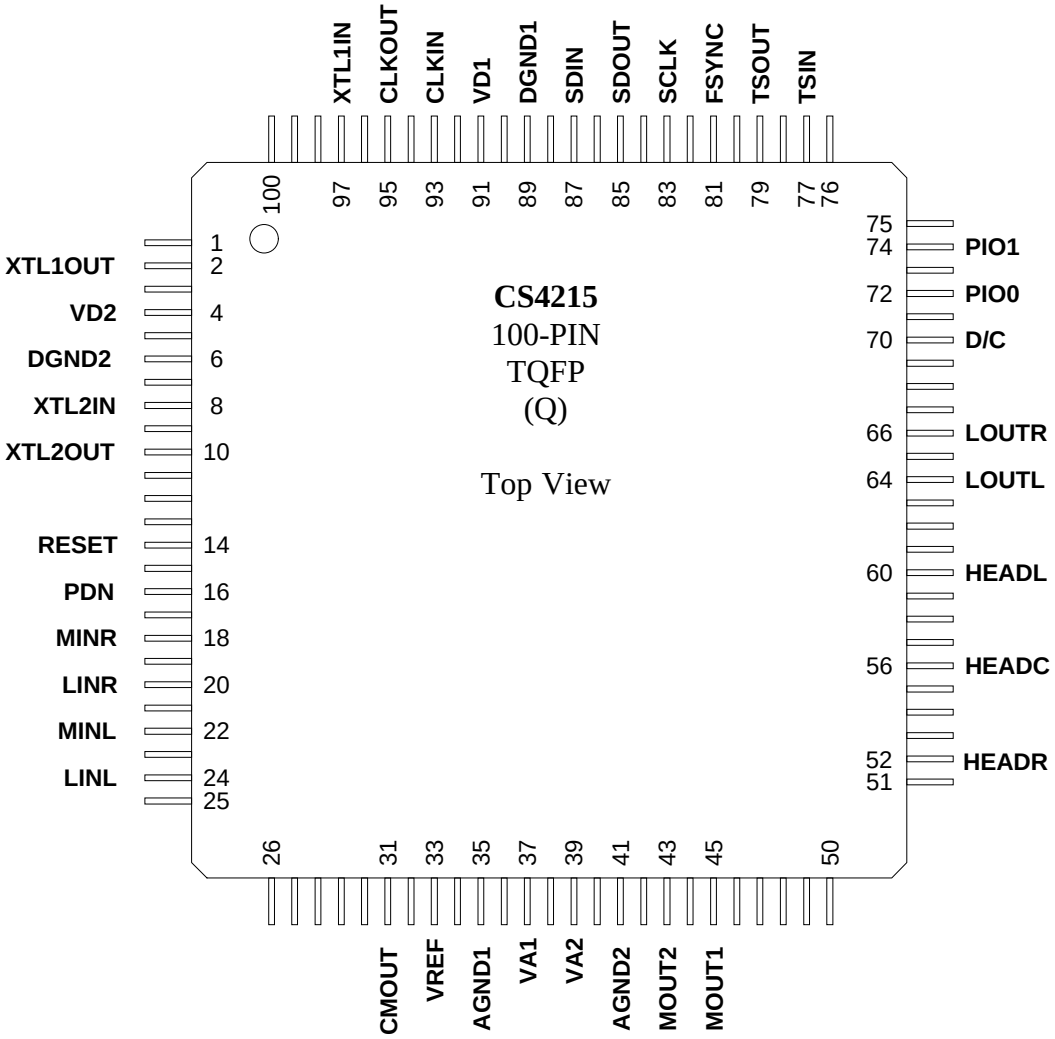
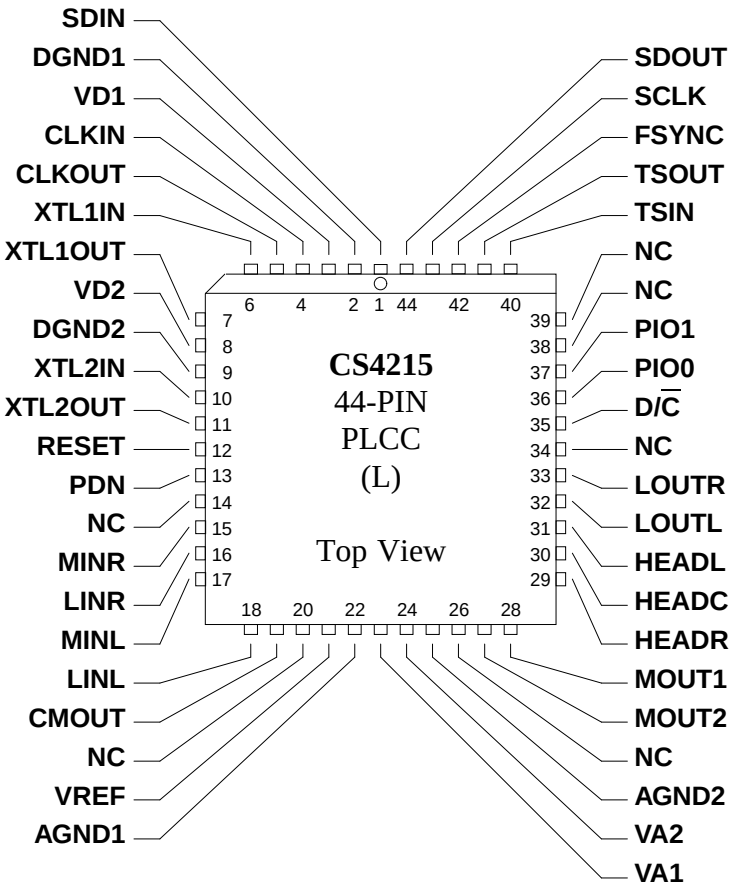


Figure 27. DAC Deviation from Linear Phase

PIN DESCRIPTIONS



Note: All unlabeled pins are No Connects



Power Supply

VA1, VA2 - Analog Power Input, Pins 23(L), 24(L), 37(Q), 39 (Q)
+5 V analog supply.

AGND1, AGND2 - Analog Ground, Pins 22(L), 25(L), 35(Q), 41(Q)
Analog ground. Must be connected to DGND1, DGND2 with zero impedance.

VD1, VD2 - Digital Power Input, Pins 3(L), 8(L), 91(Q), 4(Q)
+ 5 V digital supply.

DGND1, DGND2 - Digital Ground, Pin 2(L), 9(L), 89(Q), 6(Q)
Digital ground. Must be connected to AGND1, AGND2 with zero impedance.

Analog Inputs

LINL, LINR - Left and Right Channel Line Level Inputs, Pins 18(L), 16(L), 24(Q), 20(Q)
Line level input connections for the right and left channels.

MINL, MINR - Left and Right Channel Microphone Inputs, Pins 17(L), 15(L), 22(Q), 18(Q)
Microphone level input connections for the right and left channels.

Analog Outputs

LOUTR, LOUTL - Line Level Outputs, Pins 33(L), 32(L), 66(Q), 64(Q)
One pair of line level outputs are provided. The output level for right and left outputs can be independently varied. These outputs can be muted.

HEADR, HEADL - Headphone Outputs, Pins 29(L), 31(L), 52(Q), 60(Q)
HEADR and HEADL are intended to drive a pair of headphones. Additional current drive, along with an optional +3 dB of gain, ensures reasonable listening levels. These outputs can be muted.

HEADC - Common Return for Headphone Outputs, Pin 30(L), 56(Q)
HEADC is the return path for large currents when driving headphones from the HEADR and HEADL outputs. This pin is nominally at 2.1 V.

CMOUT - Common Mode Output, Pin 19(L), 31(Q)
Common mode voltage output. This signal may be used for level shifting the analog inputs. The load on CMOUT must be DC only, with an impedance of not less than 10kΩ. CMOUT should be bypassed with a 0.47 µF to AGND. CMOUT is nominally at +2.1V.

MOUT1, MOUT2 - Mono Speaker Outputs, Pins 28(L), 27(L), 45(Q), 43(Q)
Mono external loudspeaker differential output connections. The loudspeaker output is a mix of left and right line outputs. Independent muting of the speaker is provided. MOUT1 and MOUT2 output voltage is nominally at 2.1 V with no signal.

VREF - Voltage Reference Output, Pin 21(L), 33(Q)
The on-chip generated ADC/DAC reference voltage is brought out to this pin for decoupling purposes. This output must be bypassed with a 10 µF capacitor in parallel with a 0.1 µF capacitor to the adjacent AGND1 pin. No other external load may be connected to this output.

Digital Interface Signals

SDIN - Serial Data Input, Pin 1(L), 87(Q)
Audio data for the DACs and control information for all functions is presented to the CS4215 on this pin.

SDOUT - Serial Data Output, Pin 44(L), 85(Q)
Audio data from the ADCs and status information concerning all functions is written out by the CS4215 onto this pin.

SCLK - Serial Port Clock, Pin 43(L), 83(Q)

SCLK rising causes the data on SDOUT to be updated. SCLK falling latches the data on SDIN into the CS4215. The SCLK signal can be generated off-chip, and input into the CS4215. Alternatively, the CS4215 can generate and output SCLK in data mode.

FSYNC - Frame Sync Signal, Pin 42(L), 81(Q)

The Frame Synchronizing Signal is sampled by SCLK, with a rising edge indicating a new frame is about to start. FSYNC frequency is always the system sample rate. Each frame may have 64, 128 or 256 data bits, allowing for 1, 2 or 4 CS4215s connected to the same bus. FSYNC may be input to the CS4215, or may be generated and output by the CS4215 in data mode. When FSYNC is an input, it must be high for at least 1 SCLK period. FSYNC can stay high for the rest of the frame, but must return low at least 2 SCLKs before the next frame starts.

TSIN - Time Slot Input, Pin 40(L), 77(Q)

TSIN high for at least 1 SCLK cycle indicates to the CS4215 that the next time slot is allocated for it to use. TSIN is normally connected to the TSOUT pin of the previous device in the chain. TSIN should be connected to FSYNC for the 1st (or only) CS4215 in the chain.

TSOUT - Time Slot Output, Pin 41(L), 79(Q)

TSOUT goes high for 1 SCLK cycle, indicating that the CS4215 is about to release the data bus. Normally connected to the TSIN pin on the next device in the chain.

D/$\overline{C}$ - Data/Control Select Input, Pin 35(L), 70(Q)

When D/$\overline{C}$ is low, the information on SDIN and SDOUT is control information. When D/$\overline{C}$ is high, the information on SDIN and SDOUT is data information.

PDN - Power Down Input, Pin 13(L), 16(Q)

When high, the PDN pin puts the CS4215 into the power down mode. In this mode HEADC and CMOUT will not supply current. Power down causes all the control registers to change to the default reset state. In the power down mode, the TSOUT pin remains active, and follows TSIN delayed by less than 10 ns.

$\overline{\text{RESET}}$ - Active Low Reset Input, Pin 12(L), 14(Q)

Upon reset, the values of the control information (when D/$\overline{C}$ = 0) will be initialized to the values given in the Reset Description section of this data sheet.

Clock and Crystal Pins

XTL1IN, XTL1OUT, XTL2IN, XTL2OUT - Crystals 1 and 2 Inputs and Outputs, Pins 6(L), 7(L), 10(L), 11(L), 97(Q), 2(Q), 8(Q), 10(Q)

Input and output connections for crystals 1 and 2. One of these oscillators may provide the master clock to run the CS4215.

CLKIN - External Clock Input, Pin 4(L), 93(Q)

External clock input optionally used to clock the CS4215. The CLKIN frequency must be 256 times the maximum sample rate (FSYNC frequency).

CLKOUT - Master Clock Output, Pin 5(L), 95(Q)

Master clock output, whose frequency is always 256 times the system sample rate (FSYNC frequency). CLKOUT is active only in data mode and is low during control mode.

Miscellaneous Pins

PIO0, PIO1 - Parallel Input/Output, Pins 36(L), 37(L), 72(Q), 74(Q)

These pins are provided as general purpose digital parallel input/output and have open drain outputs. An external pull-up resistor is required. They can be read in control mode, and read and written to in data mode.

Note: All unlabeled pins are No Connects which should be left floating.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal codewidth. Units in LSB.

Total Dynamic Range

The rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (ie. attenuation bits for the DACs at full attenuation.) Units in dB.

Instantaneous Dynamic Range

The dynamic range available at any instant in time. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces to harmonic distortion components of the noise to insignificance. Units in dB.

Total Harmonic Distortion

THD is the ratio of the rms value of a signal's first five harmonic components to the rms value of the signals fundamental component. THD is calculated for the ADCs using an input signal which is 3dB below typical full-scale, and is referenced to typical full-scale. A digital full-scale output is used to calculate THD for the DACs.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz 0 dB signal present on the other channel. Units in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Frequency Response

Worst case variation in output signal level versus frequency over 10 Hz to 20 kHz. Units in dB.

Step Size

Typical delta between two adjacent gain or attenuation values. Units in dB.

Absolute Step Error

The deviation of a gain or attenuation step from a straight line passing through the no-gain/attenuation value and the full-gain/attenuation value (i.e. end points). Units in dB.

Out-of-Band Energy

The ratio of the rms sum of the energy from 0.46xFs to 2.1xFs compared to the rms full-scale signal value. Tested with 48kHz Fs giving an out-of-band energy range of 22kHz to 100kHz.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input at CMOUT. For the DACs, the deviation of the output from CMOUT with mid-scale input code. Units in volts.

APPENDIX A

This data sheet describes version 2 of the CS4215. Therefore, this appendix is included to describe the differences between versions 0,1 and version 2. This information is only useful for users that still have version 0 and version 1 devices since version 2 devices will supplant the earlier versions. The version number can be found in control mode, time slot 7. The version can also be identified by the revision letter stamped on the top of the actual chip. The revision letter immediately precedes the data code on the second line of the package marking (See *General Information* section of the Crystal Data Book). Version 0 corresponds to chip revision C, version 1 corresponds to chip revision D, and version 2 corresponds to chip revision E. Future chip revisions (ie. F, G, H) may still be version 2 since the version number only changes if there is a register change to the part that will affect driver software.

The Functional Differences Between Version 0(Rev. C) and Version 1(Rev. D)

1. FSYNC on version 0 must be ONLY one SCLK period high, whereas on version 1 FSYNC must be AT LEAST one SCLK period high.

2. When driving an external CMOS clock into one of the XTL-IN pins, version 0 devices must have a series resistor of at least 1kΩ between the CS4215 and the clock source. The resistor is needed because the codec will put XTL-IN to ground (on version 0 only) when that crystal is not selected, as is the case on power-up. In version 1 the XTL-IN pins are floated when not selected; therefore, the series resistor is not needed on version 1. Version 1 will work properly if the resistor is included.

3. The OLB and ITS bits do not exist on version 0. Writing these bits as zero makes both versions function identically; therefore, version 1 is backwards compatible with version 0.

4. When entering control mode, CLKOUT stops 4 to 12 clocks later and may start up briefly when switching master clock sources on version 0. On version 1 CLKOUT stops within two clocks and doesn't start up until data mode is entered.

5. In version 0 the headphone and speaker outputs are not short-circuit protected, whereas in version 1 they are short-circuited protected.

The functional differences between Version 1(Rev. D) and Version 2(Rev. E)

1. The MLB, HPF, and MCK2 bits in control mode do not exist in version 0 or version 1. Writing these bits as zero makes all versions functionally identical; therefore, version 2 is backwards compatible with previous versions.

2. The A/D invalid bit, ADI, in data mode does not exist in version 0 or version 1.

3. The 8-bit unsigned data format (DF1,0=3) does not exist in version 0 or version 1.

4. SDOUT contained random data during calibration in versions 0 and 1. SDOUT outputs zeros during calibration in version 2.

Semiconductor Corporation

CDB4215

CS4215 Evaluation Board

Features

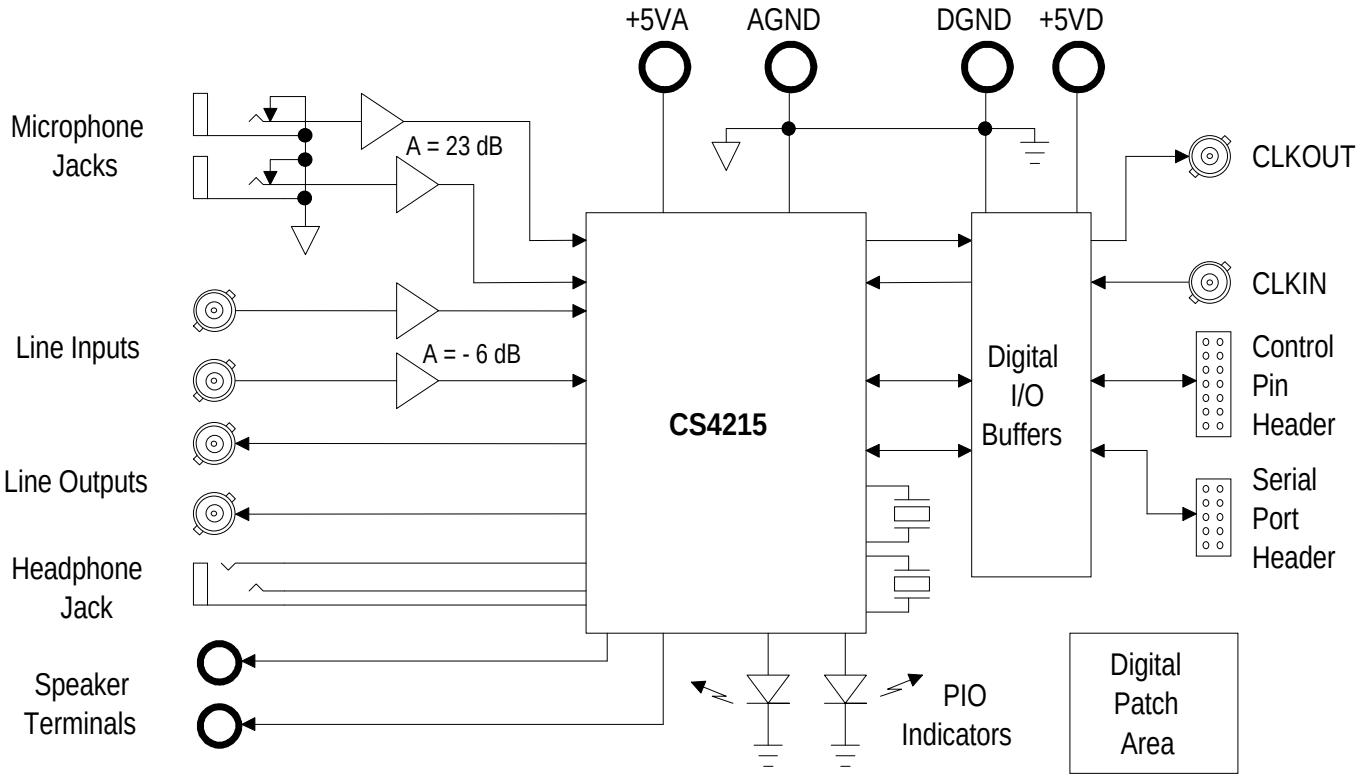
- Easy DSP Hook-Up
- Correct Grounding and Layout
- Microphone Pre-Amplifier
- Line Input Buffer
- Digital Patch Area

General Description

The CDB4215 evaluation board allows easy evaluation of the CS4215 audio multimedia codec. Analog inputs provided include two $^1/_4$" microphone jacks and two BNC line inputs. Analog outputs provided are two BNC line outputs, one stereo $^1/_4$" headphone jack and one pair of speaker terminals.

Digital interfacing is facilitated by two buffered ribbon cable headers. One contains the serial port and the other contains the codec control pins.

ORDERING INFORMATION: CDB4215



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

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GENERAL INFORMATION

The CDB4215 is designed to provide an easy platform for evaluating the performance of the CS4215 Multimedia Audio Codec. The board provides a buffered serial interface for easy connection to the serial port of a DSP or other serial device. A single +5 V power supply is all that is required to power the evaluation board.

The line input buffers are designed to accept standard CD-level inputs of 2 V_{RMS} and BNC-to-phono adapters are included to support various test setups. The microphone inputs consist of two $^1/_4$" mono jacks that are designed to accept standard single-ended dynamic or condenser microphones.

The line outputs are supplied via BNC jacks with two more BNC-to-phono adapters. The headphone output is supplied via a $^1/_4$" stereo jack and will drive headphones of 48 Ω or greater. This includes most "walkman" style headphones. Speaker terminals are provided and can be connected to speakers with an impedance of 32 Ω or greater.

The film plots of the board are included to provide an example of the optimum layout, grounding, and decoupling arrangement for the CS4215.

POWER SUPPLY CIRCUITRY

Figure 1 illustrates a portion of the CDB4215 schematic and includes the CS4215 codec along with power supply circuitry. Power is supplied to the board via two sets of binding posts, one for digital and one for analog. The analog supply must be +5 Volts and supplies power for the entire codec (both digital and analog power supply pins) along with the analog input buffers for the line and microphone inputs. The digital supply is also +5 Volts and supplies power to the digital header buffer circuitry. Space for a ferrite bead inductor, L1, has been provided so that the board may be modified to power the codec from the digital supply. Selection of L1 will depend on the characteristics of the noise on the digital supply used.

ANALOG INPUTS

The analog inputs consist of a pair of $^1/_4$" jacks for two microphones, and a pair of BNC's for line level inputs. BNC-to-phono adapters are included to allow testing of the line inputs using coax or standard audio cables.

The line-level inputs go through a buffer, Figure 2, with a gain of 0.5 which allows input signals of up to 2 V_{RMS}.

The two microphone inputs are single-ended and are designed to work with both condenser and dynamic mics. The microphone input buffer circuit, shown in Figure 3, has a gain of 23 dB thereby defining a full-scale input voltage to the mic jacks of 19.5 mVpp.

ANALOG OUTPUTS

The CDB4215 includes three analog output paths: a pair of line output BNC's, a stereo $^1/_4$" headphone jack, and a pair of mono speaker terminals.

The CS4215 drives the line outputs into an R-C filter and then to a pair of BNC's. As with the line inputs, BNC-to-phono adapters are provided for flexibility. The line outputs can drive an impedance of 10 kΩ or more, which is the typical input impedance of most audio gear.

The stereo headphone output can drive headphones with an impedance of 48 Ω or greater. This includes most "walkman" style headphones.

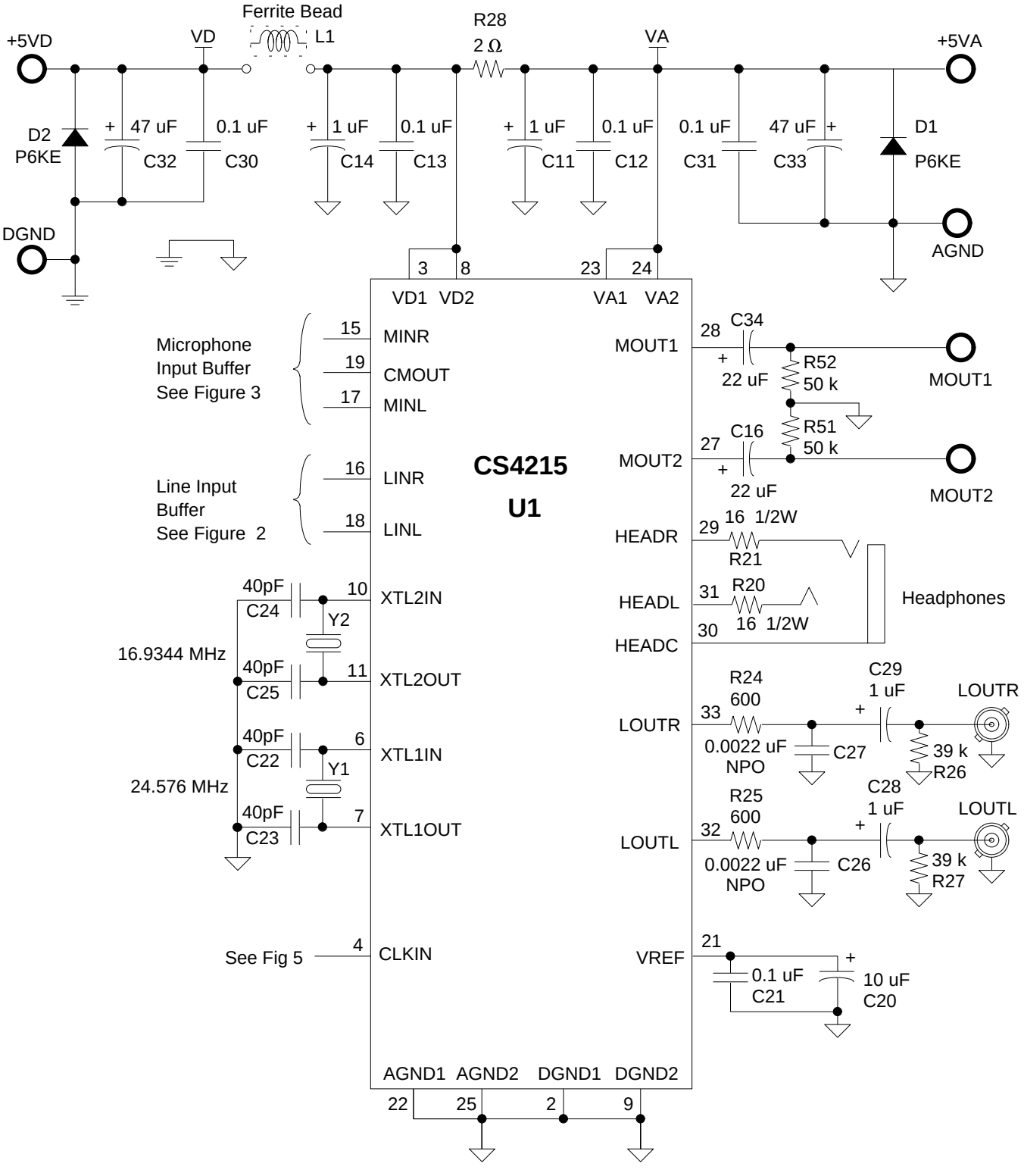


Figure 1. CS4215 & Power Supplies

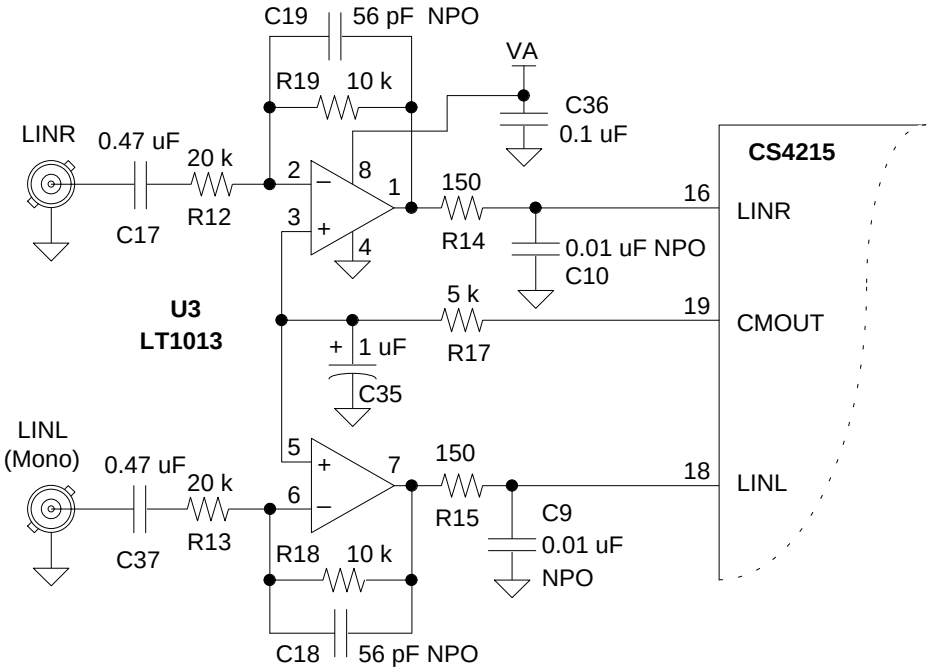


Figure 2. Line Input Buffer

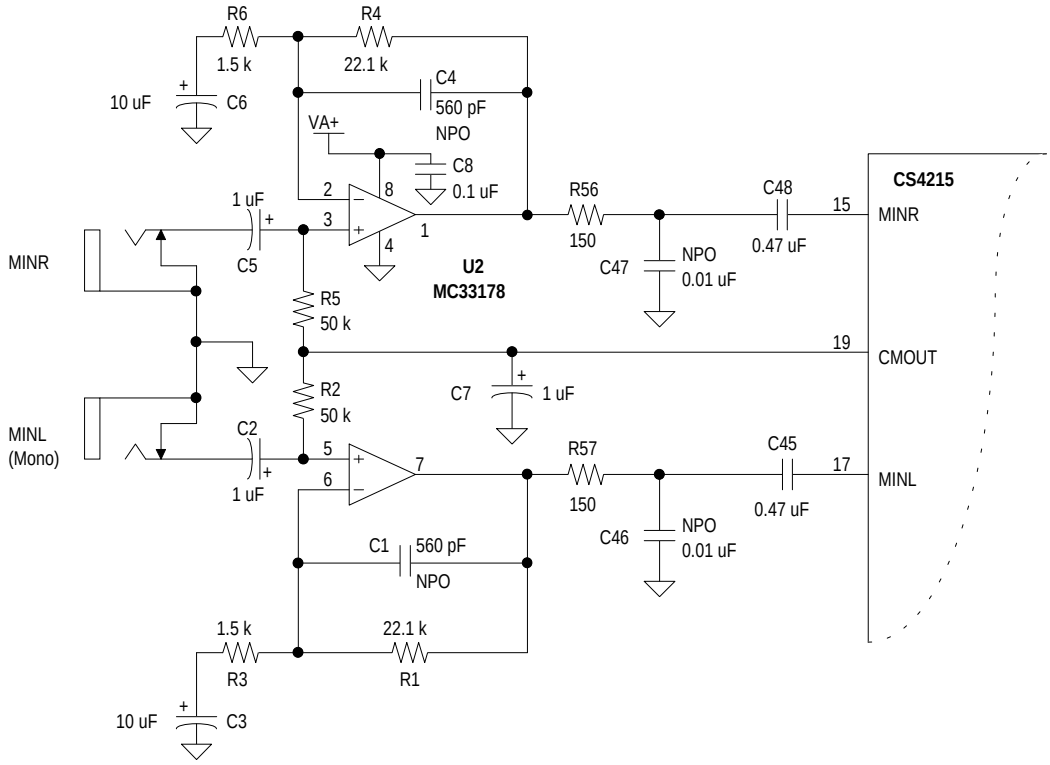


Figure 3. Microphone Input Buffer

Speaker terminals are provided and are labeled MOUT1 and MOUT2. Speakers connected to the terminals must have an impedance of 32 Ω or greater. DC blocking capacitors are included to form a high-pass filter with the speaker impedance. This filter blocks very low frequency signals which can heavily distort some inexpensive speakers.

SERIAL INTERFACE

The CDB4215 is primarily designed to evaluate the CS4215 is single chip mode, i.e. only one codec on the serial bus. This is the default state for the CDB4215 and is defined by having the P4 jumper in the "1CHIP" position, see Figure 4, which connects FSYNC to TSIN. This connection defines the board codec's time slots as the first 64 bits of the frame. The only signals that need to be connected to the DSP are the five signals on header J15. The serial interface is illustrated in Figure 4.

If the goal is to connect multiple CDB4215s on the same serial port, jumper P4 must be in the "MULTI" position which disconnects TSIN from FSYNC. The MULTI position also connects an unbuffered SDOUT to header J14. This header pin, SDOUTUB, must be used in lieu of SDOUT since SDOUT is buffered and does not go high impedance during other codec's time slots. Using the multi-chip scenario, the TSIN header pin must be connected to the previous codec's TSOUT line and the first codec's TSIN must be connected, via the header, to FSYNC.

Note that when P4 is in the 1CHIP mode, the SDOUTUB pin on header J14 is not connected to the SDOUT pin on the CS4215 and is floating.

There are two scenario's that must be addressed when connecting the CDB4215 to a DSP: one is when the codec is the master in data mode and the other is when the codec is a slave in data mode. In control mode the codec is always a slave and FSYNC and SCLK must be driven from the DSP. Since the evaluation board buffers all the signals between the codec and the DSP, the board must "know" which of the two modes is being used. Jumper P3 selects the particular mode.

Codec Master Data Mode

When the codec is to be programmed as a master in data mode, the direction of FSYNC and SCLK have to be changed between control mode and data mode. In this case the P3 jumper must be set for "M/S" which uses the D/$\overline{C}$ signal to control the direction of the buffers (U7) for SCLK and FSYNC. When P3 is set to M/S, the buffers drive the J15 header in data mode and receives FSYNC and SCLK from the header in control mode.

Codec Slave Data Mode

When the codec is to be programmed as a slave in data mode, FSYNC and SCLK are always inputs to the codec. In this mode P3 must be set to "SLAVE" which configures the FSYNC and SCLK buffers to always receive FSYNC and SCLK from the J15 header.

As stated in the CS4215 data sheet, when the codec is programmed in slave mode, XCLK = 0 in control mode, SCLK and FSYNC are inputs and must be derived from the same clock used as the master clock for the codec. Although SCLK and FSYNC must be frequency locked to the master clock, there is no phase requirement.

CONTROL PINS

All control pins, located on header J14, are defined as pins that are not essential to the DSP serial port when used in 1CHIP mode.

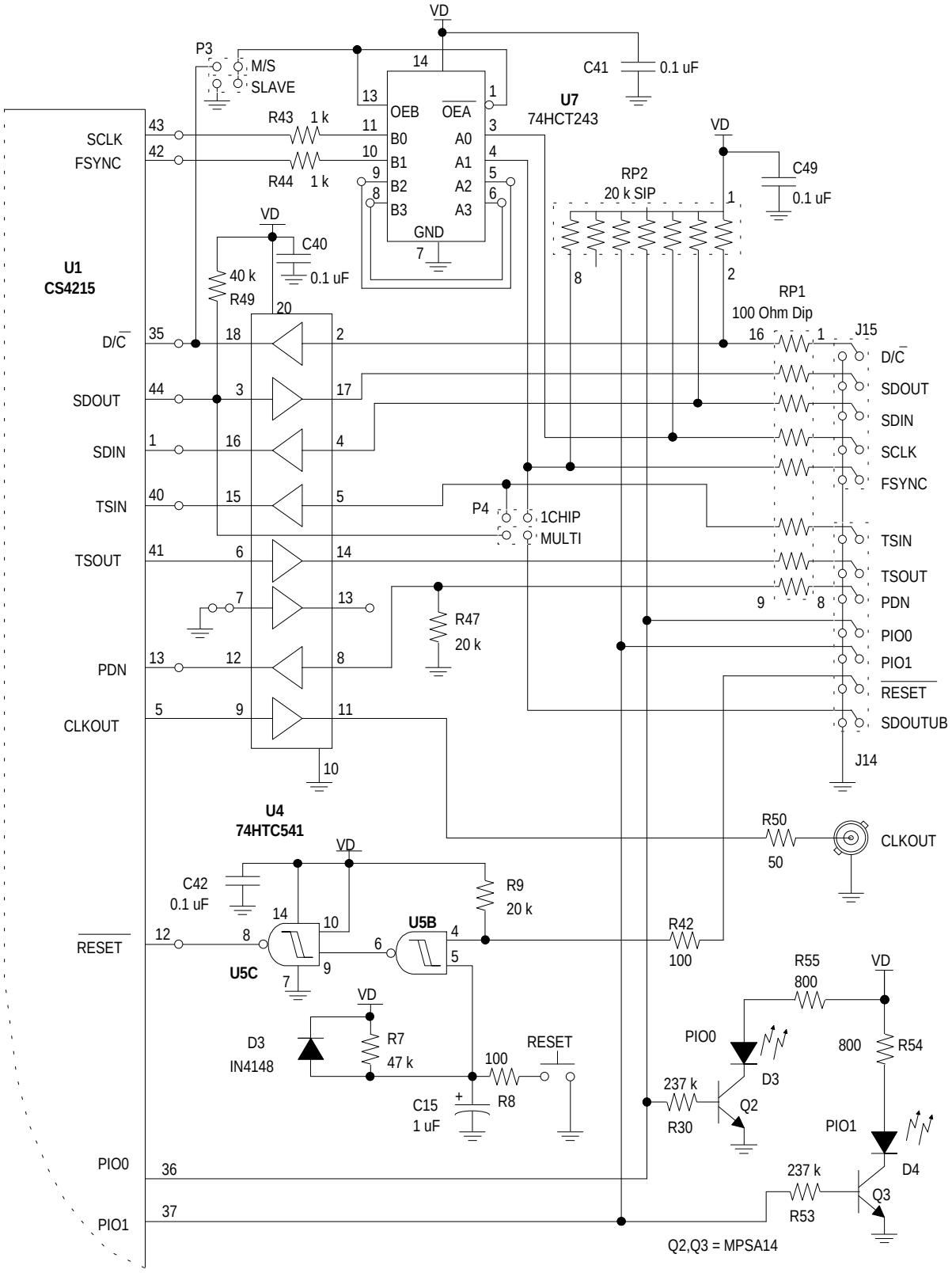


Figure 4. Digital Interface

PDN and $\overline{RESET}$

Power down, PDN, controls the PDN pin on the codec. The line has an on-board pull-down resistor thereby defining the default state as powered. This pin only needs to be controlled if the power down feature is used.

$\overline{\text{RESET}}$ controls the $\overline{\text{RESET}}$ pin on the codec and is pulled up on the board. This defines the default state as not reset. This pin only needs to be controlled if the reset feature on the codec is needed. Since the codec does require a reset at power up, a power-up reset circuit is included on the board. A reset switch is also included to reset the device without having to remove the power supply. The power-up reset plus switch are logically OR'ed with the $\overline{\text{RESET}}$ pin on header J14.

PIO Lines

The parallel input/output, PIO, lines are pulled up on the evaluation board. If they are to be used as inputs, they should be driven by open-collector gates since inadvertently setting the PIO bits low in software will force the external lines low. The PIO lines are available on header J14.

The PIO lines also go through a high-impedance buffer and drive LED's on the evaluation board. When the LED is on, the corresponding bit is 1 or high. The LED's provide a visual indication that may be used to verify that the software is writing the bits correctly.

CLOCKS

The CDB4215 can accommodate all clocking modes supported by the CS4215. A CLKIN BNC, as shown in Figure 5 allows the CLKIN pin on the CS4215 to be used as the master clock source. The two crystals listed in the CS4215 data sheet are also provided and support all the audio and multimedia standard sample frequencies. The master clock is selected via a CS4215 internal register from control mode.

The CLKOUT BNC is a buffered version of the CLKOUT pin on the CS4215. CLKOUT is always 256 times the programmed sample frequency in data mode. CLKOUT is held low in control mode.

LAYOUT ISSUES

Figure 6 contains the silk screen, Figure 7 contains the top-side copper layer, and Figure 8 contains the bottom-side copper layer of the CDB4215 evaluation board. These plots are included to provide an example of how to layout a PCB for the codec. Two of the more important aspects are the position of the ground plane split, which is next to the part - *NOT UNDER IT*, and the ground plane fill between traces on both layers, which minimizes coupling of radiated energy.

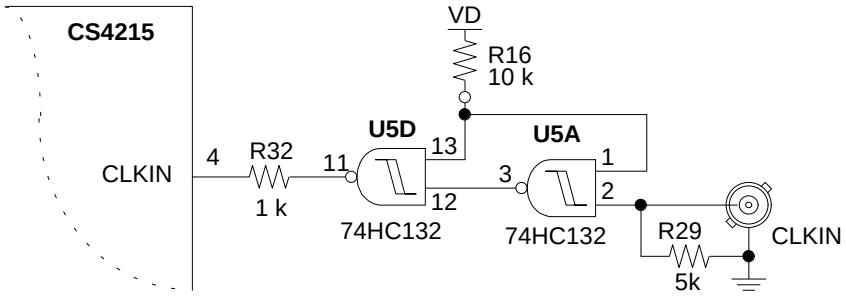


Figure 5. CLKIN

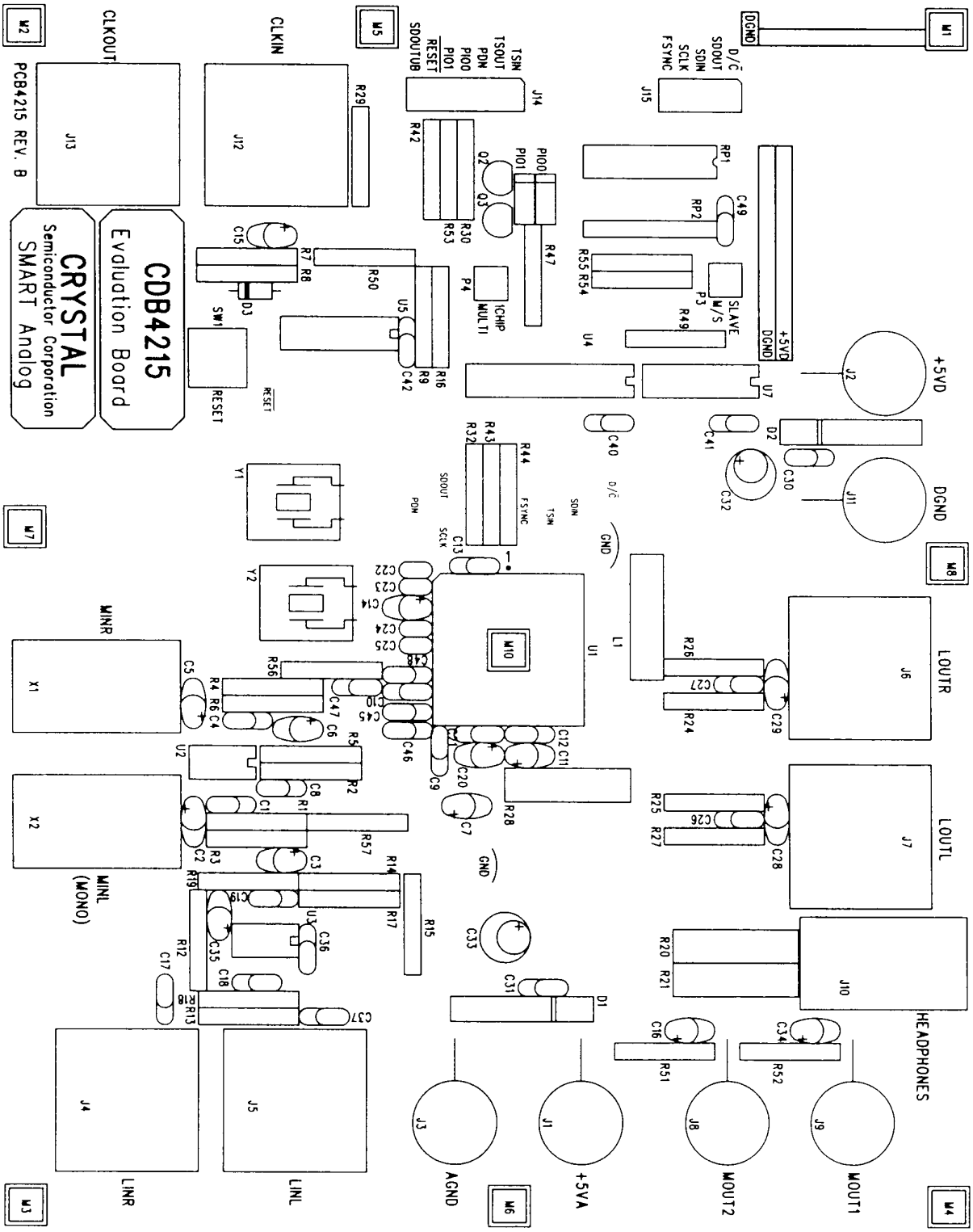


Figure 6. CDB4215 Board Silkscreen (Not to Scale)

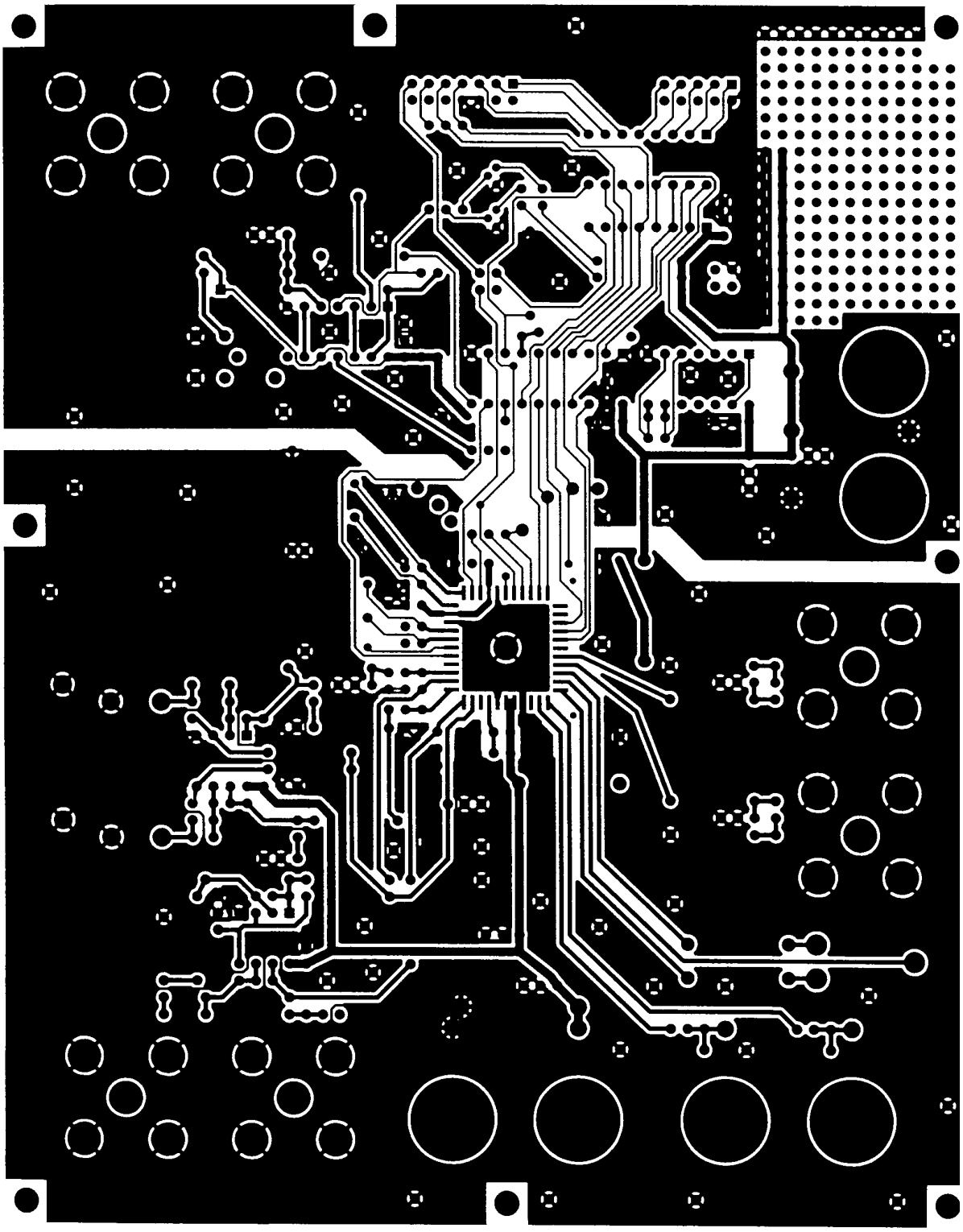


Figure 7. CDB4215 Compont Side Layout (Not to Scale)

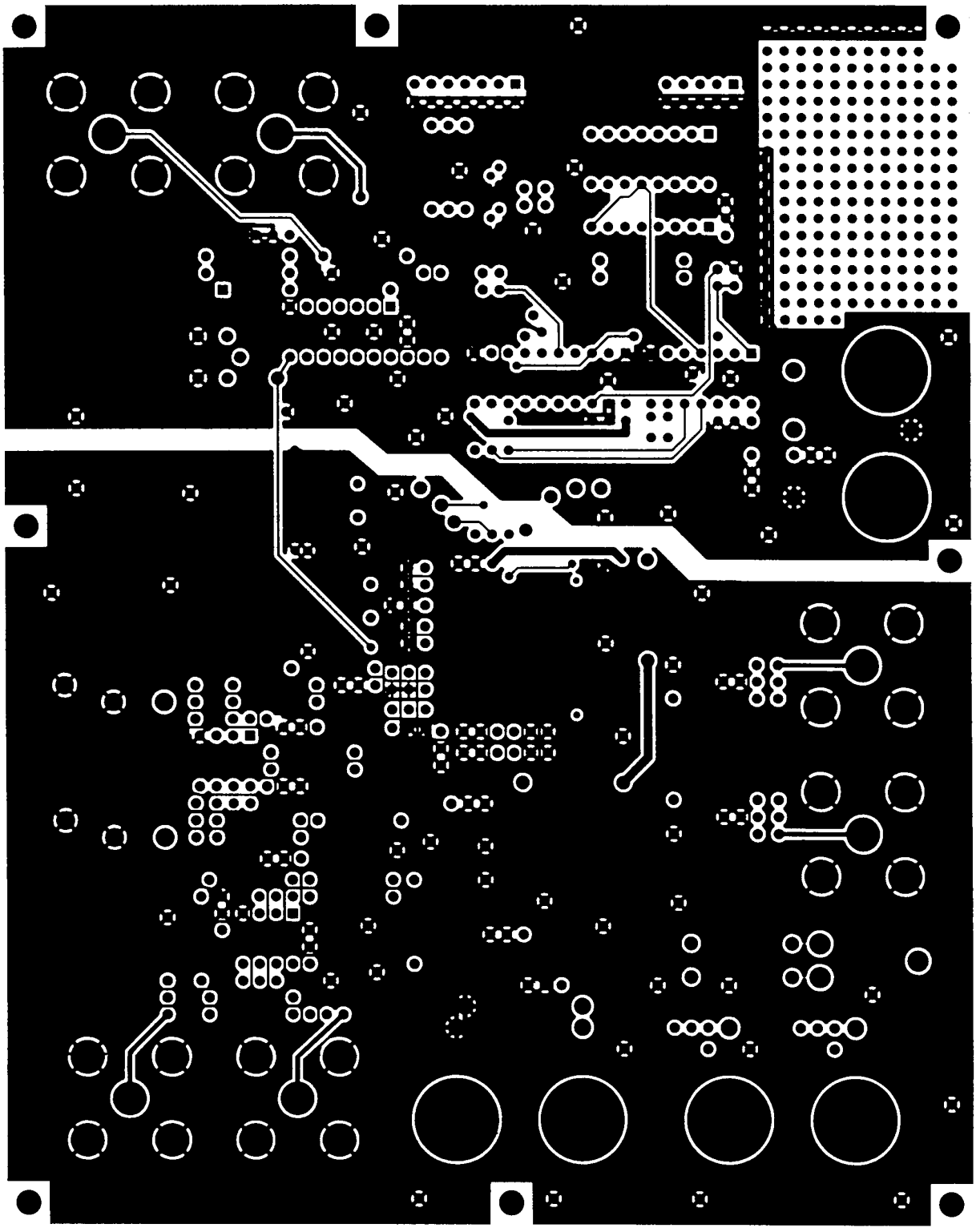
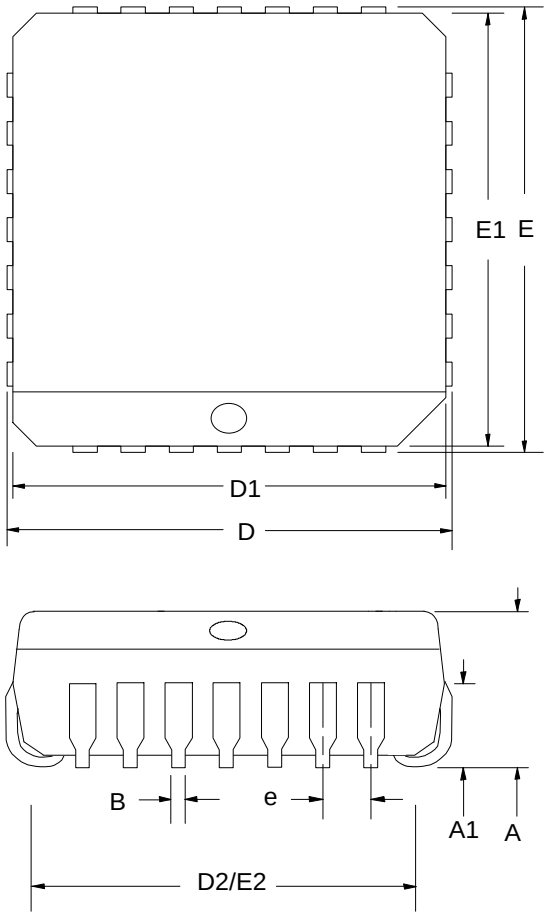
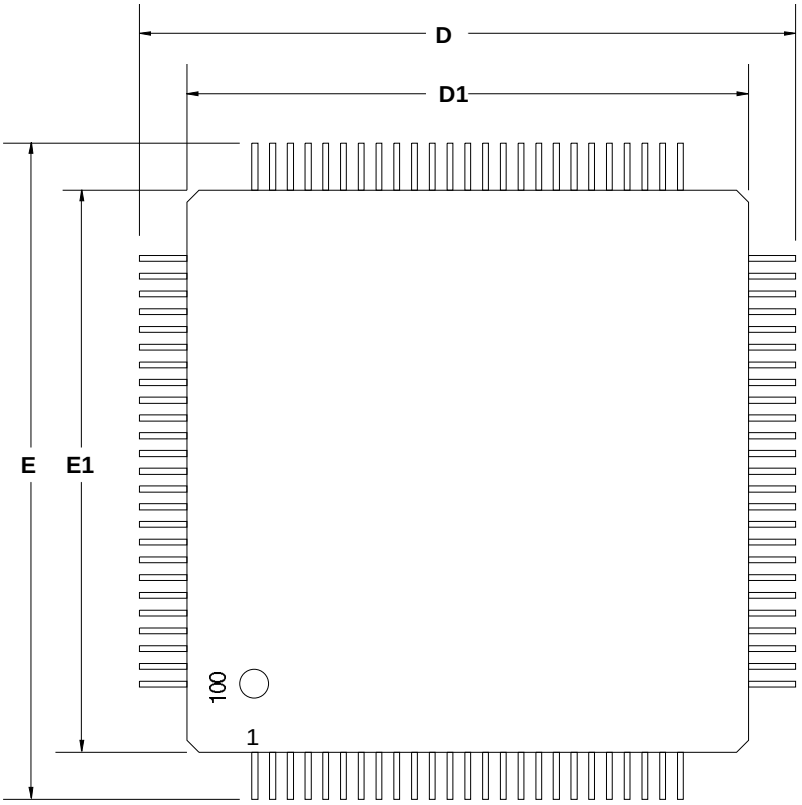


Figure 8. CDB4215 Solder Side Layout (Not to Scale)

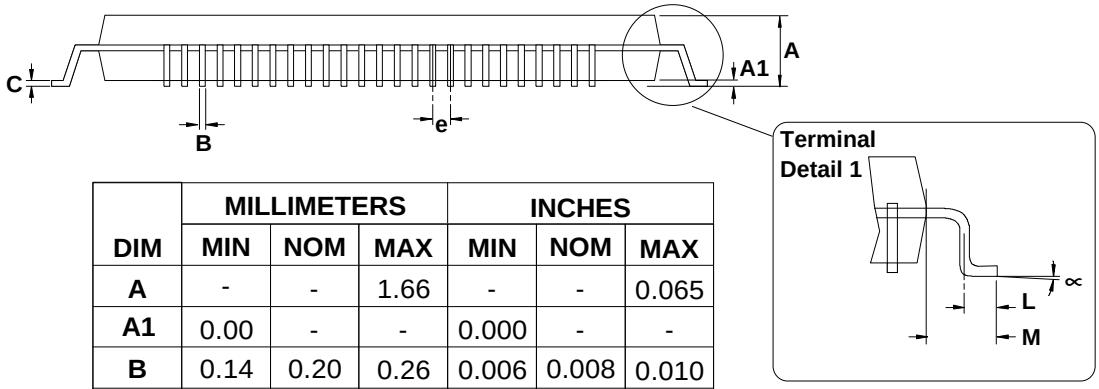


44 pin
PLCC

DIM	NO. OF TERMINALS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.20	4.45	4.57	0.165	0.175	0.180
A1	2.29	2.79	3.04	0.090	0.110	0.120
B	0.33	0.41	0.53	0.013	0.016	0.021
D/E	17.40	17.53	17.65	0.685	0.690	0.695
D1/E1	16.51	16.59	16.66	0.650	0.653	0.656
D2/E2	14.99	15.50	16.00	0.590	0.610	0.630
e	1.19	1.27	1.35	0.047	0.050	0.053



100 pin TQFP



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.66	-	-	0.065
A1	0.00	-	-	0.000	-	-
B	0.14	0.20	0.26	0.006	0.008	0.010
C	0.40	0.51	0.60	0.016	0.020	0.024
D	15.70	16.00	16.30	0.618	0.630	0.642
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.70	16.00	16.30	0.618	0.630	0.642
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.375	0.5	0.625	0.015	0.020	0.025
L	0.30	0.51	0.70	0.012	0.020	0.028
∝	0°	-	12°	0°	-	12°
M	1.00 BSC			0.039 BSC		

• Notes •



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