



256MB – 32Mx64 DDR SDRAM UNBUFFERED, w/PLL

FEATURES

- DDR266 and DDR333
- Double-data-rate architecture
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect
- Power supply: 2.5V ± 0.20V
- Standard 200 pin SO-DIMM package
 - Package height options:
 - BD4: 31.75mm (1.25")

DESCRIPTION

The WV3EG6434S is a 32Mx64 Double Data Rate SDRAM memory module based on 256Mb DDR SDRAM component. The module consists of eight 32Mx8 DDR SDRAMs in BGA package mounted on a 200 Pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

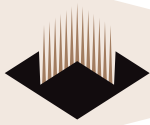
* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:

- Lead-Free or RoHS Products
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	DDR333 @CL=2.5	DDR266 @CL=2	DDR266 @CL=2.5
Clock Speed	166MHz	133MHz	133MHz
CL-tRCD-tRP	2.5-3-3	2-2-2	2.5-3-3



PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{REF}	51	V _{SS}	101	A9	151	DQ42
2	V _{REF}	52	V _{SS}	102	A8	152	DQ46
3	V _{SS}	53	DQ19	103	V _{SS}	153	DQ43
4	V _{SS}	54	DQ23	104	V _{SS}	154	DQ47
5	DQ0	55	DQ24	105	A7	155	V _{CC}
6	DQ4	56	DQ28	106	A6	156	V _{CC}
7	DQ1	57	V _{CC}	107	A5	157	V _{CC}
8	DQ5	58	V _{CC}	108	A4	158	*CK1#
9	V _{CC}	59	DQ25	109	A3	159	V _{SS}
10	V _{CC}	60	DQ29	110	A2	160	*CK1
11	DQS0	61	DQS3	111	A1	161	V _{SS}
12	DM0	62	DM3	112	A0	162	V _{SS}
13	DQ2	63	V _{SS}	113	V _{CC}	163	DQ48
14	DQ6	64	V _{SS}	114	V _{CC}	164	DQ52
15	V _{SS}	65	DQ26	115	A10/AP	165	DQ49
16	V _{SS}	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	V _{CC}
18	DQ7	68	DQ31	118	RAS#	168	V _{CC}
19	DQ8	69	V _{CC}	119	WE#	169	DQS6
20	DQ12	70	V _{CC}	120	CAS#	170	DM6
21	V _{CC}	71	NC	121	CS0	171	DQ50
22	V _{CC}	72	NC	122	*CS1#	172	DQ54
23	DQ9	73	NC	123	NC	173	V _{SS}
24	DQ13	74	NC	124	NC	174	V _{SS}
25	DQS1	75	V _{SS}	125	V _{SS}	175	DQ51
26	DM1	76	V _{SS}	126	V _{SS}	176	DQ55
27	V _{SS}	77	*DQS8	127	DQ32	177	DQ56
28	V _{SS}	78	*DM8	128	DQ36	178	DQ60
29	DQ10	79	NC	129	DQ33	179	V _{CC}
30	DQ14	80	NC	130	DQ37	180	V _{CC}
31	DQ11	81	V _{CC}	131	V _{CC}	181	DQ57
32	DQ15	82	V _{CC}	132	V _{CC}	182	DQ61
33	V _{CC}	83	NC	133	DQS4	183	DQS7
34	V _{CC}	84	NC	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	V _{SS}
36	V _{CC}	86	NC	136	DQ38	186	V _{SS}
37	CK0#	87	V _{SS}	137	V _{SS}	187	DQ58
38	V _{SS}	88	V _{SS}	138	V _{SS}	188	DQ62
39	V _{SS}	89	*CK2	139	DQ35	189	DQ59
40	V _{SS}	90	V _{SS}	140	DQ39	190	DQ63
41	DQ16	91	*CK2#	141	DQ40	191	V _{CC}
42	DQ20	92	V _{CC}	142	DQ44	192	V _{CC}
43	DQ17	93	V _{CC}	143	V _{CC}	193	SDA
44	DQ21	94	V _{CC}	144	V _{CC}	194	SA0
45	V _{CC}	95	*CKE1	145	DQ41	195	SCL
46	V _{CC}	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	V _{CCSPD}
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	V _{SS}	199	NC
50	DQ22	100	A11	150	V _{SS}	200	NC

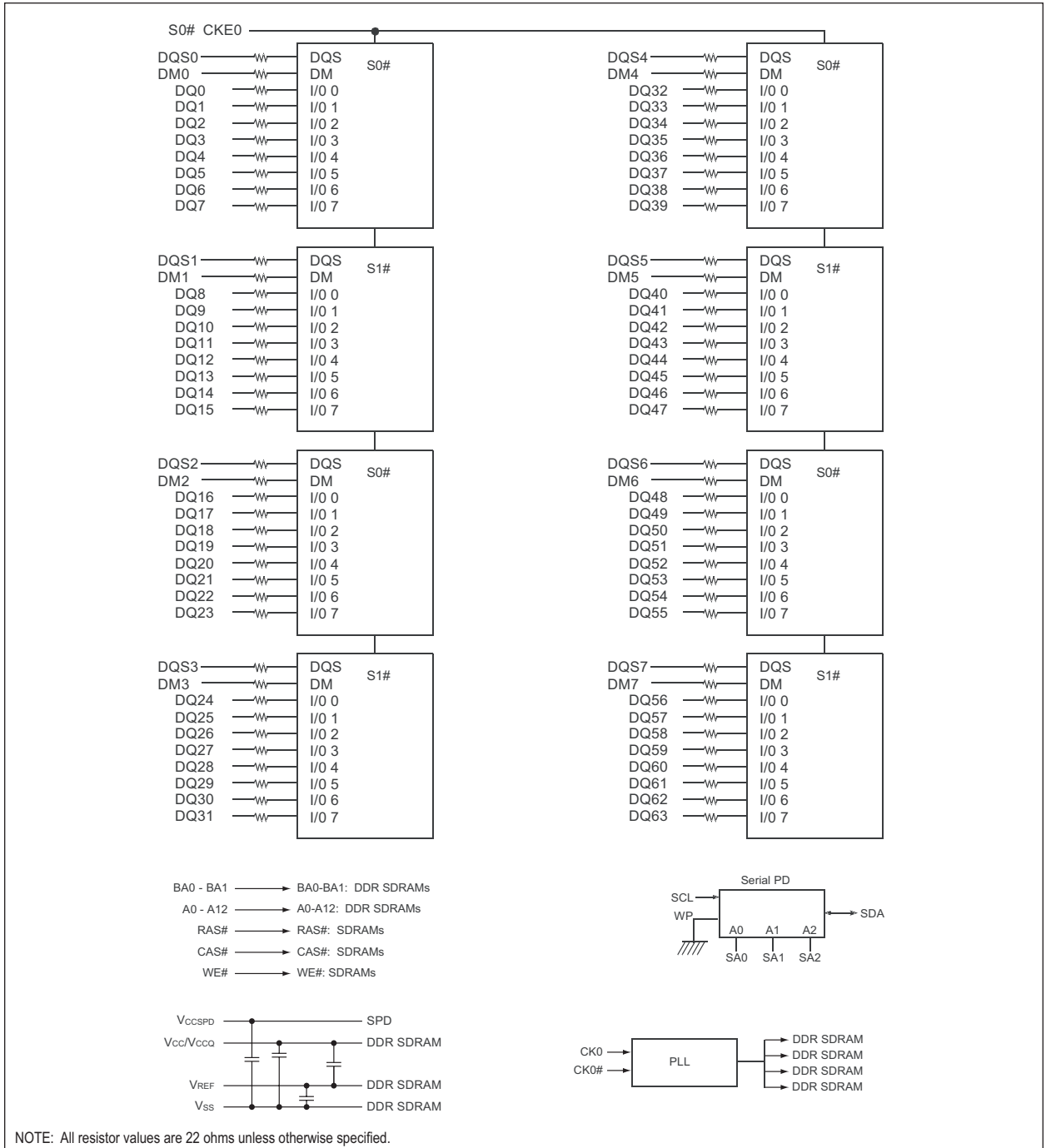
PIN NAMES

A0 – A12	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS7	Data Strobe Input/Output
CK0	Clock input
CK0#	Clock input
CKE0	Clock Enable Input
CS0#	Chip select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DM0-DM7	Data-In Mask
V _{CC}	Power Supply
V _{CCQ}	Power Supply for DQS
V _{SS}	Ground
V _{REF}	Power Supply for Reference
V _{CCSPD}	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
V _{CCID}	V _{CC} Identification Flag
NC	No Connect

* These pins are not used in this module.



FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to 3.6	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC} , V _{CCQ}	-1.0 to 3.6	V
Storage Temperature	T _{STG}	-55 to +150	°C
Power Dissipation	P _D	8	W
Short Circuit Current	I _{OS}	50	mA

Note:

- Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
- Functional operation should be restricted to recommended operating condition.
- Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

T_A = 0°C to 70°C

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V _{CC} of 2.5V)	V _{CC}	2.3	2.7	V	
I/O Supply voltage	V _{CCQ}	2.3	2.7	V	
I/O Reference voltage	V _{REF}	V _{CCQ} /2-50mV	V _{CCQ} /2+50mV	V	1
I/O Termination voltage (system)	V _{TT}	V _{REF} -0.04	V _{REF} +0.04	V	2
Input logic high voltage	V _{IH} (DC)	V _{REF} +0.15	V _{CCQ} +0.3	V	4
Input logic low voltage	V _{IL} (DC)	-0.3	V _{REF} -0.15	V	4
Input Voltage Level, CK and CK# inputs	V _{IN} (DC)	-0.3	V _{CCQ} +0.3	V	
Input Differential Voltage, CK and CK# inputs	V _{ID} (DC)	0.3	V _{CCQ} +0.6	V	3
Input crossing point voltage, CK and CK# inputs	V _{IX} (DC)	1.15	1.35	V	5
Input leakage current	I _I	-2	2	uA	
Output leakage current	I _{OZ}	-5	5	uA	
Output High Current(Normal strength driver); V _{OUT} = V _{TT} + 0.84V	I _{OH}	-16.8		mA	
Output High Current(Normal strength driver); V _{OUT} = V _{TT} - 0.84V	I _{OL}	16.8		mA	
Output High Current(Half strength driver); V _{OUT} = V _{TT} + 0.45V	I _{OH}	-9		mA	
Output High Current(Half strength driver); V _{OUT} = V _{TT} - 0.45V	I _{OL}	9		mA	

Notes:

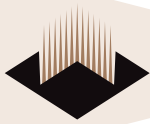
- Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
- V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK.
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHZ.
- The value of V_{IX} is expected to equal 0.5*V_{CCQ} of the transmitting device and must track variations in the dc level of the same.

CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = 2.5V, V_{REF} = 2.5V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C _{IN1}	21	pF
Input Capacitance (RAS#, CAS#, WE#)	C _{IN2}	21	pF
Input Capacitance (CKE0)	C _{IN3}	21	pF
Input Capacitance (CK0,CK0#)	C _{IN4}	3	pF
Input Capacitance (CS0#)	C _{IN5}	12	pF
Input Capacitance (DQM0-DQM8)	C _{IN6}	10	pF
Input Capacitance (BA0-BA1)	C _{IN7}	21	pF
Data input/output capacitance (DQ0-DQ63)(DQS)	C _{OUT}	10	pF

White Electronic Designs Corp. reserves the right to change products or specifications without notice.



I_{DD} SPECIFICATIONS AND TEST CONDITIONS

Recommended operating conditions, 0°C ≤ T_A ≤ 70°C, V_{CCQ} = 2.5V ±0.2V, V_{CC} = 2.5V ±0.2V

Parameter	Symbol	Conditions	DDR333@ CL=2.5	DDR266@ CL=2	DDR266@ CL=2.5	Units
Operating Current	I _{DD0}	One device bank; Active - Precharge; t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	720	640	640	mA
Operating Current	I _{DD1}	One device bank; Active-Read-Precharge; Burst = 2; t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle.	920	840	840	mA
Precharge Power-Down Standby Current	I _{DD2P}	All device banks idle; Power- down mode; t _{CK} =t _{CK} (MIN); CKE=(low)	24	24	24	mA
Idle Standby Current	I _{DD2F}	CS# = High; All device banks idle; t _{CK} =t _{CK} (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V _{IN} = V _{REF} for DQ, DQS and DM.	240	200	200	mA
Precharge Quiet Standby Current	I _{DD2Q}	CS# > = V _{IH} (min); All banks idle; CKE > = V _{IH} (min); t _{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; Address and other control inputs stable with keeping >= V _{IH} (min) or = < V _{IL} (max); V _{IN} = V _{REF} for DQ, DQS and DM	200	185	185	mA
Active Power-Down Standby Current	I _{DD3P}	One device bank active; Power-down mode; t _{CK} (MIN); CKE=(low)	280	240	240	mA
Active Standby Current	I _{DD3N}	CS# = High; CKE = High; One device bank; Active-Precharge; t _{RC} =t _{RAS} (MAX); t _{CK} =t _{CK} (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	440	360	360	mA
Operating Current	I _{DD4R}	Burst = 2; Reads; Continous burst; One device bank active;Address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (MIN); I _{OUT} = 0mA.	1280	1120	1120	mA
Operating Current	I _{DD4W}	Burst = 2; Writes; Continous burst; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (MIN); DQ,DM and DQS inputs changing twice per clock cycle.	1280	1080	1080	mA
Auto Refresh Current	I _{DD5}	t _{RC} =t _{RC} (MIN)	1360	1280	1280	mA
Self Refresh Current	I _{DD6}	CKE ≤ 0.2V	24	24	24	mA
Operating Current	I _{DD7A}	Four bank interleaving Reads (BL=4) with auto precharge with t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); Address and control inputs change only during Active Read or Write commands.	2240	2080	2080	mA

Note: I_{DD} specification is based on Samsung components. Other DRAM manufacturers specification may be different.



DETAILED TEST CONDITIONS FOR DDR SDRAM I_{DD1} & I_{DD7A}

I_{DD1} : OPERATING CURRENT : ONE BANK

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Only one bank is accessed with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I_{OUT} = 0mA
4. Timing Patterns :
 - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RCD}=2*t_{CK}, t_{TRAS}=5*t_{CK}
Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{TRAS}=5*t_{CK}
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL=2, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{TRAS}=5*t_{CK}
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RCD}=10*t_{CK}, t_{TRAS}=7*t_{CK}
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

I_{DD7A} : OPERATING CURRENT : FOUR BANKS

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Four banks are being interleaved with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are not changing. I_{OUT}=0mA
4. Timing Patterns :
 - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}
Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL2=2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=2*t_{CK}
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

Legend : A = Activate, R = Read, W = Write, P = Precharge, N = NOP

A (0-3) = Activate Bank 0-3

R (0-3) = Read Bank 0-3



DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

0°C ≤ T_A ≤ 70°C, V_{CC} = +2.5V ±0.2V, V_{CCQ} = +2.5V ±0.2V

Parameter	Symbol	335		262		265		Unit	Note	
		Min	Max	Min	Max	Min	Max			
Row cycle time	t _{RC}	60		65		65		ns		
Refresh row cycle time	t _{RFC}	72		75		75		ns		
Row active time	t _{RAS}	42	70K	45	120K	45	120K	ns		
RAS to CAS delay	t _{RCD}	18		20		20		ns		
Row precharge time	t _{RP}	18		20		20		ns		
Row active to Row active delay	t _{RRD}	12		15		15		ns		
Write recovery time	t _{WR}	15		15		15		ns		
Last data in to Read command	t _{WTR}	1		1		1		t _{CK}		
Col. address to Col. address delay	t _{CCD}	1		1		1		t _{CK}		
Clock cycle time	CL=2.0	t _{CK}	7.5	12	7.5	12	10	12	ns	5
	CL=2.5		6	12	7.5	12	7.5	12	ns	5
Clock high level width	t _{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}		
Clock low level width	t _{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}		
DQS-out access time from CK/CK#	t _{DQSK}	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns		
Output data access time from CK/CK#	t _{AC}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns		
Data strobe edge to output data edge	t _{DQSQ}	-	0.45	-	0.5	-	0.5	ns	5	
Read Preamble	t _{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}		
Read Postamble	t _{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}		
CK to valid DQS-in	t _{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t _{CK}		
DQS-in setup time	t _{WPRES}	0		0		0		ns	2	
DQS-in hold time	t _{WPRES}	0.25		0.25		0.25		t _{CK}		
DQS falling edge to CK rising-setup time	t _{DSS}	0.2		0.2		0.2		t _{CK}		
DQS falling edge from CK rising-hold time	t _{DSH}	0.2		0.2		0.2		t _{CK}		
DQS-in high level width	t _{DQSH}	0.35		0.35		0.35		t _{CK}		
DQS-in low level width	t _{DQSL}	0.35		0.35		0.35		t _{CK}		
DQS-in cycle time	t _{DSC}	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}		
Address and Control Input setup time (fast)	t _{IS}	0.75		0.9		0.9		ns	6	
Address and Control Input hold time (fast)	t _{IH}	0.75		0.9		0.9		ns	6	
Address and Control Input setup time (slow)	t _{IS}	0.8		1.0		1.0		ns	6	
Address and Control Input hold time (slow)	t _{IH}	0.8		1.0		1.0		ns	6	
Data-out high impedance time from CK/CK#	t _{HZ}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns		
Data-out low impedance time from CK/CK#	t _{LZ}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns		
Input Slew Rate (for input only pins)	t _{SL(I)}	0.5		0.5		0.5		V/ns	6	
Input Slew Rate (for I/O pins)	t _{SL(IO)}	0.5		0.5		0.5		V/ns	7	
Output Slew Rate (x4,x8)	t _{SL(O)}	1.0	4.5	1.0	4.5	1.0	4.5	V/ns		
Output Slew Rate Matching Ratio (rise to fall)	t _{SLMR}	0.67	1.5	0.67	1.5	0.67	1.5			

Note: AC Timing Parameters are based on Samsung components. Other DRAM Manufacturers parameters may be different.



DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

0°C ≤ T_A ≤ 70°C, V_{CC} = +2.5V ±0.2V, V_{CCQ} = +2.5V ±0.2V

Parameter	Symbol	335		262		265		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	t _{MRD}	12		15		15		ns	
DQ & DM setup time to DQS	t _{DS}	0.45		0.5		0.5		ns	7
DQ & DM hold time to DQS	t _{DH}	0.45		0.5		0.5		ns	7
Control & Address input pulse width	t _{IPW}	2.2		2.2		2.2		ns	
DQ & DM input pulse width	t _{DIPW}	1.75		1.75		1.75		ns	
Power down exit time	t _{PDEX}	6		7.5		7.5		ns	
Exit self refresh to non-Read command	t _{XSNR}	75		75		75		ns	4
Exit self refresh to read command	t _{XSRD}	200		200		200		t _{CK}	
Refresh interval time	t _{REFI}	7.8		7.8		7.8		us	1
Output DQS valid window	t _{QH}	t _{HP} -t _{QHS}	—	t _{HP} -t _{QHS}	—	t _{HP} -t _{QHS}	—	ns	5
Clock half period	t _{HP}	t _{CLmin} OR t _{CHmin}	—	t _{CLmin} OR t _{CHmin}	—	t _{CLmin} OR t _{CHmin}	—	ns	
Data hold skew factor	t _{QHS}		0.55		0.75		0.75	ns	
DQS write postamble time	t _{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	3
Active to Read with Auto precharge command	t _{RAP}	18		20		20			
Autoprecharge write recovery + Precharge time	t _{DAL}	(t _{WR} /t _{CK}) + (t _{RP} /t _{CK})		(t _{WR} /t _{CK}) + (t _{RP} /t _{CK})		(t _{WR} /t _{CK}) + (t _{RP} /t _{CK})		t _{CK}	

- Maximum burst refresh cycle : 8
- The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on t_{DQSS}.
- The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
- A write command can be applied with t_{RCD} satisfied after this command.
- For registered DIMMs, t_{CL} and t_{CH} are >_ 45% of the period including both the half period jitter (t_{JIT}(HP)) of the PLL and the half period jitter due to crosstalk (t_{JIT}(crosstalk)) on the DIMM.
- Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	Δt _{IS}	Δt _{IH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

- I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	Δt _{DS}	Δt _{DH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

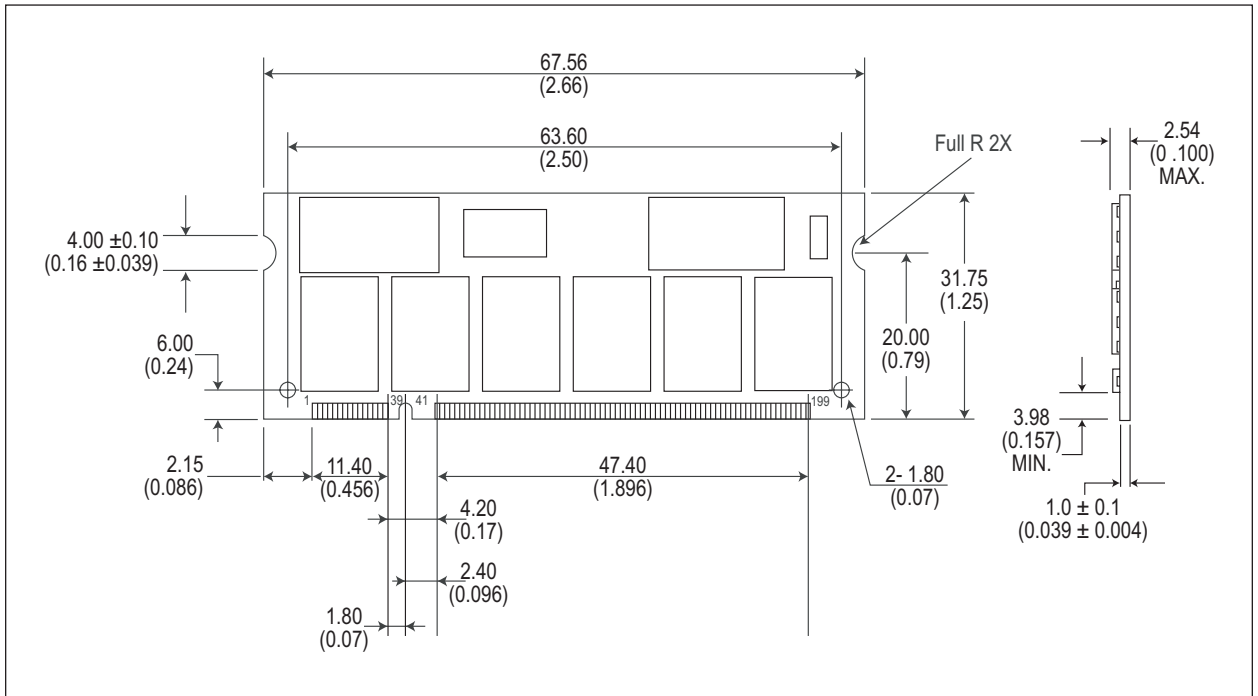


ORDERING INFORMATION FOR BD4

Part Number	Speed	CAS Latency	t _{RC} D	t _{RP}	Height*
WV3EG6434S335BD4	166MHz/333Mb/s	2.5	3	3	31.75 (1.25")
WV3EG6434S262BD4	133MHz/266Mb/s	2	2	2	31.75 (1.25")
WV3EG6434S265BD4	133MHz/266Mb/s	2.5	3	3	31.75 (1.25")

- NOTES:
- Consult Factory for availability of Lead-Free or RoHS products. (F = Lead-Free, G = RoHS Compliant)
 - Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
 - Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR BD4



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)
 TOLERANCES: ± 0.15 (0.006) UNLESS OTHERWISE SPECIFIED



Document Title

256MB – 32Mx64 DDR SDRAM UNBUFFERED, w/PLL

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	4-05	Advanced