DATA SHEET

UBA1707
Cordless telephone, answering machine line interface

Product specification
Supersedes data of 1998 Jun 11
File under Integrated Circuits, IC03

1999 Feb 17

Philips
Semiconductors

PHILIPS

Cordless telephone, answering machine line interface

UBA1707

FEATURES

Line interface

- Low DC line voltage; operates down to 1.2 V (excluding polarity guard)
- Voltage regulator with adjustable DC voltage
- DC mask for voltage or current regulation (CTR 21)
- Line current limitation for protection
- Electronic hook switch control input
- Transmit amplifier with:
  - Symmetrical inputs
  - Fixed gain
  - Large signals handling capability.
- Receive amplifier with fixed gain
- Transmit and receive amplifiers AGC for line loss compensation.

Auxiliary amplifier

- Fixed gain.

Loudspeaker channel

- Dual inputs
- Rail-to-rail output stage for single-ended load drive
- High output current capability
- Dynamic limiter to prevent distortion
- Digital volume control
- Fixed maximum gain.

General purpose switches

- Three switches with open-collector.

3-wires serial bus interface

Allows to control:

- DC mask (voltage or current regulation)
- Receive amplifier mute function
- AGC:
  - On/off
  - Slope
  - I_{start} line current.
- Auxiliary amplifier mute function
- Loudspeaker channel:
  - Input selection
  - Volume setting
  - Dynamic limiter inhibition
  - Power-down mode.
- General purpose switches state
- Global power-down mode.

Supply

Operates with external supply voltage from 3.0 to 5.5 V.

APPLICATIONS

- Cordless base stations
- Answering machines
- Mains or battery-powered telephone sets.

GENERAL DESCRIPTION

The UBA1707 is a BiCMOS integrated circuit intended for use in mains-powered telecom terminals. It performs all speech and line interface functions, DC mask for voltage or current regulation and electronic hook switch control. The device includes an auxiliary amplifier, a loudspeaker channel and general purpose switches.

Most of the characteristics are programmable via a 3-wire serial bus interface.

ORDERING INFORMATION

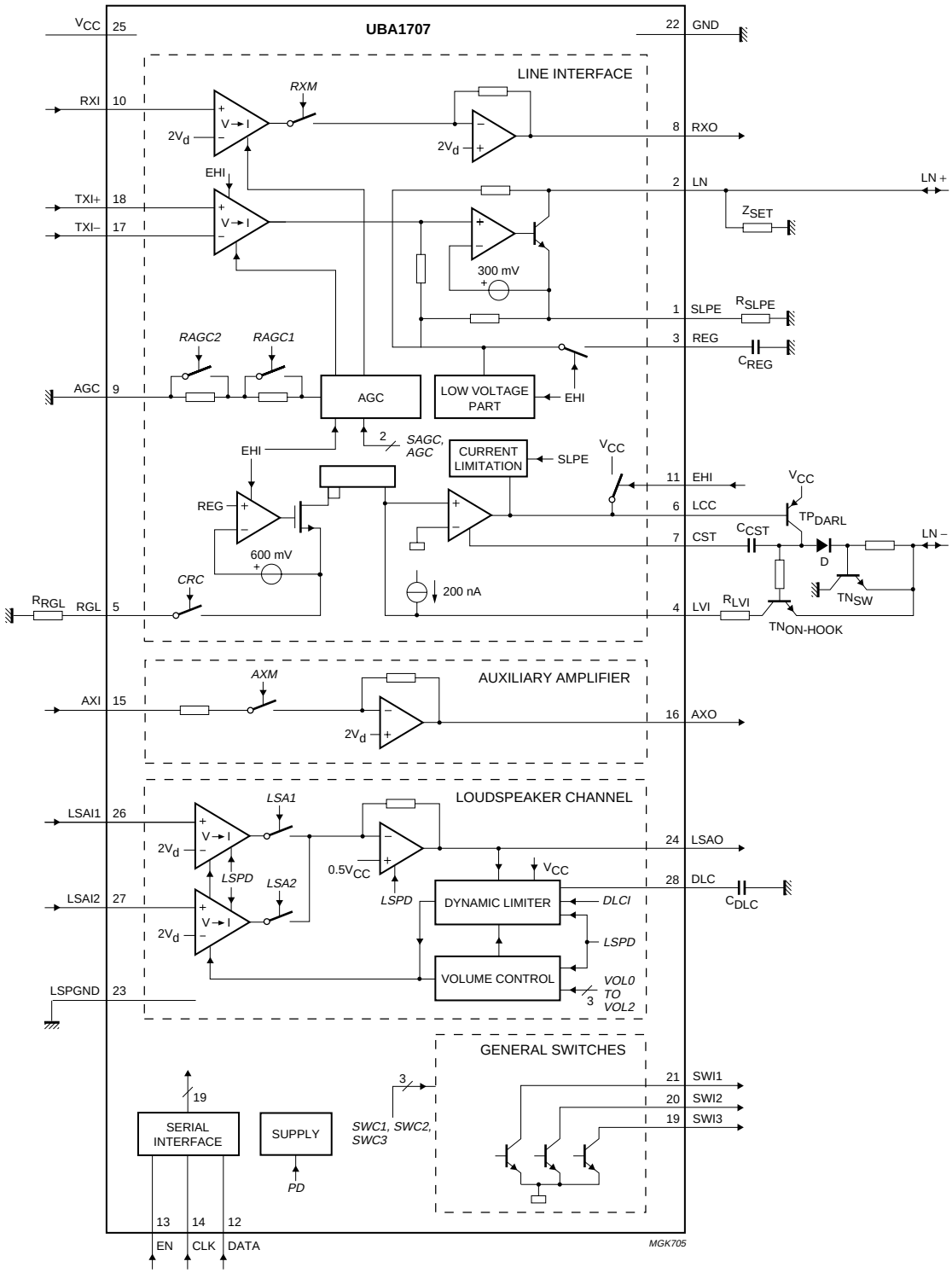
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA1707T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
UBA1707TS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

QUICK REFERENCE DATA

I_{line} = 15 mA; V_{CC} = 3.3 V; R_{SLPE} = 10 Ω; AGC pin connected to GND; Z_{line} = 600 Ω; Z_{SET} = 619 Ω; EHI = HIGH; f = 1 kHz; T_{amb} = 25 °C; bit AGC at logic 1, all other configuration bits at logic 0; measured in test circuit of Fig.17; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	operating voltage range		3.0	–	5.5	V
I_{CC}	current consumption from pin V_{CC}	normal operation; bit PD = 0	–	2.2	3.2	mA
		power-down mode; bit PD = 1	–	110	150	μA
I_{line}	line current operating range	normal operation	11	–	140	mA
		with reduced performance	3	–	11	mA
V_{LN}	DC line voltage		2.7	3.0	3.3	V
R_{REGC}	DC mask slope in current regulation mode	I_{line} > 35 mA (typical); R_{LVI} = 1 MΩ; R_{RGL} = 7.15 kΩ; bit CRC = 1	–	1.4	–	kΩ
$G_{v(trx)}$	voltage gain					
	transmit amplifier from TXI to LN	V_{TXI} = 50 mV (RMS)	10.6	11.6	12.6	dB
	receive amplifier from RXI to RXO	V_{RXI} = 2 mV (RMS)	36.9	37.9	38.9	dB
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 90 mA	–	6.5	–	dB
$G_{v(AX)}$	voltage gain from AXI to AXO	V_{AXI} = 2 mV (RMS)	30.8	31.8	32.8	dB
$G_{v(LSA)}$	voltage gain from LSAI1 or LSAI2 to LSAO for maximum volume	V_{LSAI} = 8 mV (RMS); bits LSA1 = 1 and LSA2 = 1	26.5	28	29.5	dB
$\Delta G_{v(LSA)}$	voltage gain adjustment range for loudspeaker channel	bits (VOL0, VOL1, VOL2) from (0, 0, 0) to (1, 1, 1)	–	21	–	dB
$\Delta G_{v(LSA)s}$	voltage gain adjustment step for loudspeaker channel	VOL0 from 0 to 1	–	3	–	dB

BLOCK DIAGRAM



Bit names are given in italics.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SLPE	1	connection for slope resistor
LN	2	positive line terminal
REG	3	line voltage regulator decoupling
LVI	4	negative line voltage sense input
RGL	5	reference for current regulation mode
LCC	6	line current control output
CST	7	input for stability capacitor
RXO	8	receive amplifier output
AGC	9	automatic gain control/line loss compensation adjustment
RXI	10	receiver amplifier input
EHI	11	electronic hook switch control input
DATA	12	serial bus data input
EN	13	programming serial bus enable input
CLK	14	serial bus clock input
AXI	15	auxiliary amplifier input
AXO	16	auxiliary amplifier output
TXI–	17	inverted transmit amplifier input
TXI+	18	non-inverted transmit amplifier input
SWI3	19	NPN open-collector output 3
SWI2	20	NPN open-collector output 2
SWI1	21	NPN open-collector output 1
GND	22	ground reference
LSPGND	23	ground reference for the loudspeaker amplifier
LSAO	24	loudspeaker amplifier output
V_{CC}	25	supply voltage
LSAI1	26	loudspeaker amplifier input 1
LSAI2	27	loudspeaker amplifier input 2
DLC	28	dynamic limiter timing adjustment

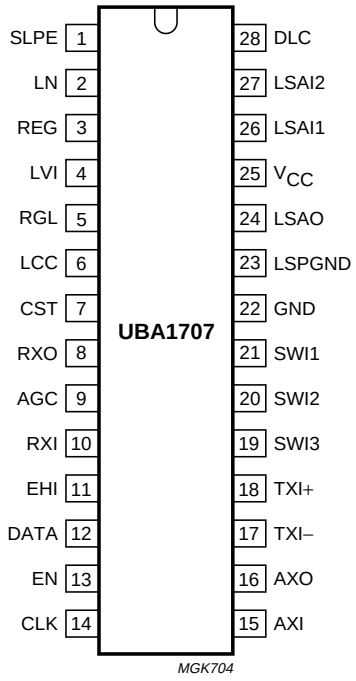


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All data given in this chapter are typical values, except when otherwise specified.

Supply (pins V_{CC} and GND; bits PD and LSPD)

The UBA1707 must be supplied with an external stabilized voltage source between pins V_{CC} and GND.

Pins GND and LSPGND must be connected together.

Without any signal, with the loudspeaker channel enabled at minimum volume and without any general purpose switch selected, the internal current consumption is 2.2 mA at V_{CC} = 3.3 V. Each selected switch (pins SWI1, SWI2, or SWI3) increases the current consumption by 600 μA.

The supply current can be reduced when the loudspeaker channel is not used by switching it off (bit LSPD at logic 1). The current consumption is then decreased by approximately 800 μA at minimum volume.

To drastically reduce current consumption, the UBA1707 is provided with a power-down mode controlled by bit PD. When bit PD is at logic 1, the current consumption from V_{CC} becomes 110 μA. In this mode, the serial interface is the only function which remains active.

Line interface

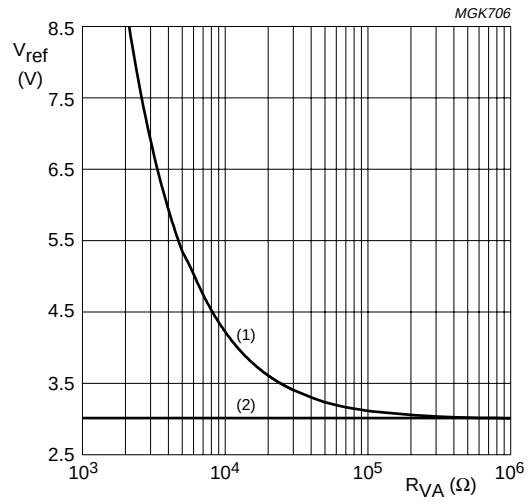
DC CHARACTERISTICS (PINS LN, SLPE, REG, CST, LVI, LCC, RGL AND GND; BIT CRC)

The IC generates a stabilized reference voltage (V_{ref}) between pins LN and SLPE. This reference voltage is equal to 2.9 V, is temperature compensated and can be adjusted by means of an external resistor (R_{VA}). It can be increased by connecting the R_{VA} resistor between pins REG and SLPE (see Fig.3).

The voltage at pin REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by a capacitor (C_{REG}) which is connected to GND. This capacitor, converted into an equivalent inductance (see Section “Set impedance”) realizes the set impedance conversion from its DC value (R_{SLPE}) to its AC value (Z_{SET} in the audio-frequency range). Figure 4 illustrates the reference voltage supply configuration. As can be seen from Fig.4, part of the line current flows into the Z_{SET} impedance network and is not sensed by the UBA1707. Therefore using the R_{VA} resistor to change value of the reference voltage will also modify all parameters related to the line current such as:

- The automatic gain control
- The DC mask management
- The low voltage area characteristics.

In the same way, changing the value of Z_{SET} also affects the characteristics. The IC has been optimized for V_{ref} = 2.9 V and Z_{SET} = 619 Ω.



(1) Influence of R_{VA} on V_{ref}.
(2) V_{ref} without influence of R_{VA}.

Fig.3 Reference voltage adjustment with R_{VA}.

The IC regulates the line voltage at pin LN which can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{ZSET} - I^* \cong I_{line} - I_{ZSET}$$

Where:

I_{line} = line current

I_{ZSET} = current flowing through Z_{SET}

I* = current consumed between LN and GND (approximately 100 μA).

The preferred value for R_{SLPE} is 10 Ω. Changing R_{SLPE} will affect more than the DC characteristics; it also influences the transmit gain, the gain control characteristics, the sidetone level and the maximum output swing on the line. However, for compliance with CTR 21 8.66 Ω is the best value for R_{SLPE}.

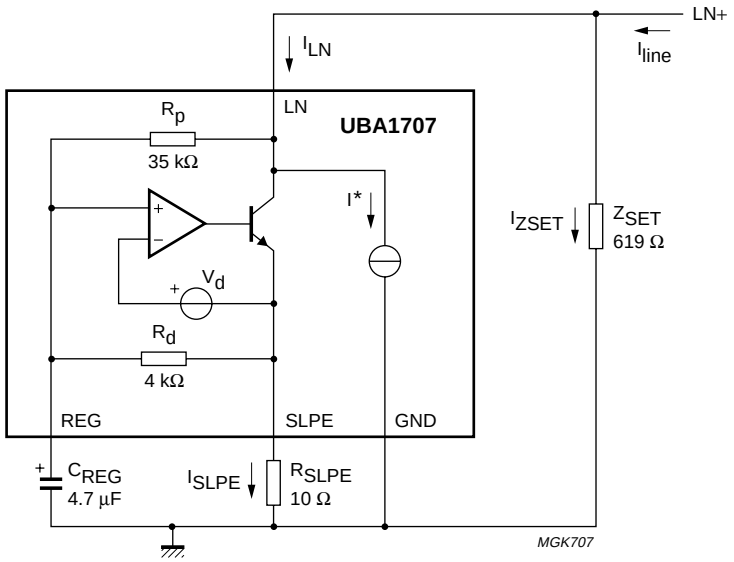


Fig.4 Reference voltage supply configuration.

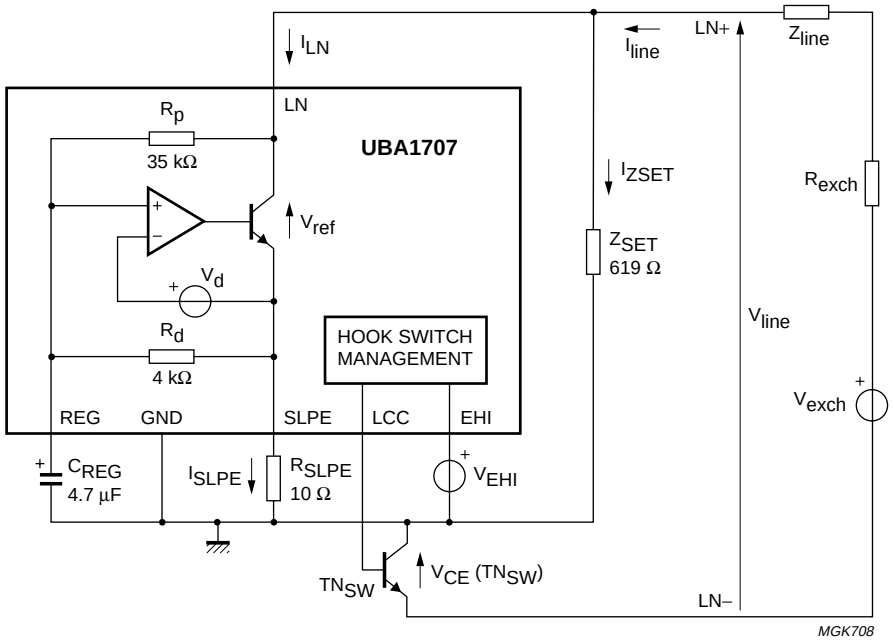


Fig.5 Line current settling simplified configuration.

The DC line current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistors of the telephone line (R_{line}) and the set (R_{SET}), the reference voltage (V_{ref}) and the voltage introduced by the transistor (TN_{SW}) used as line interrupter (see Fig.5). With a line current below I_{low} (8 mA with Z_{SET} = 619 Ω), the internal reference voltage (V_{ref}) is automatically adjusted to a lower value. This means that more sets can operate in parallel with DC line voltages (excluding the polarity guard) down to 1.2 V. At line current below I_{low}, the circuit has limited transmit and receive levels. This is called the low voltage area.

Figure 6 shows in more details how the UBA1707, in association with some external components, manages the line interrupter (TN_{SW} external transistor).

In on-hook conditions (voltage at pin EHI is LOW), the voltage at pin LCC is pulled-up to the supply voltage level (V_{CC}) to turn off the TP_{DARL} transistor. As a result, because of the R_{PLD} resistor, the TN_{SW} and $TN_{ON\text{-}HOOK}$ transistors are switched off. The $TN_{ON\text{-}HOOK}$ transistor disconnects the R_{LVI} resistor from the LN– line terminal in order to guarantee a high on-hook impedance.

In off-hook conditions (voltage at pin EHI is HIGH), an operational amplifier drives (at pin LCC) the base of TP_{DARL} which forms a current amplifier structure in association with TN_{SW}. The line current flows through TN_{SW} transistor. The $TN_{ON\text{-}HOOK}$ transistor is forced into deep saturation. A virtual ground is created at pin LVI because of the operational amplifier. A DC current (I_{LVI}) is sourced from pin LVI into the R_{LVI} resistor in order to generate a voltage source. Thus the voltage between pin GND and the negative line terminal (LN–) becomes:

$$V_{CE}\,(TN_{SW}) = R_{LVI} \times I_{LVI} + V_{CE}\,(TN_{ON\text{-}HOOK}) \cong R_{LVI} \times I_{LVI}$$

The voltage V_{line} between the line terminals LN+ and LN– can be calculated as follows:

$$V_{line} \cong V_{ref} + R_{SLPE} \times (I_{line} - I_{ZSET}) + V_{CE}\,(TN_{SW})$$

Where:

I_{line} = line current

I_{ZSET} = current flowing through Z_{SET}.

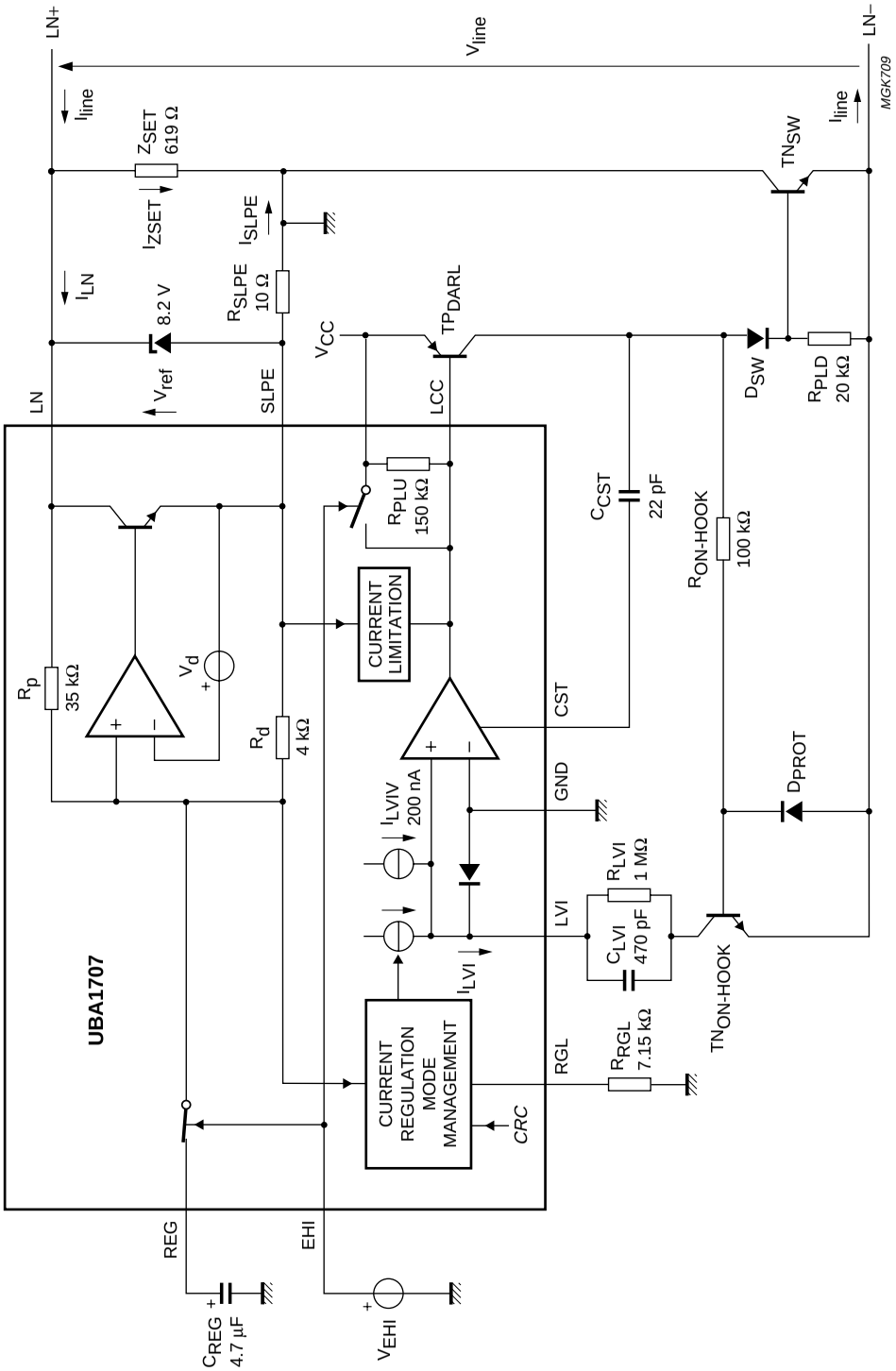
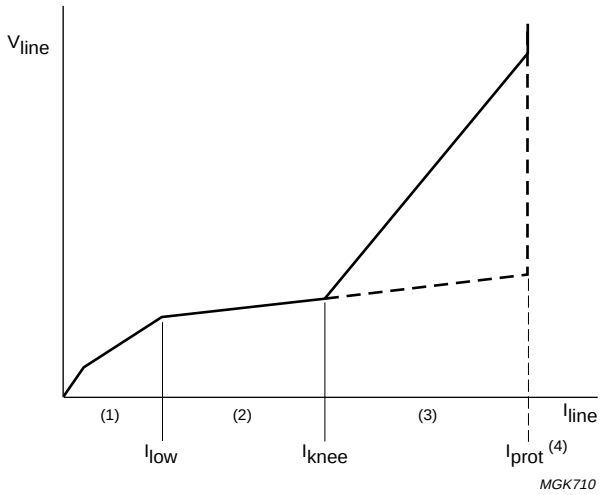


Fig.6 Line interrupter management and DC mask regulation configuration.

Bit names are given in italics.

The UBA1707 offers the possibility to choose two kinds of regulations for the DC characteristic between the line terminals LN+ and LN– (see Fig.7):

- Voltage regulation mode
- Current regulation mode.



(1) Low voltage area.
(2) Small slope (determined by R_{SLPE}).
(3) Small slope (dashed line; determined by R_{SLPE}) in voltage regulation mode.
High slope (full line; determined by R_{SLPE}, R_{LVI} and R_{RGL}) in current regulation mode.
(4) Current limitation.

Fig.7 General form of the DC mask as a function of regulation mode.

The regulation mode is selected by the bit CRC via the serial interface.

The DC mask regulation is realised by adjusting the DC voltage V_{CE} (TN_{SW}) between pin GND and line terminal LN– as a function of the line current.

Voltage regulation mode

In voltage regulation mode (bit CRC at logic 0), V_{CE} (TN_{SW}) voltage is fixed by means of a 200 nA DC constant current I_{LVIV} flowing through R_{LVI}.

Therefore V_{CE} (TN_{SW}) $\cong R_{LVI} \times I_{LVIV}$ = 200 mV in typical application (see Fig.18).

The slope $\Delta V_{line}/\Delta I_{line}$ of the V_{line}, I_{line} characteristic is $R_{REGV} \cong R_{SLPE}$.

Current regulation mode

In current regulation mode (bit CRC at logic 1), when the line current is lower than I_{knee} = 35 mA (with Z_{SET} = 619 Ω), V_{CE} (TN_{SW}) is fixed by means of a 200 nA DC constant current I_{LVIV} flowing through R_{LVI}. When the line current is higher than 35 mA, an additional current (proportional to the line current) flows through R_{LVI}. As a result, TN_{SW} works as a DC voltage source increasing with the line current. V_{CE} (TN_{SW}) can be calculated as follows:

$$V_{CE}(TN_{SW}) \cong R_{LVI} \times \left(\frac{R_{SLPE}}{R_{RGL}} \times (I_{line} - I_{knee}) + I_{LVIV} \right)$$

Where:

I_{line} = line current

R_{RGL} = resistor connected at pin RGL.

The slope $\Delta V_{line}/\Delta I_{line}$ of the V_{line}, I_{line} characteristic is determined by the ratio of resistors connected at pins SLPE, LVI and RGL, and can be calculated as follows: $R_{REGC} \cong R_{SLPE} + R_{LVI} \times \frac{R_{SLPE}}{R_{RGL}}$ = 1400 Ω in typical application (see Fig.18).

Current limitation

Whatever the selected mode is, the line current is limited to approximately 145 mA. This current is sensed on SLPE, for this purpose the external zener diode must be connected between pins LN and SLPE. The speech function no longer operates in this condition.

ELECTRONIC HOOK SWITCH CONTROL (PIN EHI)

The electronic hook switch input (EHI) controls the state of TP_{DARL} transistor. When the voltage applied at pin EHI is LOW, TP_{DARL} transistor is turned off. Voltage at pin LCC is pulled up to supply voltage (V_{CC}). TN_{SW} and $TN_{ON\text{-}HOOK}$ transistors are also turned off by means of a pull-down resistor (R_{PLD}). When the voltage applied at pin EHI is HIGH, TP_{DARL} transistor is driven by the operational amplifier at pin LCC and the regulation mode selected is operating. An internal 165 kΩ pull-up resistor is connected between pins LCC and V_{CC}.

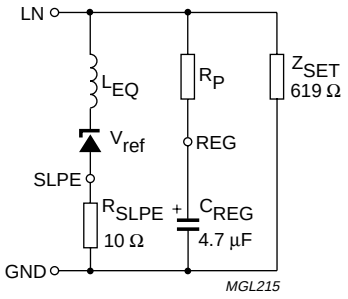
The EHI input can also be used for pulse dialling or register recall (timed loop break). During line breaks (voltage at pin EHI is LOW or open-circuit), the voltage regulator is switched off and the capacitor at pin REG is internally disconnected to prevent its discharge. As a result, the voltage stabilizer will have negligible switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the UBA1707 is in power-down mode (bit PD at logic 1), the TP_{DARL} transistor is forced to be turned off whatever the voltage applied at pin EHI.

SET IMPEDANCE

In the audio frequency range, the dynamic impedance between pins LN and GND (illustrated in Fig.8) is mainly determined by the Z_{SET} impedance.

The impedance introduced by the external TN_{SW} transistor connected between pin GND and the negative line terminal (LN–) is negligible.



$L_{eq} = C_{REG} \times R_{SLPE} \times R_P$
R_P = internal resistance = 35 kΩ.

Fig.8 Equivalent impedance between LN and GND.

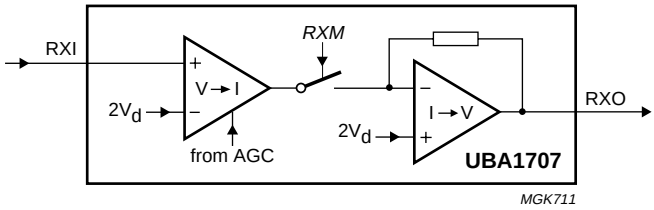
TRANSMIT AMPLIFIER (PINS TXI+ AND TXI–)

The UBA1707 has symmetrical transmit inputs TXI+ and TXI–. The input impedance between pins TXI+ or TXI– and GND is 21 kΩ. The voltage gain from pins TXI+ or TXI– to pin LN is set at 11.6 dB with 600 Ω line load (Z_{line}) and 619 Ω set impedance. The inputs are biased at $2 \times V_d \cong 1.4$ V, with V_d representing the diode voltage. Automatic gain control is provided on this amplifier for line loss compensation.

RECEIVE AMPLIFIER (PINS RXI AND RXO; BIT RXM)

The receive amplifier (see Fig.9) has one input (RXI) and one output (RXO). The input impedance between pins RXI and GND is 21 kΩ. The rail-to-rail output stage is designed to drive a 500 µA peak current. The output impedance at pin RXO is approximately 100 Ω.

The voltage gain from pin RXI to pin RXO is set at 37.9 dB. This gain value compensates typically the attenuation of the anti-sidetone network (see Fig.10). The output as well as the input are biased at $2 \times V_d \cong 1.4$ V. Automatic gain control is provided on this amplifier for line loss compensation. This amplifier can be muted by activating the receive mute function (bit RXM at logic 1).



Bit names are given in italics.

Fig.9 Receive amplifier.

SIDETONE SUPPRESSION

The UBA1707 anti-sidetone network comprising $Z_{SET}//Z_{line}$, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal} (see Fig.10) suppresses the transmitted signal in the received signal. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = Z_{SET} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{(R_{ast2} \times (R_{ast3} + R_{SLPE}))}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor ‘k’ is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice, Z_{line} varies considerably with the line type and the line length.

Therefore, the value chosen for Z_{bal} should be for an average line length which gives satisfactory sidetone suppression with short and long lines.

The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

The anti-sidetone network for the UBA1707 (see Fig.18) attenuates the receiving signal from the line by 38 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. A Wheatstone bridge configuration (see Fig.11) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *“Applications Handbook for Wired Telecom Systems, IC03b”*.

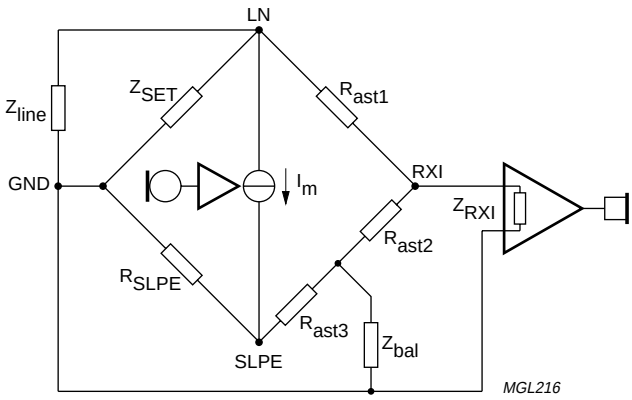


Fig.10 Equivalent circuit of UBA1707 anti-sidetone bridge.

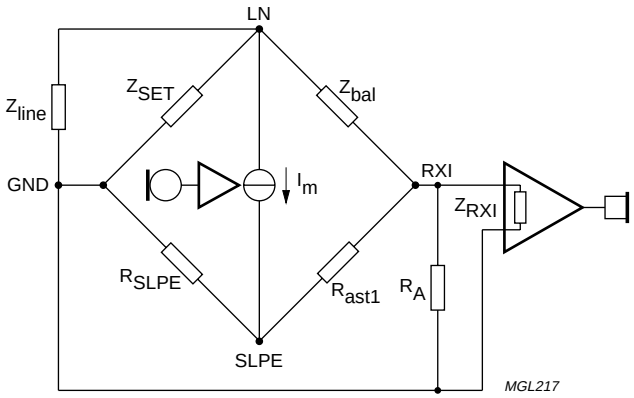


Fig.11 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

AUTOMATIC GAIN CONTROL (PIN AGC; BITS RAGC1, RAGC2, SAGC AND AGC)

The UBA1707 performs automatic line loss compensation. The automatic gain control varies the gain of the transmit amplifier and the gain of the receive amplifier in accordance with the DC line current. The control range is 6.5 dB (which roughly corresponds to a line length of 5.5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km).

When the line current is greater than I_{stop}, the voltage gains are minimum. When the line current is less than I_{start}, the voltage gains are maximum. When the AGC pin is connected to pin GND, the start line current (I_{start}) can be chosen between 22.5 and 29.5 mA via bits RAGC1 and RAGC2 through the serial interface. Two values for the I_{stop}/I_{start} ratio (slope of the AGC) are possible via the bit SAGC through the serial interface. When bit SAGC is at logic 0 then $I_{stop} = 2.7 \times I_{start}$ (optimized for voltage regulation mode). When SAGC is at logic 1 then $I_{stop} = 1.9 \times I_{start}$ (optimized for current regulation mode).

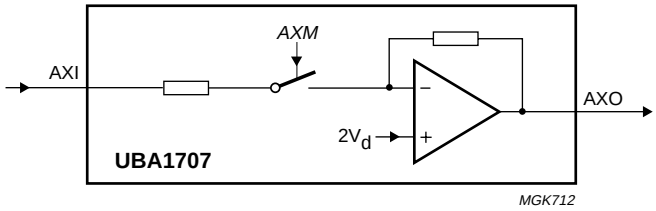
An external resistor R_{AGC} (connected between pins GND and AGC) enables the I_{start} and I_{stop} line currents to be increased (the ratio between I_{start} and I_{stop} is not affected by this external resistor). So internal and external adjustments of the automatic gain control allow optimization of the IC for many configurations of exchange supply voltage and feeding bridge resistance. Part of the line current flows into the Z_{SET} impedance network. The IC has been optimized for Z_{SET} = 619 Ω. Changing this 619 Ω value slightly modifies I_{stop} and I_{start} line currents as well as the value of the two AGC slopes.

The automatic gain control function can be disabled by setting the AGC bit to logic 0 via the serial interface or when pin AGC is left open-circuit. In this case both of the voltage gains are maximum.

Auxiliary amplifier (pins AXI and AXO; bit AXM)

The auxiliary amplifier (see Fig.12) has one input (AXI) and one output (AXO). The input impedance between pins AXI and GND is 3.8 kΩ. The rail-to-rail output stage is designed to drive a 500 μA peak current. The output impedance at pin AXO is approximately 100 Ω.

The output as well as the input are biased at $2 \times V_d \cong 1.4$ V DC voltage. The voltage gain from pin AXI to pin AXO is set at 31.8 dB.The amplifier can be muted by setting bit AXM at logic 1 via the serial interface. In this case, the input impedance between pins AXI and GND is infinite.



Bit names are given in italics.

Fig.12 Auxiliary amplifier.

Loudspeaker channel (see Fig.13)

LOUDSPEAKER AMPLIFIER (PINS LSAI1, LSAI2, LSAO AND LSPGND; BITS LSPD, LSA1 AND LSA2)

The loudspeaker amplifier has two symmetrical inputs LSAI1 and LSAI2 selectable independently by the bits LSA1 and LSA2 respectively. The input impedance between pins LSAI1or LSAI2 and GND is typically 21 kΩ. Each of these two inputs stages can accommodate signals up to 500 mV (RMS) at room temperature for less than 2% of Total Harmonic Distortion (THD) at minimum voltage gain.

The inputs are biased at $2 \times V_d \cong 1.4$ V DC voltage (whatever the state of bits LSA1 and LSA2).

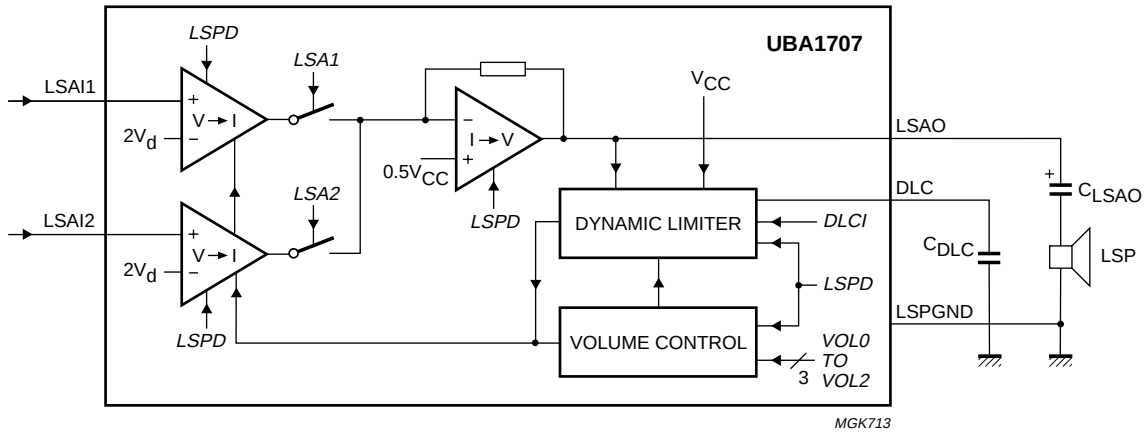
The rail-to-rail output stage is designed to power a loudspeaker connected as a single-ended load (between pins LSAO and LSPGND). The output LSAO is able to drive at least a 150 mA peak current.

As a result, it can drive loudspeaker loads down to 8 Ω at V_{CC} = 4.0 V and 16 Ω at V_{CC} = 5.5 V. The output is biased at $\frac{1}{2}V_{CC}$. Its output voltage capability is specified for continuous wave drive and depends on the value of V_{CC}.

In order to avoid crosstalk from the loudspeaker to other amplifiers, the loudspeaker current flows via pin LSPGND. This pin must be externally connected to pin GND.

The nominal value of the voltage gain for maximum volume from pins LSAI1 or LSAI2 to pin LSAO is set at 28 dB.

This amplifier is no longer supplied by setting the LSPD bit at logic 1 via the serial interface.



Bit names are given in italics.

Fig.13 Loudspeaker channel.

DYNAMIC LIMITER (PIN DLC; BIT DLCI)

The dynamic limiter of the UBA1707 prevents clipping of the loudspeaker output stage and protects the operation of the circuit when the supply voltage at V_{CC} falls below 2.7 V.

Hard clipping of the loudspeaker output stage is prevented by rapidly reducing the gain when the output stage starts to saturate. The time in which gain reduction is effected (clipping attack time) is approximately a few milliseconds. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (typically 250 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stage, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive [providing V_{LSAI} is below 500 mV (RMS)].

When the supply voltage drops below an internal threshold voltage of 2.7 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When the supply voltage exceeds 2.7 V, the gain of the loudspeaker amplifier is increased again.

The hard clipping of the dynamic limiter can be inhibited by setting the DLCI bit at logic 1, via the serial interface.

The dynamic limiter is no longer supplied by setting the LSPD bit at logic 1. In this case, the C_{DLC} capacitor charge is maintained to allow the gain of the loudspeaker amplifier to return to its nominal value as soon as the loudspeaker channel is supplied again.

VOLUME CONTROL (BITS VOL0, VOL1 AND VOL2)

The loudspeaker amplifier voltage gain can be reduced in steps of 3 dB via the serial interface (via bits VOL0, VOL1 and VOL2). These bits provide 7 steps of voltage gain adjustment. The voltage gain is maximum when all bits are at logic 1 and is reduced by 21 dB when all bits are at logic 0.

General purpose switches (pins SWI1, SWI2 and SWI3; bits SWC1, SWC2 and SWC3)

The UBA1707 is equipped with 3 general purpose open-collector switches which short the pins SWI1, SWI2 and SWI3 to ground. They are respectively controlled by bits SWC1, SWC2 and SWC3 and have an operating voltage limited to 12 V. The outputs have to be current biased.

For a bias current between 2 and 20 mA, the AC impedance is 30 Ω maximum.

Serial interface (pins DATA, CLK and EN)

A simple 3-wire unidirectional serial bus is used to program the circuit. The 3 wires of the bus are EN, CLK and DATA. The data sent to the device is loaded in bursts framed by EN. Programming clock edges (falling edges) and their appropriate data bits are ignored until EN goes active HIGH. The programmed information is loaded into the addressed register when EN returns inactive (LOW) or left open-circuit.

During normal operation, EN should be kept LOW. Only the last 8 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored and no check is made on the number of clock pulses. It can always capture new programming data even during global power-down (bit PD at logic 1).

Data is entered with the most significant bit first. The leading 6 bits make up the data field (bits D0 to D5) while the trailing 2 bits are the address field (bits ADO and AD1). The first bit entered is D5, the last bit AD0. This organisation allows to send only the number of bits of the addressed register.

Figure 16 shows the serial timing diagram. Table 1 gives the list of registers.

When the supply voltage V_{CC} drops below 2.5 V, all register files are set in the initial state (see Table 1) defined by the power-up reset. At start-up, the circuit is in power-down mode.

In the event that the IC is used in a noisy environment, it is advised to periodically refresh the content of registers**.**

Table 1 Register description

BIT NAME	FUNCTION	POLARITY	DATA	ADDRESS	STATE AT POWER-UP RESET
Register 0: general purpose switches state and DC mask regulation mode					
SWC1	SWI1 output connection	0: SWI1 switched off	D0	(AD1, AD0) = (0,0)	0
		1: SWI1 switched on			
SWC2	SWI2 output connection	0: SWI2 switched off	D1		0
		1: SWI2 switched on			
SWC3	SWI3 output connection	0: SWI3 switched off	D2		0
		1: SWI3 switched on			
un	unused	must be set to logic 0	D3		0
CRC	current regulation mode	0: voltage regulation	D4		0
		1: current regulation			
Register 1: automatic gain control					
RAGC1	AGC range selection 1		D0	(AD1, AD0) = (0,1)	0
RAGC2	AGC range selection 2		D1		0
SAGC	AGC slope selection	0: 2.7 type slope; note 1	D2		0
		1: 1.9 type slope; note 1			
AGC	line loss compensation mode	0: AGC inhibited	D3		0
		1: AGC enabled			
Register 2: loudspeaker channel					
LSA1	loudspeaker channel input 1 selection	0: LSAI1 unselected	D0	(AD1, AD0) = (1,0)	0
		1: LSAI1 selected			
LSA2	loudspeaker channel input 2 selection	0: LSAI2 unselected	D1		0
		1: LSAI2 selected			
LSPD	loudspeaker channel power-down	0: channel on	D2		0
		1: channel in power-down			
VOL0	volume control (least significant bit)		D3		0
VOL1	volume control		D4		0
VOL2	volume control (most significant bit)		D5		0
Register 3: mute functions and power-down					
AXM	auxiliary amplifier mute	0: amplifier enabled	D0	(AD1, AD0) = (1,1)	0
		1: amplifier muted			
RXM	receive amplifier mute	0: amplifier enabled	D1		0
		1: amplifier muted			
PD	reduced consumption mode	0: normal operating mode	D2		1
		1: power-down mode			
DLCI	dynamic limiter inhibit	0: limiter enabled	D3		0
		1: limiter inhibited			

Note

1. See Section “Automatic gain control (pin AGC; bits RAGC1, RAGC2, SAGC and AGC)”.

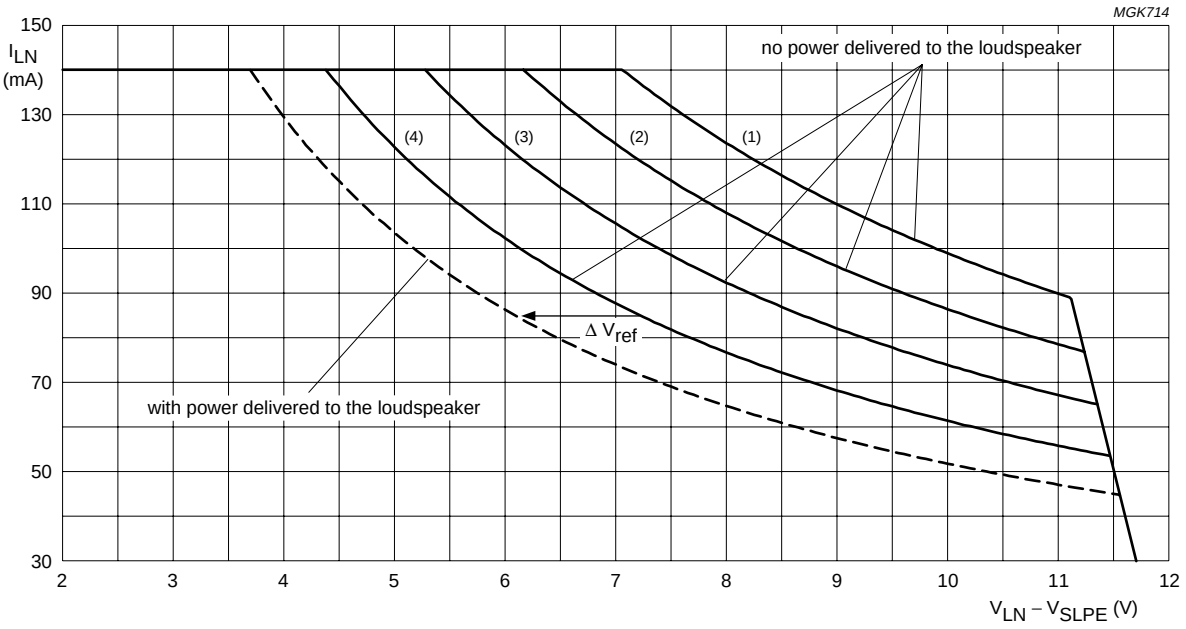
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage on pin V_{CC}		GND – 0.4	5.5	V
V_{LN}	positive continuous line voltage on pin LN		GND – 0.4	12.0	V
	repetitive line voltage during switch-on or line interruption		GND – 0.4	13.2	V
V_{SWIn}	voltage on pins SWI1, SWI2, and SWI3	continuous	GND – 0.4	12.0	V
		during switching	GND – 0.4	13.2	V
$V_{n(max)}$	maximum voltage on all other pins		GND – 0.4	V_{CC} + 0.4	V
I_{LN}	current sunk by pin LN	see Figs 14 and 15	–	150	mA
I_{SWIn}	continuous current sunk by pins SWI1, SWI2, and SWI3	bit SWCn = 1	–	20	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; see Figs 14 and 15			
	UBA1707T		–	625	mW
	UBA1707TS		–	416	mW
T_{stg}	IC storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air		
	UBA1707T		70	K/W
	UBA1707TS		104	K/W



LINE	T_{amb} (°C)	P_{tot} (mW)
(1)	45	1000
(2)	55	875
(3)	65	750
(4)	75	625

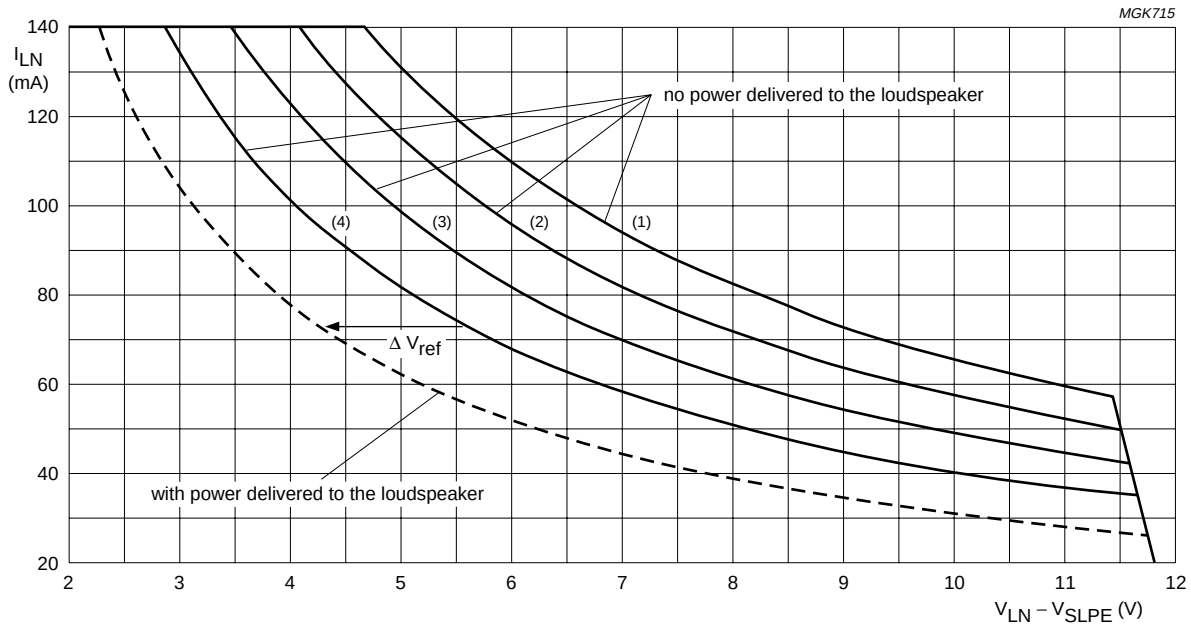
The line current value can be calculated from I_{LN} value as follows:

$$I_{line} = \frac{I_{LN} \times (R_{SET} + R_{SLPE}) + V_{LN} - V_{SLPE}}{R_{SET}}$$ where R_{SET} is the resistive part of Z_{SET}.

When power is delivered to a loudspeaker with R_L impedance, the curves must be shifted to the left by:

$$\Delta V_{ref} = \frac{V_{CC}^{2}}{2 \times \pi^{2} \times R_L \times I_{LN}}$$ with maximum power dissipated by the loudspeaker amplifier (dotted line given for V_{CC} = 5.5 V, R_L = 16 Ω).

Fig.14 Safe operating area (UBA1707T).



LINE	T_{amb} (°C)	P_{tot} (mW)
(1)	45	666
(2)	55	583
(3)	65	500
(4)	75	416

The line current value can be calculated from I_{LN} value as follows:

$$I_{line} = \frac{I_{LN} \times (R_{SET} + R_{SLPE}) + V_{LN} - V_{SLPE}}{R_{SET}}$$ where R_{SET} is the resistive part of Z_{SET}.

When power is delivered to a loudspeaker with R_L impedance, the curves must be shifted to the left by:

$$\Delta V_{ref} = \frac{V_{CC}^2}{2 \times \pi^2 \times R_L \times I_{LN}}$$ with maximum power dissipated by the loudspeaker amplifier (dotted line given for V_{CC} = 5.5 V, R_L = 16 Ω).

Fig.15 Safe operating area (UBA1707TS).

CHARACTERISTICS

I_{line} = 15 mA; V_{CC} = 3.3 V; R_{SLPE} = 10 Ω; AGC pin connected to GND; Z_{line} = 600 Ω; Z_{SET} = 619 Ω; EHI = HIGH; f = 1 kHz; T_{amb} = 25 °C; bit AGC at logic 1, all other configuration bits at logic 0; measured in test circuit of Fig.17; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{CC} and GND; bit PD)						
V_{CC}	operating supply voltage		3.0	–	5.5	V
I_{CC}	current consumption from pin V_{CC}		–	2.2	3.2	mA
$I_{CC(pd)}$	current consumption from pin V_{CC} in power-down mode	bit PD = 1	–	110	150	μA
Line interface (pins LN, SLPE and REG)						
DC CHARACTERISTICS						
V_{ref}	stabilized voltage between pins LN and SLPE	I_{line} = 11 to 140 mA	2.6	2.9	3.2	V
V_{LN}	DC line voltage between pins LN and GND	I_{line} = 2 mA	–	1.2	–	V
		I_{line} = 4 mA	–	1.8	–	V
		I_{line} = 15 mA	2.7	3.0	3.3	V
		I_{line} = 140 mA	–	4.35	–	V
$V_{LN(Rext)}$	DC line voltage between pins LN and GND with an external resistor R_{VA}	$R_{VA(SLPE–REG)}$ = 8 kΩ	–	4.5	–	V
$\Delta V_{LN(T)}$	DC line voltage variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	–	8.0	–	mV
Masks regulation (pins LCC, LVI, CST and RGL; bit CRC)						
DC CHARACTERISTICS						
$I_{LCC(max)}$	maximum current sunk by pin LCC		500	–	–	μA
$R_{int(LCC)}$	internal resistance between pins V_{CC} and LCC		–	165	–	kΩ
Voltage regulation mode						
I_{LVIV}	current sourced from pin LVI	bit CRC = 0	–	200	–	nA
Current regulation mode						
I_{knee}	start line current for current regulation mode	bit CRC = 1	–	35	–	mA
R_{REGC}	DC mask slope in current regulation mode	$I_{line} > I_{knee}$; R_{LVI} = 1 MΩ; R_{RGL} = 7.15 kΩ; bit CRC = 1	–	1.4	–	kΩ
Current limitation						
I_{prot}	current limitation level		–	145	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Electronic hook-switch control (pin EHI)						
V_{IH}	HIGH-level input voltage		2.3	–	V_{CC} + 0.4	V
V_{IL}	LOW-level input voltage	V_{CC} = 3.0 to 5.5 V	GND – 0.4	–	$0.3V_{CC}$	V
I_{bias}	input bias current	input level = HIGH	1	2	5	μA
Transmit amplifier (pins TXI+, TXI– and LN)						
$\|Z_i\|$	input impedance	between pins TXI+ and GND or TXI– and GND	–	21	–	kΩ
		between pins TXI+ and TXI–	–	36	–	kΩ
$G_{v(TX)}$	voltage gain from TXI+/TXI– to LN	V_{TXI} = 50 mV (RMS)	10.6	11.6	12.6	dB
$\Delta G_{v(TX)(f)}$	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.3	–	dB
$\Delta G_{v(TX)(T)}$	voltage gain variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
CMRR	common mode rejection ratio		–	65	–	dB
PSRR	power supply rejection ratio		–	36	–	dB
$V_{LN(max)(rms)}$	maximum sending signal (RMS value)	I_{line} = 15 mA; THD = 2%	1.2	1.4	–	V
		I_{line} = 4 mA; THD = 10%	–	0.26	–	V
$V_{iTX(max)(rms)}$	maximum transmit input voltage (RMS value) for 2% THD on pin LN	I_{line} = 15 mA	–	0.35	–	V
		I_{line} = 90 mA	–	0.75	–	V
$V_{no(LN)}$	noise output voltage at pin LN	pins TXI+ and TXI– short-circuited through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	–74	–	dBmp
Receive amplifier (pins RXI and RXO; bit RXM)						
$\|Z_i\|$	input impedance between pins RXI and GND		–	21	–	kΩ
$G_{v(RX)}$	voltage gain from RXI to RXO	V_{RXI} = 2 mV (RMS)	36.9	37.9	38.9	dB
$\Delta G_{v(RX)(f)}$	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(RX)(T)}$	voltage gain variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–	±0.3	–	dB
PSRR	power supply rejection ratio		–	68	–	dB
THD	total harmonic distortion	V_{RXI} = 2 mV (RMS)	–	0.03	–	%
		V_{RXI} = 12.5 mV (RMS)	–	2	–	%
		V_{RXI} = 19.5 mV (RMS); I_{line} = 90 mA	–	2	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{no(RXO)(rms)}$	noise output voltage at pin RXO (RMS value)	RXI open-circuit; psophometrically weighted (P53 curve)	–	–81	–	dBVp
$\Delta G_{v(RX)(m)}$	voltage gain reduction from pin RXI to RXO when muted	V_{RXI} = 10 mV (RMS); bit RXM = 1	–	80	–	dB
Automatic gain control (pin AGC; bits RAGC1, RAGC2, SAGC and AGC)						
$\Delta G_{v(trx)}$	gain control range for transmit and receive amplifiers with respect to I_{line} = 15 mA	I_{line} = 90 mA	–	6.5	–	dB
I_{start}	highest line current for maximum gain	bits RAGC1 = 1; RAGC2 = 1	–	22.5	–	mA
		bits RAGC1 = 1; RAGC2 = 0	–	25	–	mA
		bits RAGC1 = 0; RAGC2 = 1	–	27	–	mA
		bits RAGC1 = 0; RAGC2 = 0	–	29.5	–	mA
I_{stop}	lowest line current for minimum gain when I_{start} = 23 mA	bits SAGC = 0; RAGC1 = 1; RAGC2 = 1	–	62	–	mA
		bits SAGC = 1; RAGC1 = 1; RAGC2 = 1	–	43	–	mA
$\Delta G_{v(trxoff)}$	gain variation for transmit and receive amplifiers when AGC is off	bit AGC = 0; I_{line} = 15 to 140 mA	–	–	±0.2	dB
Amplifiers						
AUXILIARY AMPLIFIER (PINS AXI AND AXO; BIT AXM)						
$\lvert Z_i \rvert$	input impedance between pins AXI and GND		–	3.8	–	kΩ
$G_{v(AX)}$	voltage gain from pin AXI to AXO	V_{AXI} = 2 mV (RMS)	30.8	31.8	32.8	dB
$\Delta G_{v(AX)(f)}$	voltage gain variation with frequency referenced to 1 kHz	f = 300 to 3400 Hz	–	±0.2	–	dB
$\Delta G_{v(AX)(T)}$	voltage gain variation with temperature referenced to 25 °C	T_{amb} = –25 to +75 °C	–	±0.2	–	dB
PSRR	power supply rejection ratio		–	79	–	dB
$V_{no(AXO)(rms)}$	noise output voltage at pin AXO (RMS value)	pin AXI connected to pin GND through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	–83	–	dBVp
$\Delta G_{v(AX)(m)}$	voltage gain reduction from pin AXI to AXO when amplifier muted	V_{AXI} = 10 mV (RMS); bit AXM = 1	–	80	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LOUDSPEAKER CHANNEL (PINS LSAI1, LSAI2, LSAO, DLC AND LSPGND; BITS LSA1, LSA2, LSPD, VOL0, VOL1, VOL2 AND DLCI)						
Loudspeaker amplifier						
$\lvert Z_i \rvert$	input impedance between pins LSAI1 or LSAI2 and GND	bits LSA1 = 1, LSA2 = 1	–	21	–	kΩ
$G_{v(LSA)}$	voltage gain from LSAI1 or LSAI2 to LSAO for maximum volume	V_{LSAI} = 8 mV (RMS); bits LSA1 = 1, LSA2 = 1	26.5	28	29.5	dB
$\Delta G_{v(LSA)(f)}$	voltage gain variation with frequency referenced to 1 kHz	V_{LSAI} = 8 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
$\Delta G_{v(LSA)(T)}$	voltage gain variation with temperature referenced to 25 °C	T_{amb} = −25 to +75 °C	–	±0.3	–	dB
$V_{LSAI(rms)}$	maximum input voltage between pins LSAI1 or LSAI2 and GND (RMS value)	V_{CC} = 5.0 V; $G_{v(LSA)}$ = 7 dB; for 2% of THD in input stage	–	500	–	mV
$V_{no(LSAO)(rms)}$	noise output voltage at pin LSAO (RMS value)	pin LSAI1 (with bits LSA1 = 1, LSA2 = 0) or pin LSAI2 (with bits LSA1 = 0, LSA2 = 1) connected to pin GND through 200 Ω in series with 10 μF; psophometrically weighted (P53 curve)	–	–80	–	dBVp
Output capability						
$V_{LSAO(p-p)}$	output voltage capability at pin LSAO (peak-to-peak value)	V_{CC} = 5.0 V; $G_{v(LSA)}$ = 28 dB; V_{LSAI} = 100 mV (RMS); R_L = 16 Ω	3.0	3.6	–	V
		V_{CC} = 3.3 V; $G_{v(LSA)}$ = 28 dB; V_{LSAI} = 100 mV (RMS); R_L = 8 Ω	–	2.0	–	V
$\lvert I_{LSAO(max)} \rvert$	maximum current capability at pin LSAO (peak value)		150	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dynamic limiter						
t_{att}	attack time	V_{CC} = 3 V; $G_{v(LSA)}$ = 28 dB				
		when V_{LSAI} jumps from 20 mV (RMS) to 20 mV (RMS) + 10 dB; bit DLCI = 0	–	–	5	ms
		when V_{CC} drops below 2.7 V; bit DLCI = don't care	–	1	–	ms
t_{rel}	release time	V_{CC} = 3 V; $G_{v(LSA)}$ = 28 dB; when V_{LSAI} jumps from 20 mV (RMS) + 10 dB to 20 mV (RMS); bit DLCI = 0	–	250	–	ms
THD	total harmonic distortion at V_{LSAI} = 20 mV (RMS) + 10 dB	V_{CC} = 3 V; $G_{v(LSA)}$ = 28 dB; t > t_{att}	–	0.5	5	%
Volume control						
$\Delta G_{v(LSA)}$	voltage gain adjustment range	bits (VOL0, VOL1, VOL2) from (0, 0, 0) to (1, 1, 1)	–	21	–	dB
$\Delta G_{v(LSA)(s)}$	voltage gain adjustment step	VOL0 from 0 to 1	–	3	–	dB
Switches (pins SWI1, SWI2 and SWI3; bits SWC1, SWC2 and SWC3)						
$\lvert Z_{i(off)} \rvert$	AC impedance between pins SWIn and GND when not selected	bit SWCn = 0	700	–	–	kΩ
$\lvert Z_{i(on)} \rvert$	AC impedance between pins SWIn and GND when selected	2 mA < I_{SWIn} < 20 mA; bit SWCn = 1	–	–	30	Ω
Serial interface (pins DATA, CLK and EN)						
V_{IH}	HIGH-level input voltage		2.3	–	V_{CC} + 0.4	V
V_{IL}	LOW-level input voltage	V_{CC} = 3 to 5.5 V	GND – 0.4	–	0.3V_{CC}	V
I_{bias}	input bias current	input level = HIGH	1	2	5	µA
C_i	input capacitance at pins DATA, CLK and EN		–	4	–	pF

SERIAL BUS TIMING CHARACTERISTICS

V_{CC} = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Serial programming clock; pin CLK				
f_{clk}	clock frequency	0	300	kHz
Enable programming; pin EN				
t_{START}	delay to falling clock edge	1	–	µs
t_{END}	delay from last rising clock edge	0.1	–	µs
$t_{W(min)}$	minimum inactive pulse width	1.5	–	µs
$t_{SU;EN}$	enable set-up time to next clock edge	0.1	–	µs
Serial data; pin DATA				
$t_{SU;DATA}$	input data to clock set-up time	2	–	µs
$t_{HD;DATA}$	input data to clock hold time	2	–	µs

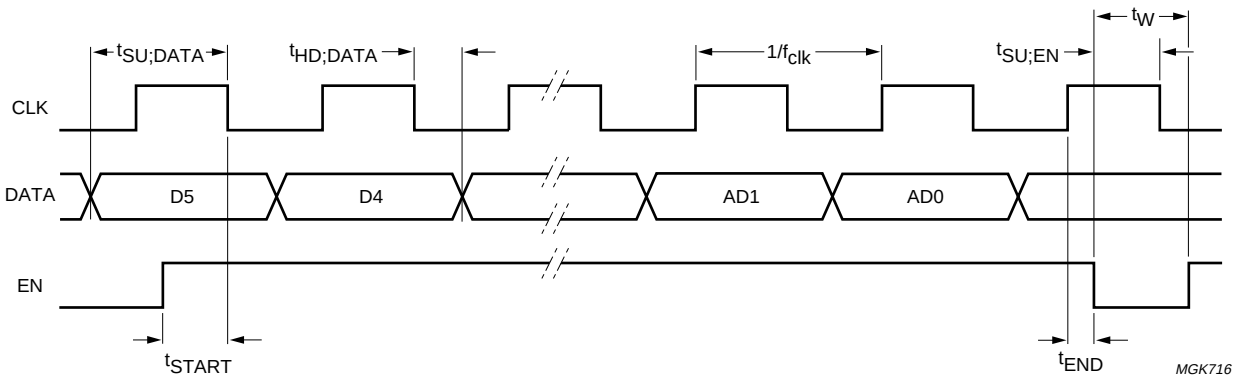


Fig.16 Serial bus timing diagram.

TEST AND APPLICATION INFORMATION

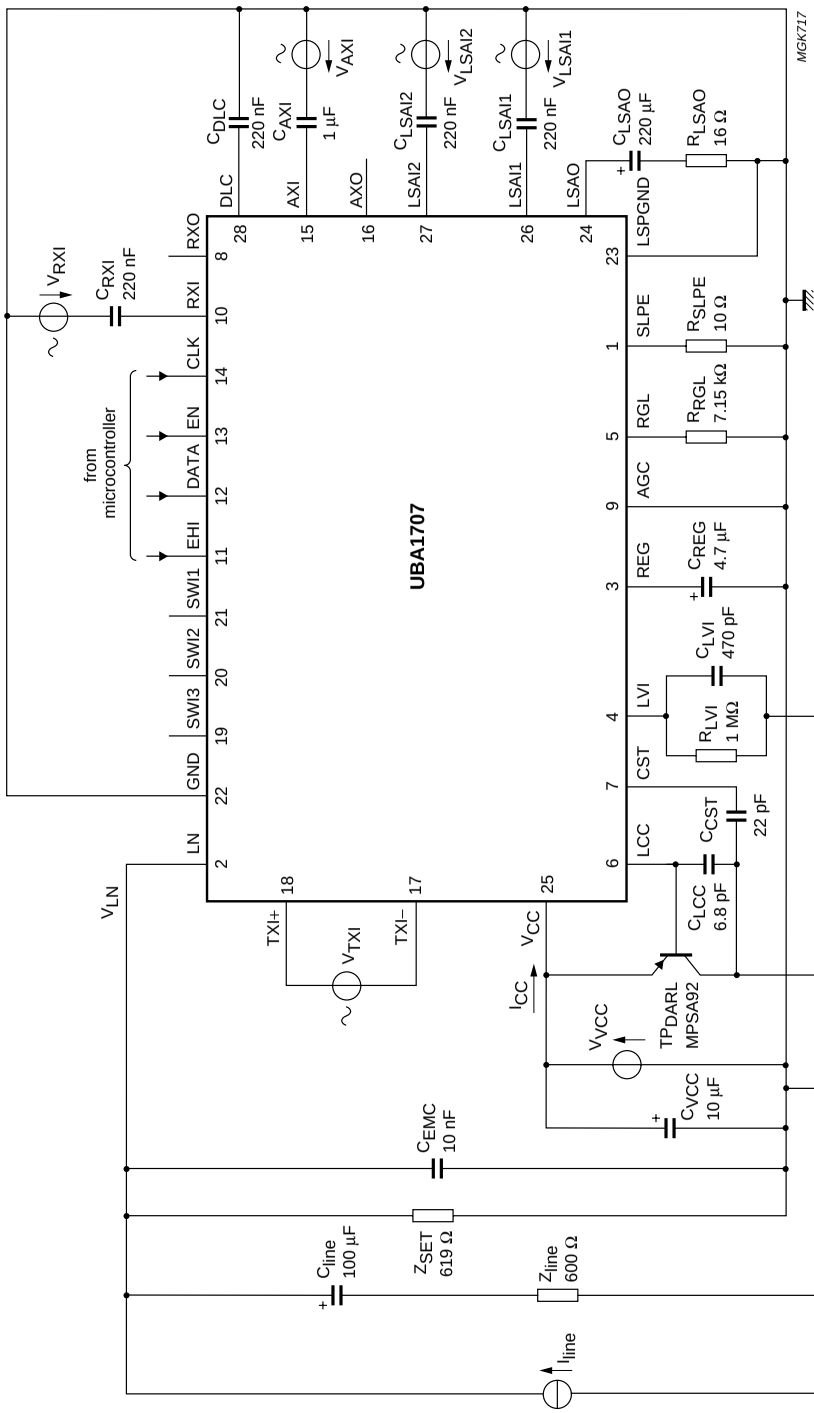


Fig.17 Test circuit.

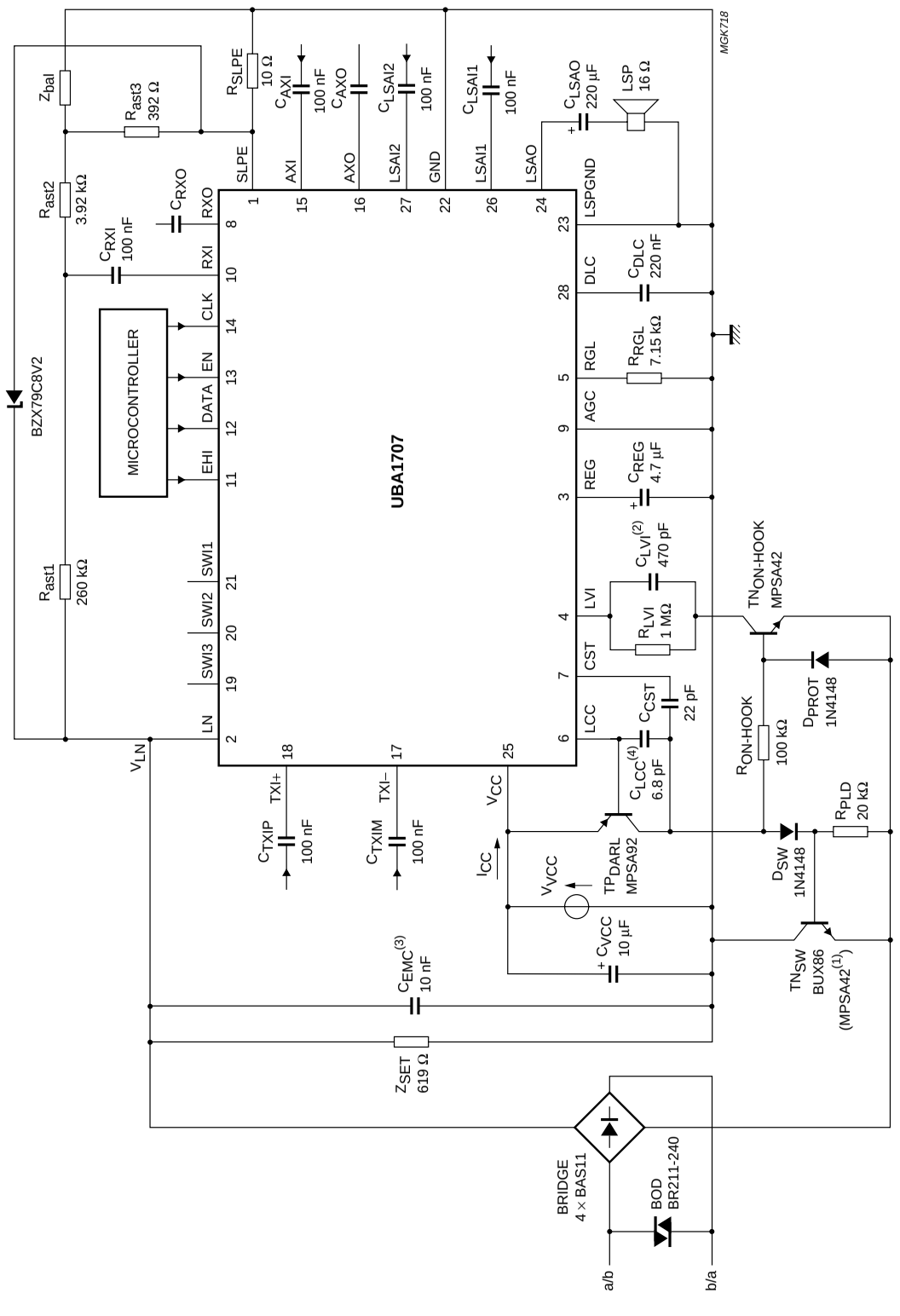
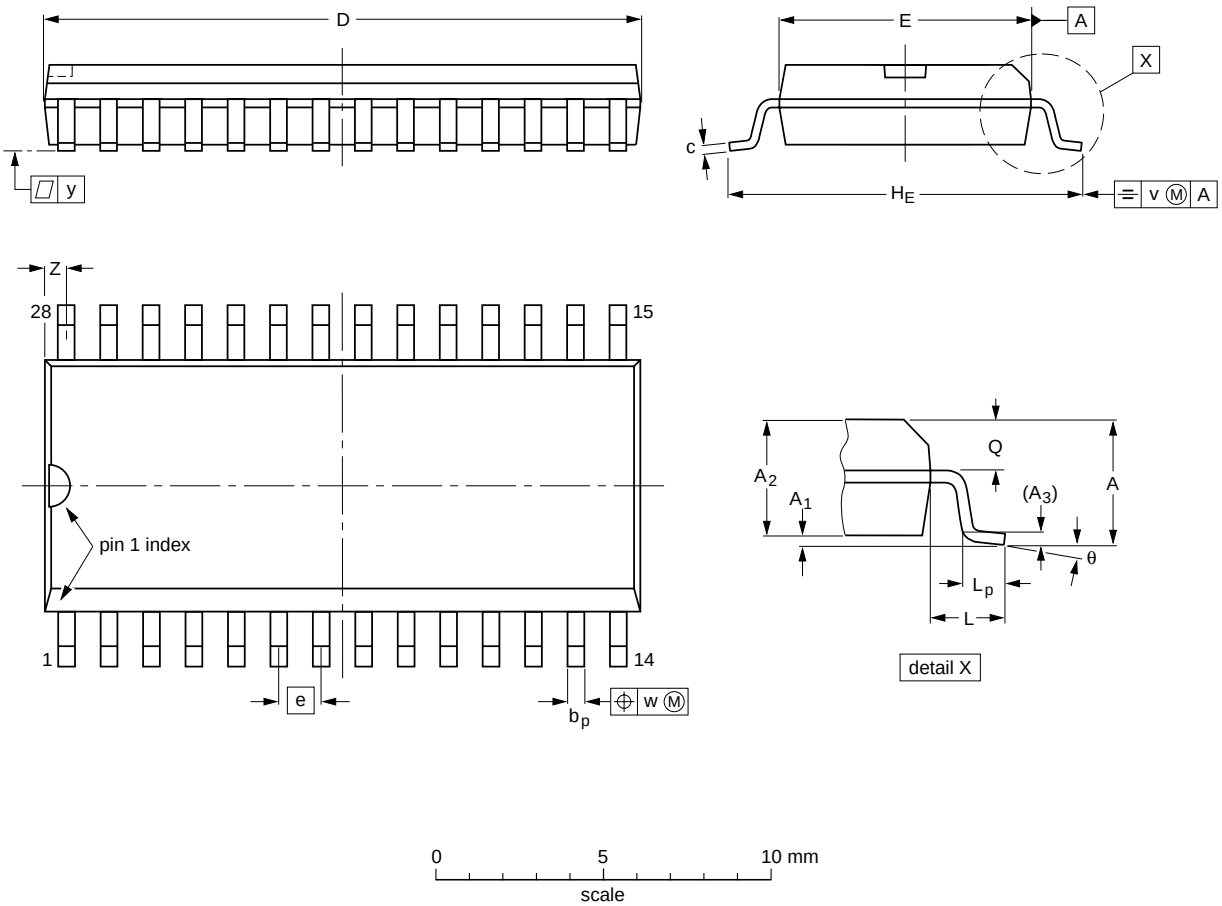


Fig.18 Typical application.

(1) In case of low line current in voltage regulation mode.
(2) Only required in current regulation mode.
(3) To improve EMC performance; necessary for stability.
(4) To improve stability only in current regulation mode.

PACKAGE OUTLINES

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

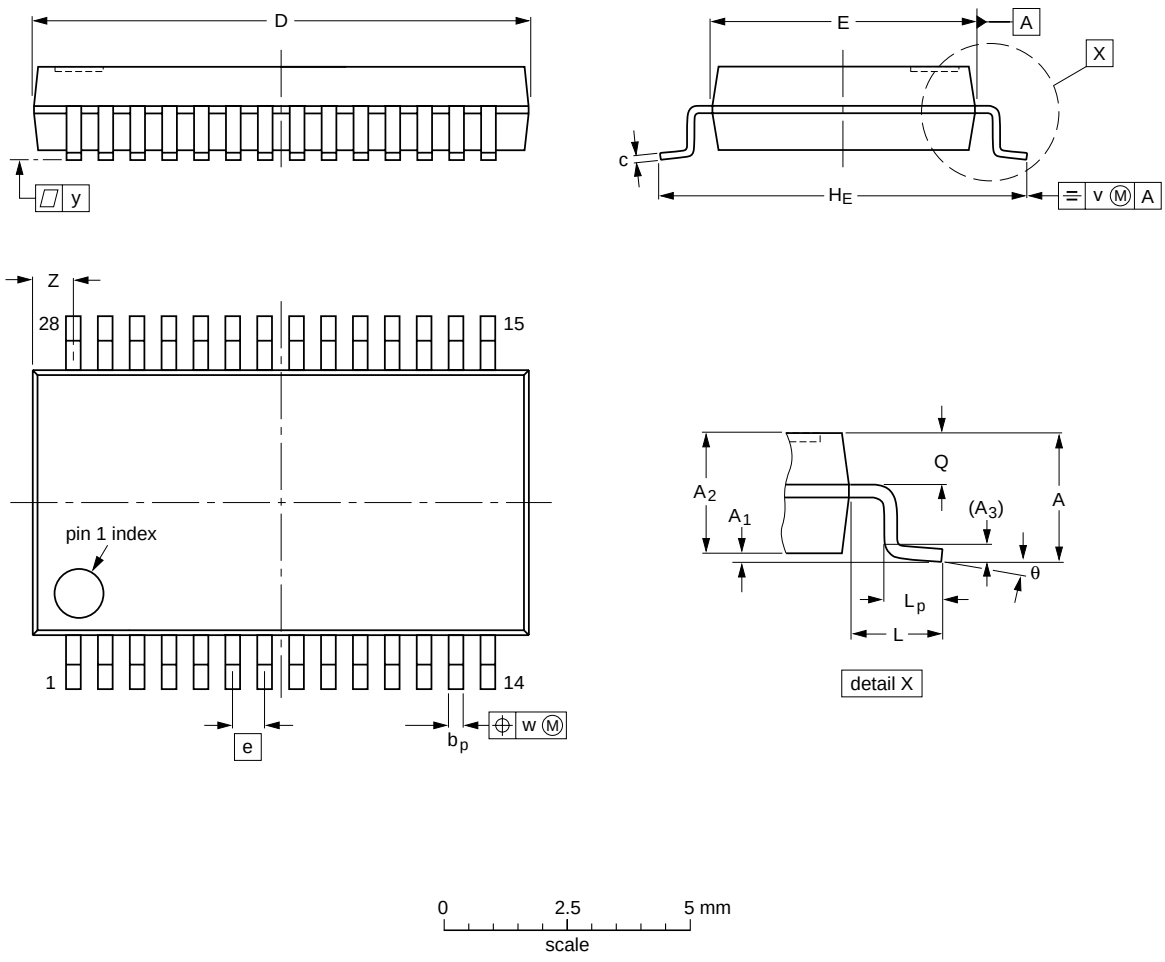
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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Where application information is given, it is advisory and does not form part of the specification.	

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