E1 TRANSCEIVER

FEATURES

- Monolithic single chip device which integrates a full-featured E1 framer with on-chip analog line interface.
- Provides frame synchronization and frame generation for a G.704/G.706 2.048 Mbit/s signal with capability to support the optional signalling and CRC multiframes.
- Supports HDB3 or AMI line coding and accepts gapped data streams to support higher rate demultiplexing.
- Supports both 75 Ohm and 120 Ohm G.703 line interfaces.
- Provides Channel Associated Signalling extraction/insertion, programmable idle code substitution, digital milliwatt code substitution, data inversion and up to 3 multiframes of signalling debounce on a per channel basis.
- Optionally extracts/inserts the datalink from/to timeslot 16 to receive/transmit Common Channel Signalling.
- Pin compatible with the PM4341A T1XC T1 Transceiver.
- Software compatible with the PM6344 EQUAD E1 Framer, and PM6388 EOCTL E1 Framer.
- Provides an 8-bit microprocessor bus interface for configuration, control and status monitoring.
- Low-power 5V CMOS technology.
- Available in a high density 80-pin (14 by 14mm) PQFP or in a 68-pin PLCC package.

APPLICATIONS

- E1 & E3 Multiplexers
- Digital Loop Carriers
- E1 Frame Relay Interfaces
- E1 ATM UNI Interfaces
- E1 Channel Service Units (CSUs) and Data Service Units (DSUs)
- Digital Access and Cross-Connect Systems (DACS) and Electronic Digital Cross-Connect Systems (EDSX)
- SDH Add/Drop Multiplexers (ADM)
- ISDN Primary Rate Interfaces (PRI)
- Digital Private Branch Exchanges (PBX)
- E1 & E3 Test Equipment

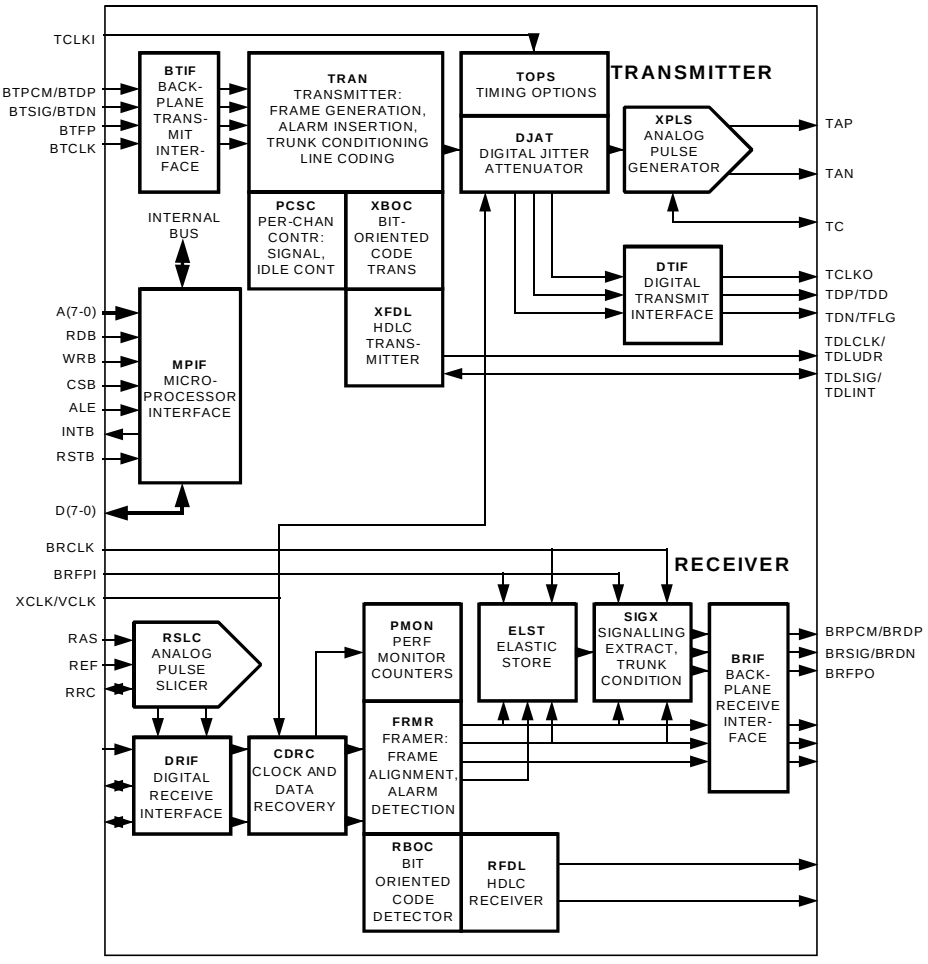
RECEIVE SECTION

- Provides indications of loss of signal, loss of frame alignment (OOF), loss of signalling multiframe alignment and loss of CRC multiframe alignment.
- Declares red and AIS alarms using Q.516 recommended integration periods
- Supports line and path performance monitoring according to ITU-T recommendations. Accumulators are provided for CRC-4 errors, Far End Block Errors, Frame sync errors, and Line Code Violations.
- Provides an integral HDLC/LAPD interface which may be used for terminating a CCS or National Bits datalink.
- Provides a two frame elastic store for jitter and wander attenuation.
- Provides programmable trunk conditioning on a per channel basis.

TRANSMIT SECTION

- Supports transmission of AIS, timeslot 16 AIS, remote alarm signal or remote multiframe alarm signal.
- Provides an integral HDLC/LAPD interface which may be used for generating a CCS or National Bits datalink.
- Provides an integrated digital phase locked loop for generation of a low jitter transmit clock.
- Provides a FIFO buffer for jitter attenuation and rate conversion.
- Provides programmable trunk conditioning which forces trouble code substitution and signalling conditioning on a per channel basis.

BLOCK DIAGRAM

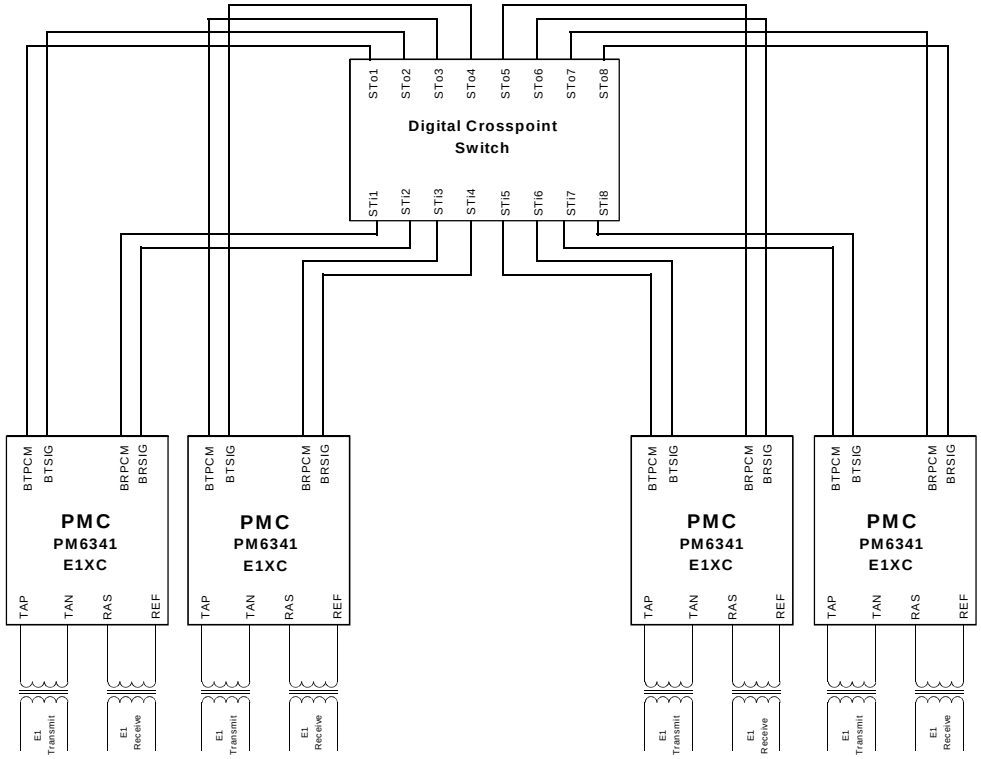


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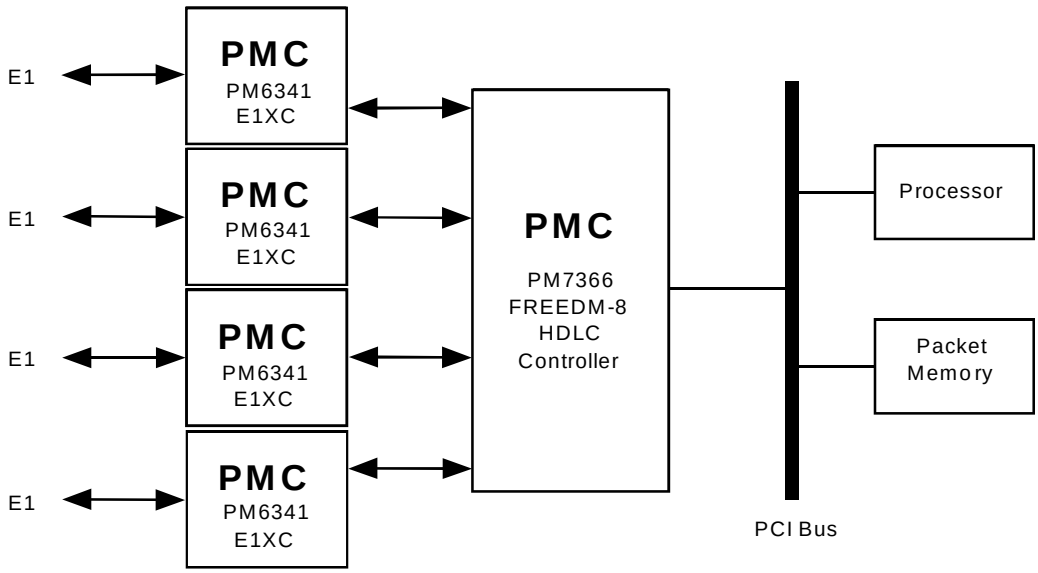
E1 TRANSCEIVER

TYPICAL APPLICATIONS:

1/0 CROSS-CONNECT WITH E1 INTERFACE:



FULLY CHANNELIZED QUAD E1 HDLC CARD:



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