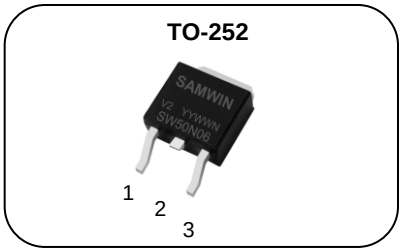
N-channel Enhanced mode TO-252 MOSFET

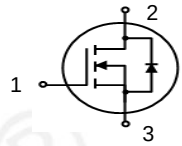
Features

- High ruggedness
- Low $R_{DS(ON)}$ (Typ 11mΩ)@V_{GS}=10V
  (Typ 14mΩ)@V_{GS}=4.5V
- Low Gate Charge (Typ 59nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application:Electronic Ballast, Motor Control
  Synchronous Rectification, Inverter



1. Gate 2. Drain 3. Source

BV_{DSS} : 60V
I_D : 50A
$R_{DS(ON)}$: 14mΩ @V_{GS}=4.5V
11mΩ @V_{GS}=10V



General Description

This power MOSFET is produced with advanced technology of SAMWIN.
This technology enable the power MOSFET to have better characteristics, including fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics.

LEAD-FREE RoHS

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW D 50N06V2	SW50N06V2	TO-252	REEL

Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to source voltage		60	V
I_D	Continuous drain current (@T_C=25°C)		50*	A
	Continuous drain current (@T_C=100°C)		31.5*	A
I_{DM}	Drain current pulsed	(note 1)	200	A
V_{GS}	Gate to source voltage		±20	V
E_{AS}	Single pulsed avalanche energy	(note 2)	81	mJ
E_{AR}	Repetitive avalanche energy	(note 1)	9	mJ
dv/dt	Peak diode recovery dv/dt	(note 3)	5	V/ns
P_D	Total power dissipation (@T_C=25°C)		78	W
	Derating factor above 25°C		0.6	W/°C
T_{STG}, T_J	Operating junction temperature & storage temperature		-55 ~ + 150	°C
T_L	Maximum lead temperature for soldering purpose, 1/8 from case for 5 seconds.		300	°C

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thjc}	Thermal resistance, Junction to case	1.6	°C/W

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Electrical characteristic (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	60			V
ΔBV_{DSS} / ΔT_J	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25°C		0.04		V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=60V, V_{GS}=0V			1	uA
		V_{DS}=48V, T_C=125°C			50	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=20V, V_{DS}=0V			100	nA
	Gate to source leakage current, reverse	V_{GS}=-20V, V_{DS}=0V			-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	1		3	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D=25A		11	14	mΩ
		V_{GS}=4.5V, I_D=25A		14	17	mΩ
G_{fs}	Forward transconductance	V_{DS}=10V, I_D=25A		80		S
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		2570		pF
C_{oss}	Output capacitance			175		
C_{rss}	Reverse transfer capacitance			170		
$t_{d(on)}$	Turn on delay time	V_{DS}=30V, I_D=50A, R_G=25Ω, V_{GS}=10V (note 4,5)		24		ns
t_r	Rising time			100		
$t_{d(off)}$	Turn off delay time			166		
t_f	Fall time			66		
Q_g	Total gate charge	V_{DS}=50V, V_{GS}=10V, I_D=50A (note 4,5)		59		nC
Q_{gs}	Gate-source charge			9		
Q_{gd}	Gate-drain charge			22		

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			50	A
I_{SM}	Pulsed source current				200	A
V_{SD}	Diode forward voltage drop.	I_S=50A, V_{GS}=0V			1.4	V
t_{rr}	Reverse recovery time	I_S=50A, V_{GS}=0V, dI_F/dt=100A/us		18		ns
Q_{rr}	Reverse recovery charge			8.7		nC

※. Notes

1. Repeatitive rating : pulse width limited by junction temperature.
2. L =0.18mH, I_{AS} =30A, V_{DD}=50V, R_G=25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 50A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25°C
4. Pulse Test : Pulse Width ≤ 300us, duty cycle ≤ 2%.
5. Essentially independent of operating temperature.

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Fig. 1. On-state characteristics

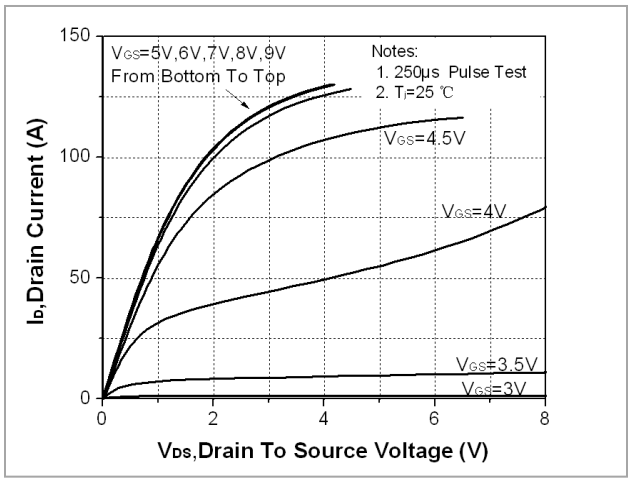


Fig. 2. On-resistance variation vs. drain current and gate voltage

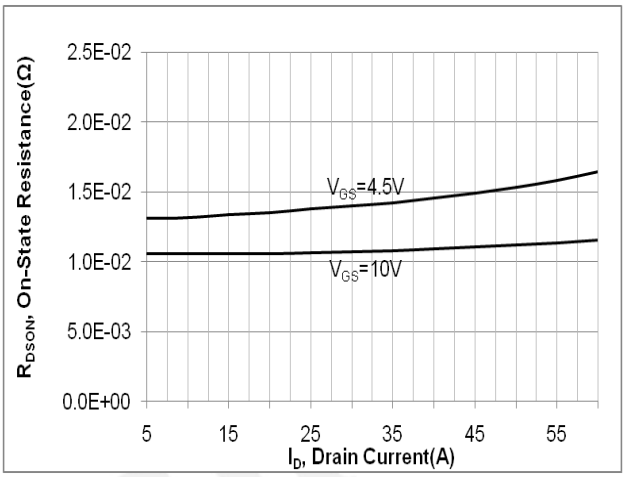


Fig. 3. Gate charge characteristics

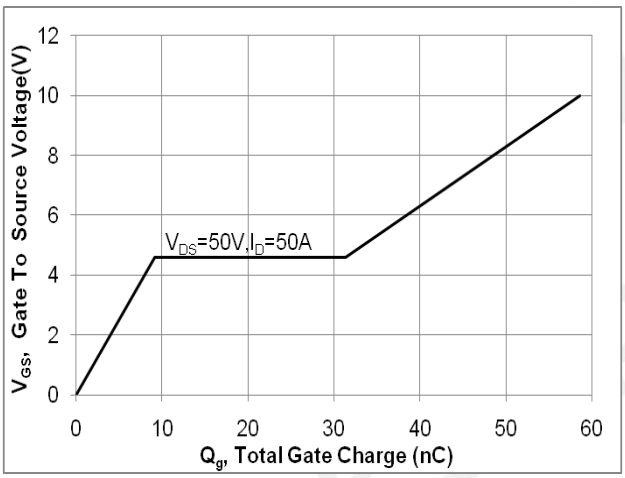


Fig. 4. On-state current vs. diode forward voltage

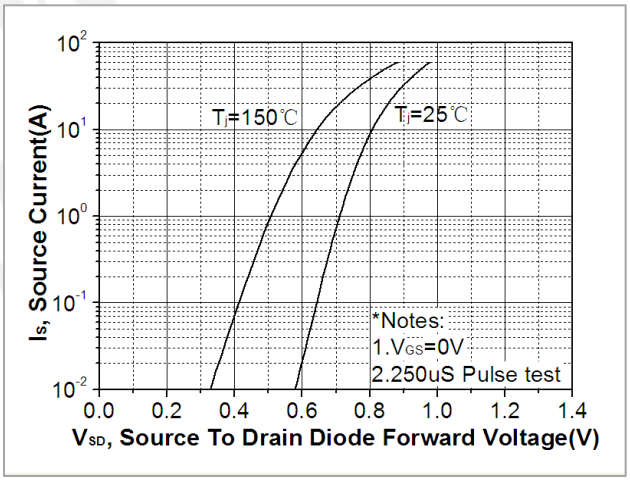


Fig 5. Breakdown voltage variation vs. junction temperature

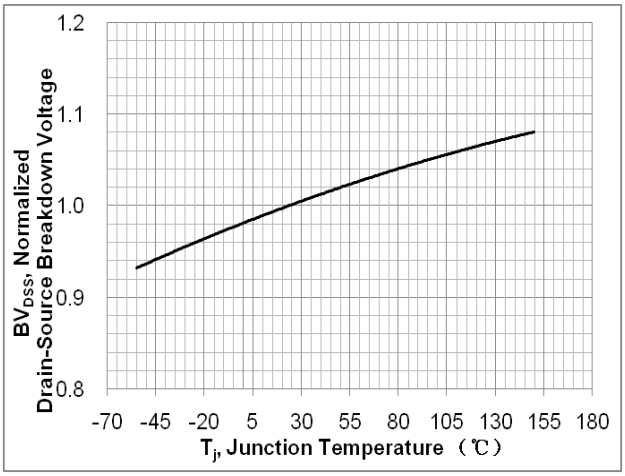
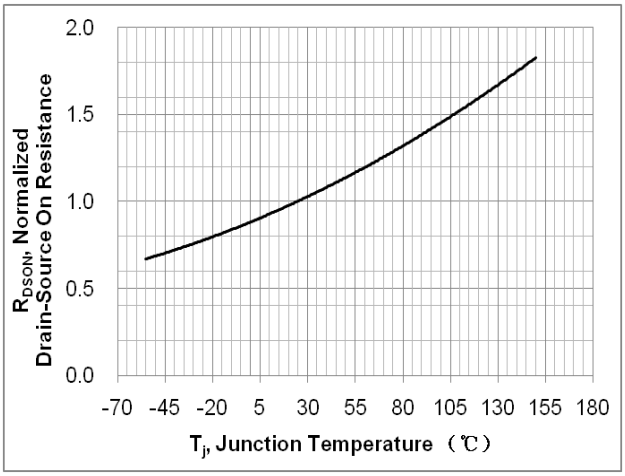


Fig. 6. On-resistance variation vs. junction temperature



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Fig. 7. Maximum safe operating area

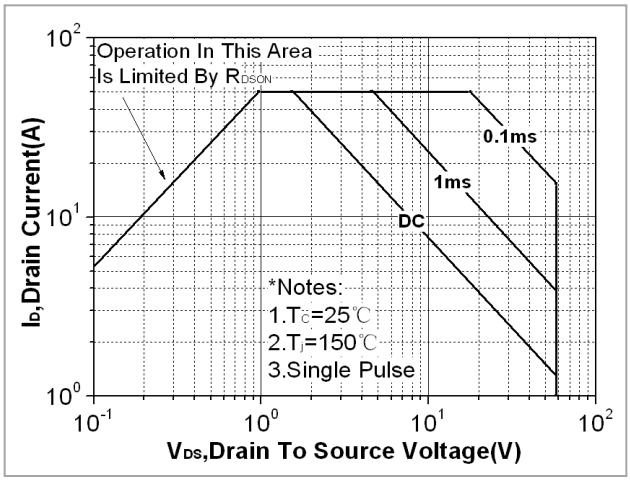


Fig. 8. Capacitance Characteristics

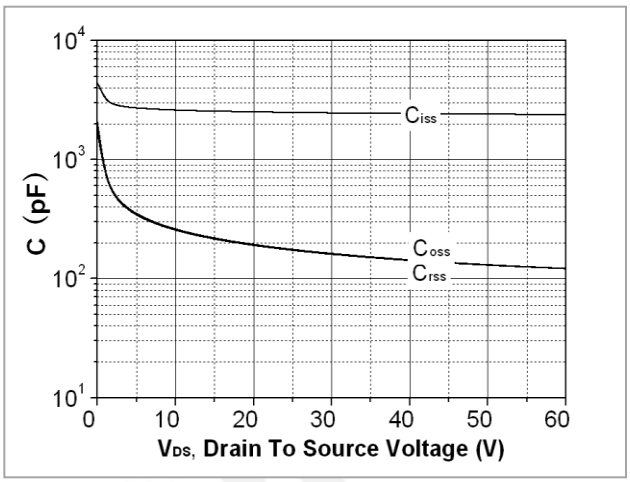


Fig. 9. Transient thermal response curve

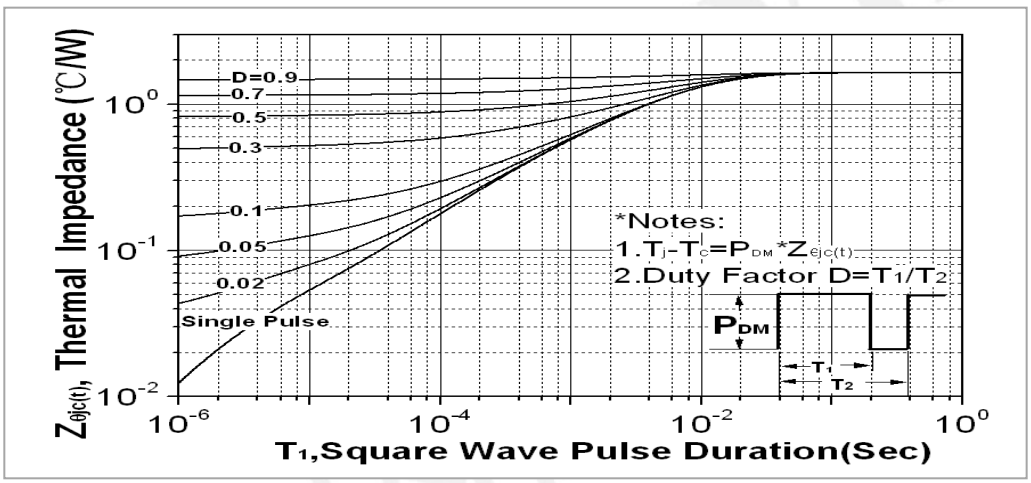
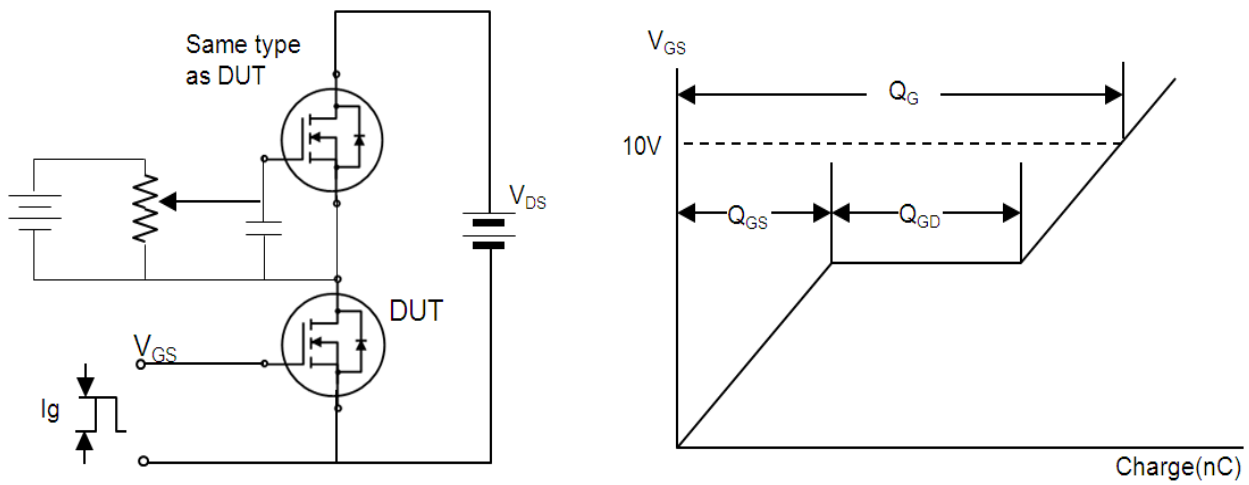


Fig. 10. Gate charge test circuit & waveform



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Fig. 11. Switching time test circuit & waveform

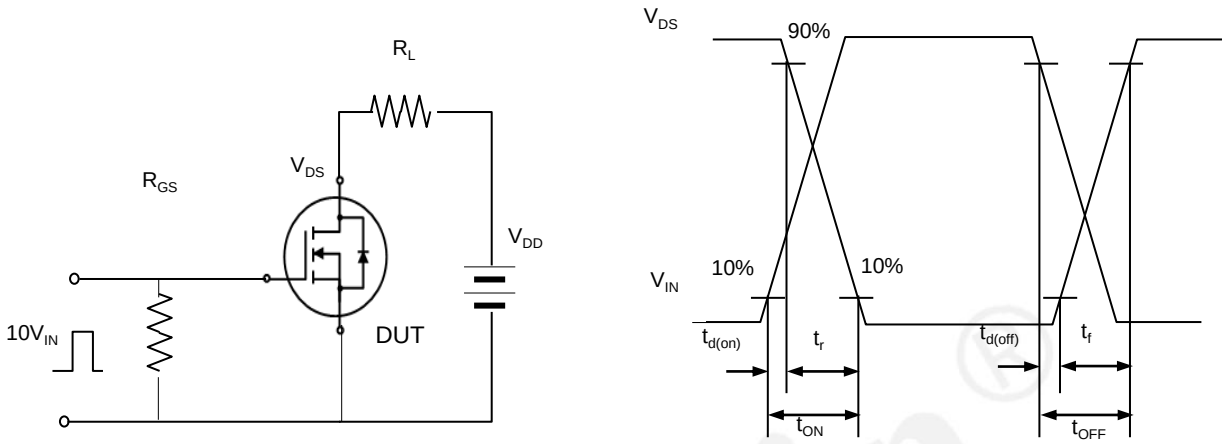


Fig. 12. Unclamped Inductive switching test circuit & waveform

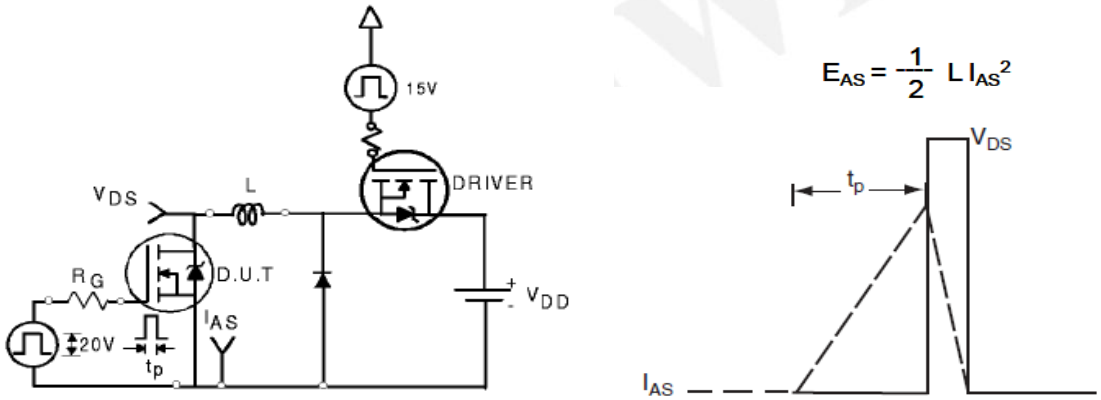
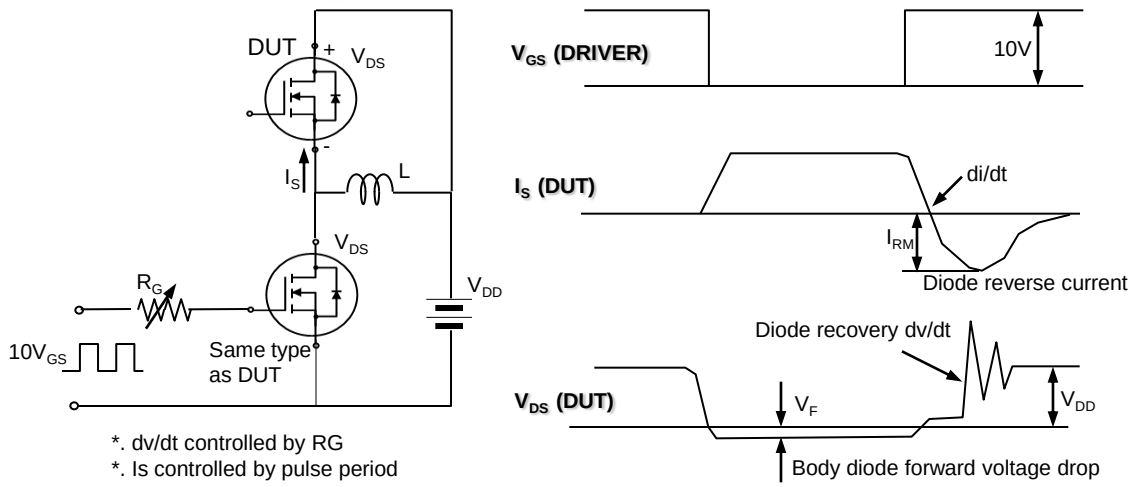


Fig. 13. Peak diode recovery dv/dt test circuit & waveform



*. dv/dt controlled by RG
*. Is controlled by pulse period

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* Qualification standards can also be found on the Web site (**http://www.semipower.com.cn**)
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