

# N-Channel JFET Monolithic Dual



## U443 / U444

### FEATURES

- High Gain .....  $g_{fs} > 6 \text{ mS typical}$
- Low Leakage .....  $I_g < 1 \text{ pA typical}$
- Low Noise

### APPLICATIONS

- Differential Wideband Amplifiers
- VHF/UHF Amplifiers
- Test and Measurement
- Multi-Chip/Hybrids

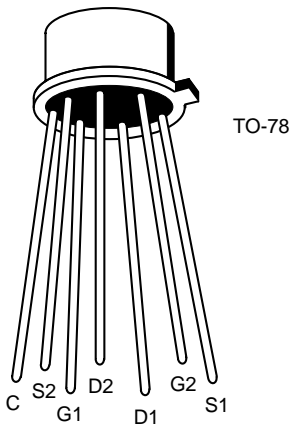
### DESCRIPTION

The U443 Series is an N-Channel Monolithic Dual JFET designed for high speed amplifier circuits. Featuring high gain ( $> 6 \text{ mS typical}$ ), low leakage ( $< 1 \text{ pA typical}$ ) and low noise this device is an excellent choice for high performance test and measurement, wideband amplifiers and VHF/UHF circuits.

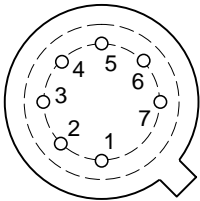
### ORDERING INFORMATION

Part	Package	Temperature Range
U443-4	Hermetic M0-002AG (TO-78)	-55°C to +150°C
XU443-4	Sorted Chips in Carriers	-55°C to +150°C

### PIN CONFIGURATION



- 1 SOURCE 1
- 2 DRAIN 1
- 3 GATE 1
- 4 CASE/BODY
- 5 SOURCE 2
- 6 DRAIN 2
- 7 GATE 2



BOTTOM VIEW

CJ1

**ABSOLUTE MAXIMUM RATINGS** ( $T_A = 25^{\circ}\text{C}$  unless otherwise noted)

Parameter/Test Condition	Symbol	Limit	Unit
Gate-Drain Voltage	$V_{GD}$	-25	V
Gate-Source Voltage	$V_{GS}$	-25	V
Gate-Gate Voltage	$V_{GG}$	$\pm 50$	V
Forward Gate Current	$I_G$	50	mA
Power Dissipation (per side)	$P_D$	367	mW
(total)		500	mW
Power Derating (per side)		3	mW/ $^{\circ}\text{C}$
(total)		4	mW/ $^{\circ}\text{C}$
Operating Junction Temperature	$T_J$	-55 to 150	$^{\circ}\text{C}$
Storage Temperature	$T_{stg}$	-65 to 200	$^{\circ}\text{C}$
Lead Temperature (1/16" from case for 10 seconds)	$T_L$	300	$^{\circ}\text{C}$

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^{\circ}\text{C}$  unless otherwise noted)

SYMBOL	CHARACTERISTCS	TYP <sup>1</sup>	U443		U444		UNIT	TEST CONDITIONS		
			MIN	MAX	MIN	MAX				
STATIC										
V <sub>(BR)GSS</sub>	Gate-Source Breakdown Voltage	-35	-25		-25		V	I <sub>G</sub> = -1μA, V <sub>DS</sub> = 0V		
V <sub>GS(OFF)</sub>	Gate-Source Cut off Voltage	-3.5	-1	-6	-1	-6		V <sub>DS</sub> = 10V, I <sub>D</sub> = 1nA		
I <sub>DSS</sub>	Saturation Drain Current <sup>2</sup>	15	6	30	6	30	mA	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V		
I <sub>GSS</sub>	Gate Reverse Current	-1		-500		-500	pA	V <sub>GS</sub> = -15V, V <sub>DS</sub> = 0V		
		-2					nA	T <sub>A</sub> = 150°C		
I <sub>G</sub>	Gate Operating Current	-1		-500		-500	pA	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA		
		-0.3					nA	T <sub>A</sub> = 125°C		
V <sub>GS(F)</sub>	Gate-Source Forward Voltage	0.7					V	I <sub>G</sub> = 1mA, V <sub>DS</sub> = 0V		
DYNAMIC										
g <sub>fs</sub>	Common-Source Forward Transconductance	6	4.5	9	4.5	9	mS	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA f = 1kHz		
g <sub>os</sub>	Common-Source Output Conductance	70		200		200	μS			
C <sub>iss</sub>	Common-Source Input Capacitance	3					pF	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA f = 1MHz		
C <sub>rss</sub>	Common-Source Reverse Transfer Capacitance	1								
$\bar{e}_n$	Equivalent Input Noise Voltage	4					nV/√Hz	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA f = 10kHz		
MATCHING										
V <sub>GS1</sub> -V <sub>GS2</sub>	Differential Gate-Source Voltage	6		10		20	mV	V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA		
$\Delta \mid \frac{V_{GS1}-V_{GS2}}{\Delta T}$	Gate-Source Voltage Differential Change with Temperature	20					μV/ °C	T = -55 to 25°C	V <sub>DG</sub> =10V, I <sub>D</sub> = 5mA	
		20						T = 25 to 125°C		
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.97						V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V		
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.97						V <sub>DG</sub> = 10V, I <sub>D</sub> = 5mA f= 1 kHz		
CMRR	Common Mode Rejection Ratio	85					dB	V <sub>DD</sub> = 5 to 10V, I <sub>D</sub> = 5mA		

NOTES: 1. For design aid only, not subject to production testing.  
2. Pulse test;  $PW = 300\mu\text{s}$ , duty cycle  $\leq 3\%$ .