National Semiconductor

LMX2541

PRELIMINARY
July 2, 2009

Ultra-Low Noise PLLatinum Frequency Synthesizer with Integrated VCO

General Description

The LMX2541 is an ultra low noise frequency synthesizer which integrates a high performance delta-sigma fractional N PLL, a VCO with fully integrated tank circuit, and an optional frequency divider. The PLL offers an unprecedented normalized noise floor of -225 dBc/Hz and can be operated with up to 104 MHz of phase-detector rate (comparison frequency) in both integer and fractional modes. The PLL can also be configured to work with an external VCO.

The LMX2541 integrates several low-noise, high precision LDOs and output driver matching network to provide higher supply noise immunity and more consistent performance, while reducing the number of external components. When combined with a high quality reference oscillator, the LMX2541 generates a very stable, ultra low noise signal.

The LMX2541 is offered in a family of 6 devices with varying VCO frequency range from 1990 MHz up to 4 GHz. Using a flexible divider, the LMX2541 can generate frequencies as low as 31.6 MHz. The LMX2541 is a monolithic integrated circuit, fabricated in a proprietary BiCMOS process. Device programming is facilitated using a three-wire MICROWIRE interface that can operate down to 1.8 volts. Supply voltage ranges from 3.15 to 3.45 volts. The LMX2541 is available in a 36 pin 6x6x0.8 mm Lead-Free Leadless Leadframe Package (LLP).

Device	VCO Frequency
LMX2541SQ2060E	1990 - 2240
LMX2541SQ2380E	2200 - 2530
LMX2541SQ2690E	2490 - 2865
LMX2541SQ3030E	2810 - 3230
LMX2541SQ3320E	3130 - 3600
LMX2541SQ3740E	3480 - 4000

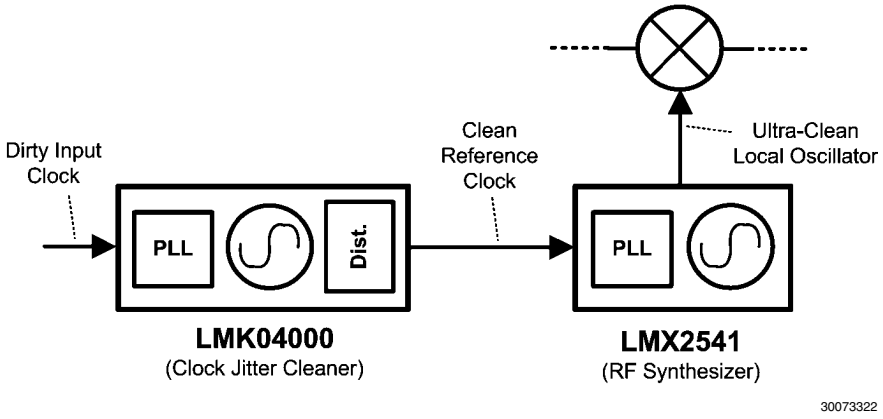
Features

- **Very Low RMS Noise and Spurs**
  - -225 dBc/Hz Normalized PLL Phase Noise
  - Integrated RMS Noise (100 Hz - 20 MHz)
    - 2 mrad (100 Hz - 20 MHz) at 2.1 GHz
    - 3.5 mrad (100 Hz - 20 MHz) at 3.5 GHz
- Ultra Low-Noise Integrated VCO
- External VCO Option (Internal VCO Bypassed)
- VCO Frequency Divider 1 to 63 (all values)
- Programmable Output Power
- Up to 104 MHz Phase Detector Frequency
- Integrated Low-Noise LDOs
- Programmable Charge Pump Output
- Partially Integrated Loop Filter
- Digital Frequency Shift Keying (FSK) Modulation Pin
- Integrated Reference Crystal Oscillator Circuit
- Hardware and Software Power Down
- FastLock Mode with Cycle Slip Reduction
- Analog and Digital Lock Detect
- 1.6 V Logic Compatibility

Target Applications

- Wireless Infrastructure (UMTS, LTE, WiMax)
- Broadband Wireless
- Wireless Meter Reading
- Test and Measurement

System Diagram



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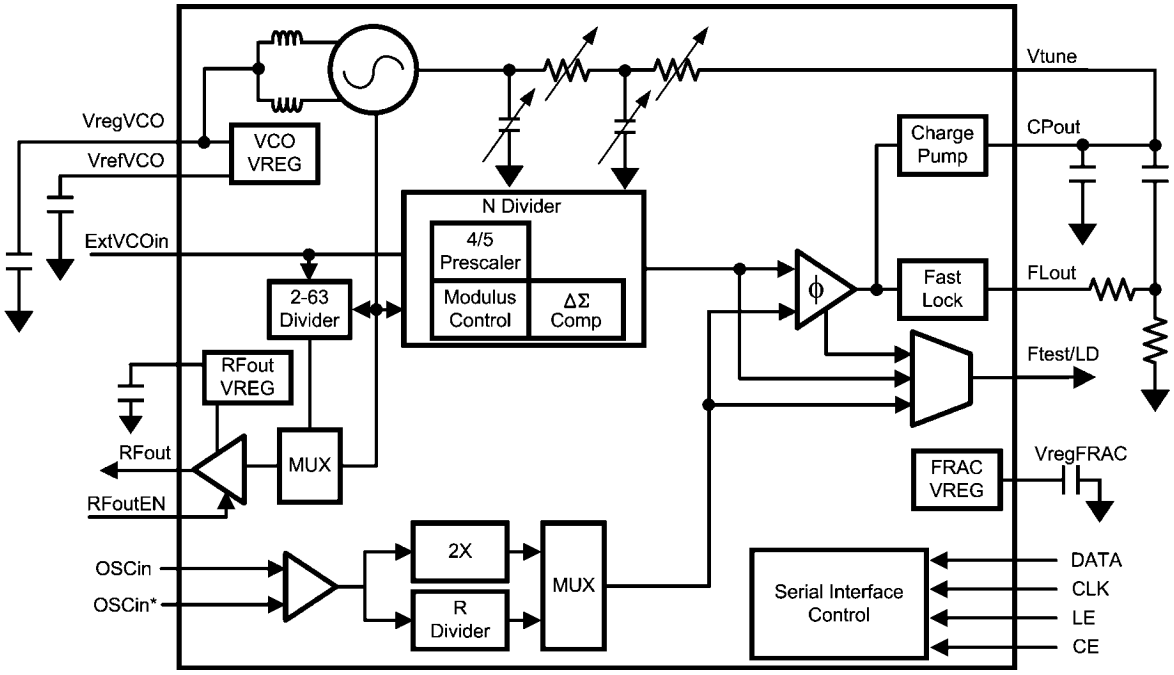
LMX2541 Frequency Chart

Divide Value	2060E		2380E		2690E		3030E		3320E		3740E	
	Start	Stop	Start	Stop	Start	Stop	Start	Stop	Start	Stop	Start	Stop
1	1990.0	2240.0	2200.0	2530.0	2490.0	2865.0	2810.0	3230.0	3130.0	3600.0	3480.0	4000.0
2	995.0	1120.0	1100.0	1265.0	1245.0	1432.5	1405.0	1615.0	1565.0	1800.0	1740.0	2000.0
3	663.3	746.7	733.3	843.3	830.0	955.0	936.7	1076.7	1043.3	1200.0	1160.0	1333.3
4	497.5	560.0	550.0	632.5	622.5	716.3	702.5	807.5	782.5	900.0	870.0	1000.0
5	398.0	448.0	440.0	506.0	498.0	573.0	562.0	646.0	626.0	720.0	696.0	800.0
6	331.7	373.3	366.7	421.7	415.0	477.5	468.3	538.3	521.7	600.0	580.0	666.7
7	284.3	320.0	314.3	**361.4**	355.7	**409.3**	401.4	**461.4**	447.1	**514.3**	497.1	**571.4**
8	248.8	**280.0**	275.0	316.3	311.3	358.1	351.3	403.8	391.3	450.0	435.0	500.0
…	…	…	…	…	…	…	…	…	…	…	…	…
63	31.6	35.6	34.9	40.2	39.5	45.5	44.6	51.3	49.7	57.1	55.2	63.5

All devices have continuous frequency coverage below a divide value of 8 (7 for most devices) down to their minimum frequency achievable with divide by 63. The numbers in bold show the upper end of this minimum continuous frequency range. Below 570 MHz, all devices can be used down to their minimum frequency of Min (f_{VCO}) / 63.

Functional Block Diagram



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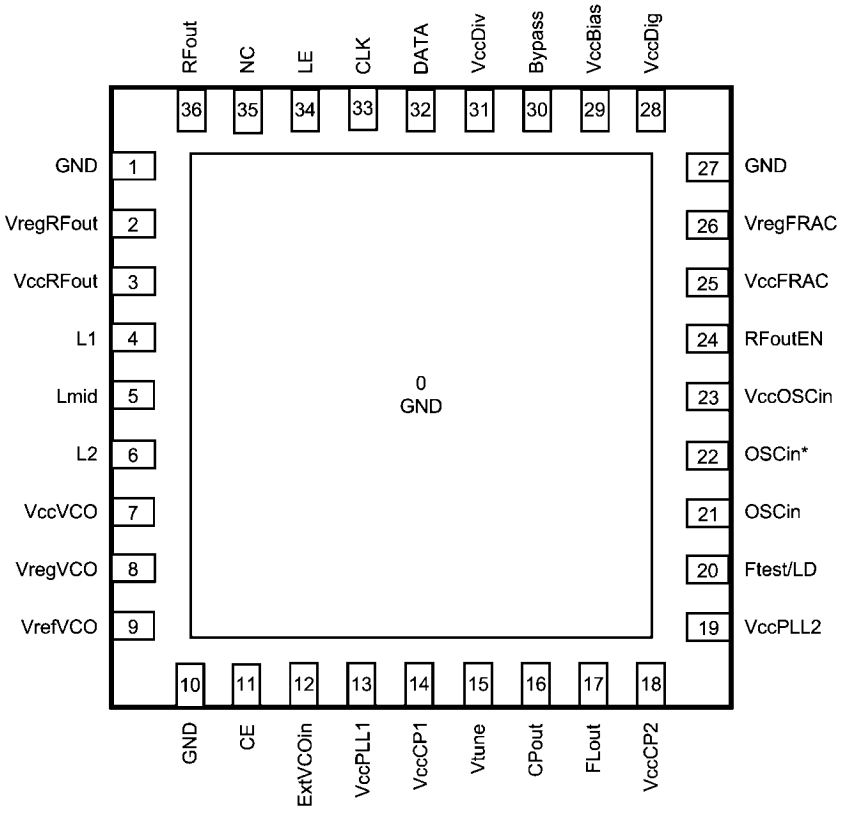
Connection Diagram

36-Pin SQ Package (Top View)



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Pin Descriptions

Pin #	Name	Type	Description
0	GND	GND	The DAP pad must be grounded.
1	GND	GND	
2	VregRFout	LDO Output	LDO Output for RF output buffer.
3	VccRFout	Supply (LDO Input)	Supply for the RF output buffer.
4	L1	NC	Do not connect this pin.
5	Lmid	NC	Do not connect this pin.
6	L2	NC	Do not connect this pin.
7	VccVCO	Supply (LDO Input)	Supply for the VCO.
8	VregVCO	LDO Output	LDO Output for RF output buffer.
9	VrefVCO	LDO Bypass	LDO Bypass
10	GND	GND	
11	CE	CMOS	Chip Enable. The device needs to be programmed for this pin to properly power down the device.
12	ExtVCOin	RF Input	Optional input for use with an external VCO. This pin should be AC coupled if used or left open if not used.
13	VccPLL1	Supply	Power supply for PLL N counter.
14	VccCP1	Supply	Power supply for PLL charge pump up current.
15	Vtune	High-Z Input	Tuning voltage input to the VCO.
16	CPout	Output	Charge pump output.
17	FLout	Output	Fastlock output.
18	VccCP2	Supply	Power supply for PLL charge pump down current.
19	VccPLL2	Supply	Power supply for PLL R Counter
20	Ftest/LD	Output	Software controllable multiplexed CMOS output. Can be used to monitor PLL lock condition.
21	OSCin	High-Z Input	Oscillator input signal. If not being used with an external crystal, this input should be AC coupled.
22	OSCin*	High-Z Input	Complementary oscillator input signal. Can also be used with an external crystal. If not being used with an external crystal, this input should be AC coupled.
23	VccOSCin	Supply	Supply for the OSCin buffer.
24	RFoutEN	Input	Software programmable output enable pin.
25	VccFRAC	Supply (LDO Input)	Power Supply for the fractional circuitry.
26	VregFRAC	LDO Output	Regulated power supply used for the fractional delta-sigma circuitry.
27	GND	GND	
28	VccDig	Supply	Supply for digital circuitry, such the MICROWIRE.
29	VccBias	Supply	Supply for Bias circuitry that is for the whole chip.
30	Bypass	Bypass	Put a cap to the VccBias pin.
31	VccDiv	Supply	Supply for the output divider
32	DATA	High-Z Input	MICROWIRE serial data input. High impedance CMOS input. This pin must not exceed 3.45 V.
33	CLK	High-Z Input	MICROWIRE clock input. High impedance CMOS input. This pin is used for the digital FSK modulation feature. This pin must not exceed 3.45 V.
34	LE	High-Z Input	MICROWIRE Latch Enable input. High impedance CMOS input. This pin must not exceed 3.45 V.
35	NC	NC	No connect.
36	RFout	RF Output	RF output. Must be AC coupled if used.

Absolute Maximum Ratings (Notes 1, 2, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Parameter	Symbol	Ratings	Units
Power Supply Voltage	Vcc	-0.3 to 3.6	V
Input Voltage to pins other than Vcc Pins (Note 4)	V_{IN}	-0.3 to (Vcc+0.3)	V_{IN}
Storage Temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (solder 4 sec.)	T_L	+ 260	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage (All Vcc Pins)	Vcc	3.15	3.3	3.45	V
Ambient Temperature	T_A	-40		+85	°C

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only to for the test conditions listed.

Note 2: This Device is a high performance RF integrated circuit with an ESD rating < 2kV and is ESD sensitive. Handling and assembly of this device should only be done at ESD-free workstations.

Note 3: Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is only implied at these or any other conditions in excess of those given in the

Note 4: Never to exceed 3.6 V.

Electrical Characteristics

(3.15 V ≤ V_{CC} ≤ 3.45 V, -40°C ≤ T_A ≤ 85 °C; except as specified. Typical values are at Vcc = 3.3 V, 25 C.)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Current Consumption							
I_{CC}	Entire ChipPower Supply Current with all blocks enabled	Default Power Mode (Note 5)	VCO_DIV>1		170	204	mA
			VCO_DIV=1		130	156	
I_{PLL}	Current for External VCO Mode (Note 6)	RFoutEN = LOW			72	85	mA
I_{DIV}	Current for Divider Only Mode	VCO_DIV >1 Default Power Mode			84	102	mA
$I_{CC}PD$	Power Down Current	CE = 0 V, Device Initialized			100	250	µA
Oscillator (Normal Mode Operation with XO=0)							
$I_{IH}OSC$ in	Oscillator Input High Current for OSCin and OSCin*	V_{IH} = 2.75 V				300	µA
$I_{IL}OSCin$	Oscillator Input Low Current for OSCin and OSCin* pins	V_{IL} = 0		-100			µA
f_{OSCin}	Frequency Range	Limited to ½ · f_{PD} when the Oscillator doubler is enabled.		5		900	MHz
dv_{OSCin}	Slew Rate	Single-Ended Mode		150			V/µs
v_{OSCin}	Oscillator Sensitivity	Single-Ended		0.2		2.0	Vpp
		Differential		0.4		3.1	
Oscillator (Crystal Mode with XO=1)							
f_{XTAL}	Crystal Frequency Range	V_{IH} = 2.75 V		5		20	MHz
ESR_{XTAL}	Crystal Equivalent Series Resistance	This a requirement for the crystal, not a characteristic of the LMX2541.				100	Ω
P_{XTAL}	Power Dissipation in Crystal	This requirement is for the crystal, not a characteristic of the LMX2541.		TBD			µW
C_{OSCin}	Input Capacitance of OSCin				6		pF
PLL							
f_{PD}	Phase Detector Frequency					104	MHz
I_{CPout}	Charge Pump Output Current Magnitude	CPG = 1X			100		µA
		CPG = 2X			200		
		CPG = 3X			300		
		...			...		
		CPG=32X			3200		
$I_{CPout}TRI$	CP TRI-STATE Current	0.4 V < V_{CPout} < Vcc - 0.4			1	5	nA
$I_{CPout}MM$	Charge Pump Sink vs. Source Mismatch	V_{CPout} = Vcc / 2 T_A = 25°C			3	10	%
$I_{CPout}V$	Charge Pump Current vs. CP Voltage Variation	0.4 V < V_{CPout} < Vcc - 0.4 T_A = 25°C			4		%
$I_{CPout}T$	CP Current vs. Temperature Variation	V_{CPout} = Vcc / 2			8		%
LN(f) (Note 7)	Normalized PLL 1/f Noise $LN_{PLL_flicker}$(10 kHz)	CPG = 1X			-116		dBc/Hz
		CPG = 32X			-124.5		
	Normalized PLL Noise Floor $LN_{PLL_flat(1\ Hz)}$	CPG = 1X			-220.8		dBc/Hz
		CPG = 32X			-225.4		
$f_{ExtVCOin}$	PLL Input Frequency	RFout Buffer Enabled and VCO_DIV > 1		400		4000	MHz
		RFout Buffer Disabled and VCO_DIV = 1		400		6000	
$p_{ExtVCOin}$	PLL Input Sensitivity	$f_{ExtVCOin}$ ≤ 4 GHz		-15		3	dBm
		$f_{ExtVCOin}$ > 4 GHz		-5		3	

Symbol	Parameter	Conditions		Min	Typ	Max	Units
VCO Specifications							
f_{VCO}	Internal VCO Frequency Range	Mode = Full Chip Mode This is the frequency before the VCO divider.	2060E	1990		2240	MHz
			2380E	2200		2530	
			2690E	2490		2865	
			3030E	2810		3230	
			3320E	3130		3600	
			3740E	3480		4000	
ΔT_{CL}	Maximum Allowable Temperature Drift for Continuous Lock	(Note 6),(Note 8)		125			°C
p_{RFout}	RF Output Power	Maximum Frequency Default Power Mode VCO_DIV=1	2060E		3.5		dBm
			2380E		2.8		
			2690E		1.6		
			3030E		1.2		
			3320E		0.2		
			3740E		- 0.3		
ΔP_{RFout}	Change in Output Power (Note 6)	Fixed Temperature with 100 MHz frequency change at the output			1		dB
		Fixed frequency with a change over the entire temperature range			0.5		
K_{Vtune}	Fine Tuning Sensitivity	The lower number in the range applies when the VCO is at its lowest frequency and the higher number applies when the VCO is at its highest frequency. A linear approximation can be used for frequencies between these two cases.	2060E		13 - 23		MHz/V
			2380E		16 - 30		
			2690E		17 - 32		
			3030E		20 - 37		
			3320E		21 - 37		
			3740E		27 - 42		
HS_{RFout}	Second Harmonic	Default Power Mode (Note 5) 50 Ω Load; VCO_DIV=1	2060E		-20	-15	dBc
			2380E				
			2690E				
			3030E				
			3320E				
			3740E				
		Default Power Mode (Note 5) 50 Ω Load; VCO_DIV=3	2060E		-20	-15	
			2380E				
			2690E				
			3030E				
			3320E				
			3740E				
PSH_{VCO}	VCO Frequency Pushing	$C_{VregVCO}$ = 4.7 µF,Open Loop			600		kHz/V
$PULL_{VCO}$	VCO Frequency Pulling	VSWR 1.7 to 1 (6 dB Pad)	VCO_DIV = 1		±800		kHz
			VCO_DIV > 1		±60		
σ_{Φ}	RMS Phase Error	Integration Bandwidth = 100 Hz to 20 MHz Middle VCO Frequency 100 MHz Wenzel Crystal Reference Integer Mode Optimized Loop Bandwidth	2060E		1.6		mRad
			2380E		1.8		
			2690E		2.1		
			3030E		2.1		
			3320E		2.3		
			3740E		2.6		

Symbol	Parameter	Conditions		Min	Typ	Max	Units
VCO Phase Noise (Note 9)							
$L(f)_{Fout}$	Phase Noise 2060E	f_{RFout} = Min VCO Frequency	10 kHz Offset		-89.7		dBc/Hz
			100 kHz Offset		-113.7		
			1 MHz Offset		-134.9		
			10 MHz Offset		-155.4		
			20 MHz Offset		-160.3		
		f_{RFout} = Max VCO Frequency	10 kHz Offset		-86.5		
			100 kHz Offset		-111.4		
			1 MHz Offset		-132.8		
			10 MHz Offset		-153.4		
			20 MHz Offset		-158.5		
$L(f)_{Fout}$	Phase Noise 2380E	f_{RFout} = Min VCO Frequency	10 kHz Offset		-87.9		dBc/Hz
			100 kHz Offset		-112.7		
			1 MHz Offset		-133.8		
			10 MHz Offset		-154.2		
			20 MHz Offset		-159.5		
		f_{RFout} = Max VCO Frequency	10 kHz Offset		--83.4		
			100 kHz Offset		-109.1		
			1 MHz Offset		-130.8		
			10 MHz Offset		-151.8		
			20 MHz Offset		-157.5		
$L(f)_{Fout}$	Phase Noise 2690E	f_{RFout} = Min VCO Frequency	10 kHz Offset		-86.9		dBc/Hz
			100 kHz Offset		-111.8		
			1 MHz Offset		-133.3		
			10 MHz Offset		-154.2		
			20 MHz Offset		-159.4		
		f_{RFout} = Max VCO Frequency	10 kHz Offset		-82.3		
			100 kHz Offset		-108.4		
			1 MHz Offset		-130.3		
			10 MHz Offset		-151.1		
			20 MHz Offset		-156.7		
$L(f)_{Fout}$	Phase Noise 3030E	f_{RFout} = Min VCO Frequency	10 kHz Offset		-86.1		dBc/Hz
			100 kHz Offset		-110.5		
			1 MHz Offset		-132.0		
			10 MHz Offset		-152.2		
			20 MHz Offset		-157.1		
		f_{RFout} = Max VCO Frequency	10 kHz Offset		-82.2		
			100 kHz Offset		-107.7		
			1 MHz Offset		-129.4		
			10 MHz Offset		-150.5		
			20 MHz Offset		-156.1		

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$L(f)_{Fout}$	Phase Noise 3320E	f_{RFout} = Min VCO Frequency	10 kHz Offset		-84.1		dBc/Hz
			100 kHz Offset		-109.1		
			1 MHz Offset		-130.7		
			10 MHz Offset		-151.6		
			20 MHz Offset		-156.9		
		f_{RFout} = Max VCO Frequency	10 kHz Offset		-82.0		
			100 kHz Offset		-107.0		
			1 MHz Offset		-128.5		
			10 MHz Offset		-149.6		
			20 MHz Offset		-155.2		
$L(f)_{Fout}$	Phase Noise 3740E	f_{RFout} = Min VCO Frequency	10 kHz Offset		-83.9		dBc/Hz
			100 kHz Offset		-108.3		
			1 MHz Offset		-129.9		
			10 MHz offset		-150.6		
			20 MHz Offset		-156.5		
		f_{RFout} = Max VCO Frequency	10 kHz Offset		-81.6		
			100 kHz Offset		-106.5		
			1 MHz Offset		-127.7		
			10 MHz Offset		-148.6		
			20 MHz Offset		-154.2		

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Digital Interface (DATA, CLK, LE, CE, Ftest/LD, FLout,RFoutEN)							
V_{IH}	High-Level Input Voltage			1.6		Vcc	V
V_{IL}	Low-Level Input Voltage					0.4	V
I_{IH}	High-Level Input Current	V_{IH} = 1.75, XO = 0		-3.0		3.0	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0 V , XO = 0		-3.0		3.0	µA
V_{OH}	High-Level Output Voltage	I_{OH} = 500 µA		2.0			V
V_{OL}	Low-Level Output Voltage	I_{OL} = -500 µA			0.0	0.4	V
I_{Leak}	Leakage Current	Ftest/LD and FLout Pins Only	Attached to Vcc	-10		10	nA
			Attached to GND	-10		10	nA
MICROWIRE Timing							
t_{CE}	Clock to Enable Low Time	See Data Input Timing		25			ns
t_{CS}	Data to Clock Set Up Time	See Data Input Timing		25			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing		20			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing		25			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing		25			ns
t_{CES}	Enable to Clock Set Up Time	See Data Input Timing		25			ns
t_{EWH}	Enable Pulse Width High	See Data Input Timing		25			ns

Note 5: The LMX2541 RFout power level is programmable with the program words of VCOGAIN, OUTTERM, and DIVGAIN. Changing these words can change the output power of the VCO as well as the current consumption of the output buffer. For the purpose of consistency in electrical specifications, "Default Power Mode" is defined to be the settings of VCOGAIN = OUTTERM = DIVGAIN = 12.

Note 6: Not tested in production. Guaranteed by characterization.

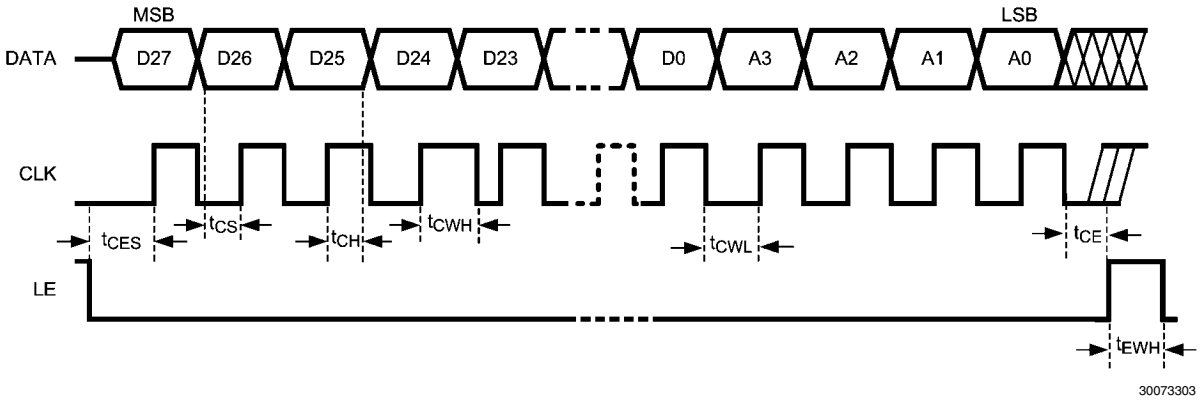
Note 7: Consult the applications section for more details on these parameters.

Note 8: Maximum Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction from the value it was at the time that the R0 register was last programmed, and still have the device stay in lock. The action of programming the R0 register, even to the same value, activates a frequency calibration routine. This implies that the device will work over the entire frequency range, but if the temperature drifts more than the maximum allowable drift for continuous lock, then it will be necessary to reload the R0 register to ensure that it stays in lock. Regardless of what temperature the device was initially programmed at, the temperature can never drift outside the frequency range of -40°C $\leq T_A \leq$ 85°C without violating specifications.

Note 9: The VCO phase noise is measured assuming that the loop bandwidth is sufficiently narrow that the VCO noise dominates. The phase noise is measured with AC_TEMP_COMP = 5 and the device is reloaded at each test frequency. The typical performance characteristics section shows how the VCO phase noise varies over temperature and frequency.

Note 10: See Typical Performance Characteristics for more information.

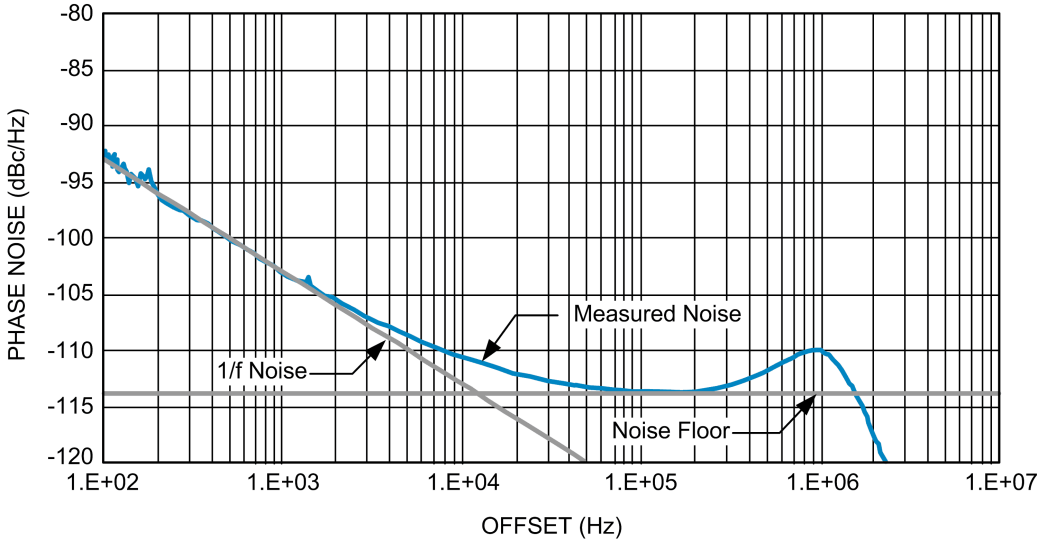
Serial Data Timing Diagram



The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the LE signal, the data is sent from the shift registers to an actual counter. A slew rate of at least 30 V/µs is recommended for these signals. After the programming is complete, the CLK, DATA, and LE signals should be returned to a low state. If the CLK and DATA lines are toggled while the in VCO is in lock , as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during the time of this programming.

Typical Performance Characteristics (Not Guaranteed)

PLL Phase Noise



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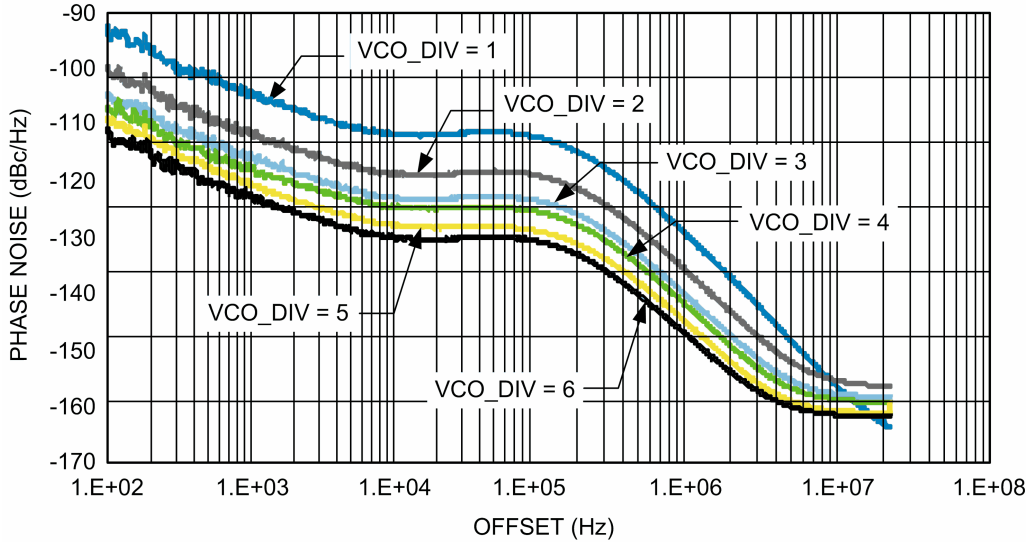
The above plot demonstrates the PLL phase noise of the LMX2541SQ3700E operating at 3700 MHz output frequency, phase detector frequency of 100 MHz, and charge pump gain of 32X. The loop bandwidth was made as wide as possible to fully expose the PLL phase noise and reference source was a 100 MHz Wenzel crystal. This measurement was done in integer mode. To better understand the impact of using fractional mode, consult the applications section.

The measured noise is the sum of the PLL 1/f noise and noise floor. At offsets below 1 kHz, the PLL 1/f noise is dominates and changes as 10 dB/decade. The noise at 1 kHz is dominated by this 1/f noise and has a value of -103 dBc/Hz. In the 100 - 200 kHz offset range, the noise is -113.7 dBc/Hz and is dominated by the PLL noise floor. It can be shown that if the effects of the loop filter peaking and the 1/f noise are subtracted away from this measurement, it would be about 0.6 dB better.

If the phase detector frequency is changed with the VCO frequency held constant, the PLL noise floor will change, but the 1/f noise will remain the same. If the VCO frequency is changed, both the 1/f noise and PLL noise floor change as 20 dB/decade.

Divider Noise Floor vs. Divider Value Value
(f_{VCO} = 3700 MHz, Various values for VCO_DIV)



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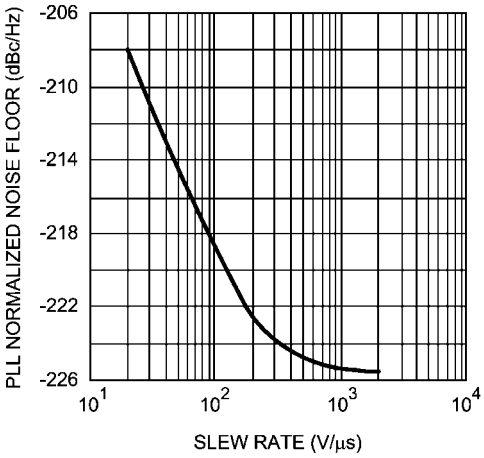
When the divider is engaged (VCO_DIV >0), then the entire system phase noise is reduced by a factor of 20 × log(VCO_DIV). However, the noise floor of the divider will also add to this noise as is visible at far offsets. Note that the noise floor for Bypass mode is lower because the VCO divider is not engaged.

PLL Normalized Noise Floor vs. Slew Rate (K_{PD} = 32X)



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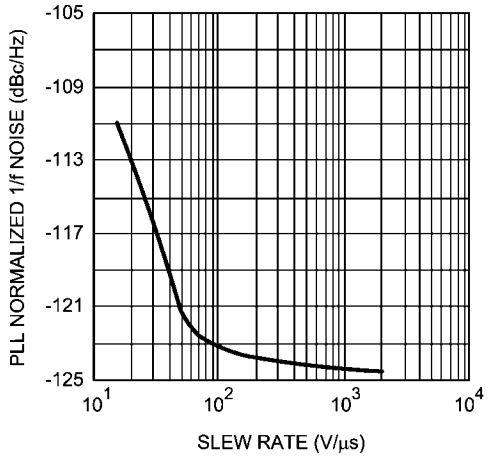
PLL Normalized 1/f Noise vs. Slew Rate (K_{PD} = 32X)



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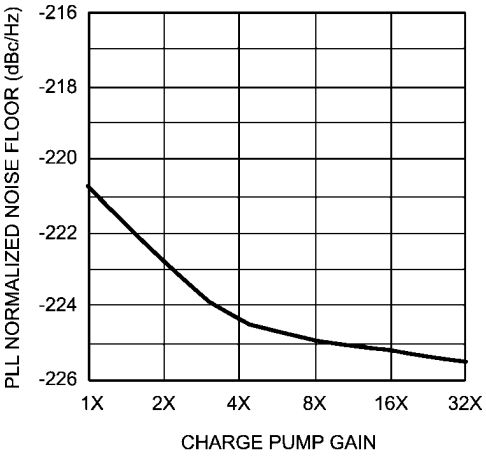
PLL Normalized Noise Floor vs. Charge Pump Gain (Slew Rate = 2000 V/µs)



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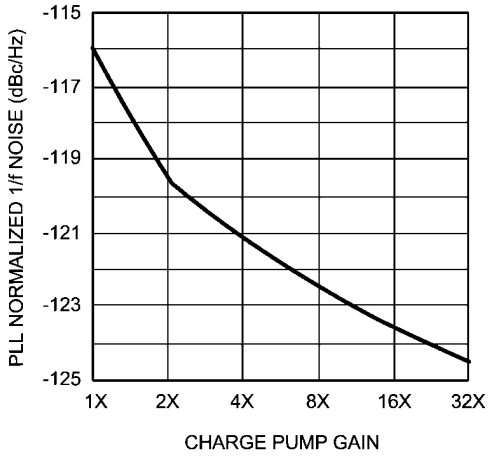
PLL Normalized 1/f Noise vs. Charge Pump Gain (Slew Rate = 2000 V/µs)



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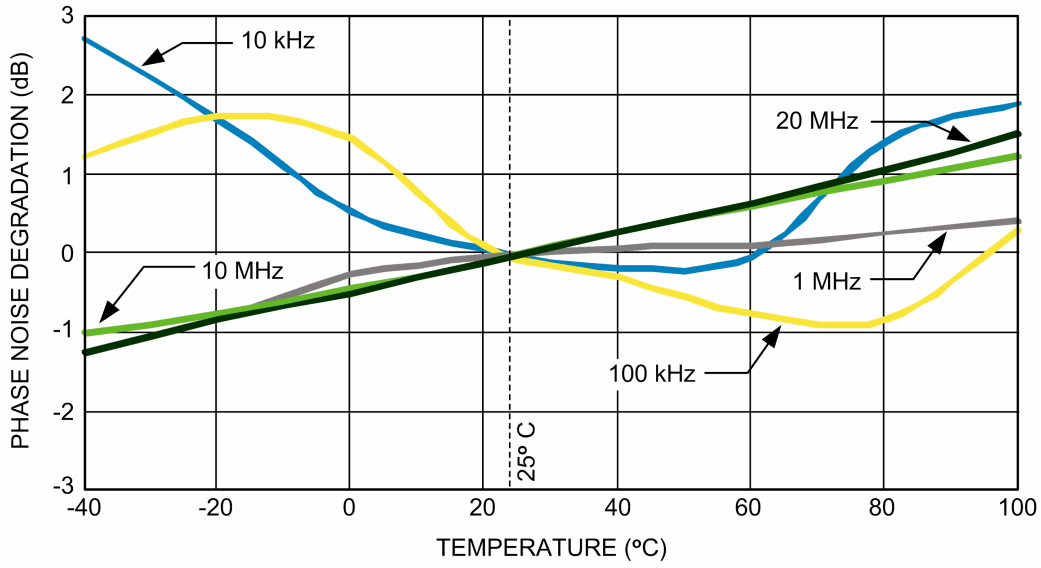
VCO Phase Noise Degradation vs. Temperature and Offset (VCO Relocked at Each Temperature Vcc = 3.3 V, AC_TEMP_COMP = 5)



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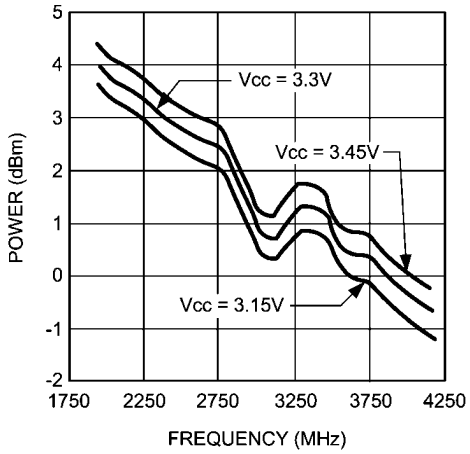
The above plot shows how much the VCO phase noise typically change over temperature relative to room temperature. The typical values for represent an average over all frequencies and part options and therefore there are some small variations over part options and frequencies that are not shown .VCO phase noise numbers room temperature are reported in the electrical specifications. A negative value indicates a phase noise improvement.

Relative VCO Phase Noise Over Temperature Drift (AC_TEMP_COMP = 25, Vcc = 3.3 V)

Temperature		Phase Noise Change in Celsius for Various Offsets				
Lock	**Current**	**10 kHz**	**100 kHz**	**1 MHz**	**10 MHz**	**20 MHz**
-40	-40	+0.4	-2.0	-1.6	-1.8	-1.6
-40	25	+0.3	+0.5	+0.5	+0.5	+0.4
-40	85	+0.9	+2.0	+2.4	+2.5	+2.3
25	-40	+0.2	-2.2	-1.7	-2.0	-1.8
25	25	This is the default condition to which these other numbers are normalized to.				
25	85	+0.6	+1.5	+2.0	+2.0	+1.9
85	-40	+0.2	-2.2	-1.7	-1.9	-1.8
85	25	+0.2	+0.2	+0.3	+0.2	+0.2
85	85	+0.6	+1.8	+2.2	+2.3	+2.1

The above table shows the typical degradation for VCO phase noise when the VCO is locked at one temperature and the temperature is allowed to drift to another temperature. A negative value indicates a phase noise improvement.

Output Power vs Voltage (VCO_DIV = 1, VCOGAIN = 12, OUTTERM = 12, T_A = 25°C)



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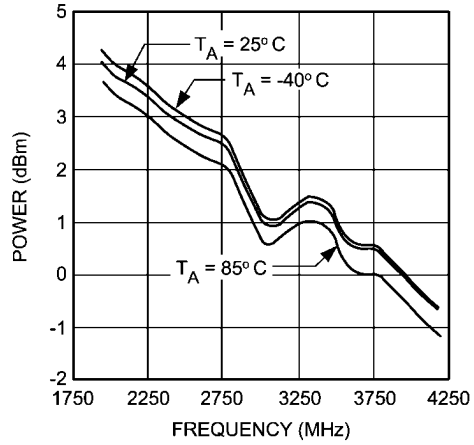
Output Power vs. Temperature (VCO_DIV = 1, VCOGAIN = 12, OUTTERM = 12, Vcc = 3.3 V)



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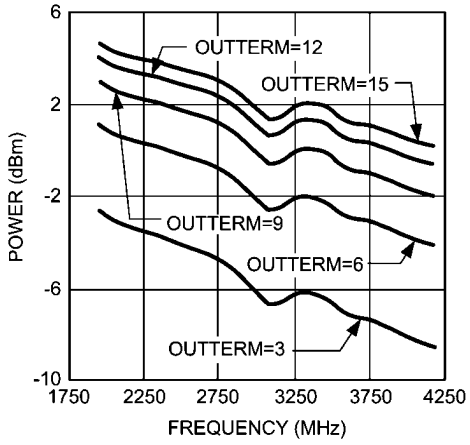
Output Power vs. OUTTERM and FREQUENCY (VCO_DIV = 1, TA = 25 °C, Vcc = 3.3 V, VCOGAIN = 12)



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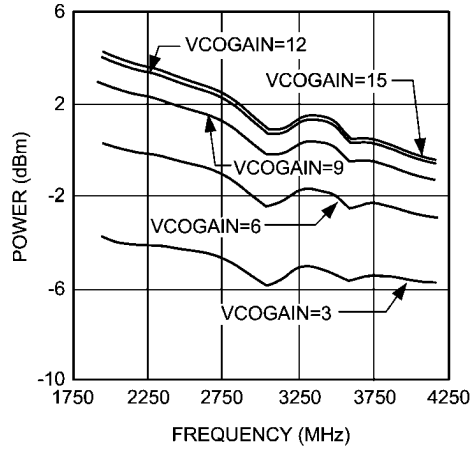
Output Power vs. VCOGAIN and FREQUENCY (VCO_DIV = 1, T_A = 25 °C, Vcc = 3.3 V, OUTTERM = 12)



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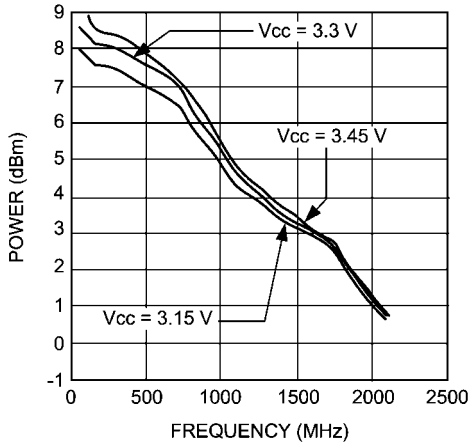
The above plots show the trends in output power as a function of temperature, voltage, and frequency. For states where VCOGAIN and OUTTERM are not 12, the table below shows how the output power is modified based on these programmable settings.

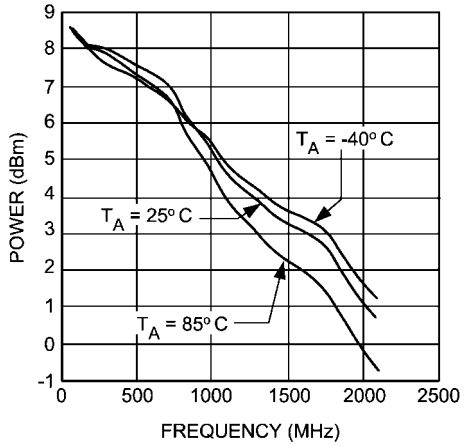
Change in Output Power in Bypass Mode as a Function of VCOGAIN and OUTTERM

		VCOGAIN				
		3	**6**	**9**	**12**	**15**
OUTTERM	**3**	-9.7	-8.4	-7.9	-7.8	-7.9
	6	-6.6	-4.5	-3.6	-3.4	-3.6
	9	-5.7	-3.1	-1.7	-1.3	-1.3
	12	-5.4	-2.5	-0.8	0.0	0.1
	15	-5.3	-2.2	-0.3	0.8	1.1

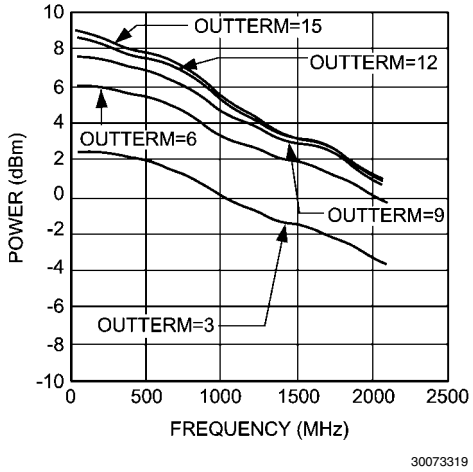
Output Power vs Voltage
(VCO_DIV > 1, VCOGAIN = 12, OUTTERM = 12, T_A = 25°C)



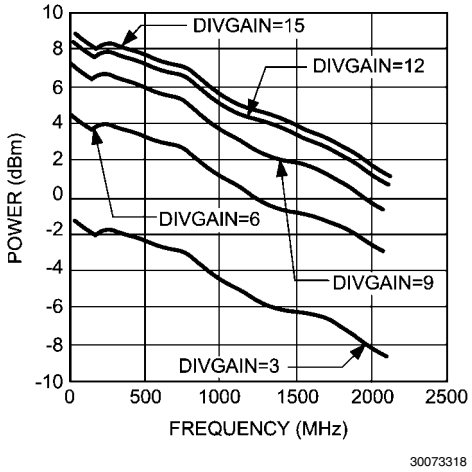
Output Power vs. Temperature
(VCO_DIV > 1, DIVGAIN = OUTTERM = 12, Vcc = 3.3 V)



Output Power vs. OUTTERM and FREQUENCY
(VCO_DIV = 1, TA = 25 °C, Vcc = 3.3 V, VCOGAIN = 12)



Output Power vs. DIVGAIN and FREQUENCY
(VCO_DIV > 1, T_A = 25 °C, Vcc = 3.3 V, OUTTERM = 12)



The table below shows the RELATIVE output power to the case of VCOGAIN = OUTTERM = 12.

Change in Output Power in Divided Mode as a Function of DIVGAIN and OUTTERM

		DIVGAIN				
		3	**6**	**9**	**12**	**15**
OUTTERM	**3**	-10.2	-9.8	-9.8	-9.9	-9.9
	6	-6.1	-4.4	-4.3	-4.3	-4.4
	9	-5.7	-2.4	-1.5	-1.4	-1.4
	12	-5.5	-2.1	-0.7	0.0	0.3
	15	-5.5	-2.0	-0.5	0.2	0.7

1.0 Functional Description

The LMX2541 is a low power, high performance frequency synthesizer system which includes the PLL, VCO, and partially integrated loop filter. The following sections give a discussion of the various blocks of this device.

1.1 REFERENCE OSCILLATOR INPUT PINS

There are three basic ways that the OSCin/OSCin* pins may be configured as shown in the table below:

Mode	Description	XO Bit
Crystal	Device is used with a crystal oscillator	1
Single -Ended	Device is driven with a single-ended source, such as a TCXO.	0
Differential	Use this mode when driving with a differential signal, such as an LVDS signal.	0

In addition to the way that the OSCin/OSCin* pins are driven, there are also bits that effect the frequency that the chip uses. The OSC_FREQ word needs to be programmed correctly, or the VCO may have issues locking to the proper frequency, since the VCO frequency calibration is based on this word.

Word Name	Function
OSC_FREQ	This needs to be set correctly if the internal VCO is used for proper calibration.
OSC2X	This allows the oscillator frequency to be doubled. The R divider is bypassed in this case.

Higher slew rates tend to yield the best fractional spurs and phase noise, so a square wave signal is best for OSCin. Single ended mode and differential mode have similar results if a square wave is used to drive the OSCin pin. If using a sine wave, higher frequencies tend to work better due to their higher slew rates.

1.2 R DIVIDER

The R divider divides the OSCin frequency down to the phase detector frequency. If the doubler is enabled, then the R divider is bypassed.

1.3 PHASE DETECTOR AND CHARGE PUMP

The phase detector compares the outputs of the R and N dividers and generates a correction current corresponding to the phase error. This charge pump current is software programmable to 32 different levels.The phase detector frequency, f_{PD}, can be calculated as follows:

$$f_{PD} = f_{OSCin} / R$$

1.4 N DIVIDER AND FRACTIONAL CIRCUITRY

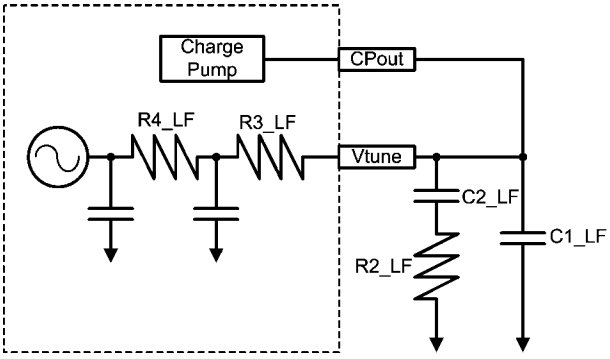
The N divider in the LMX2541 includes fractional compensation and can achieve any fractional denominator (PLL_DEN) from 1 to 4,194,303. The integer portion, PLL_N, is the whole part of the N divider value and the fractional portion, PLL_NUM / PLL_DEN, is the remaining fraction. PLL_N, PLL_NUM, and PLL_DEN are software programable. So in general, the total N divider value, N, is determined by:

$$N = PLL_N + PLL_NUM / PLL_DEN$$

The order of the delta sigma modulator is programmable from integer mode to fourth order. There are also several dithering modes that are also programmable. In order to make the fractional spurs consistent, the modulator is reset any time that the R0 register is programmed.

1.5 PARTIALLY INTEGRATED LOOP FILTER

The LMX2541 integrates the third pole (formed by R3_LF and C3_LF) and fourth pole (formed by R4_LF and C4_LF) of the loop filter. The values for these integrated components can be programmed independently through the MICROWIRE interface. The larger the values of these components, the stronger the attenuation of the internal loop filter. The maximum attenuation can be achieved by setting the internal resistors and capacitors to their maximum value and the minimum attenuation can be attained by setting all of these to their minimum setting. This partially integrated loop filter can only be used in full chip mode.



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1.6 LOW NOISE, FULLY INTEGRATED VCO

The LMX2541 includes a fully integrated VCO, including the inductors. The VCO (Voltage Controlled Oscillator) takes the voltage from the loop filter and converts this into a frequency. The VCO frequency is related to the other frequencies and divider values as follows:

$$f_{VCO} = f_{PD} \times N = f_{OSCin} \times N / R$$

In order to the reduce the VCO tuning gain and therefore improve the VCO phase noise performance, the VCO frequency range is divided into many different frequency bands. This creates the need for frequency calibration in order to determine the correct frequency band given a desired output frequency. The frequency calibration routine is activated any time that the R0 register is programmed. It is important that the OSC_FREQ word is set correctly to have this work correctly. The time that the frequency calibration takes is dependent on f_{OSCin} and the size of the frequency change. As a general rule of thumb, this time improves for higher OSCin frequencies and is on the order of 200 us for an OSCin freqency of 100 MHz and a small frequency change. For frequency changes on the order of the entire VCO tuning range, this time is closer to 300 us.

The VCO also has an internal amplitude calibration algorithm to optimize the phase noise which is also activated any time the R0 register is programmed. The optimum internal settings for this are temperature dependent. If the temperature is allowed to drift too much without being re-calibrated, some minor phase noise degradation could result. For applications where this is an issue, the AC_TEMP_COMP word can be used to sacrifice phase noise at room temperature in order to improve the VCO phase noise over all temperatures. The maximum allowable drift for continuous lock, ΔT_{CL}, is stated

in the electrical specifications. For this part, a number of +125 C means the part will never lose lock if the part is operated under recommended operating conditions.

1.7 PROGRAMMABLE VCO DIVIDER

The VCO divider can programmed to any value from 2 to 63 as well as bypass mode if device is in full chip mode. In external VCO mode or divider mode, all values except bypass mode can be used for the VCO divider. The VCO divider is not in the feedback path between the VCO and the PLL and therefore has no impact on the PLL loop dynamics. After this programmable divider is changed, it may be beneficial to reprogram the R0 register to recallibrate the VCO . The frequency at the RFout pin is related to the VCO frequency and divider value, VCO_DIV, as follows:

$$f_{RFout} = f_{VCO} / VCO_DIV$$

When this divider is enabled, there will be some far-out phase noise contribution to the VCO noise. Also, it may be beneficial for VCO phase noise to reprogram the R0 register to recalibrate the VCO if the VCO_DIV value is changed from bypass to divided, or vise-versa.

The duty cycle for this divider is always 50%, even for odd divide values. Because of the architecture of this divider that allows it to work to high frequencies and always have a 50% duty cycle, there are a few extra considerations:

- In divider only mode, there must be 5 clock cycles on the CLK pin after the divide value is programmed in order to cause the divide value to properly changed. It is fine to use more than 5 clock cycles for this purpose.
- For a divde of 4 or 5 ONLY, the R4 register needs to be programmed one more time after the R0 register is loaded in order to synchronize the divider. Failure to do so will cause the wrong divide values. Furthermore, if the VCO signal ever goes away, as is the case when the part is powered down, it is necessary to reprogram the R4 register again to re-synchronize the divider.

1.8 PROGRAMMABLE RF OUTPUT BUFFER

The output power at the RFout pin can be programmed to various levels as well as on and off states. The output state of this pin is controlled by the RFoutEN pin as well as the RFOUT word. The RF output buffer can be disabled while still keeping the PLL in lock. In addition to this, the actual output power level of this pin can be adjusted using the VCOGAIN, DIVGAIN, and OUTTERM programming words.

1.9 POWERDOWN MODES

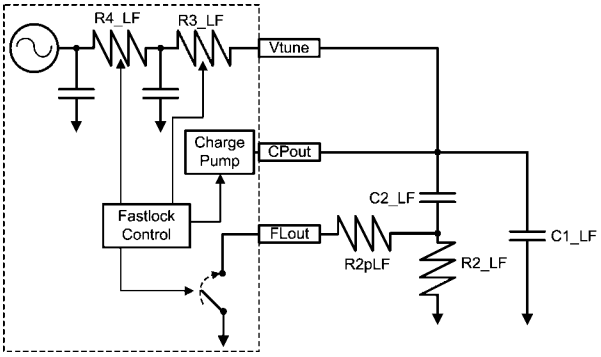
The LMX2541 can be powered up and down using the CE pin or the POWERDOWN bit. When the device is powered down, the programming and VCO calibration information is retained, so it is not necessary to re-program the device when the device comes out of the powered down state (The one exception is when the VCO_DIV value is 4 or 5, which has already been discussed.). The following table shows how to use the bit and pin.

CE Pin	POWERDOWN Bit	Device State
Low	Don't Care	Powered Down
High	0	Powered Up
	1	Powered Down

The device can be programmed in the powerdown state. However, the VCO frequency needs to be changed when the device is powered up because the VCO calibration does not run in the powerdown state. Also, the special programming for VCO_DIV = 4 or 5 has to be done when the part is powered up. In order for the CE pin to properly power the device down when it is held low, the all the registers in the device need to have been programmed at least one time.

1.10 FASTLOCK

The LMX2541 includes the Fastlock™ feature that can be used to improve the lock times. When the frequency is changed, a timeout counter is used to engage the fastlock for a programmable amount of time. During the time that the device is in Fastlock, the FLout pin changes from high impedance to low, thus switching in the external resistor R2-pLF with R2_LF as well as changing the internal loop filter values for R3_LF and R4_LF.



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The following table showshow the charge pump gain, loop filter resistors, and FLout pin change between normal operation and Fastlock.

Parameter	Normal Operation	Fastlock
Charge Pump Gain	CPG	FL_CPG
Loop Filter Resistor R3_LF	R3_LF	FL_R3_LF
Loop Filter Resistor R4_LF	R4_LF	FL_R4_LF
FLout Pin	High Impedance	Low

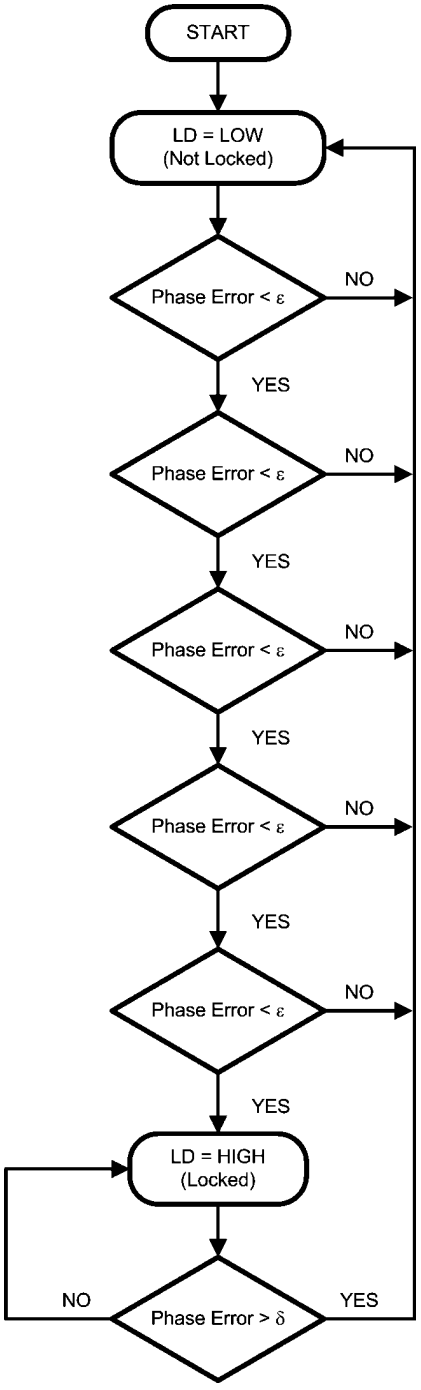
Once the loop filter values and charge pump gain are known for normal mode operation, they can be determined for fastlock operation as well. In normal operation, one can not use the highest charge pump gain and still use fastlock because there will be no larger current to switch in. If the resistors and the charge pump current are done simultaneously, then the phase margin can be preserved while increasing the loop bandwidth by a factor of K as shown in the following table:

Parameter	Symbol	Calculation
Charge pump gain in Fastlock	FL_CPG	Typically choose to be the largest value.
Loop Bandwidth Multiplier	K	K = sqrt (FL_CPG/CPG)
Internal Loop Filter Resistor	FL_R3_LF	FL_R3_LF = R3_LF / K
Internal Loop Filter Resistor	FL_R4_LF	FL_R4_LF = R4_LF / K
External Loop Filter Resistor	R2pLF	R2pLF = R2_LF / (K - 1)

1.11 LOCK DETECT

The Ftest/LD pin of the LMX2541 can be configured to support both analog and digital lock detect. The analog lock detect is generally more of a legacy feature and requires an external RC. When configured for push-pull analog lock detect, the Ftest/LD is high with narrow pulses which corresponds to when the charge pump is on. This waveform can be integrated with an RC filter to generate a lock detect signal. The open drain lock detect is similar pin puts out short low pulses when the charge pump comes on. An external RC filter can be used to integrate this information. Open drain analog lock detect is typically implemented with an RC filter followed by a pull-up resistor. The pull-up resistor can be much larger than the resistor in the RC filter in order to make unbalanced time constants for improved sensitivity.

The digital lock detect function can be selected for the Ftest/LD pin. The digital lock detect circuitry compares the difference between the phase of the inputs to the phase detector with a RC generated delay of ε. To indicate a locked state (Lock = HIGH) the phase error must be less than ε for 5 consecutive phase detector cycles. Once in lock (Lock = HIGH), the RC delay is changed to δ. To indicate an out of lock state (Lock = LOW), the phase error must become greater than δ. The values of ε and δ are programmable with the DLOCK word.



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2.0 General Programming Information

The LMX2541 is programmed using several 32-bit registers used to control the LMX2541 operation. A 32-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a data field and an address field. The last 4 register bits, CTRL[3:0] form the address field, which is used to decode the internal register address. The remaining 28 bits form the data field DATA[27:0]. While LE is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When LE goes high, data is transferred from the data field into the selected register bank. For initial device programming the register programming sequence must be done in the order as shown in the register map. The action of programming register R7 resets all the registers to default values, including hidden registers. The programming of register R1 and R0 is also special for the device when operating in full chip mode because the action of programming either one of these registers activates the VCO calibration. For changes after this initial setup, see the Applications Information section.

2.01 Register Map

The following table lists the registers as well as the order that they should be programmed. Register 7 is programmed first and the action of programming register R7 resets all the registers after the LE pin is pulled to a low state. Register R0 is programmed last because it activates the VCO calibration. The one exception to this is when the VCO_DIV value is 4 or 5. Consult the programming section on VCO_DIV for more details.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[27:0]																												C3	C2	C1	C0
R7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1
R13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	VCO_DIV_OPT[2:0]			1	1	0	1
R8	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	1	1	0	0	1	1	1	AC_TEMP_COMP[4:0]					1	0	0	0
R6	0	0	0	0	0	0	0	0	0	0	0	1	1	1	VCOGAIN[3:0]				OUTTERM[3:0]				DIVGAIN[3:0]				RFOUT [1:0]		0	1	1	0
R5	1	0	1	FL_CPG[4:0]				FL_R4_LF [2:0]			FL_R3_LF[2:0]			FL_TOC[13:0]															0	1	0	1
R4	C4_LF[3:0]				C3_LF[3:0]				R4_LF[2:0]			R3_LF[2:0]			VCO_DIV[5:0]						OSC_FREQ[7:0]								0	1	0	0
R3	FSK	0	0	DLOCK[2:0]			CPT	DITH [1:0]		ORDER[2:0]			FDM	OSC _2X	CPP	MUX[3:0]				CPG[4:0]					XO	PWDN	MODE [1:0]		0	0	1	1
R2	0	0	0	0	0	1	DEN[21:0]																						0	0	1	0
R1	0	0	0	0	PLL_NUM[21:16]						PLL_N[17:12]						PLL_R[11:0]												0	0	0	1
R0	PLL_NUM[15:0]																PLL_N[11:0]												0	0	0	0

2.1 REGISTER R7

Although Register 7 has no elective bits to program, it is very important to program this register because the action of doing so with the bit sequence shown in the register map resets all the registers, including hidden registers with test bits that are not disclosed. Register 7 should always be programmed first, because it will clear out all other programming information. The register reset occurs only after the LE signal has transitioned from low to high and back to low again.

2.1.1 REGISTER R13

This register needs to be programmed only in the event that the RFout pin is being used and VCO_DIV = 1.

VCO_DIV_OPT[2:0]

This word optimizes the RFout power level based on the VCO divider in the case that VCO_DIV = 1. In this case, this word should be programmed to 15. Otherwise, this word does not need to be programmed.

Condition	VCO_DIV_OPT
VCO_DIV = 1, RFout pin not disabled	7
All other conditions	0, but does not need to be programmed.

2.1.2 REGISTER R8

AC_TEMP_COMP[4:0]

This word optimizes the VCO phase noise for possible temperature drift. When the VCO frequency is changed, the internal tuning algorithm optimizes the phase noise for the current temperature. In fixed frequency applications, temperature drift may lead to sub-optimal phase noise over time. In dynamic frequency applictions, the re-tuning of the VCO frequency overcomes this problem because the phase noise is re-optimized each time the VCO frequency is changed. The AC_TEMP_COMP word can be used to optimize the VCO phase noise for temerature drift for these different scenarios. The following table indicates which values of this word should be used for each scenario.

AC_TEMP_COMP	Application Type
5	Dynamic Frequency
24	Fixed Frequency
All Other States	Invalid

2.2 REGISTER R6

Register R6 has words that impact the output power of the RFout pin.

RFOUT[1:0] - RFout enable pin

This word works in combination with the EN_RFout Pin to control the state of the RFout pin.

RFOUT	EN_RFout Pin	RFout Pin State
0	Don't Care	Disabled
2	Don't Care	Enabled
1 or 3	Low	Disabled
	High	Enabled

DIVGAIN[3:0], VCOGAIN[3:0], and OUTTERM[3:0] - Power Controls for RFout

These three words may be programmed in a value from 0 to 15 and work in conjunction to control the output power level of the RFout pin. Increasing any of these values increases the output power at the expense of higher current consumption of the buffer. Although there may be more than one way to get the same output power, some combinations may have lower current. The typical performance characteristics show these trade-offs. The default setting for all these bits is 12. The value of VCO_DIV determines which two of these three words have an impact.

VCO_DIV	Bits that Impact Power
1 (Bypass)	OUTTERM, VCOGAIN
>1 (Not Bypass)	OUTTERM, DIVGAIN

2.3 REGISTER R5

This register controls the fastlock mode which enables a wider loop bandwidth when the device is changing frequencies.

FL_TOC[13:0] -- Time Out Counter for FastLock

When the value of this word is 3 or less, FastLock time out counter is disabled, and the FLout pin can be used for general purpose I/O. When this value is 4 or greater, the time out counter is engaged for the amount of phase detector cycles shown in the table below.

TOC Value	FLout Pin State	Fastlock Engagement Time
0	High Impedance	Disabled
1	Low	Always Engaged
2	Low	Disabled
3	High	Disabled
4	Low	Engaged for 4 × 2 Phase DetectorCycles
.	.	.
16383	Low	Engaged for 16383 × 2 Phase Detector Cycles

When this count is active, the FLout Pin is grounded, the FastLock current is engaged, and the resistors R3 and R4 are also potentially changed. The table below summarizes the bits that control various values in and out of FastLock.

FastLock State	FLout	Charge Pump Current	R3_LF Value	R4_LF Value
Not Engaged	High Impedance	CPG	R3_LF	R4_LF
Engaged	Grounded	FL_CPG	FL_R3_LF	FL_R4_LF

FL_R3_LF[2:0] -- Value for Internal Loop Filter Resistor R3 During Fastlock

FL_R3_LF Value	R3 Resistor During Fastlock (kΩ)
0	Low (200 Ω)
1	1
2	2
3	4
4	16
5-7	Reserved

FL_R4_LF[2:0] -- Value for Internal Loop Filter Resistor R4 During Fastlock

FL_R4_LF Value	R3 Resistor During Fastlock (kΩ)
0	Low (200 Ω)
1	1
2	2
3	4
4	16
5-7	Reserved

FL_CPG[4:0] -- Charge Pump Current for Fastlock

When FastLock is enabled, this is the charge pump current that is used for faster lock time.

FL_CPG	Fastlock Charge Pump State	Typical Fastlock Charge Pump Current at 3.3 Volts (µA)
0	1X	100
1	2X	200
2	3X	300
3	4X	400
...	...	...
31	32X	3200

2.4 REGISTER R4

This register controls miscellaneous functions of the device. The action of programming the R4 register also synchronizes the VCO divider, which is necessary when VCO_DIV = 4 or 5.

OSC_FREQ [7:0] -- OSCin Frequency for VCO Calibration Clocking

This word is used for the VCO frequency calibration. This word should be set to the OSCin frequency rounded to the nearest MHz.

OSC_FREQ	OSCin Frequency
0	Illegal State
1	1 MHz
2	2 MHz
...	...
255	255 MHz

VCO_DIV[5:0] - VCO Divider

The output of the VCO is divided by the value of VCO_DIV, which can range from 1 (Bypass Mode) to 63 and all values in between. There are a few special considerations. The VCO divider can only be set to bypass mode when the device is operating in full chip mode. Also, there is one extra programming step required to synchronize the VCO divider when it has a value of 4 or 5. This extra programming step is to load all registers as normal and then re-load register R4 with the same value. . When VCO_DIV=4 or 5, it is also necessary to re-synchronize the divider in Fulll chip mode whenever the R0 or R1 registers are reprogrammed, or in External VCO or Divider Only mode whenever the VCO signal goes away temporarily. This re-synchronization is ONLY for VCO_DIV values of 4 and 5.

When VCO_DIV is 4 or 5 ONLY, the R4 register needs to be programmed one additional time (after the R0 register is loaded) with the same value after the VCO signal (or ExtVCOin) signal is applied. If the VCO signal ever goes away, as is the case when the chip is powered down, or the VCO signal is taken away in External VCO or Divider Only mode, the R4 register needs to be re-loaded again to re-synchronize the divider.

VCO_DIV	VCO Output Divide	Comments
0	n/a	Illegal State
1	Bypass Mode	This state only available for MODE=Full Chip Mode
2	Divide by 2	
3	Divide by 3	
4	Divide by 4	Extra programming is required for divide by 4 and divide by 5 only. Refer to the functional description for more details.
5	Divide by 5	
6	Divide by 6	
...	...	
62	Divide by 62	
63	Divide by 63	

R3_LF[2:0] -- Value for Internal Loop Filter Resistor R3

This word controls the state of the internal loop filter resistor R3_LF when the device is in Full Chip Mode and Fastlock is not active.

R3_LF Value	R3 Resistor During Fastlock (kΩ)
0	Low (200 Ω)
1	1
2	2
3	4
4	16
5-7	Reserved

R4_LF[2:0] -- Value for Internal Loop Filter Resistor R4

This word controls the state of the internal loop filter resistor R4_LF when the device is in Full Chip Mode and Fastlock is not active.

R4_LF Value	R3 Resistor During Fastlock (kΩ)
0	Low (200 Ω)
1	1
2	2
3	4
4	16
5-7	Reserved

C3_LF[3:0] -- VALUE FOR C3 IN THE INTERNAL LOOP FILTER

This word controls the state of the internal loop filter resistor C3_LF when the device is Full Chip Mode.

C3_LF	C3 (pF)
0	0
1	1
2	5
3	6
4	10
5	11
6	15
7	16
8	20
9	21
10	25
11	26
12	30
13	31
14	35
15	26

C4_LF[3:0] -- VALUE FOR C4 IN THE INTERNAL LOOP FILTER

This word controls the state of the internal loop filter resistor C4_LF when the device is Full Chip Mode.

C4_LF	C4 (pF)
0	0
1	5
2	20
3	25
4	40
5	45
6	60
7	65
8	100
9	105
10	120
11	125
12	140
13	145
14	160
15	165

2.5 REGISTER R3

This register controls miscellaneous features of the device.

MODE[1:0] -- Operational Mode

The LMX2541 can be run in several operational modes as listed in the table below:

MODE	Name	Divider	PLL	VCO
0	Full	Enabled	Enabled	Enabled
1	External VCO	Enabled	Enabled	Disabled
2	Divider Only	Enabled	Disabled	Disabled
3	Test (Reserved)	Enabled	Enabled	Enabled

PWDN -- Powerdown Bit

Enabling this bit powers down the entire device, although register and VCO calibration information is retained.

XO - Crystal Oscillator Mode Select

When this bit is enabled, a crystal with appropriate load capacitors can be attached between the OSCin and OSCin* pins in order to form a crystal oscillator.

CPG[4:0] -- Charge Pump Current

This word programs the charge pump current gain. The current is programmable between 100 uA and 3.2 mA in 100 uA steps.

CPG	Charge Pump State	Typical Charge Pump Current (µA)
0	1X	100
1	2X	200
2	3X	300
3	4X	...
...	...	
31	32X	3200

MUX[3:0] -- Multiplexed Output for Ftest/LD Pin

The MUX[3:0] word is used to program the output of the Ftest/LD Pin. This pin can be used for a general purpose I/O pin, a lock detect pin, and for diagnostic purposes. When programmed to the digital lock detect state, the output of the Ftest/LD pin will be high when the device is in lock, and low otherwise. The output voltage level of the Ftest/LD is not equal to the supply voltage of the device, but rather is given by V_{OH} and V_{OL} in the electrical characteristics specification.

Because the Ftest/LD pin is close to the OSCin pin, the state of this pin can have an impact on the performance of the device. If any of the diagnostic modes (8-13) are used, the OSCin sensitivity can be severely degraded, so these should only be used for diagnoistic purposes. The fractional spurs can also be impacted a little by fractional spurs. The Push-Pull digital lock detect modes, like mode 3, tend to have the best fractional spurs, so these states are recommended, even if the digital lock detect function is not needed.

MUX	Output Type	Function	Comments
0	High Impedance	Disabled	**General Purpose I/O Modes**
1	Push-Pull	Logical High State	
2	Push-Pull	Logical Low State	
3	Push-Pull	Digital Lock Detect	**Lock Detect Modes** Consult Functional Description for more details State 3 is recommended for optimal spurious performance.
4	Push-Pull	Inverse Digital Lock Detect	
5	Open Drain	Digital Lock Detect	
6	Open Drain	Analog Lock Detect	
7	Push-Pull	Analog Lock Detect	
8	Push-Pull	N Divider	**Diagnostic Modes** These allow the user to view the outputs of the N divider, R divider, and phase frequency detector (PFD) and are intended only for diagnostic purposes. Typically, the output is narrow pulses, but when the output is divded by 2, there is a 50% duty cycle. The use of these modes (including R Divider) can degrade the OSCin sensitivity.
9	Push-Pull	N Divider / 2	
10	Push-Pull	R Divider	
11	Push-Pull	R Divider / 2	
12	Push-Pull	PFD Up	
13	Push-Pull	PFD Down	
14-15	N/A	Reserved	

CPP - Charge Pump Polarity

This bit sets the polarity of the phase detector.

CPP	Charge Pump Polarity	Typical Applications
0	Positive	External VCO Mode
1	Negative	Full Chip Mode External VCO Mode with an inverting active filter.

OSC2X-- OSCin Frequency Doubler

Enabling this bit doubles the OSCin frequency. This is useful in achieving a higher phase detector frequency to improve PLL phase noise, push out noise from the delta sigma modulator, and sometimes reduce fractional spurs . Note that when this bit is enabled, the R divider is bypassed.

OSC_2X	State
0	Normal
1	OSCin frequency is doubled

FDM - Extended Fractional Denomoinator Mode Enable

Enabling this bit allows the fractional numerator and denominator to be expanded from 10 bits to 22 bits. In 10-bit mode, only the first 10 bits of the fractional numerator and denominator are considered. Disabling this saves about 0.5 mA of current. When using FSK mode, this bit has to be disabled.

FDM	Fractional Mode
0	10-bit
1 (Default)	22-bit

ORDER[2:0] -- Delta Sigma Modulator Order

This word determines the order of the delta sigma modulator in the PLL. In general, higher order fractional modulators tend to reduce the primary fractional spurs that occur at increments of the channel spacing, but can also create spurs that are at a fraction of the channel spacing. The optimal choice of modulator order is very application specific, however, a third order modulator is a good starting point. The first order modulator has no analog compensation or dithering

ORDER	Delta Sigma Modulator	Mode	Comments
0	Disabled	Integer	Allows larger N Counter
1	First Order	Fractional	This has no analog compensation or dithering
2	Second Order		Traditional Delta Sigma Operation
3	Third Order		
4	Fourth Order		
5-7	Illegal States	n/a	n/a

DITH[1:0] -- Dithering

Dithering randomizes the delta sigma modulator output. This reduces sub-fractional spurs at the expense of adding phase noise. In general, it is recommended to keep the dithering strength at None or Weak for most applications. Dithering should never be used when the device is used in integer mode or a first order modulator. When using dithering with the other delta sigma modulator orders, it is beneficial to disable it in the case where the fractional numerator is zero, since it can actually create sub-fractional spurs.

DITH	Dithering Strength
0	Weak
1	Medium
2	Strong
3	Disabled

CPT - Charge Pump Tri-state

When this bit is enabled, the charge pump is tri-stated. The Tri-state mode could be useful for open loop modulation applications or as diagnostic tool for measuring the VCO noise, but is generally not used.

CPT	Charge Pump
0	Normal Operation
1	Tri-state

DLOCK[2:0] - Controls for Digital Lock detect

This word is controls operation of the digital lock detect function through selection of the window sizes (ε and δ). In order to indicate the PLL is locked, there must be 5 consecutive phase detector output cycles in which the time offset between the R and N counter outputs is less than ε. This will cause the Ftest/LD pin output to go high. Once lock is indicated, it will remain in this state until the time offset between the R and N counter outputs exceeds δ. If the OSCin signal goes away, the digital lock detect circuit will reliably indicate an unlocked condition. Consult the functional description for more details. A larger window size makes the lock detect circuit less sensitive. The window size is limited by the phase detector frequency, f_{PD}.

DLOCK	Maximum f_{PD}	Window Size (ns)	
		ε	δ
0 (Default)	All	3	3
1	TBD	5.5	5.5
2	TBD	8	8
3	TBD	10.5	10.5
4	TBD	13	13
5	TBD	15.5	15.5
6 -7	Reserved	Reserved	Reserved

FSK - Frequency Shift Keying

This bit enables a binary FSK modulation mode using the PLL N counter. Consult the applications section for more details.

FSK	FSK Mode
0	Disabled
1	Enabled

2.6 REGISTER R2

This word contains all the bits of the fractional denominator. These bits apply if the device is being used fractional mode.

PLL_DEN[21:0] -- Fractional Denominator

These bits determine the fractional denominator.

	PLL_DEN[21:0]																					
Fractional Denominator																						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2.7 REGISTERS R1 AND R0

Both registers R1 and R0 contain information for the PLL R counter, N counter, and fractional numerator. The action of programming either one of these registers, even to the same value, runs the VCO calibration when the device has the internal VCO operating. There are some programming words that are split across these two registers.

PLL_R[11:0] -- PLL R Divider Value

The R divider divides the OSCin signal. Note that if the doubler is enabled, the R divider is bypassed.

	PLL_R[11:0]											
0	Illegal State											
1	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	0	0	1	1
...	...	...	...	...	...	...	...	...	...	...	...	...
4095	1	1	1	1	1	1	1	1	1	1	1	1

PLL_N[17:0] PLL N Divider Value

When using integer mode, the PLL N divider value is split up into two different locations. In fractional mode, only the 12 LSB bits of the N counter are used. Based on the order of the modulator, the range is shown in the table below.

		PLL_N[17:12]						PLL_N[11:0]											
<12	Integer Mode	Divide Values below 12 are prohibited																	
12		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
13		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
...		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
262143		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12	Fractional Mode	Possible with first order modulator only																	
13-14		Possible with first or second order modulator																	
15-16		Possible with first, second, or third order modulators only																	
17		x	x	x	x	x	x	0	0	0	0	0	0	0	1	0	0	0	1
18		x	x	x	x	x	x	0	0	0	0	0	0	0	1	0	0	1	0
...		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
4090		x	x	x	x	x	x	1	1	1	1	1	1	1	1	1	0	1	0
4091 -4092		Possible with a first, second, or third order modulator only																	
4093		Possible with a first or second order modulator only																	
4094		Possible with a first order modulator only																	

PLL_NUM[21:0] -- Fractional Numerator

The fractional numerator is formed by the NUM word that is split between two registers and applies in fractional mode only.

	PLL_NUM[21:15]							PLL_NUM[14:0]														
Fractional Numerator																						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
...																						
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

3.0 Applications Information

3.1 TYPICAL CONNECTIONS

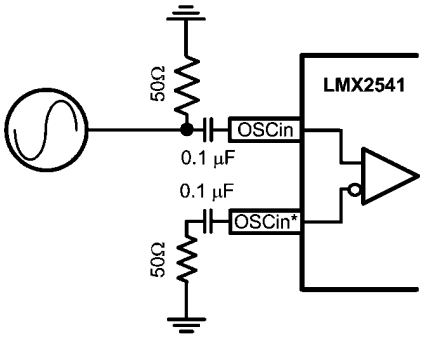
The components used at various pins can have an impact on the performance of this part, particularly fractional spurs. The following table contains guidelines for pin components and configurations for using the device in full chip mode with the fractional engine running.

Pin(s)	Connection Recommendations
RFout	Input should be AC coupled to this pin. If using external VCO mode, this pin can be left open.
RFoutEN	If not using this pin, leave it open and program the device accordingly.
L1 L2 Lmid	Do not connect these pins, but include the pads so the device will solder correctly.
VccOSC VccDIG VccFRAC VccPLL1	For the best fractional spurs, bypass to ground with a ferrite bead and shunt 0.1 uF capacitor.
VregRFout	Attach a series 10 Ω resistor and 1 uF capacitor to ground
VregVCO	Attach a shunt 4.7 uF capacitor to ground.
VregFrac	Attach a series 10 Ω and 1 uF capacitor to ground.
VrefVCO	Attach a shunt 0.1 uF capacitor to ground.
VccDiv VccRFout VccCP1 VccCP2	It is acceptable to short these directly to the power plane.
GND	Each pin should have a dedicated connection to the ground plane.
GND DAP	This should be grounded and not connected to other ground pins.

3.1.1 OSCin/OSCin* Connections

For single-ended operation, the signal is driven into the OSCin pin. The OSCin* pin is terminated the same as the OSCin pin. This is a typical case if the device is driven by a TCXO. For both single-ended and differential operation, the input is AC coupled because the OSCin/OSCin* pins self-bias to an optimal DC operating point. Better performance for both phase noise and fractional spurs is obtained for signals with a higher slew rate, such as a square wave. This is especially important for lower frequency signals, since slower frequency sine waves have lower slew rates. Fractional spurs are typically a several dB better when running in differential mode as opposed to single-ended mode.

Single-Ended Operation



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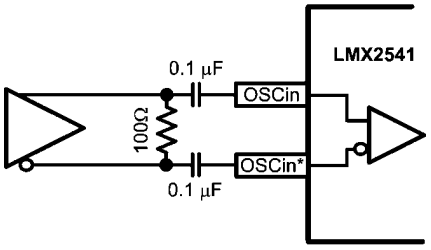
For differential operation, as is the case when using an LVDS or LVPECL driver, a 100 Ω resistor is placed across the OSCin/OSCin* traces

Differential Operation



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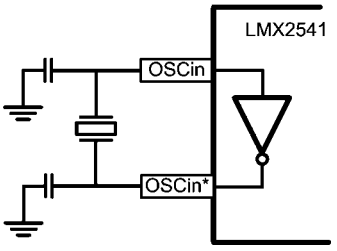
A third way to configure the device is in crystal mode (XO = 1). For this, the crystal is placed across the OSCin/OSCin* pins. Crystals are specified for a specific load capacitance, C_{Load}. .The load capacitors shown in the figure each have a value of $C_{Load}/2$.

Crystal Mode Operation



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3.2 CURRENT CONSUMPTION

The current consumption of the LMX2541 has many factors that influence it. Determining the current consumption for the entire device involves knowing which blocks are powered up and adding their currents together. For instance, the output buffer current can be impacted by the software controllable settings. Various blocks such as the VCO divider can be powered up and down in many different combinations. The typical current consumption for default setup conditions for each of the blocks is shown in the following table.

Block	Current (mA)
RF Output Buffer	40
VCO Divider	32
Internal PLL (Includes Counters, Charge Pump, and OSCin Buffer) (Excludes Fractional Engine)	78
PLL Fractional Engine	5

3.3 FRACTIONAL SPURS

Primary Fractional Spurs

The primary fractional spurs occur at multiples of the channel spacing and can change based on the fraction. For instance, if the phase detector frequency is 10 MHz, and the channel spacing is 100 kHz, then this could be achieved using a fraction of 1/100. The fractional spurs would be at offsets that are multiples 100 kHz.

Sub-Fractional Spurs

Sub-fractional spurs spurs occur at sub-multiples of the channel spacing, Fch. For instance, in the above example, there could be a sub-fractional spur at 50 kHz. The occurrence of these spurs is dependent on the modulator order. Integer mode and the first order modulator never have sub-fractional spurs. If the fractional denominator can be chosen to avoid factors of 2 or 3, then there will also be no sub-fractional spurs. Sub-fractional spurs get worse for higher order modulators. Dithering tends to reduce sub-fractional spurs at the expense of increasing PLL phase noise. The following table provides guidance on predicting sub-fractional spur offset frequencies.

Sub-Fractional Spur Offset Frequencies vs. Modulator Order and Fractional Denominator Factors

ORDER	Fractional Denominator Factors			
	No Factor of 2 or 3	Factor of 2 but not 3	Factor of 3 but not 2	Factor of 2 and 3
Integer Mode	None	None	None	None
1st Order Modulator	None	None	None	None
2nd Order Modulator	None	Fch/2	None	Fch/2
3rd Order Modulator	None	Fch/2	Fch/3	Fch/6
4th Order Modulator	None	Fch/4	Fch/3	Fch/12

Impact of VCO_DIV on Fractional spurs

Because the fractional and sub-fractional spur levels do not depend on output frequency, there is a big benefit to division. In general, every factor of 2 gives a 6 dB improvement to fractional spurs. Also, since the spur offset frequency is not divided, the channel spacing at the VCO can be also increased to improve the spurs. However, if the on-chip VCO is used, crosstalk can cause spurs at a frequency of f_{RFout} mod f_{PD}. Consider the following example of a 50 MHz phase detector frequency and VCO_DIV = 2. If the VCO is at 3000.1 MHz and divided by 2 to get 1500.05 MHz, there will be a spur at an offset of 50 kHz (1500.05 MHz mod 50 MHz). However, if the VCO frequency is at 3050.1 MHz, the output will be at 1525.05 MHz, but the spur will be at a much farther offset that can easily be filtered by the loop filter of 25.05 MHz (1525.05 MHz mod 50 MHz).

3.4 PLL PHASE NOISE

Disregarding the impact of reference oscillator noise, loop filter resistor thermal noise, and loop filter shaping, the phase noise of the PLL can be decomposed into three components: flicker noise, flat noise, and fractional noise. These noise sources add in an RMS sense to produce the total PLL noise. In other words:.

$$L_{PLL}(f) = 10\cdot\log(10^{(L_{PLL_flat}(f)/10)} + 10^{(L_{PLL_flicker}(f)/10)} + 10^{(L_{PLL_fractional}(f)/10)}$$

Symbol	Potential Influencing Factors				
	f	f_{VCO}	f_{PD}	K_{PD}	FRAC
$L_{PLL_flat}(f)$	No	Yes	Yes	Yes	No
$L_{PLL_flicker}(f)$	Yes	Yes	No	Yes	No
$L_{PLL_fractional}(f)$	Yes	No	Yes	No	Yes

The preceding table shows which factors of offset frequency (f), VCO frequency (f_{VCO}), phase detector frequency (f_{PD}), charge pump gain (K_{PD}), and the fractional settings (FRAC) can potentially influence each phase noise component. The fractional settings include the fraction, modulator order, and dithering.

For the flat noise and flicker noise, it is possible to normalize each of these noise sources into a single index. By normalizing these noise sources to an index, it makes it possible to calculate the flicker and flat noise for an arbitrary condition. These indices are reported in the electrical characteristics section and in the typical performance curves.

Noise Component	Index	Relationship
$L_{PLL_flat}(f)$	LN_{PLL_flat} (1 Hz)	$L_{PLL_flat}(f) = LN_{PLL_flat(1\ Hz)} + 20\cdot\log(N) + 10\cdot\log(f_{PD})$
$L_{PLL_flicker}(f)$	$LN_{PLL_flicker}$ (10 kHz)	$L_{PLL_flicker}(f) = LN_{PLL_flicker}(10\ kHz) - 10\cdot\log(10\ kHz / f) + 20\cdot\log(f_{VCO} / 1\ GHz)$

The flat noise is dependent on the PLL N divider value (N) and the phase detector frequency (f_{PD}) and the 1 Hz Normalized phase noise ($LN_{PLL_flat(1\ Hz)}$). The 1 Hz normalized phase noise can also depend on the charge pump gain as well. In order to make an accurate measurement of just the flat noise component, the offset frequency must be chosen sufficiently smaller then the loop bandwidth of the PLL, and yet large enough to avoid a substantial noise contribution from the reference and PLL flicker noise. This becomes easier to measure for lower phase detector frequencies.

The flicker noise, also known as 1/f noise, can be normalized to 1 GHz carrier frequency and 10 kHz offset, $LN_{PLL_flicker}$(10 kHz). Flicker noise can dominate at low offsets from the carrier and has a 10 dB/decade slope and improves with higher charge pump currents and at higher offset frequencies . To accurately measure the flicker noise it is important to use a high phase detector frequency and a clean crystal to make it such that this measurement is on the 10 dB/decade slope close to the carrier. $L_{PLL_flicker}(f)$ can be masked by the refer-

ence oscillator performance if a low power or noisy source is used.

For integer mode or a first order modulator, there is no fractional noise (disregarding fractional spurs). For higher order modulators, the fractional engine may or may not add significant phase noise depending on the fraction and choice of dithering.

3.5 IMPACT OF MODULATOR ORDER, DITHERING, AND LARGER EQUIVALENT FRACTIONS ON SPURS AND PHASE NOISE

To achieve a fractional N value, an integer N divider is modulated between different values. This gives rise to three main degrees of freedom with the LMX2541 delta sigma engine: the modulator order, dithering, and the way that the fractional portion is expressed. The first degree of freedom, the modulator order, can be selected as zero (integer mode), one, two, three, or four. One simple technique to better understand the impact of the delta sigma fractional engine on noise and spurs is to tune the VCO to an integer channel and observe the impact of changing the modulator order from integer mode to a higher order. A higher fractional modulator order in theory yields lower primary fractional spurs. However, this can also give rise to sub-fractional spurs in some applications. The second degree of freedom is dithering. Dithering seeks to improve the sub-fractional spurs by randomizing the sequence of N divider values. In theory, a perfectly randomized sequence would eliminate all sub-fractional spurs, but add phase noise by spreading the energy that would otherwise be contained in the spurs. The third degree of freedom is the way that the fraction is expressed. For example, 1/10 can be expressed as a larger equivalent fraction of 100000/1000000. Using larger equivalent fractions tends to increase randomization similar to dithering. In general, the very low phase noise of the LMX2541 exposes the modulator noise when dithering and large fractions are used, so use these with caution. The avid reader is highly encouraged to read application note 1879 for more details on fractional spurs. The following table summarizes the relationships between spur types, phase noise, modulator order, dithering and fractional expression.

Noise/Spur Type	Action		
	Increase Modulator Order	**Increase Dithering**	**Using Larger Equivalent Fractions**
Phase Noise	WORSE (But only for larger fractions or more dithering)	WORSE	WORSE
Primary Fractional Spur	BETTER	NO IMPACT	NO IMPACT
Sub-Fractional Spurs	WORSE (Creates more sub-fractional spurs)	BETTER	BETTER

3.6 MODULATOR ORDER

In general, the fractional mode of the PLL enables the use of a higher phase detector frequency relative to the channel spacing, which enables the in-band noise of the PLL to be lower. The choice of modulator order to be used in fractional mode is based on how much higher f_{PD} can be made relative to the channel spacing and the acceptable spur levels. The LMX2541 has a programmable modulator order which allows the user to make a trade-off between PLL noise and primary and sub-fractional spur performance. The following table provides some general guidelines for choosing modulator order: Note that the spurs due to crosstalk will not be impacted by modulator order.

ORDER	Guidelines for use
Integer Mode	— Use if f_{PD} can be made very high without using a fractional N value. — Use if it is not desired to make f_{PD} higher using a fractional N value. This could be the case if the loop bandwidth is very narrow and smaller loop filter capacitors are desired.
1st Order Modulator	— Use 1st order if f_{PD} can be increased by at least a factor of four over the integer case and fractional spur frequencies and levels are acceptable. — If the channel spacing is 5 MHz or greater, the 1st order modulator may provide better spur performance than integer mode.
2nd Order Modulator 3rd Order Modulator 4th Order Modulator	— If the spurs of the 1st order modulator are unacceptable, use a higher order modulator. If the spurious components are due to crosstalk they will not be improved by increasing modulator order. In this case , use the lowest order modulator that gives acceptable performance. — Use if the spurs of the 1st order modulator are unacceptable. — In general, use the lowest order modulator unless a higher order modulator yields an improvement in primary fractional spurs. If the spurious components are due to crosstalk, they will not be improved by increasing the modulator order.

3.7 PROGRAMMABLE OUTPUT POWER WITH ON/OFF

The RFoutEN pin an RFOUT word can be used to turn the RFout pin on and off while still keeping the VCO running and in lock. In addition to being able to turn the output buffer on and off, it can also be programmed in various steps using the VCOGAIN, DIVGAIN, and OUTTERM programming words. There are tables in the typical performance characteristics section that discuss the impact of these words on the output power. In addition to impacting the output power, these words also impact the current consumption of the device. This data was obtained as an average over all frequencies. In general, it is desirable to find the combination of programming words that gives the lowest current consumption for a given output power level. All numbers reported are relative to the case of VCOGAIN = OUTTERM = 12. According to this data, using a VCOGAIN or OUTTERM value of 12 or greater yields only a small increase in output power, but a large increase in current consumption.

Change in Current Consumption in Bypass Mode as a Function of VCOGAIN and OUTTERM

		VCOGAIN				
		3	6	9	12	15
OUTTERM	3	-26.0	-22.3	-18.6	-15.1	-11.8
	6	-18.5	-15.5	-12.6	-9.7	-6.9
	9	-11.1	-9.0	-6.9	-4.7	-2.5
	12	-3.8	-2.6	-1.4	0.0	+1.5
	15	+3.3	+3.7	+4.0	+4.5	+5.3

Change in Current Consumption in Divided Mode as a Function of DIVGAIN and OUTTERM

		DIVGAIN				
		3	6	9	12	15
OUTTERM	3	-24.4	-16.2	-8.3	-0.5	+7.1
	6	-21.7	-14.6	-7.6	-0.7	+6.0
	9	-18.7	-12.6	-6.8	-0.7	+5.2
	12	-15.9	-10.1	-5.0	0.0	+4.9
	15	-13.3	-8.0	-3.2	+1.3	+5.6

3.8 LOOP FILTER

Loop filter design can be rather complicated, but there are design tools and references available at www.national.com. The loop bandwidth can impact the size of loop filter capacitors and also how the phase noise is filtered. For optimal integrated phase noise, choose the bandwidth to be about 20% wider than the frequency where the in-band PLL phase noise (as described in *3.4 PLL PHASE NOISE*) and open loop VCO noise cross. This optimal loop bandwidth may need adjustment depending on the application requirements. Reduction of spurs can be achieved by reducing the loop bandwidth. On the other hand, a wider loop bandwidth may be required for faster lock time. Note that using the integrated loop filter components can lead to a significant restriction on the loop bandwidth and should be used with care. 2 kΩ for R3_LF and R4_LF is a good starting point. If the integrated loop filter restricts the loop bandwidth, then first try to relieve this restriction by reducing the integrated loop filter resistors and then reduce the capacitors only if necessary.

3.9 CONFIGURING THE LMX2541 FOR OPTIMAL PERFORMANCE

1. **Determine the Channel Spacing (f_{CH})**
   For a system that has a VCO that tunes over several frequencies, the channel spacing is the tuning increment. In the case that the VCO frequency is fixed, this channel spacing is the greatest number that divides both the VCO frequency and the OSCin frequency.
2. **Determine OSCin Frequency (f_{OSCin})**
   If the OSCin frequency is not already determined, then there are several considerations. A higher frequency is generally, but not always, preferable. One reason for this is that it has a higher slew rate if it is a sine wave. Another reason is that the clock for the VCO frequency calibration is based on the OSCin frequency and in general will run faster for higher OSCin frequencies.
   Although a higher OSCin frequency is desirable, there are also reasons to use a lower frequency. If the OSCin frequency is strategically chosen, the worst case fractional spur channels might fall out of band. Also, if the OSCin frequency can be chosen such that the fractional denominator can avoid factors of 2 and/or 3, the sub-fractional spurs can be reduced.
3. **Determine the Phase Detector Frequency (f_{PD}) , Charge Pump Gain (K_{PD}) and Fractional Denominator (FDEN)**
   In general, choose the highest phase detector frequency and charge pump gain, unless it leads to loop filter capacitor values that are unrealistically large for a given loop bandwidth. In this case, reducing either the phase detector frequency or the charge pump gain can yield more feasible capacitor values. Other reasons for not using the highest charge pump gain is to allow some adjustment margin to compensate for changes in the VCO gain or allow the use of Fastlock.
   For choosing the fractional denominator, start with FDEN = f_{PD}/f_{CH}. As discussed previously, there might be reasons to choose larger equivalent fractions.
4. **Design the Loop Filter**
5. **Determine the Modulator Order**
6. **Determine Dithering and Potential Larger Equivalent Fractional Value**

3.9 EXTERNAL VCO MODE

The LMX2541 also has provisions to be driven with an external VCO as well. In this mode, the user has the option of using the RFout pin output, although if this pin is used, the VCO input frequency is restricted to 4 GHz. If not used, the RFout pin should be left open. The VCO input is connected to the ExtVCOin pin. Because the internal VCO is not being used, the part option that is being used does not have a large impact on phase noise or spur performance. It is also possible to switch between both Full Chip mode and External VCO mode.

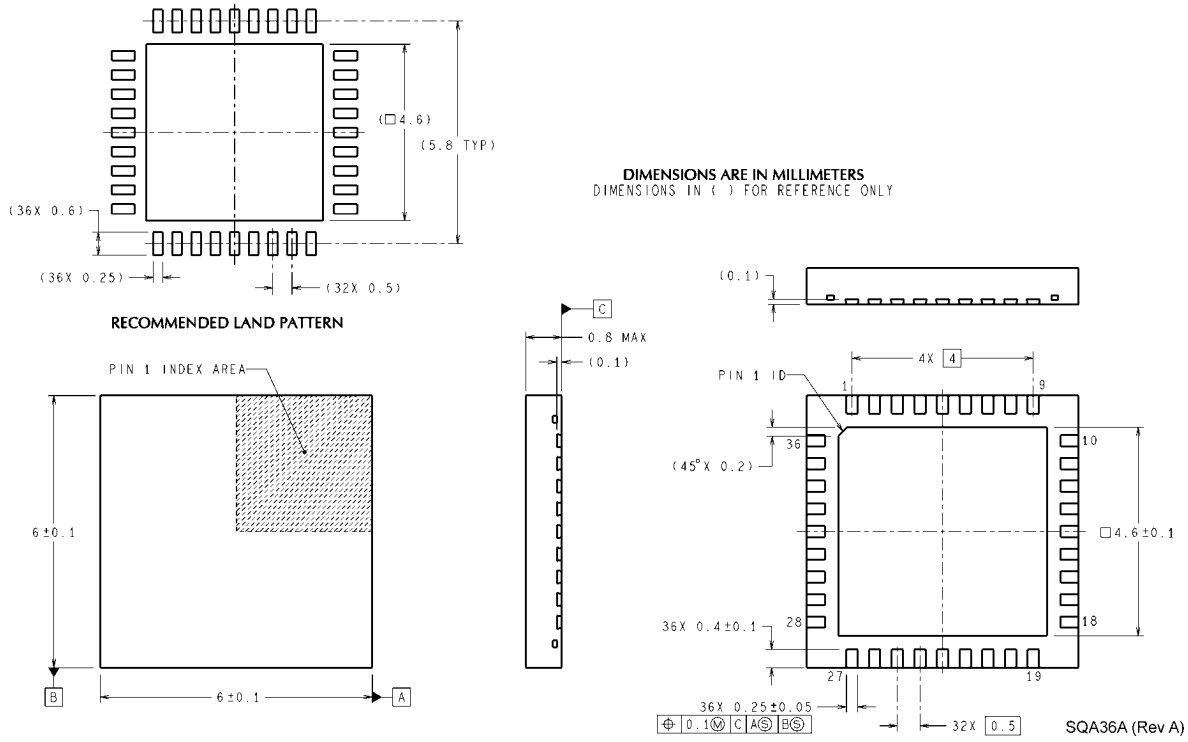
3.10 DIGITAL FSK MODE

The LMX2541 supports 2-level digital frequency shift keying (FSK) modulation. The bit rate is limited by the loop bandwidth of the PLL loop. As a general rule of thumb, it is desirable to have the loop bandwidth at least twice the bit rate. This is achieved by changing the N counter rapidly between two states. The fractional numerator and denominator are restricted to a length of 12 bits. The 12 LSB's of the numerator and denominator set the center frequency, Fcenter, and the 10 MSB's of the numerator set the frequency deviation, Fdev. The LMX2541 has the ability to switch between two different numerator values based on the voltage at the DATA pin. When DATA is low, the output frequency will be Fcenter – Fdev and when the DATA pin is high the output frequency will be Fcenter + Fdev.A limitation of the FSK mode is that it does not function on integer channels and the frequency deviation can not cause the N counter to cross integer boundaries. When using FSK mode, the FDM bit needs to be set to zero.

Ordering Information

Device	Marking	Package
LMX2541SQ2060E	412060E	SQA36A
LMX2541SQ2380E	412380E	SQA36A
LMX2541SQ2690E	412690E	SQA36A
LMX2541SQ3030E	413030E	SQA36A
LMX2541SQ3320E	413320E	SQA36A
LMX2541SQ3740E	413740E	SQA36A

Physical Dimensions inches (millimeters) unless otherwise noted



Consult www.national.com/analog/packaging ->LLP footprints in gerber footprint for more complete information on soldering this device reliably.

Leadless Leadframe Package (NS Package Number SQA36A), (Bottom View)

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

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Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
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