

# PCA9306 双路双向 I<sup>2</sup>C 总线和 SMBus 电压电平转换器

## 1 特性

- 适用于 I<sup>2</sup>C 应用中的 SDA 和 SCL 线路的 2 位双向转换器
- 与 I<sup>2</sup>C 和系统管理总线 (SMBus) 兼容
- 小于 1.5ns 的最大传播延迟, 适应标准模式和快速模式 I<sup>2</sup>C 器件和多个主控器
- 可实现以下电压之间的电压电平转换
  - 1.2V V<sub>REF1</sub> 和 1.8V、2.5V、3.3V 或 5V V<sub>REF2</sub>
  - 1.8V V<sub>REF1</sub> 和 2.5V、3.3V 或 5V V<sub>REF2</sub>
  - 2.5V V<sub>REF1</sub> 和 3.3V 或 5V V<sub>REF2</sub>
  - 3.3V V<sub>REF1</sub> 和 5V V<sub>REF2</sub>
- 在无方向引脚的情况下提供双向电压转换
- 输入和输出端口之间 3.5Ω 的低导通状态电阻可减少信号失真
- 漏极开路 I<sup>2</sup>C I/O 端口 (SCL1、SDA1、SCL2 和 SDA2)
- 5V 耐压 I<sup>2</sup>C 和 I/O 端口可支持混合模式信号操作
- 针对 EN 为低电平的高阻抗 SCL1、SDA1、SCL2 和 SDA2 引脚
- 无闭锁操作可在 EN 为低电平时实现隔离
- 采用直通引脚排列以简化印刷电路板布线
- 闩锁性能超过 100mA, 符合 JESD 78 II 类规范
- ESD 保护性能超出 JESD 22 标准
  - 2000V 人体放电模型 (A114-A))
  - 1000V 充电器件模型 (C101)

## 2 应用

- I<sup>2</sup>C、SMBus、PMBus、MDIO、UART、低速 SDIO、GPIO 和其他双信号接口
- 服务器
- 路由器 (电信交换设备)
- 个人计算机
- 工业自动化

## 3 说明

PCA9306 器件是一款采用使能 (EN) 输入的双路双向 I<sup>2</sup>C 和 SMBus 电压电平转换器, 可在 1.2V 至 3.3V V<sub>REF1</sub> 和 1.8V 至 5.5V V<sub>REF2</sub> 的范围内工作。

PCA9306 器件可以在 1.2V 到 5V 之间实现双向电压转换而无须使用方向引脚。此开关具有低导通状态电阻 (R<sub>ON</sub>), 可以在最短传播延迟情况下建立连接。当 EN 为高电平时, 转换器开关打开, 并且 SCL1 和 SDA1 I/O 被分别连接至 SCL2 和 SDA2 I/O, 从而实现端口间的双向数据流。当 EN 为低电平时, 转换器开关关闭, 在端口之间存在一个高阻抗状态。

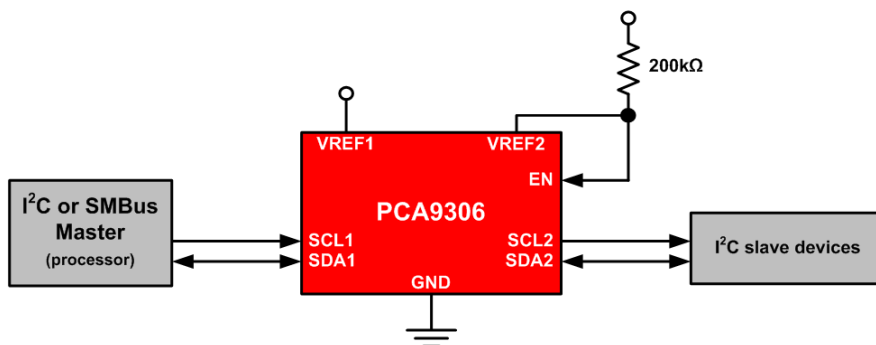
除了电压转换, PCA9306 器件还可用于将 400kHz 总线与 100kHz 总线隔离开, 方法是在快速模式通信过程中控制 EN 引脚以断开较慢总线的连接。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
PCA9306	SSOP (8)	2.95mm x 2.80mm
	VSSOP (8)	2.30mm x 2.00mm
	X2SON (8)	1.40mm x 1.00mm
	DSBGA (8)	1.98mm x 0.98mm

(1) 如需了解所有可用封装, 请见数据表末尾的可订购产品附录。

简化应用示意图



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision L (April 2016) to Revision M	Page
• Changed the DQE package family From: VSSON to X2SON .....	4
• Added new section to <i>Overview</i> .....	9
• Changed the labels in <a href="#">Figure 19</a> . The red curve is > 2 V, the black curve is ≤ 2 V. ....	18

Changes from Revision K (October 2014) to Revision L	Page
• 将“导通状态连接”更改为“导通状态电阻” .....	1
• 删除了机器模型 ESD 额定值 .....	1
• 在“说明”部分的最后一句中，在“100kHz”后增加了“总线”两字 .....	1
• 更改了 <i>器件信息</i> 表中的封装尺寸 .....	1
• Replaced pinout diagrams .....	4
• Added I/O column to the <i>Pin Functions</i> table .....	4
• Deleted RVH package from <i>Pin Configuration and Functions</i> section .....	4
• Moved $T_{stg}$ from <i>Handling Ratings</i> to <i>Absolute Maximum Ratings</i> .....	5
• Changed <i>Handling Ratings</i> to <i>ESD Ratings</i> .....	5
• Added a note following the <i>Electrical Characteristics</i> table .....	6
• Added <a href="#">Figure 4</a> to the <i>Parameter Measurement Information</i> section .....	8
• Changed <a href="#">Figure 5</a> .....	8
• Changed "repeater" to "level shifter" in second paragraph of the <i>Overview</i> section .....	9
• Changed the <a href="#">Design Requirements</a> table .....	17
• Deleted the bottommost row of the <i>Design Requirements</i> table .....	17
• Corrected equation from $f_{knee} = 0.5 / RT$ (10%–80%) to $f_{knee} = 0.5 / RT$ (10%–90%) .....	18

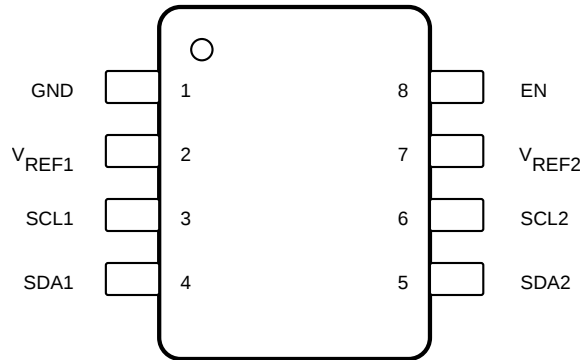
**Changes from Revision J (October 2010) to Revision K**

**Page**

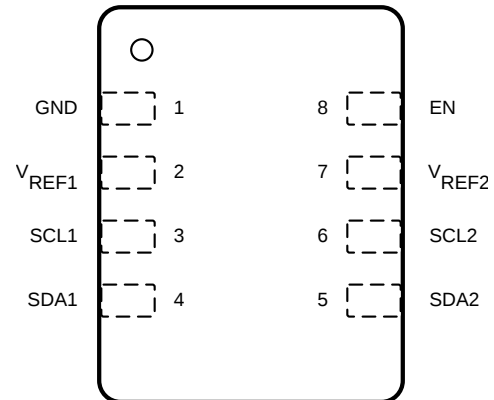
• 已添加 引脚配置和功能部分，处理额定值表，特性 说明 部分、器件功能模式、应用和实施 部分、电源相关建议 部 分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分 .....	<b>1</b>
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## 5 Pin Configuration and Functions

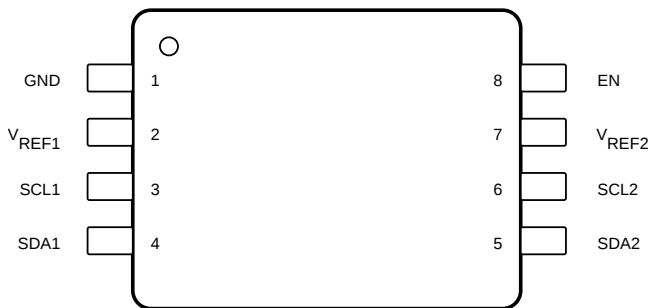
**DCT Package  
8-Pin SSOP  
Top View**



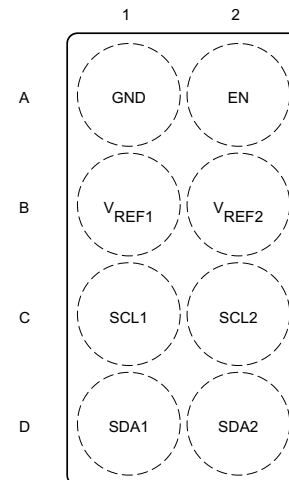
**DQE Package  
8-Pin X2SON  
Top View**



**DCU Package  
8-Pin VSSOP  
Top View**



**YZT Package  
8-Pin DSBGA  
Top View**



### Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DCT, DCU, DQE	YZT		
EN	8	A2	I	Switch enable input
GND	1	A1	—	Ground, 0 V
SCL1	3	C1	I/O	Serial clock, low-voltage side
SCL2	6	C2	I/O	Serial clock, high-voltage side
SDA1	4	D1	I/O	Serial data, low-voltage side
SDA2	5	D2	I/O	Serial data, high-voltage side
V <sub>REF1</sub>	2	B1	I	Low-voltage-side reference supply voltage for SCL1 and SDA1
V <sub>REF2</sub>	7	B2	I	High-voltage-side reference supply voltage for SCL2 and SDA2

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>REF1</sub>	DC reference voltage range		−0.5	7	V
V <sub>REF2</sub>	DC reference bias voltage range		−0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		−0.5	7	V
V <sub>I/O</sub>	Input/output voltage range <sup>(2)</sup>		−0.5	7	V
	Continuous channel current			128	mA
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		−50	mA
T <sub>J(max)</sub>	Maximum junction temperature			125	°C
T <sub>stg</sub>	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and input/output negative voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V <sub>I/O</sub>	Input/output voltage	SCL1, SDA1, SCL2, SDA2	0	5.5	V
V <sub>REF1</sub> <sup>(1)</sup>	Reference voltage		0	5.5	V
V <sub>REF2</sub> <sup>(1)</sup>	Reference voltage		0	5.5	V
EN	Enable input voltage		0	5.5	V
I <sub>PASS</sub>	Pass switch current			64	mA
T <sub>A</sub>	Operating ambient temperature		−40	85	°C

- (1) To support translation, V<sub>REF1</sub> supports 1.2 V to V<sub>REF2</sub> - 0.6 V. V<sub>REF2</sub> must be between V<sub>REF1</sub> + 0.6 V to 5.5 V. See [Typical Application](#) for more information.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		PCA9306				UNIT
		DCT	DCU	DQE	YZT	
		8 PINS	8 PINS	8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	189.6	210.1	246.5	125.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	119.6	81.9	149.1	1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	102.1	88.8	100	62.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	44.5	8.3	17.1	3.4	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	101	88.4	99.8	62.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input clamp voltage		I <sub>I</sub> = −18 mA,	EN = 0 V				−1.2	V
I <sub>IH</sub>	Input leakage current		V <sub>I</sub> = 5 V,	EN = 0 V				5	μA
C <sub>i(EN)</sub>	Input capacitance		V <sub>I</sub> = 3 V or 0				11		pF
C <sub>io(off)</sub>	Off capacitance	SCLn, SDAn	V <sub>O</sub> = 3 V or 0,	EN = 0 V			4	6	pF
C <sub>io(on)</sub>	On capacitance	SCLn, SDAn	V <sub>O</sub> = 3 V or 0,	EN = 3 V			10.5	12.5	pF
R <sub>ON</sub> <sup>(2)</sup>	On-state resistance	SCLn, SDAn	V <sub>I</sub> = 0	I <sub>O</sub> = 64 mA	EN = 4.5 V		3.5	5.5	Ω
					EN = 3 V		4.7	7	
					EN = 2.3 V		6.3	9.5	
			V <sub>I</sub> = 0	I <sub>O</sub> = 15 mA	EN = 1.5 V		25.5	32	
					EN = 4.5 V	1	6	15	
					EN = 3 V	20	60	140	
V <sub>I</sub> = 1.7 V <sup>(3)</sup>	I <sub>O</sub> = 15 mA	EN = 2.3 V		20	60	140			

(1) All typical values are at  $T_A = 25^\circ\text{C}$ .

(2) Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals, at the indicated current through the switch. Minimum ON-state resistance is determined by the lowest voltage of the two terminals.

(3) Measured in current sink configuration only (See Figure 4)

## 6.6 Switching Characteristics AC Performance (Translating Down) (EN = 3.3 V)<sup>(1)</sup>

over recommended operating ambient temperature range, EN = 3.3 V,  $V_{IH} = 3.3$  V,  $V_{IL} = 0$ ,  $V_M = 1.15$  V (unless otherwise noted) (see Figure 4).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50$ pF		$C_L = 30$ pF		$C_L = 15$ pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	SCL2 or SDA2	SCL1 or SDA1	0	0.8	0	0.6	0	0.3	ns
$t_{PHL}$			0	1.2	0	1	0	0.5	

(1) Translating down: the high-voltage side driving toward the low-voltage side

## 6.7 Switching Characteristics AC Performance (Translating Down) (EN = 2.5 V)<sup>(1)</sup>

over recommended operating ambient temperature range, EN = 2.5 V,  $V_{IH} = 3.3$  V,  $V_{IL} = 0$ ,  $V_M = 0.75$  V (unless otherwise noted) (see Figure 4).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50$ pF		$C_L = 30$ pF		$C_L = 15$ pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	SCL2 or SDA2	SCL1 or SDA1	0	1	0	0.7	0	0.4	ns
$t_{PHL}$			0	1.3	0	1	0	0.6	

(1) Translating down: the high-voltage side driving toward the low-voltage side

## 6.8 Switching Characteristics AC Performance (Translating Up) (EN = 3.3 V)<sup>(1)</sup>

over recommended operating ambient temperature range, EN = 3.3 V,  $V_{IH} = 2.3$  V,  $V_{IL} = 0$ ,  $V_T = 3.3$  V,  $V_M = 1.15$  V,  $R_L = 300$  Ω (unless otherwise noted) (see Figure 4).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50$ pF		$C_L = 30$ pF		$C_L = 15$ pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	SCL1 or SDA1	SCL2 or SDA2	0	0.9	0	0.6	0	0.4	ns
$t_{PHL}$			0	1.4	0	1.1	0	0.7	

(1) Translating up: the low-voltage side driving toward the high-voltage side

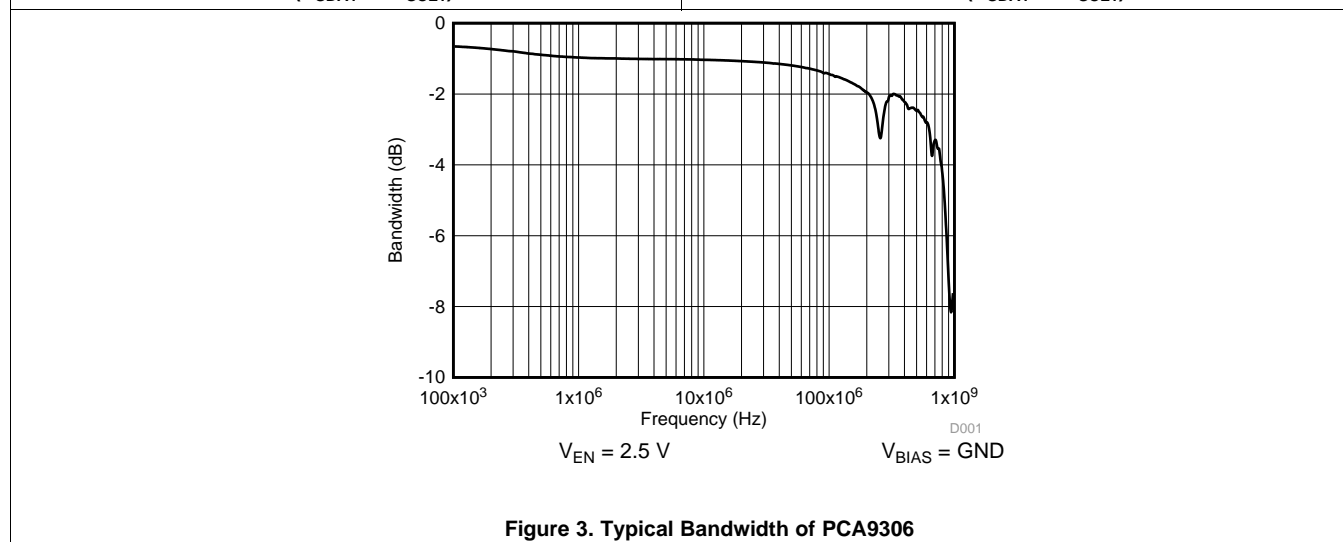
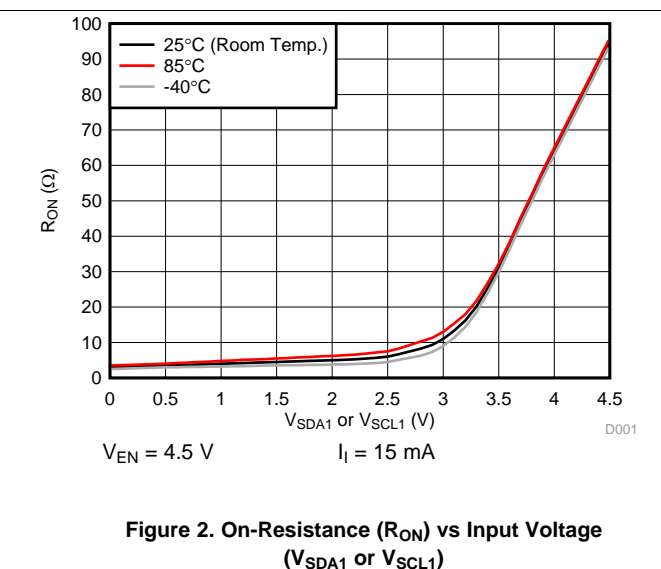
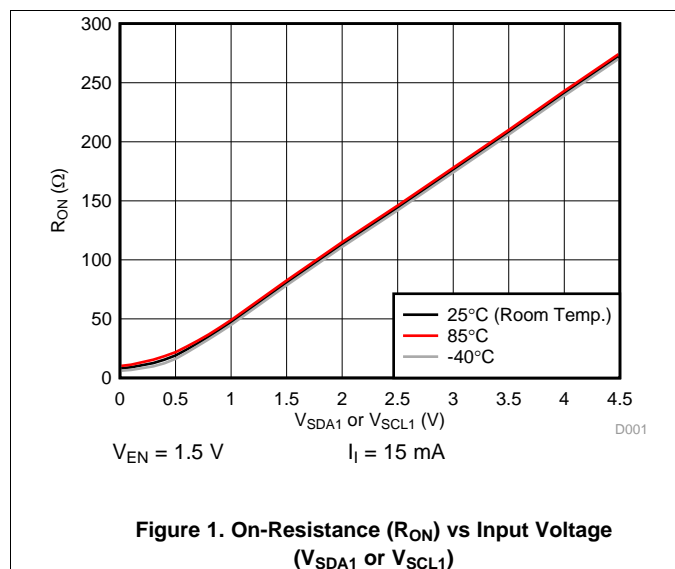
## 6.9 Switching Characteristics AC Performance (Translating Up) (EN = 2.5 V)<sup>(1)</sup>

over recommended operating ambient temperature range, EN = 2.5 V,  $V_{IH} = 2.3$  V,  $V_{IL} = 0$ ,  $V_T = 3.3$  V,  $V_M = 0.75$  V,  $R_L = 300$   $\Omega$  (unless otherwise noted) (see Figure 4).

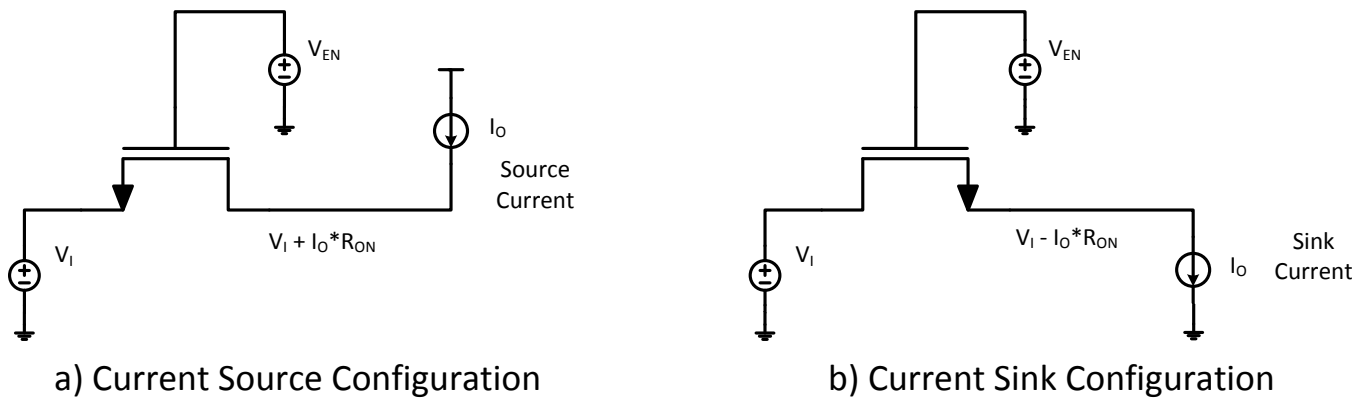
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50$ pF		$C_L = 30$ pF		$C_L = 15$ pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	SCL1 or SDA1	SCL2 or SDA2	0	1	0	0.6	0	0.4	ns
$t_{PHL}$			0	1.3	0	1.3	0	0.8	

(1) Translating up: the low-voltage side driving toward the high-voltage side

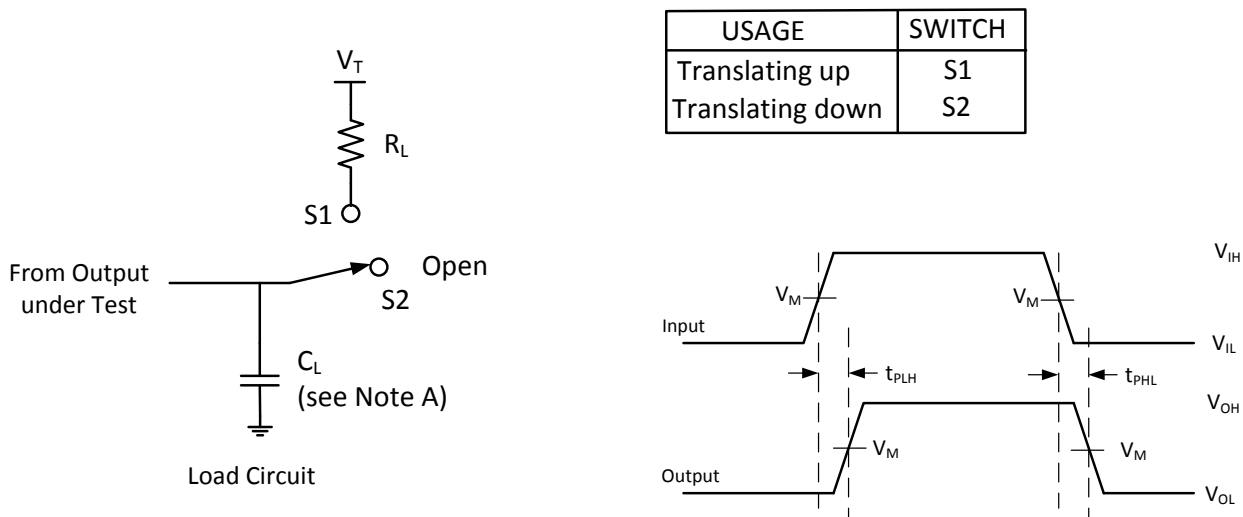
## 6.10 Typical Characteristics



## 7 Parameter Measurement Information



**Figure 4. Current Source and Current Sink Configurations for  $R_{ON}$  Measurements**



NOTES: A.  $C_L$  includes probe and jig capacitance

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .

C. The outputs are measured one at a time, with one transition per measurement.

**Figure 5. Load Circuit for Outputs**



## 8 Detailed Description

### 8.1 Overview

The PCA9306 device is a dual bidirectional I<sup>2</sup>C and SMBus voltage-level translator with an enable (EN) input and operates without use of a direction pin. The voltage supply range for  $V_{REF1}$  is 1.2 V to 3.3 V and the supply range for  $V_{REF2}$  is 1.8 V to 5.5 V.

The PCA9306 device can also be used to run two buses, one at 400-kHz operating frequency and the other at 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be disconnected by using the EN pin when the 400-kHz operation of the main bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the level shifter.

In I<sup>2</sup>C applications, the bus capacitance limit of 400 pF restricts the number of devices and bus length. The capacitive load on both sides of the PCA9306 device must be taken into account when approximating the total load of the system, ensuring the sum of both sides is under 400 pF.

Both the SDA and SCL channels of the PCA9306 device have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete-transistor voltage-translation solutions, because the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less-ESD-resistant devices.

#### 8.1.1 Definition of threshold voltage

This document references a threshold voltage denoted as  $V_{th}$ , which appears multiple times throughout this document when discussing the NFET between  $V_{REF1}$  and  $V_{REF2}$ . The value of  $V_{th}$  is approximately 0.6 V at room temperature.

#### 8.1.2 Correct Device Set Up

In a normal set up shown in Figure 6, the enable pin and  $V_{REF2}$  are shorted together and tied to a 200-k $\Omega$  resistor, and a reference voltage equal to  $V_{REF1}$  plus the FET threshold voltage is established. This reference voltage is used to help pass lows from one side to another more effectively while still separating the different pull up voltages on both sides.

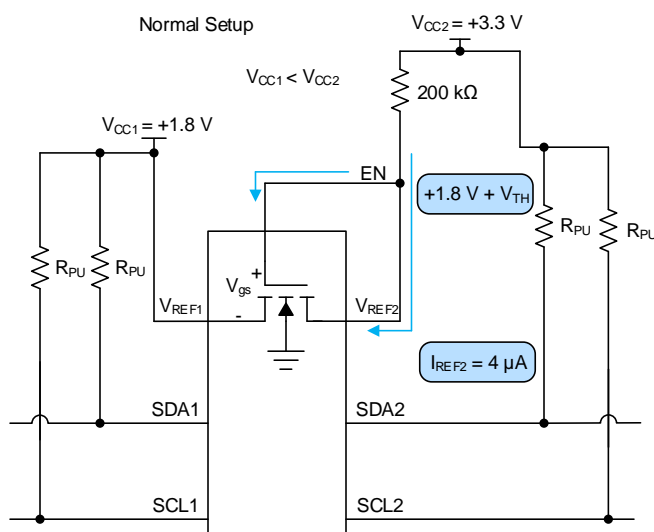
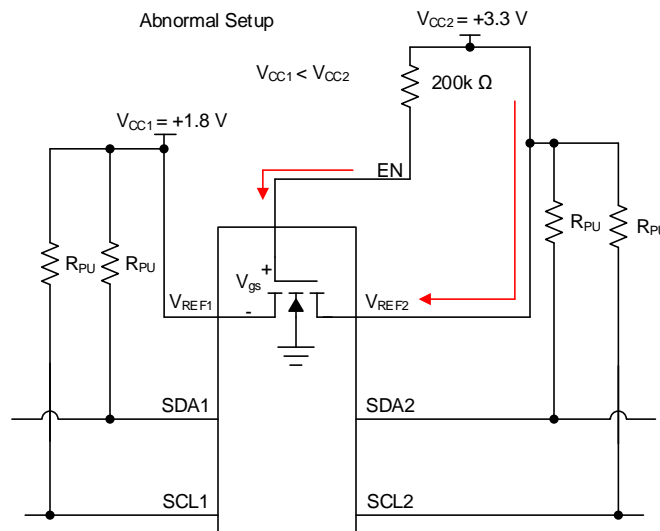


Figure 6. Normal Setup

## Overview (continued)

Care should be taken to ensure  $V_{REF2}$  has an external resistor tied between it and  $V_{CC2}$ . If  $V_{REF2}$  is tied directly to the  $V_{CC2}$  rail without a resistor, then there is no external resistance from the  $V_{CC2}$  to  $V_{CC1}$  to limit the current such as in Figure 7. This effectively looks like a low impedance path for current to travel through and potentially break the pass FET if the current flowing through the pass FET is larger than the absolute maximum continuous channel current specified in section 6.1. The continuous channel current is larger with a higher voltage difference between  $V_{CC1}$  and  $V_{CC2}$ .

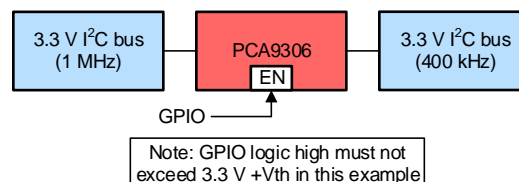
Figure 7 shows an improper set up. If  $V_{CC2}$  is larger than  $V_{CC1}$  but less than  $V_{th}$ , the impedance between  $V_{CC1}$  and  $V_{CC2}$  is high resulting in a low drain to source current, which does not cause damage to the device. Concern arises when  $V_{CC2}$  becomes larger than  $V_{CC1}$  by  $V_{th}$ . During this event, the NFET turns on and begin to conduct current. This current is dependent on the gate to source voltage and drain to source voltage.



**Figure 7. Abnormal Setup**

### 8.1.3 Disconnecting a Slave from the Main I2C Bus Using the EN Pin

PCA9306 can be used as a switch to disconnect one side of the device from the main I2C bus. This can be advantageous in multiple situations. One instance of this situation is if there are devices on the I2C bus which only supports fast mode (400 kHz) while other devices on the bus support fast mode plus (1 MHz). An example of this is displayed in Figure 8.



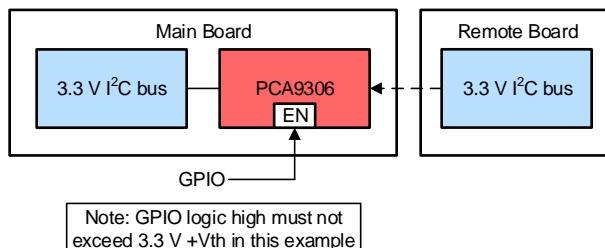
**Figure 8. Example of an I2C bus with multiple supported frequencies**

In this situation, if the master is on the 1 MHz side then communicating at 1 MHz should not be attempted if PCA9306 were enabled. It needs to be disabled for PCA9306 to avoid possibly glitching state machines in devices which were designed to operate correctly at 400 kHz or slower. When PCA9306 is disabled, the master can communicate with the 1 MHz devices without disturbing the 400 kHz bus. When the PCA9306 is enabled, communication across both sides at 400 kHz is acceptable.

## Overview (continued)

### 8.1.4 Supporting Remote Board Insertion to Backplane with PCA9306

Another situation where PCA9306 is advantageous when using its enable feature is when a remote board with I2C lines needs to be attached to a main board (backplane) with an I2C bus such as in Figure 9. If connecting a remote board to a backplane is not done properly, the connection could result in data corruption during a transaction or the insertion could generate an unintended pulse on the SCL line. Which could glitch an I2C device state machine causing the I2C bus to get stuck.

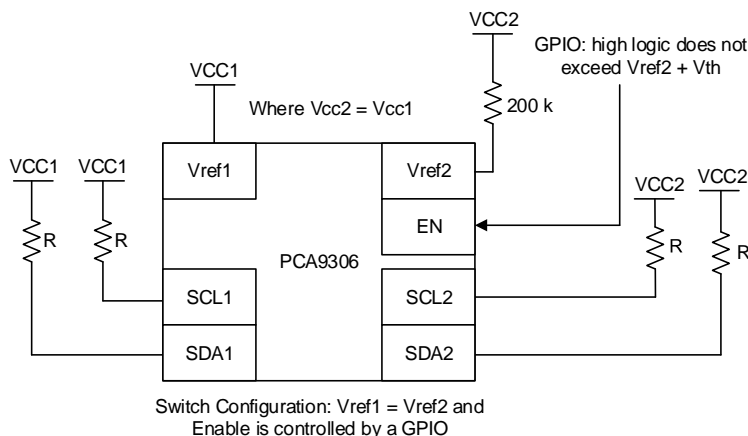


**Figure 9. An example of connecting a remote board to a main board (backplane)**

PCA9306 can be used to support this application because it can be disabled while making the connection. Then it is enabled once the remote board is powered on and the buses on both sides are IDLE.

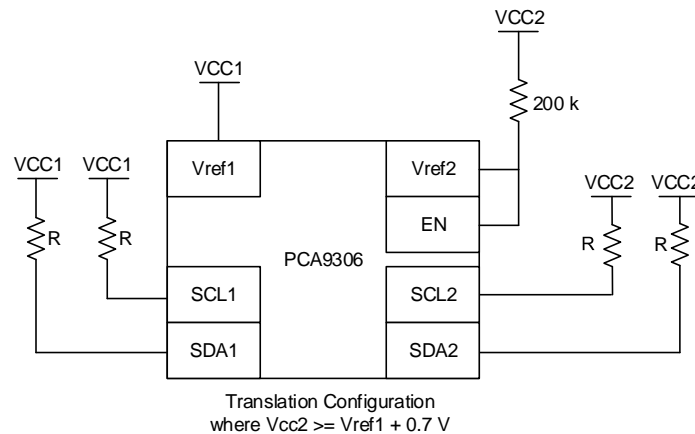
### 8.1.5 Switch Configuration

PCA9306 has the capability of being used with its  $V_{REF1}$  voltage equal to  $V_{REF2}$ . This essentially turns the device from a translator to a device which can be used as a switch, and in some situations this can be useful. The switch configuration is shown in Figure 10 and translation mode is shown in Figure 11.



**Figure 10. Switch Configuration**

## Overview (continued)

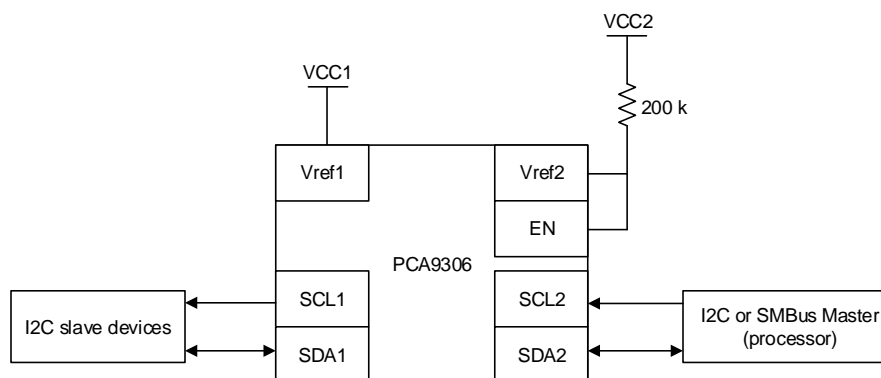


**Figure 11. Translation Configuration**

When PCA9306 is in the switch configuration ( $V_{REF1} = V_{REF2}$ ), the propagation delays are different compared to the translator configuration. Taking a look at the propagation delays, if the pull up resistance and capacitance on both sides of the bus are equal, then in switch mode the PCA9306 has the same propagation delay from side one to two and side two to one. The propagation delays become lower when  $V_{CC1}/V_{CC2}$  is larger. For example, the propagation delay at 1.8 V is longer than at 5 V in the switching configuration. When PCA9306 is in translation mode, side one propagate lows to side two faster than side two can propagate lows to side 1. This time difference becomes larger the larger the difference between  $V_{CC2}$  and  $V_{CC1}$  becomes.

### 8.1.6 Master on Side 1 or Side 2 of Device

I2C and SMBus are bidirectional protocol meaning devices on the bus can both transmit and receive data. PCA9306 was designed to allow for signals to be able to be transmitted from either side, thus allowing for the master to be able to placed on either side of the device. Figure 12 shows the master on side two as opposed to the diagram on page 1 of this data sheet.



**Figure 12. Master on side 2 of PCA9306**

## Overview (continued)

### 8.1.7 LDO and PCA9306 Concerns

The  $V_{REF1}$  pin can be supplied by a low-dropout regulator (LDO), but in some cases the LDO may lose its regulation because of the bias current from  $V_{REF2}$  to  $V_{REF1}$ . If the LDO cannot sink the bias current, then the current has no other paths to ground and instead charges up the capacitance on the  $V_{REF1}$  node (both external and parasitic). This results in an increase in voltage on the  $V_{REF1}$  node. If no other paths for current to flow are established (such as back biasing of body diodes or clamping diodes through other devices on the  $V_{REF1}$  node), then the  $V_{REF1}$  voltage ends up stabilizing when  $V_{gs}$  of the pass FET is equal to  $V_{th}$ . This means  $V_{REF1}$  node voltage is  $V_{CC2} - V_{th}$ . Note that any slaves/masters running off of the LDO now see the  $V_{CC2} - V_{th}$  voltage which may cause damage to those slaves/masters if they are not rated to handle the increased voltage.

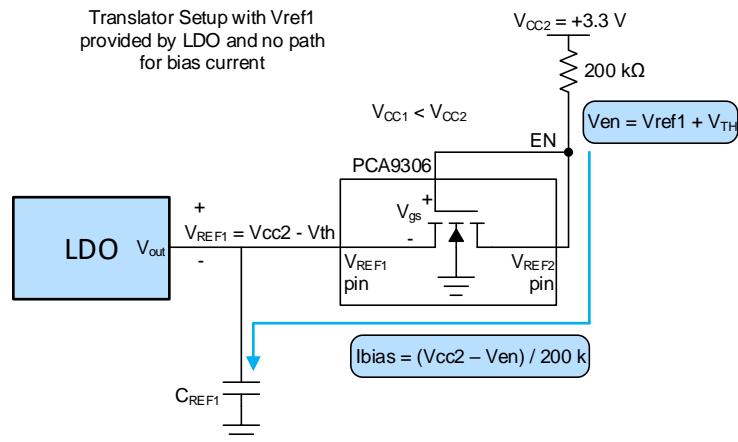


Figure 13. Example of no leakage current path when using LDO

To ensure LDO does not lose regulation due to the bias current of PCA9306, a weak pull down resistor can be placed on  $V_{REF1}$  to ground to provide a path for the bias current to travel. The recommended pull down resistor is calculated by Equation 4 where 0.75 gives about 25% margin for error incase bias current increases during operation.

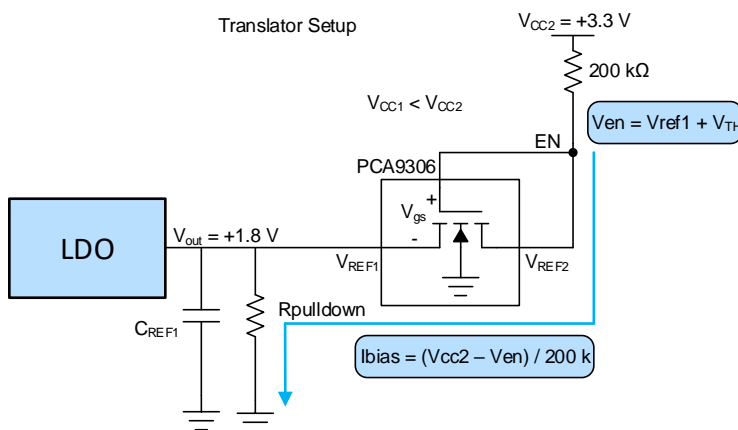


Figure 14. Example with Leakage current path when using an LDO

$$V_{en} = V_{REF1} + V_{th}$$

where

- $V_{th}$  is approximately 0.6 V

$$I_{bias} = (V_{CC2} - V_{en}) / 200k$$

$$R_{pulldown} = V_{OUT} / I_{bias}$$

$$\text{Recommended } R_{pulldown} = R_{pulldown} \times 0.75$$

(1)

(2)

(3)

(4)

## Overview (continued)

### 8.1.8 Current Limiting Resistance on $V_{REF2}$

The resistor is used to limit the current between  $V_{REF2}$  and  $V_{REF1}$  (denoted as  $R_{CC}$ ) and helps to establish the reference voltage on the enable pin. The 200k resistor can be changed to a lower value; however, the bias current proportionally increases as the resistor decreases.

$$I_{bias} = (V_{CC2} - V_{en})/R_{CC} : V_{en} = V_{REF1} + V_{th}$$

where

- $V_{th}$  is approximately 0.6V (5)

Keep in mind  $R_{CC}$  should not be sized low enough that  $I_{CC}$  exceeds the absolute maximum continuous channel current specified in section 6.1 which is described in [Equation 6](#).

$$R_{CC(min)} \geq (V_{CC2} - V_{en})/0.128 : V_{en} = V_{REF1} + V_{th}$$

where

- $V_{th}$  is approximately 0.6V (6)

## 8.2 Functional Block Diagram

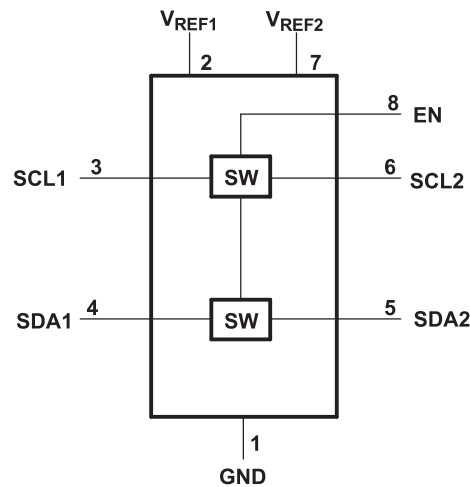


Figure 15. Block Diagram of PCA9306

## 8.3 Feature Description

### 8.3.1 Enable (EN) Pin

The PCA9306 device is a double-pole, single-throw switch in which the gate of the transistors is controlled by the voltage on the EN pin. In [Figure 16](#), the PCA9306 device is always enabled when power is applied to  $V_{REF2}$ . In [Figure 17](#), the device is enabled when a control signal from a processor is in a logic-high state.

### 8.3.2 Voltage Translation

The primary feature of the PCA9306 device is translating voltage from an I<sup>2</sup>C bus referenced to  $V_{REF1}$  up to an I<sup>2</sup>C bus referenced to  $V_{DPU}$ , to which  $V_{REF2}$  is connected through a 200-k $\Omega$  pullup resistor. Translation on a standard, open-drain I<sup>2</sup>C bus is achieved by simply connecting pullup resistors from SCL1 and SDA1 to  $V_{REF1}$  and connecting pullup resistors from SCL2 and SDA2 to  $V_{DPU}$ . Information on sizing the pullup resistors can be found in the [Sizing Pullup Resistors](#) section.

## 8.4 Device Functional Modes

INPUT EN <sup>(1)</sup>	TRANSLATOR FUNCTION
H	Logic Lows are propagated from one side to the other, Logic Highs blocked (independent pull up resistors passively drive the line high)
L	Disconnect

(1) The SCL switch conducts if EN is  $\geq 0.6$  V higher than SCL1 or SCL2. The same is true of SDA.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 General Applications of I<sup>2</sup>C

As with the standard I<sup>2</sup>C system, pullup resistors are required to provide the logic-high levels on the translator bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I<sup>2</sup>C devices in addition to SMBus devices. Standard-mode I<sup>2</sup>C devices only specify 3 mA in a generic I<sup>2</sup>C system where standard-mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used. When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by  $V_{REF1}$ . When the SDA1 port is high, the SDA2 port is pulled to the pullup supply voltage of the drain ( $V_{DPU}$ ) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2 channel.

### 9.2 Typical Application

Figure 16 and Figure 17 show how these pullup resistors are connected in a typical application, as well as two options for connecting the EN pin.

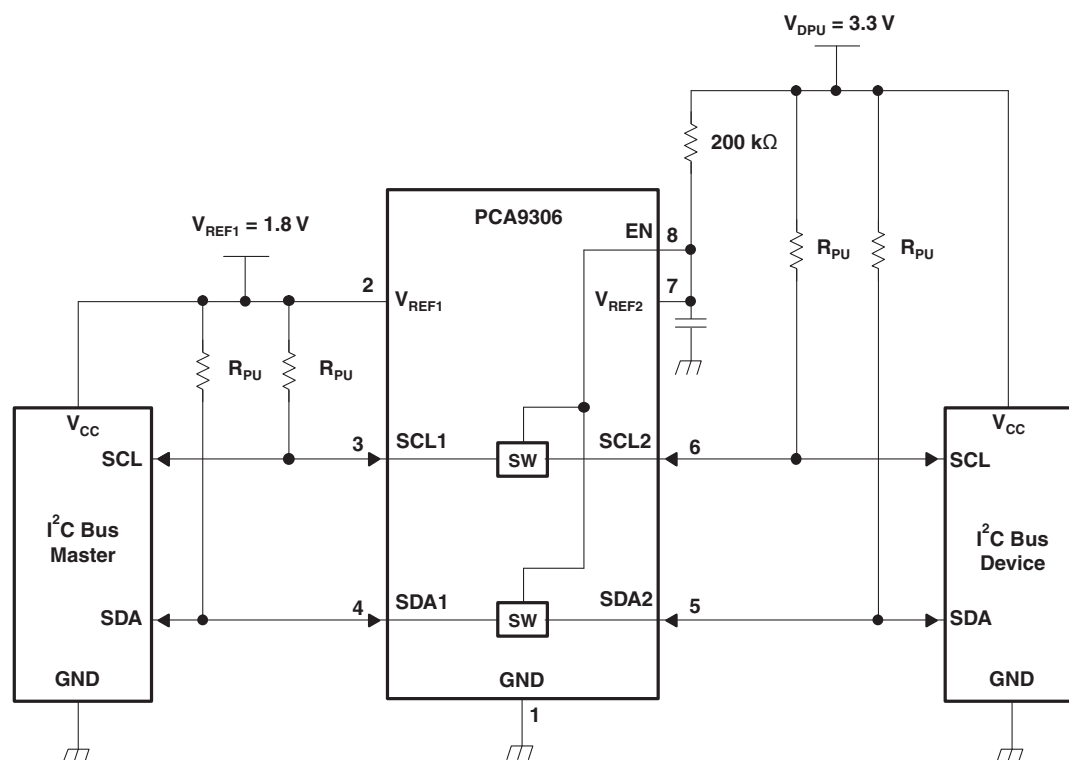


Figure 16. Typical Application Circuit (Switch Always Enabled)



## Typical Application (continued)

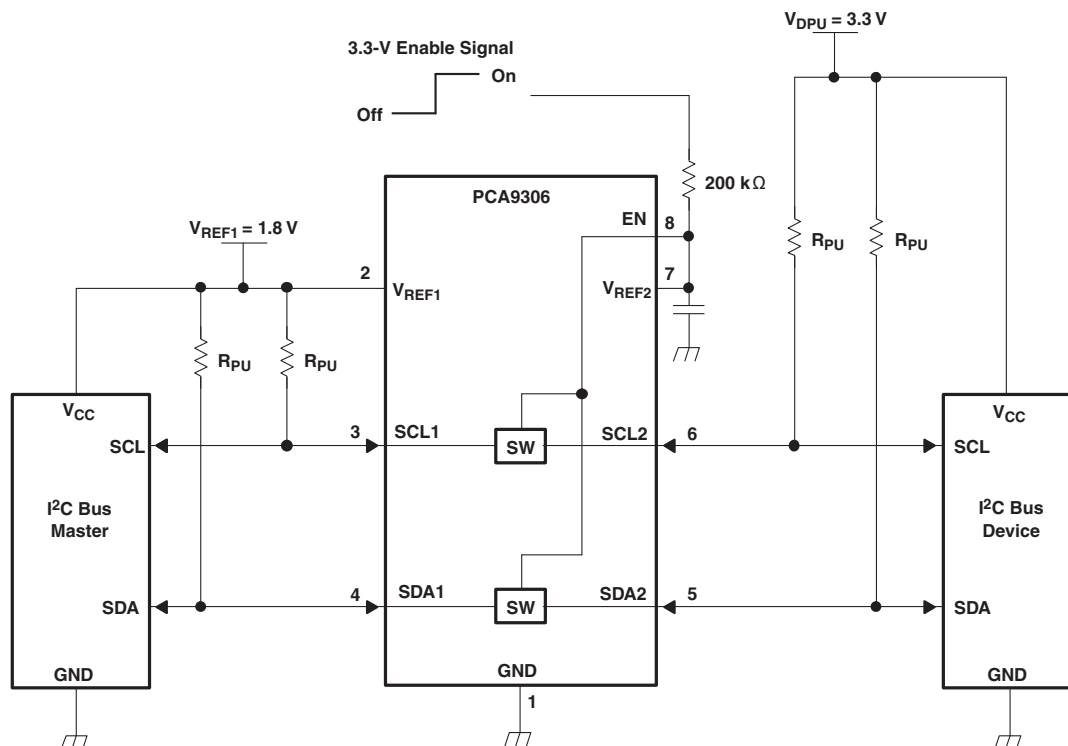


Figure 17. Typical Application Circuit (Switch Enable Control)

### 9.2.1 Design Requirements

		MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>REF2</sub>	Reference voltage	V <sub>REF1</sub> + 0.6	2.1	5	V
EN	Enable input voltage	V <sub>REF1</sub> + 0.6	2.1	5	V
V <sub>REF1</sub>	Reference voltage	1.2	1.5	4.4	V
I <sub>PASS</sub>	Pass switch current		6		mA
I <sub>REF</sub>	Reference-transistor current		5		μA

(1) All typical values are at T<sub>A</sub> = 25°C.

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Bidirectional Voltage Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V<sub>REF2</sub> and both pins pulled to high-side V<sub>DPU</sub> through a pullup resistor (typically 200 kΩ). This allows V<sub>REF2</sub> to regulate the EN input. A 100-pF filter capacitor connected to V<sub>REF2</sub> is recommended. The I²C bus master output can be push-pull or open-drain (pullup resistors may be required) and the I²C bus device output can be open-drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to V<sub>DPU</sub>). However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state capable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open-drain, no direction control is needed.

#### 9.2.2.2 Sizing Pullup Resistors

To get an estimate for the range of values that can be used for the pullup resistor, please refer to the application note [SLVA689](#). [Figure 18](#) and [Figure 19](#) respectively show the maximum and minimum pullup resistance allowable by the I²C specification for standard-mode (100 kHz) and fast-mode (400 kHz) operation.

### 9.2.2.3 PCA9306 Bandwidth

The maximum frequency of the PCA9306 device depends on the application. The device can operate at speeds of > 100 MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application.

Figure 3 shows a bandwidth measurement of the PCA9306 device using a two-port network analyzer.

However, this is an analog type of measurement. For digital applications, the signal should not degrade up to the fifth harmonic of the digital signal. As a rule of thumb, the frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is very important in determining the overall shape of the digital signal. In the case of the PCA9306 device, digital clock frequency of >100 MHz can be achieved.

The PCA9306 device does not provide any drive capability like the PCA9515 or PCA9517 series of devices. Therefore, higher-frequency applications require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the PCA9306 device is being driven by standard CMOS push-pull output driver. Ideally, it is best to minimize the trace length from the PCA9306 device on the sink side (1.8 V) to minimize signal degradation.

You can then use a simple formula to compute the maximum *practical* frequency component or the *knee* frequency ( $f_{knee}$ ). All fast edges have an infinite spectrum of frequency components. However, there is an inflection (or *knee*) in the frequency spectrum of fast edges where frequency components higher than  $f_{knee}$  are insignificant in determining the shape of the signal.

To calculate  $f_{knee}$ :

$$f_{knee} = 0.5 / RT \text{ (10\%–90\%)} \quad (7)$$

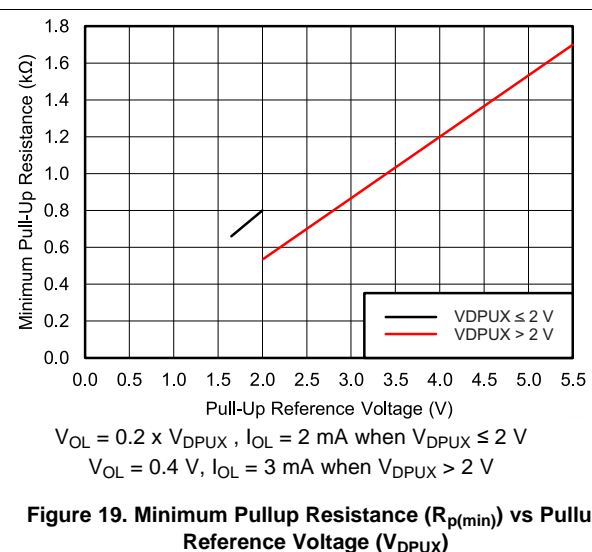
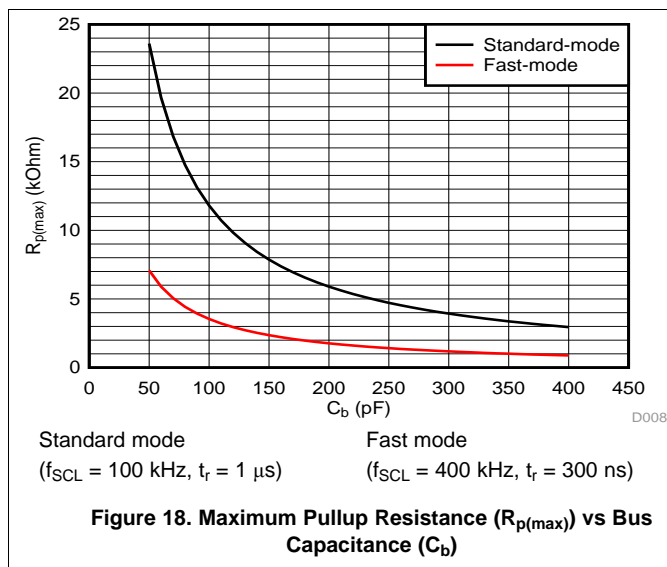
$$f_{knee} = 0.4 / RT \text{ (20\%–80\%)} \quad (8)$$

For signals with rise-time characteristics based on 10- to 90-percent thresholds,  $f_{knee}$  is equal to 0.5 divided by the rise time of the signal. For signals with rise-time characteristics based on 20- to 80-percent thresholds, which is very common in many current device specifications,  $f_{knee}$  is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that help maximize the performance of the device:

- Keep trace length to a minimum by placing the PCA9306 device close to the I<sup>2</sup>C output of the processor.
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pullup resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected.

### 9.2.3 Application Curve



## 10 Power Supply Recommendations

For supplying power to the PCA9306 device, the  $V_{REF1}$  pin can be connected directly to a power supply. The  $V_{REF2}$  pin must be connected to the  $V_{DDU}$  power supply through a 200-k $\Omega$  resistor. Failure to have a high-impedance resistor between  $V_{REF2}$  and  $V_{DDU}$  results in excessive current draw and unreliable device operation. It is also worth noting, that in order to support voltage translation, the PCA9306 must have the EN and VREF2 pins shorted and then pulled up to  $V_{DDU}$  through a high-impedance resistor.

## 11 Layout

### 11.1 Layout Guidelines

For printed-circuit board (PCB) layout of the PCA9306 device, common PCB layout practices should be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other on leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. The 100-pF filter capacitor should be placed as close to  $V_{REF2}$  as possible. A larger decoupling capacitor can also be used, but a longer time constant of two capacitors and the 200-k $\Omega$  resistor results in longer turnon and turnoff times for the PCA9306 device. These best practices are shown in Figure 20.

For the layout example provided in Figure 20, it would be possible to fabricate a PCB with only two layers by using the top layer for signal routing and the bottom layer as a split plane for power ( $V_{CC}$ ) and ground (GND). However, a four-layer board is preferable for boards with higher-density signal routing. On a four-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface-mount component pad, which must attach to  $V_{CC}$  or GND, and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace must be routed to the opposite side of the board, but this technique is not demonstrated in Figure 20.

### 11.2 Layout Example

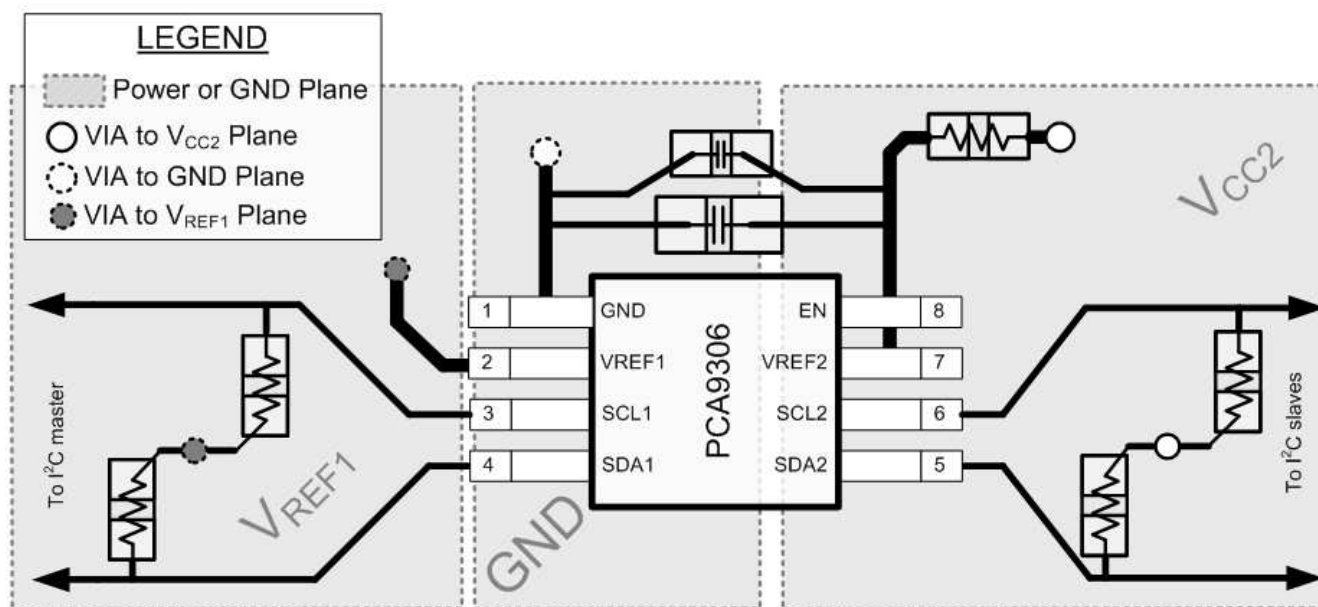


Figure 20. PCA9306 Layout Example

## 12 器件和文档支持

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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### 12.5 术语表

**SLYZ022** — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是适用于指定器件的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航面板。

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## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9306DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BD (S, Y)	<a href="#">Samples</a>
PCA9306DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BD (S, Y)	<a href="#">Samples</a>
PCA9306DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BD (S, Y)	<a href="#">Samples</a>
PCA9306DCTT	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BD (S, Y)	<a href="#">Samples</a>
PCA9306DCTTE4	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BD (S, Y)	<a href="#">Samples</a>
PCA9306DCTTG4	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BD (S, Y)	<a href="#">Samples</a>
PCA9306DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	(7BDP, 7BDS, BD) 7Y	<a href="#">Samples</a>
PCA9306DCURE4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BDS	<a href="#">Samples</a>
PCA9306DCURG4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BDS	<a href="#">Samples</a>
PCA9306DCUT	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	(7BDP, 7BDS, BD) 7Y	<a href="#">Samples</a>
PCA9306DCUTE4	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BDS	<a href="#">Samples</a>
PCA9306DCUTG4	ACTIVE	VSSOP	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	7BDS	<a href="#">Samples</a>
PCA9306DQER	ACTIVE	X2SON	DQE	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(3M, 7F)	<a href="#">Samples</a>
PCA9306YZTR	ACTIVE	DSBGA	YZT	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7F	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9306DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
PCA9306DCTT	SM8	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
PCA9306DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.05	3.3	1.0	4.0	8.0	Q3
PCA9306DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
PCA9306DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
PCA9306DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
PCA9306DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
PCA9306DQER	X2SON	DQE	8	5000	180.0	9.5	1.15	1.6	0.5	4.0	8.0	Q1
PCA9306YZTR	DSBGA	YZT	8	3000	180.0	8.4	1.02	2.02	0.75	4.0	8.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9306DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
PCA9306DCTT	SM8	DCT	8	250	182.0	182.0	20.0
PCA9306DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
PCA9306DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
PCA9306DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
PCA9306DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
PCA9306DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
PCA9306DQER	X2SON	DQE	8	5000	184.0	184.0	19.0
PCA9306YZTR	DSBGA	YZT	8	3000	182.0	182.0	20.0

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



## NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

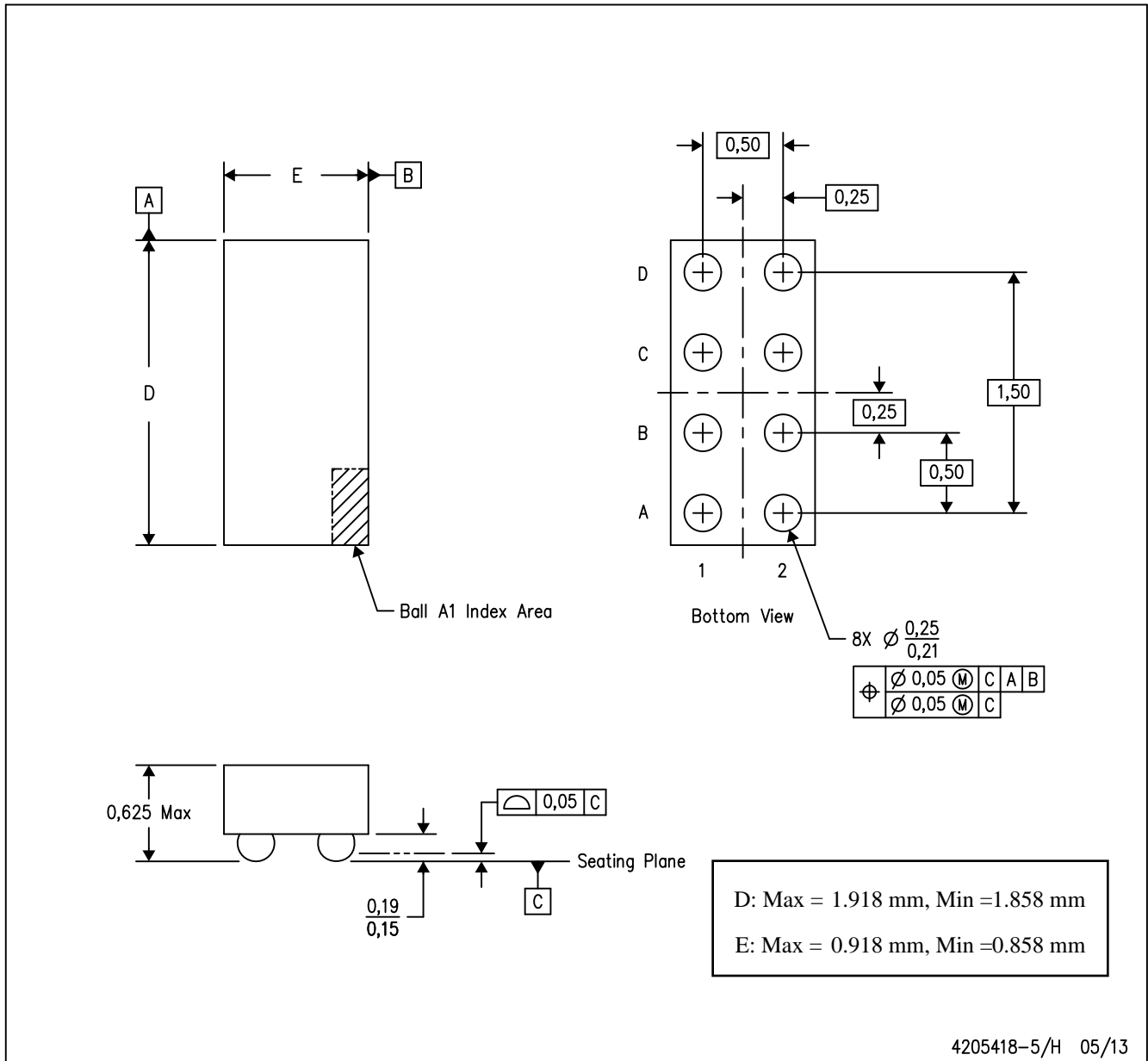
PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZT (R-XBGA-N8)

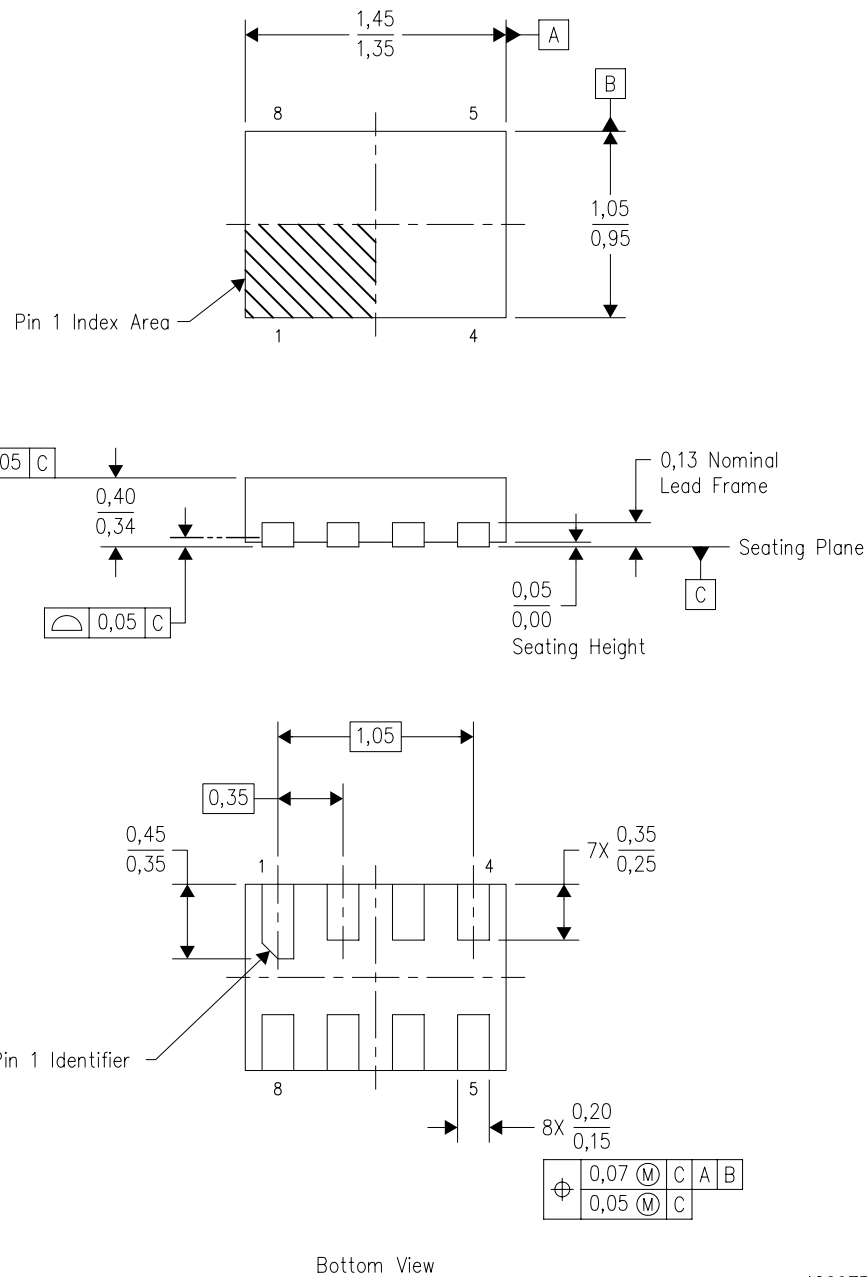
DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

DQE (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

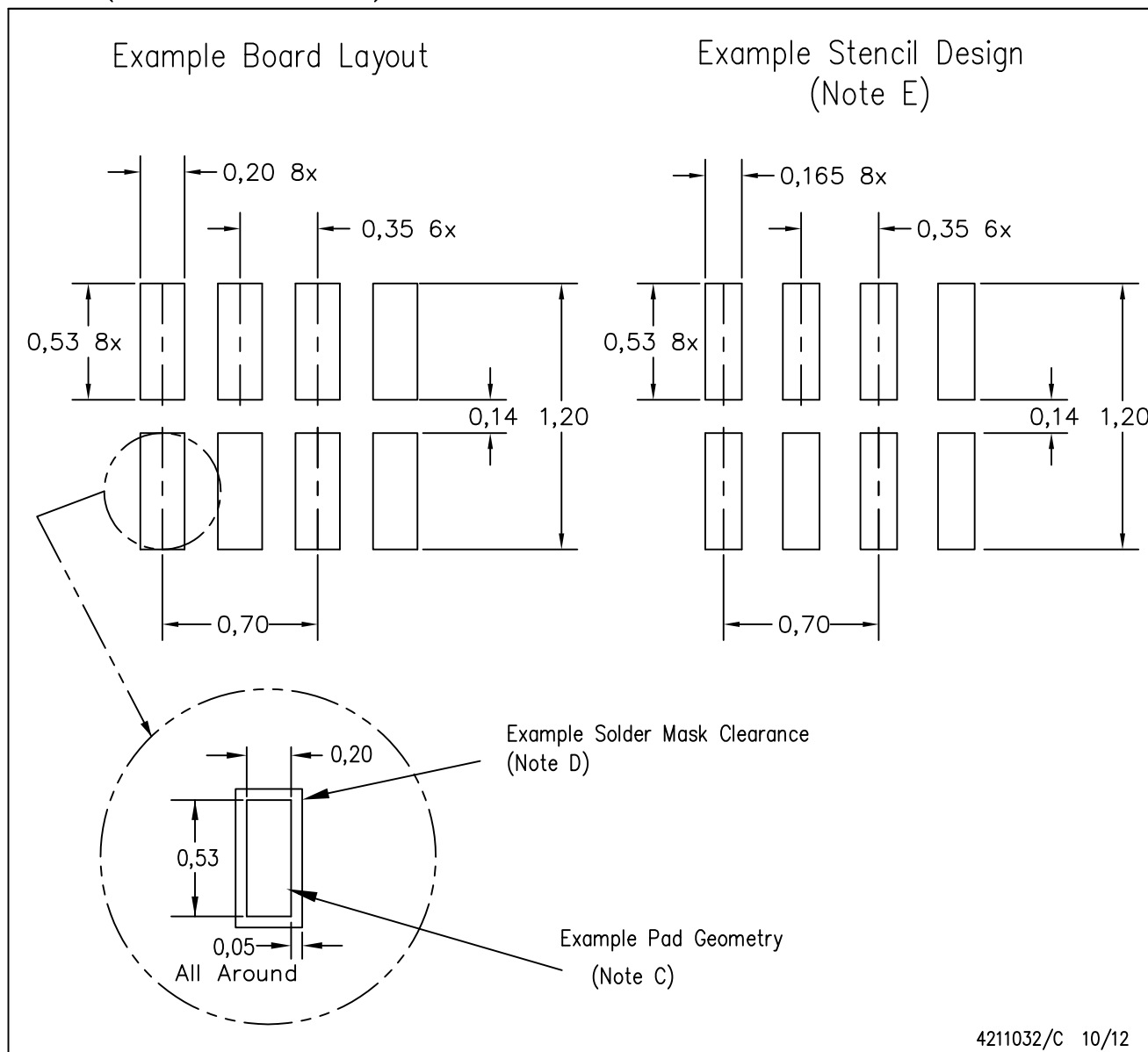


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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - D. This package complies to JEDEC MO-287 variation X2EAF.

DQE (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.  
If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
  - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Over-printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
  - H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
  - I. Component placement force should be minimized to prevent excessive paste block deformation.

## DCT (R-PDSO-G8)

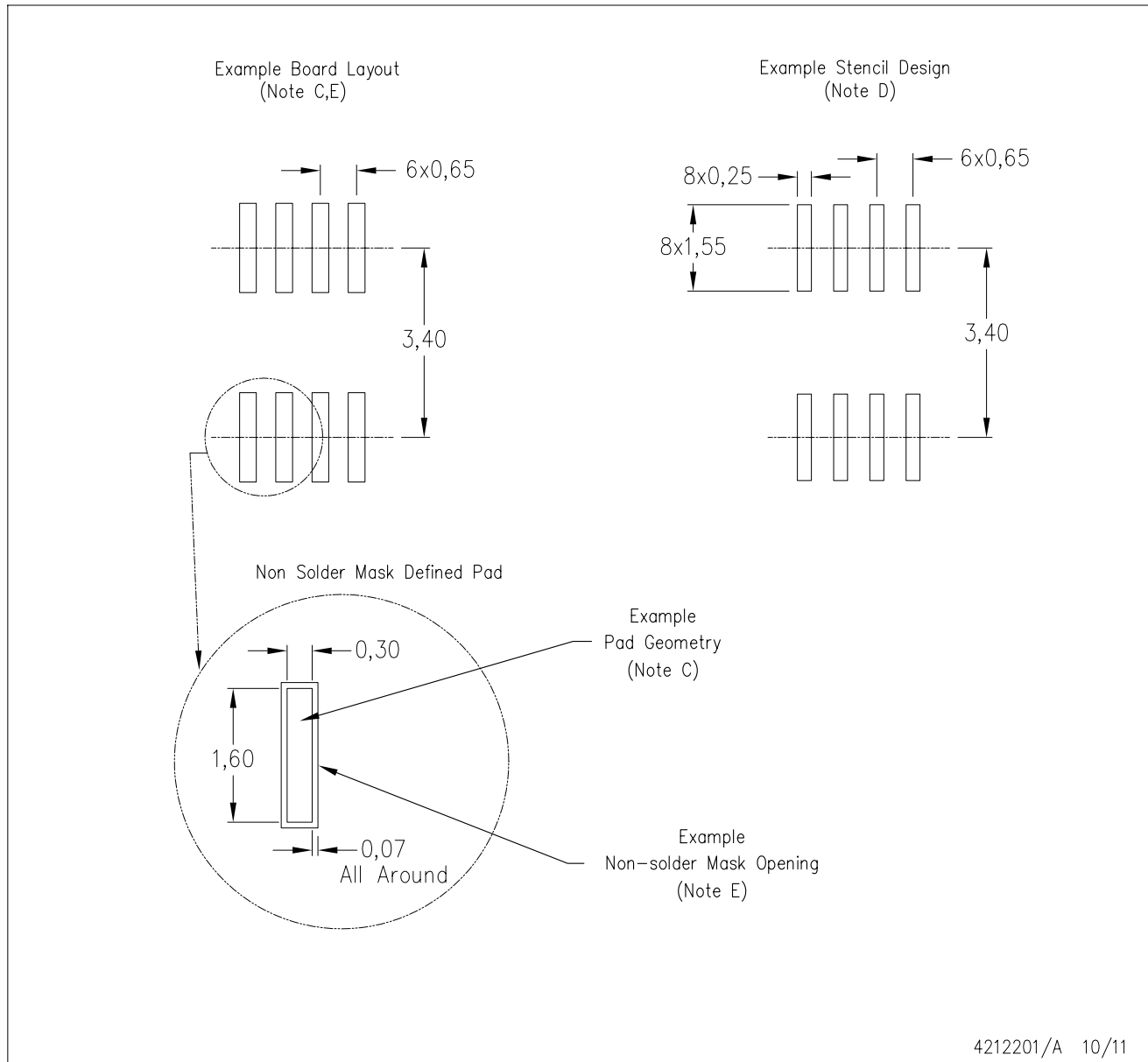
## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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