CY7C271
CY7C274

32K x 8 Power Switched and Reprogrammable PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 30 ns (Commercial)**
  - **— 35 ns (Military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 715 mW (military)**
- **Super low standby power**
  - **— Less than 165 mW when deselected**
- **EPROM technology 100% programmable**
- **Slim 300-mil package (7C271)**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

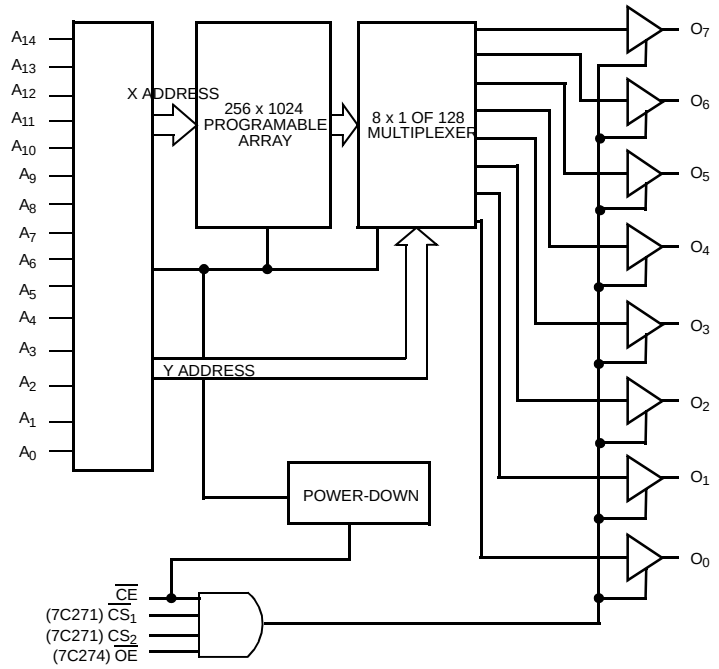
Functional Description

The CY7C271 and CY7C274 are high-performance 32,768-word by 8-bit CMOS PROMs. When disabled ($\overline{CE}$ HIGH), the 7C271/7C274 automatically powers down into a low-power stand-by mode. The CY7C271 is packaged in the 300-mil slim package. The CY7C274 is packaged in the industry standard 600-mil package. Both the CY7C271 and CY7C274 are available in a cerDIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C271 and CY7C274 offer the advantage of lower power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

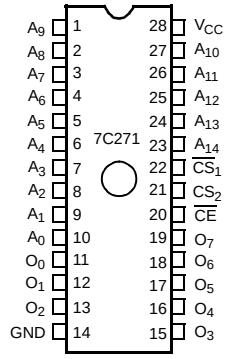
Reading the 7C271 is accomplished by placing active LOW signals on $\overline{CS_1}$ and $\overline{CE}$, and an active HIGH on CS_2. Reading the 7C274 is accomplished by placing active LOW signals on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines (A_0–A_{14}) will become available on the output lines (O_0–O_7).

Logic Block Diagram

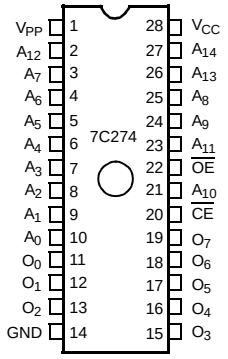


Pin Configurations

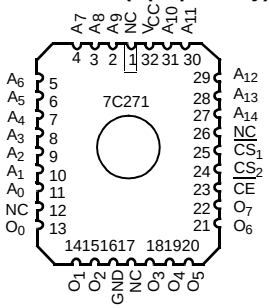
DIP/Flatpack



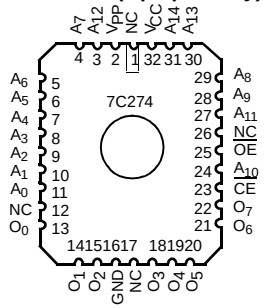
DIP/Flatpack



LCC/PLCC (Opaque Only)



LCC/PLCC (Opaque Only)



Selection Guide

		7C274-30	7C271-35 7C274-35	7C271-45 7C274-45	7C271-55	Unit
Maximum Access Time		30	35	45	55	ns
Maximum Operating Current	Com'l	120	120	120	120	mA
	Military		130	130	130	mA
Standby Current	Com'l	30	30	30	30	mA
	Military		40	40	40	mA

Maximum Ratings[1]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[2]	–55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[3]

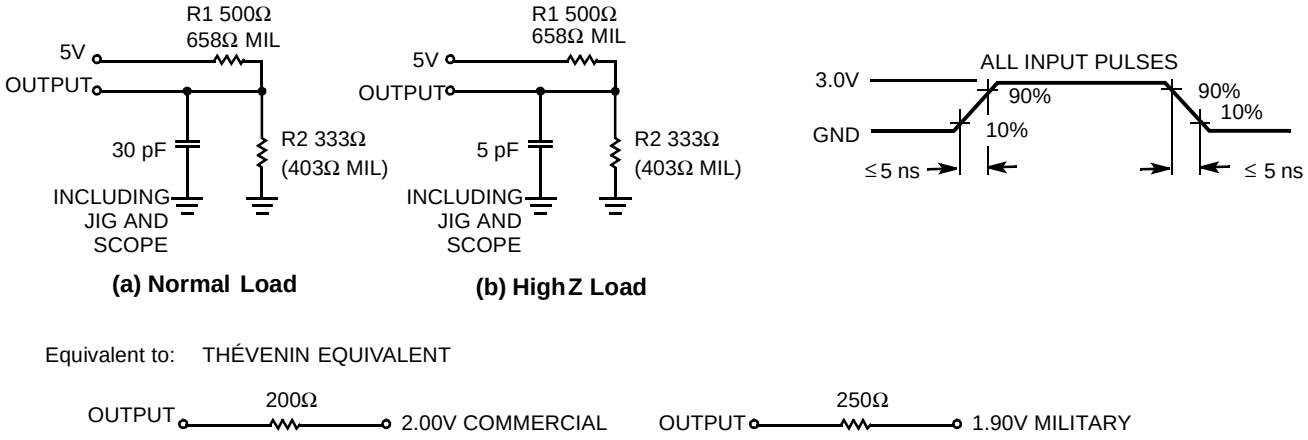
Parameter	Description	Test Conditions		7C271- 35, 45, 55 7C274-30, 35, 45,		Unit
				Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA[4]			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–40	+40	µA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		–20	–90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V, I_{OUT} = 0 mA, $\overline{CE}$=V_{IL}	Commercial		120	mA
			Military		130	
I_{SB}	Standby Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}, I_{OUT} = 0 mA	Commercial		30	mA
			Military		40	
V_{PP}	Programming Supply Voltage			12	13	V
I_{PP}	Programming Supply Current				50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4	V

Notes:
1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. 6.0 mA military
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms[6]

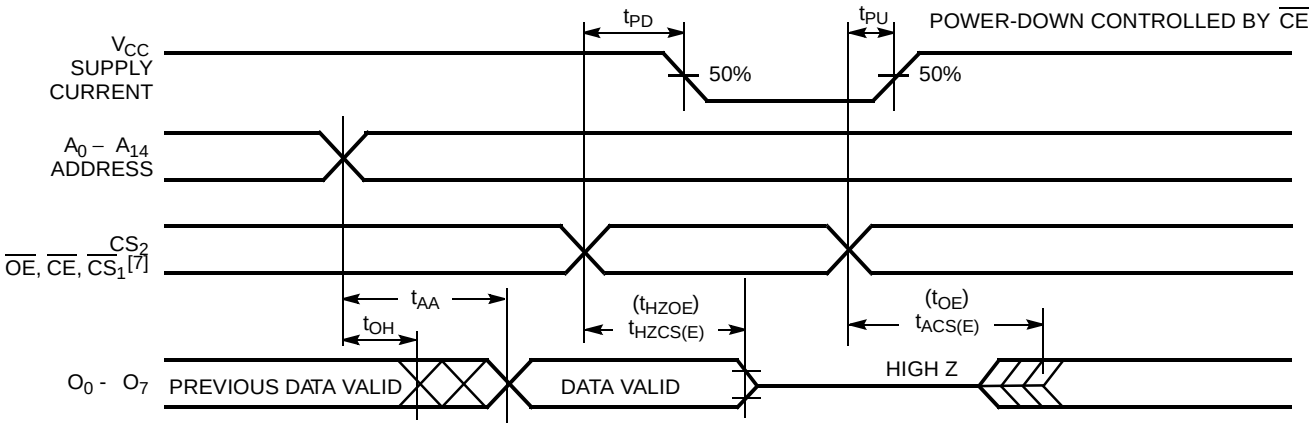


Switching Characteristics Over the Operating Range[3,6]

Parameter	Description	7C274-30		7C271-35 7C274-35		7C271-45 7C274-45		7C271-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		30		35		45		55	ns
t_{HZCS}	Chip Select Inactive to High Z ($\overline{CS}_1$ and CS_2, 7C271 Only)		20		25		30		30	ns
t_{ACS}	Chip Select Active to Output Valid ($\overline{CS}_1$ and CS_2, 7C271 Only)		20		25		30		30	ns
t_{HZOE}	Output Enable Inactive to High Z ($\overline{OE}$, 7C274 Only)		20		20		25		25	ns
t_{OE}	Output Enable Active to Output Valid ($\overline{OE}$, 7C274 Only)		20		20		25		25	ns
t_{HZCE}	Chip Enable Inactive to High Z ($\overline{CE}$ Only)		35		40		50		60	ns
t_{ACE}	Chip Enable Active to Output Valid ($\overline{CE}$ Only)		35		40		50		60	ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		35		40		50		60	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Note:
6. See Introduction to CMOS PROMs for general information on testing.

Switching Waveform



Note:
7. CS_2 and $\overline{CS_1}$ are used on the 7C271 only. $\overline{OE}$ is used on the 7C274 only.

Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the CY7C271 and CY7C274 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY7C271 or CY7C274 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. CY7C271 Mode Selection

		Pin Function[8]				
	Read or Output Disable	**A_{14}–A_0**	**CE**	**CS_2**	**CS_1**	**O_7–O_0**
Mode	**Other**	**A_{14}–A_0**	**VFY**	**PGM**	**V_{PP}**	**D_7–D_0**
Read		A_{14}–A_0	V_{IL}	V_{IH}	V_{IL}	O_7–O_0
Power Down		A_{14}–A_0	V_{IH}	X	X	High Z
Output Disable		A_{14}–A_0	X	V_{IL}	X	High Z
Output Disable		A_{14}–A_0	X	X	V_{IH}	High Z
Program		A_{14}–A_0	V_{IHP}	V_{ILP}	V_{PP}	D_7–D_0
Program Verify		A_{14}–A_0	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	O_7–O_0
Program Inhibit		A_{14}–A_0	V_{IHP}	V_{IHP}	V_{PP}	High Z
Blank Check		A_{14}–A_0	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	O_7–O_0

Table 2. CY7C274 Mode Selection

Mode		Pin Function[8]				
	Read or Output Disable	A_{14}–A_0	OE	CE	V_{PP}	O_7–O_0
	Other	A_{14}–A_0	VFY	PGM	V_{PP}	D_7–D_0
Read		A_{14}–A_0	V_{IL}	V_{IL}	Note 9	O_7–O_0
Output Disable		A_{14}–A_0	V_{IH}	X	X	High Z
Power Down		A_{14}–A_0	X	V_{IH}	X	High Z
Program		A_{14}–A_0	V_{IHP}	V_{ILP}	V_{PP}	D_7–D_0
Program Verify		A_{14}–A_0	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	O_7–O_0
Program Inhibit		A_{14}–A_0	V_{IHP}	V_{IHP}	V_{PP}	High Z
Blank Check		A_{14}–A_0	V_{ILP}	V_{IHP}/V_{ILP}	V_{PP}	O_7–O_0

Note:
8. X can be V_{IL} (V_{ILP}) or V_{IH} (V_{IHP}).
9. V_{PP} should be tied to V_{CC} ±5% in read mode.

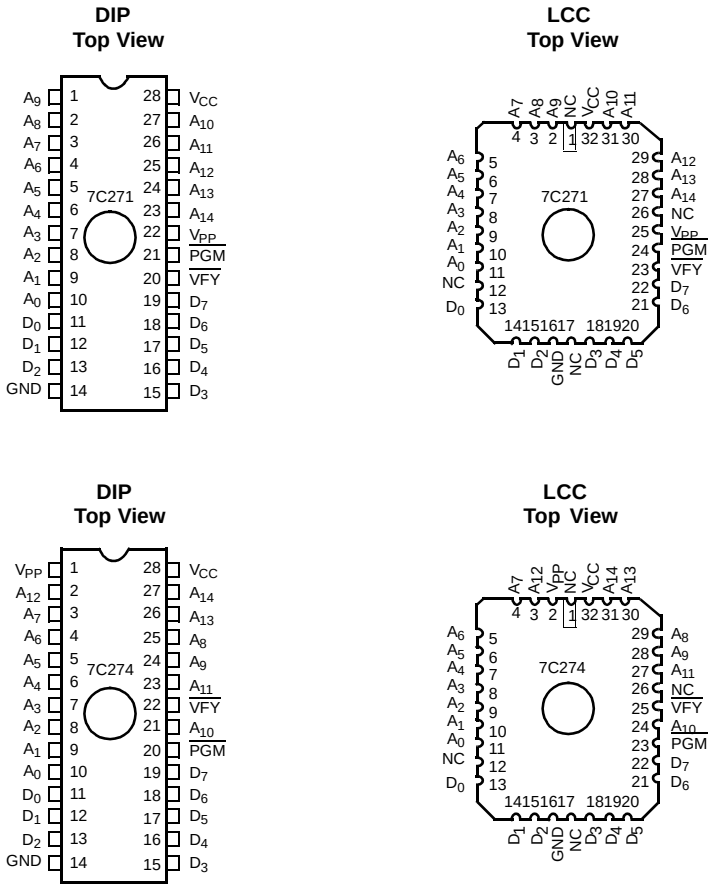
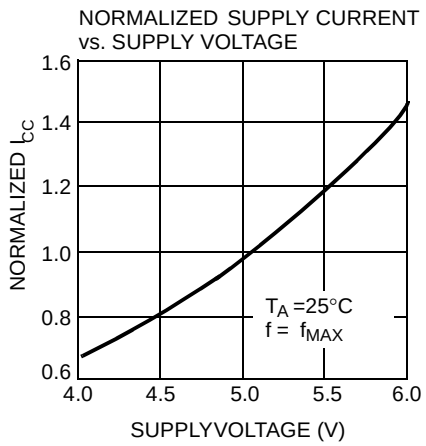
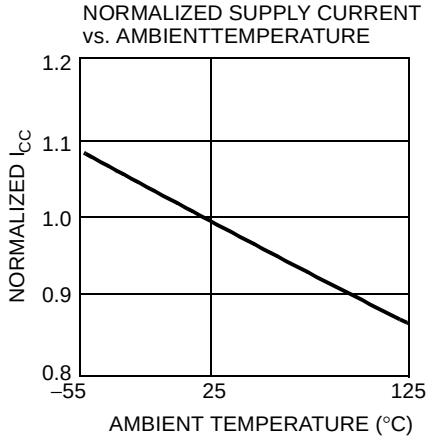
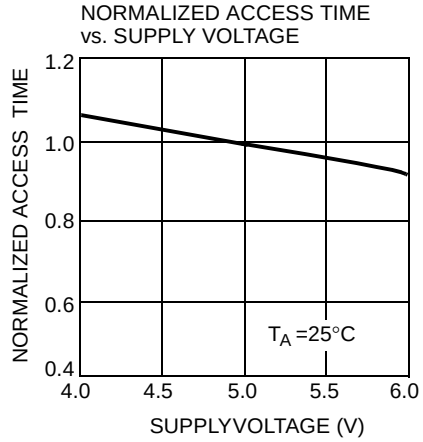


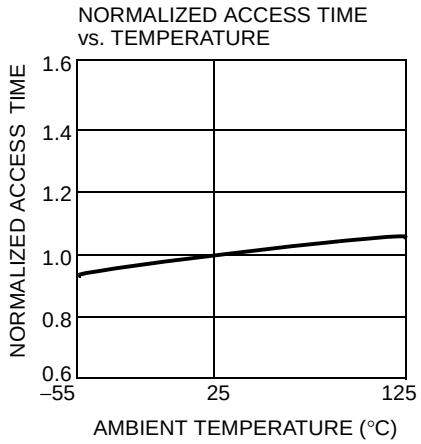
Figure 1. Programming Pinouts

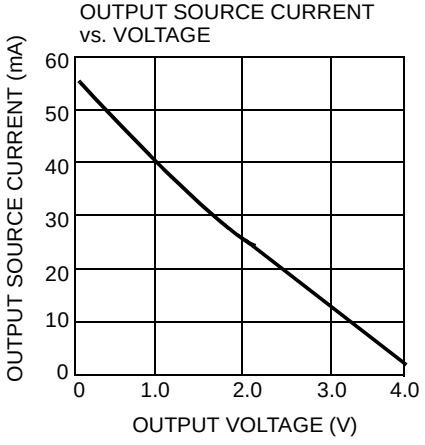
Typical DC and AC Characteristics

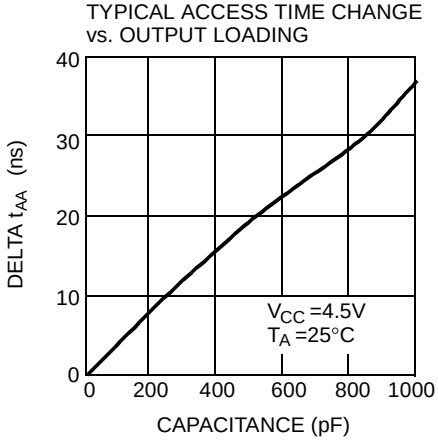


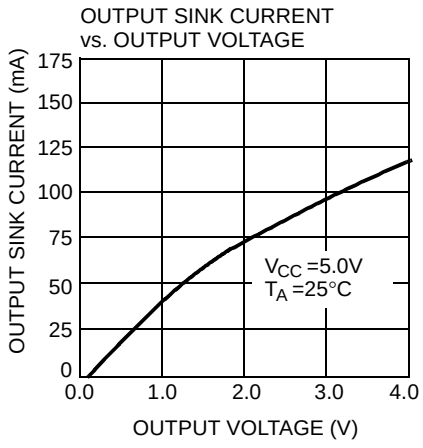


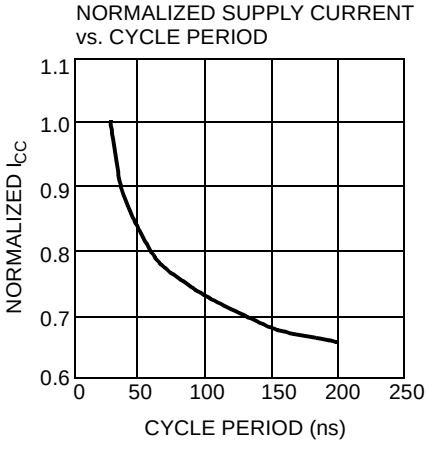












C271-14

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
30	CY7C274-30WC	W16	28-Lead (600-Mil) Windowed CerDIP	Commercial
35	CY7C271-35WMB	W22	28-Lead (300-Mil) Windowed CerDIP	Military
	CY7C274-35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
45	CY7C271-45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C271-45WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C274-45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C274-45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	Military
55	CY7C271-55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C271-55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS}[10]	7, 8, 9, 10, 11
t_{OE}[11]	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11

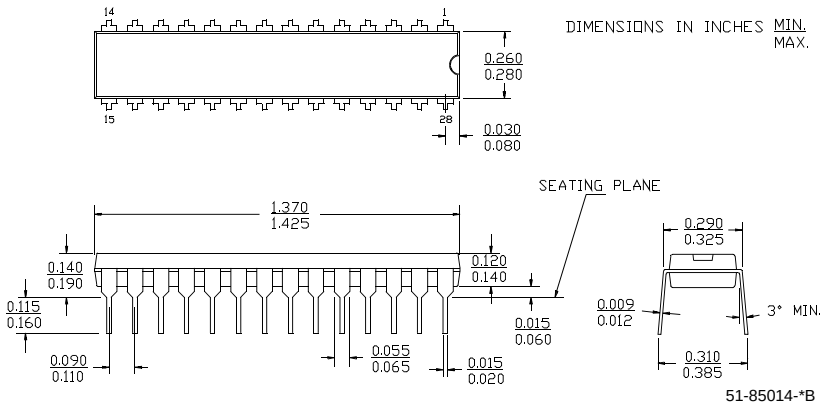
Note:
10. 7C271 only ($\overline{CS}_1$ and CS_2).
11. 7C274 only.

SMD Cross Reference

SMD Number	Suffix	Cypress Number
5962-89817	01ZX	CY7C271-55QMB
5962-89817	02XX	CY7C271-45WMB
5962-89817	02ZX	CY7C271-45QMB

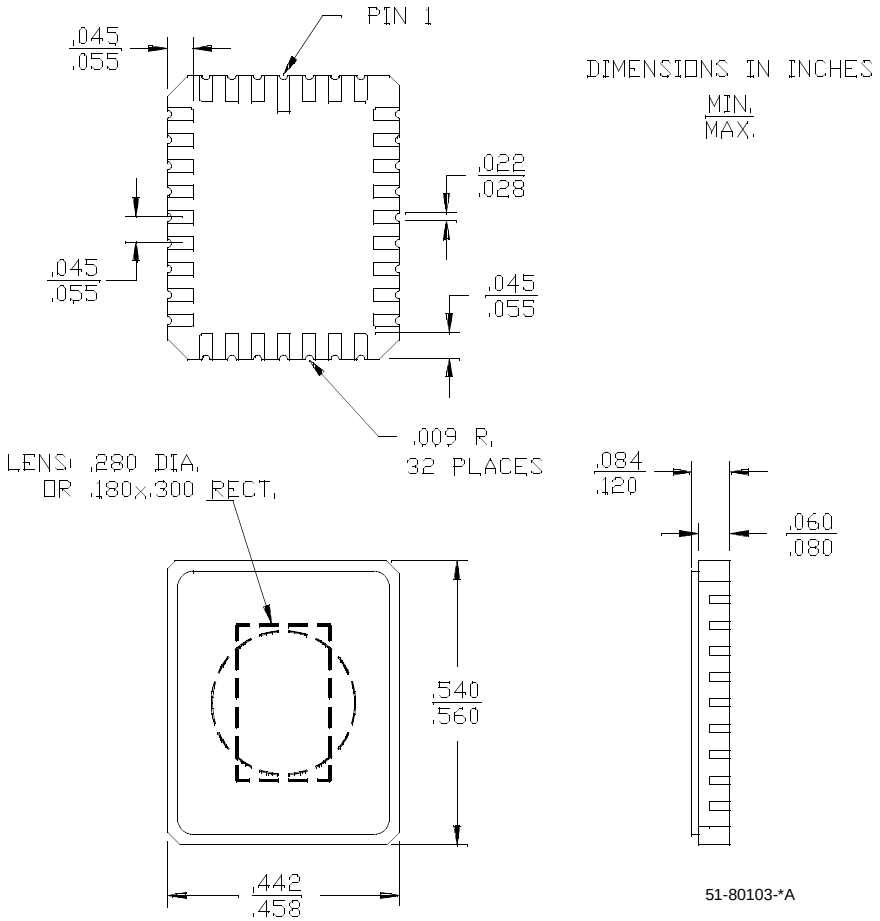
Package Diagrams

28-Lead (300-Mil) Molded DIP P21



51-85014-*B

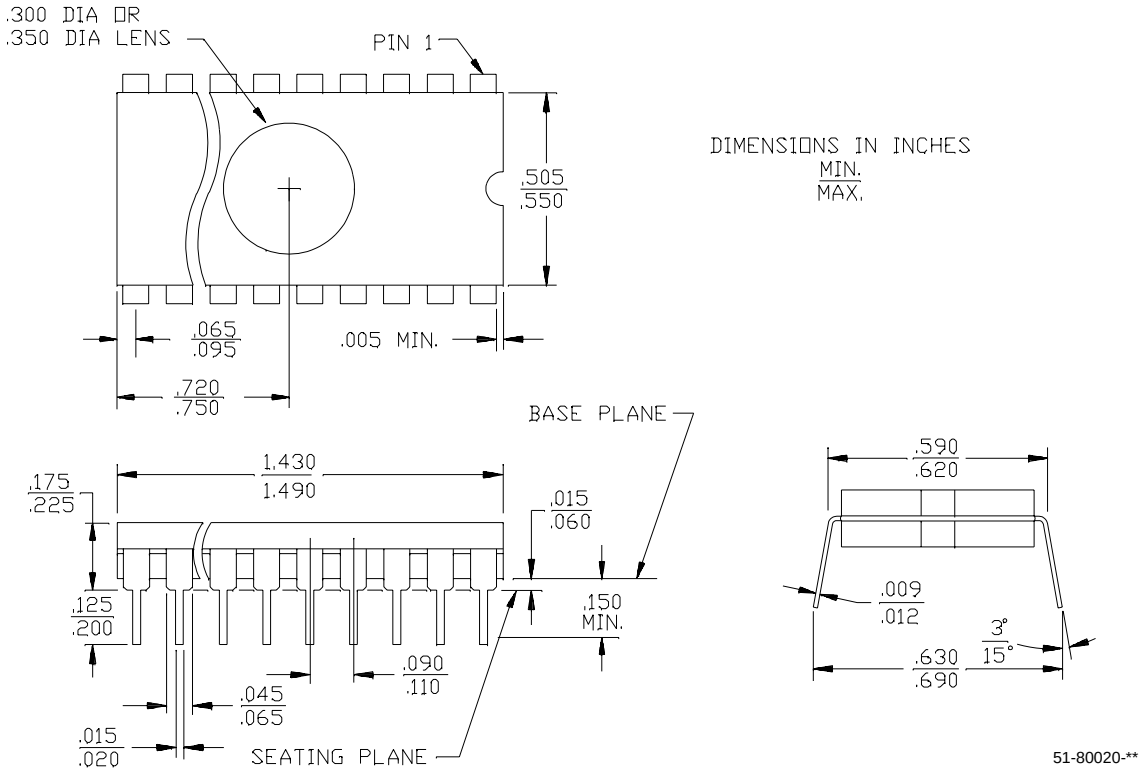
32-Pin Windowed Rectangular Leadless Chip Carrier Q55
MIL-STD-1835 C-12



51-80103-*A

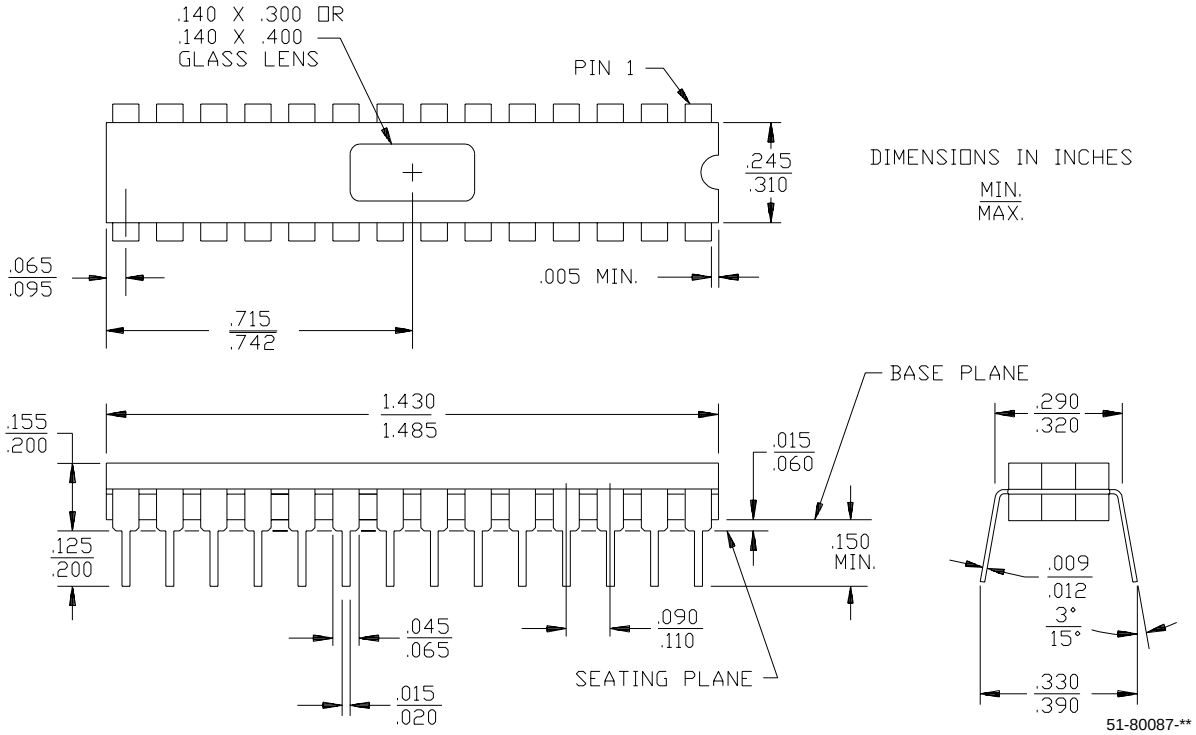
Package Diagrams (continued)

28-Lead (600-Mil) Windowed CerDIP W16
MIL-STD-1835 D-10 Config. A



Package Diagrams (continued)

28-Lead (300-Mil) Windowed CerDIP W22
MIL-STD-1835 D-15 Config. A



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Document History Page

Document Title: CY7C271 CY7C274 32K x 8 Power Switched and Reprogrammable PROM Document Number: 38-04008				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	113864	3/8/02	DSG	Change from Spec number: 38-00068 to 38-04008
A*	118899	10/10/02	GBI	Updating Ordering Information
*B	122249	12/27/02	RBI	Add power up requirements to Operating Conditions information