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BCM8705 PRODUCT Brief



SERIAL 10-GBE/FIBRE CHANNEL TRANSCEIVER WITH WIS LAYER AND XAUI™ INTERFACE

FEATURES

- **Fully integrated CMU, CDR, SerDes, limiting amplifier, EyeOpener®, and 4-lane XAUI™ interface**
  - PMD interface supported serial rates: 9.953/10.3125/ 10.5188-Gbps
  - Receive equalization on XAUI and 10G serial interfaces
  - Transmit pre-emphasis and amplitude control on XAUI interface
  - 10G PMD interface phase and decision threshold adjust
- **WIS layer for EOS/WAN applications**
- **SONET performance monitoring**
- **Supports Broadcom's StrataXGS® Ethernet switches service aware flow control (SAFC) protocol**
- **Meets and exceeds industry standard**
  - IEEE 802.3™ae serial Ethernet transceiver (LAN/WAN PHY), MDIO Clause 45 management interface with extended indirect address register access
  - 10-Gigabit Fibre Channel draft, rev 3.0
  - Support for XFP/XFI interfaces
  - Support for XENPAK/X2 3.0 and XPAK MSA optical module standards
- **Additional features**
  - Jumbo packets support in WAN mode
  - Reference clock output for XFP module reference clock
  - I^2C master to control XFP module from device
  - Staged power-up mode to minimize in-rush current
  - Loopback modes supporting IEEE standards modes
  - Built-in self-test (BIST) and PRBS generator/checker
- **Pin-compatible with the BCM8704**
- **Low power: LAN mode 900 mW, WAN mode 1.0W to 1.1W**
- **Available in 13-mm x 13-mm and 17-mm x 17-mm plastic BGA (Pb-free version also available)**

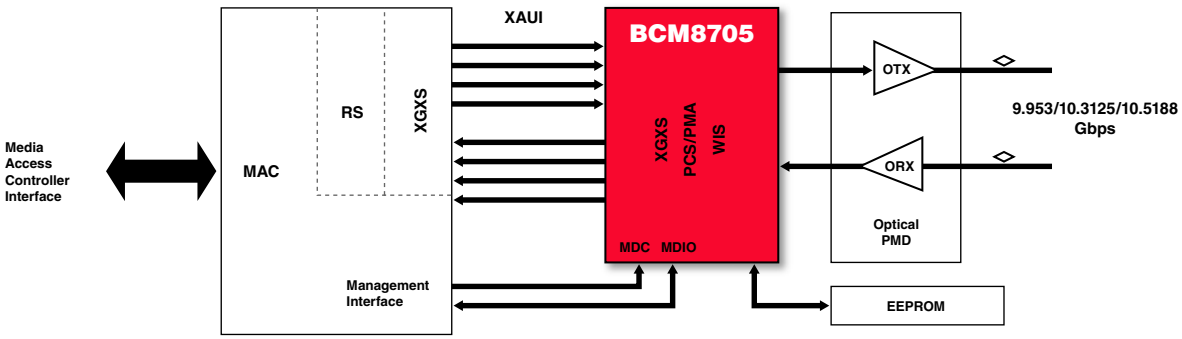
SUMMARY OF BENEFITS

- **Best performance for LAN (10-GbE) and WAN (OC-192 SONET) application**
- **Universal design for 10-GbE, SONET, and 10 GFC for XENPAK/X2 module**
  - Compliant to XENPAK/X2 3.0 and XPAK MSA optical module standards
- **Integrated and compact design allows for high-density line card applications**
- **Upgrade path for existing Broadcom LAN PHY transceivers**
- **Build-in features reduce external components**
  - Clean-up PLL
  - 2.5V voltage regulator output
  - In-rush current limits

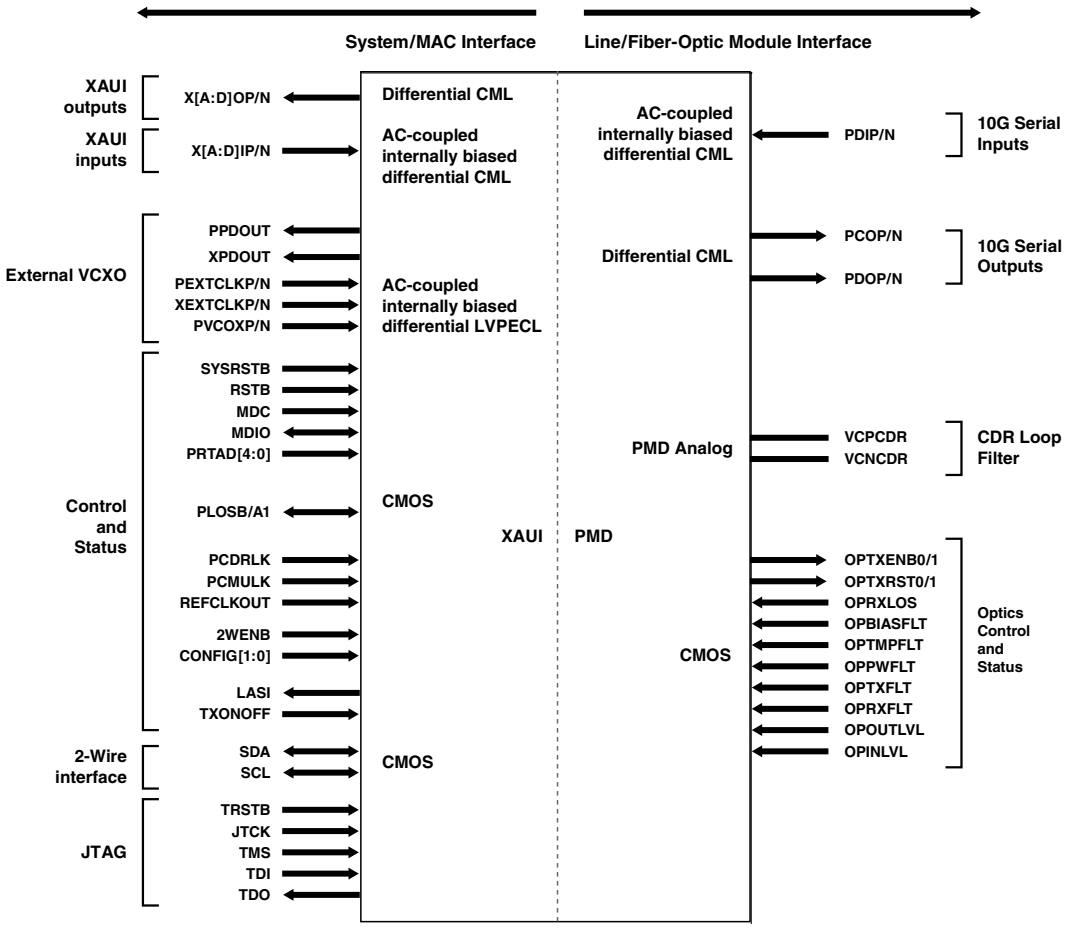
APPLICATIONS

- **XENPAK, X2, XPAK modules**
- **Interface to XFP modules**
- **LAN/MAN/WAN switch/routers**
- **Hubs and repeaters**
- **Network interface cards (NICs)**

BCM8705 Block Diagram



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BCM8705 Fully Integrated Interface

The BCM8705 Ethernet/Fibre Channel/SONET LAN/WAN PHY is a fully integrated serialization/deserialization (9.953/10.3125/10.5188-Gbps) interface device performing the extension functions for a 10-gigabit serial Ethernet reconciliation sublayer (RS) interface. The XGXS, PCS, and PMA functions include 8B/10B coding, 64B/66B coding, SerDes, WIS, clock multiplication unit (CMU), and clock and data recovery (CDR).

For WAN applications, a WIS-compliant framer with flexible clocking modes allows transmission of Ethernet traffic over a WAN network.

On-chip clock synthesis is performed by the high-frequency low-jitter phase-locked loops for the PMD and XAUI output retimers. Individual PMD and XAUI clock recovery is performed on the device by synchronizing directly to their respective incoming data streams. Elastic buffers are provided to allow the XAUI and PMD interfaces to operate in asynchronous configuration. Only an external 155.52/156.25/159.38-MHz oscillator is required for the reference clock input.

The BCM8705 is available in a 13-mm × 13-mm, 256-pin FBGA with a 0.8-mm ball pitch and also in a 17-mm x 17-mm, 256-pin 1-mm ball pitch RoHS-compliant package.

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