MAX3243 具有 ±15-kV ESD (HBM) 保护的 3V 至 5.5V 多通道 RS-232 线路驱动器/接收器

1 特性

- 由 3V 至 5.5V V_{CC} 电源供电
- 用于 IBM™ PC/AT™ 串行端口的单芯片和单电源接口
- 使用人体放电模型 (HBM) 时，RS-232 总线引脚 ESD 保护为 ±15kV
- 符合或超出 TIA/EIA-232-F 和 ITU V.28 标准的要求
- 三个驱动器和五个接收器
- 速率高达 250kbit/s
- 低活动电流：300 µA（典型值）
- 低待机电流：1 µA（典型值）
- 外部电容器：4 × 0.1 µF
- 接受 5V 逻辑输入及 3.3V 电源
- 始终有效同相接收器输出 (ROUT2B)
- 工作温度
  - MAX3243C：0°C 至 70°C
  - MAX3243I：–40°C 至 85°C
- 串行鼠标驱动能力
- 自动断电功能，在没有检测到有效 RS-232 信号时禁用驱动器输出

2 应用

- 电池供电型系统
- 平板电脑
- 笔记本电脑
- 便携式计算机
- 手持设备

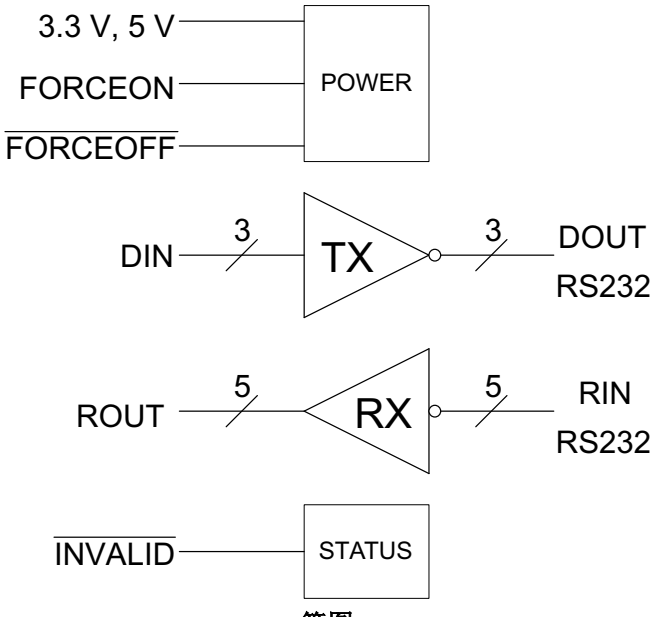
3 说明

MAX3243 器件包含三个线路驱动器和五个线路接收器，非常适合用于 DE-9 DTE 接口。引脚对引脚（串行端口连接引脚，包括 GND）±15kV ESD (HBM) 保护。灵活的电源功能可自动省电。特殊输出 ROUT2B 和 INVALID 始终启用，以检查振铃指示灯和有效的 RS232 输入。

器件信息

器件型号	封装(1)	封装尺寸
MAX3243	SSOP (28)	10.29 mm × 5.30 mm
	SOIC (28)	17.90mm × 7.50mm
	TSSOP (28)	9.70mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简图

Table of Contents

4 Revision History

Changes from Revision O (January 2015) to Revision P (October 2022) **Page**

- Changed the *Thermal Information* table 5
- Changed the MAX value of I_{CC} Supply current auto-powerdown disabled from 1 mA to 1.2 mA in *Electrical Characteristics—Auto Power Down* 5

Changes from Revision N (May 2009) to Revision O (January 2015) **Page**

- 添加了*应用*、*器件信息* 表、*引脚功能* 表、*ESD* 等级 表、*热性能信息* 表、*典型特性*、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械*、*封装和可订购信息* 部分 1
- 删除了*订购信息*表 1

5 Pin Configuration and Functions

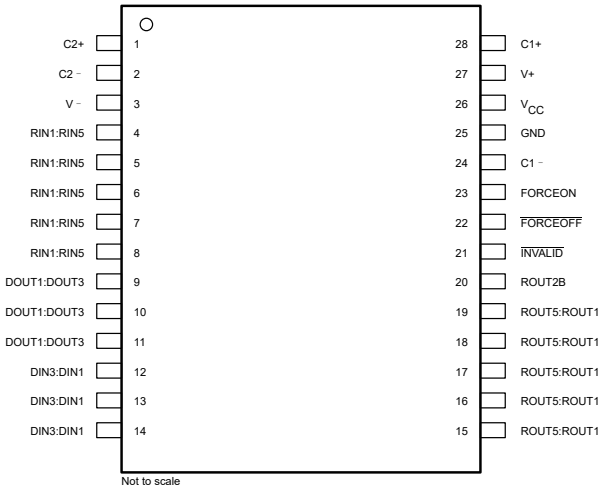


图 5-1. DB, DW, or PW Package (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C2+	1	—	Positive lead of C2 capacitor
C2 –	2	—	Negative lead of C2 capacitor
V –	3	O	Negative charge pump output for storage capacitor only
RIN1:RIN5	4, 5, 6, 7, 8	I	RS232 line data input (from remote RS232 system)
DOUT1:DOUT3	9, 10, 11	O	RS232 line data output (to remote RS232 system)
DIN3:DIN1	12, 13, 14	I	Logic data input (from UART)
ROUT5:ROUT1	15, 16, 17, 18, 19	O	Logic data output (to UART)
ROUT2B	20	O	Always Active non-inverting output for RIN2 (normally used for ring indicator)
$\overline{\text{INVALID}}$	21	O	Active low output when all RIN are unpowered
$\overline{\text{FORCEOFF}}$	22	I	Low input forces DOUT1-5, ROUT1-5 high Z per 节 8.4
FORCEON	23	I	High forces drivers on. Low is automatic mode per 节 8.4
C1 –	24	—	Negative lead on C1 capacitor
GND	25	—	Ground
V_{CC}	26	—	Supply Voltage, Connect to 3V to 5.5V power supply
V+	27	O	Positive charge pump output for storage capacitor only
C1+	28	—	Positive lead of C1 capacitor

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive output supply voltage range(2)		–0.3	7	V
V–	Negative output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Driver, $\overline{\text{FORCEOFF}}$, FORCEON	–0.3	6	V
		Receiver	–25	25	
V_O	Output voltage range	Driver	–13.2	13.2	V
		Receiver, $\overline{\text{INVALID}}$	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

6.2 ESD Ratings

			MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 RIN , DOUT, and GND pins (1)	15000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 All other pins(1)	3000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(1) (See 图 9-1)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V_{CC} = 3.3 V	2		5.5	V
			V_{CC} = 5 V	2.4		5.5	
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		0.8	V
V_I	Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature		MAX3243C	0		70	°C
			MAX3243I	–40		85	

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.4 Thermal Information

THERMAL METRIC[1]		DB	DW	PW	UNIT
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.1	59.0	70.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.8	28.8	21.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	30.3	29.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	7.8	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.0	30.0	28.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics – – Auto Power Down

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1] (see 图 9-1)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
I_{CC}	Supply current Auto-powerdown disabled	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}. T_A = 25°C For DB and PW package		0.3	1.2	mA
	Supply current Auto-powerdown disabled	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}. T_A = 25°C For DW package		0.3	1	mA
	Supply current Powered off	No load, $\overline{FORCEOFF}$ at GND. T_A = 25°C		1	10	µA
	Supply current Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded, All DIN are grounded. T_A = 25°C		1	10	
I_I	Input leakage current of $\overline{FORCEOFF}$, FORCEON	V_I = V_{CC} or V_I at GND		±0.01	±1	µA
V_{IT+}	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}			2.7	V
V_{IT-}	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	-2.7			V
V_T	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	-0.3		0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = -1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	V_{CC} - 0.6			V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}			0.4	V

(1) Test conditions are C1 – C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2 – C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.6 Electrical Characteristics – – Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see 图 9-1)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at R_L = 3 kΩ to GND			5	5.4		V
V_{OL}	Low-level output voltage	All DOUT at R_L = 3 kΩ to GND			– 5	– 5.4		V
V_O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V_{CC}, 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA			±5			V
I_{IH}	High-level input current	$V_I = V_{CC}$				±0.01	±1	μA
I_{IL}	Low-level input current	V_I at GND				±0.01	±1	μA
V_{hys}	Input hysteresis						±1	V
I_{OS}	Short-circuit output current(3)	V_{CC} = 3.6 V,	V_O = 0 V			±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V					
r_o	Output resistance	V_{CC}, V+, and V – = 0 V,	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND,	V_O = ±12 V,	V_{CC} = 3 to 3.6 V			±25	μA
			V_O = ±10 V,	V_{CC} = 4.5 to 5.5 V			±25	

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

6.7 Electrical Characteristics – – Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see 图 9-1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OH} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})			0.5		V
I_{off}	Output leakage current (except ROUT2B)	$\overline{FORCEOFF}$ = 0 V		±0.05	±10	μA
r_I	Input resistance	V_I = ±3 V or ±25 V	3	5	7	kΩ

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.8 Switching Characteristics – – Auto Power Down

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 7-5)

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
t_{valid}	Propagation delay time, low- to high-level output	V_{CC} = 5 V	1	μs
$t_{invalid}$	Propagation delay time, high- to low-level output	V_{CC} = 5 V	30	μs
t_{en}	Supply enable time	V_{CC} = 5 V	100	μs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.9 Switching Characteristics – – Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2) (see 图 9-1)
MAX3243C, MAX3243I

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
	Maximum data rate	R_L = 3 kΩ One DOUT switching,	C_L = 1000 pF See 图 7-1	150	250		kbit/s
$t_{sk(p)}$	Pulse skew(3)	R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 2500 pF See 图 7-3		100		ns
SR(tr)	Slew rate, transition region (see 图 7-1)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 1000 pF	6		30	V/ µ s
			C_L = 150 pF to 2500 pF	4		30	

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1 – C4 = 0.1 µ F at V_{CC} = 3.3 V + 0.3 V; C1 = 0.047 µ F, C2 – C4 = 0.33 µ F at V_{CC} = 5 V ± 0.5 V.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6.10 Switching Characteristics – – Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2)

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See 图 7-3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output		150	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See 图 7-4	200	ns
t_{dis}	Output disable time		200	ns
$t_{sk(p)}$	Pulse skew(3)	See 图 7-3	50	ns

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1 – C4 = 0.1 µ F at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µ F, C2 – C4 = 0.33 µ F at V_{CC} = 5 V ± 0.5 V.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6.11 Typical Characteristics

V_{CC} = 3.3 V

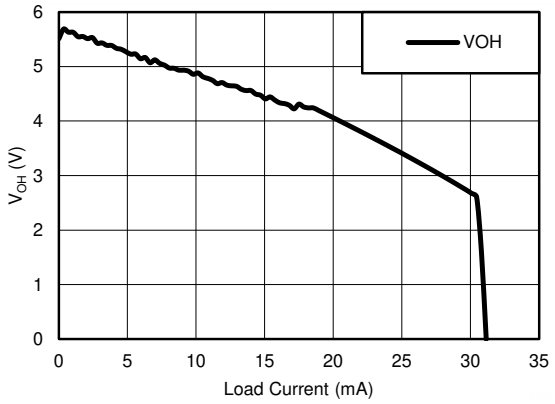


图 6-1. DOUT VOH vs Load Current

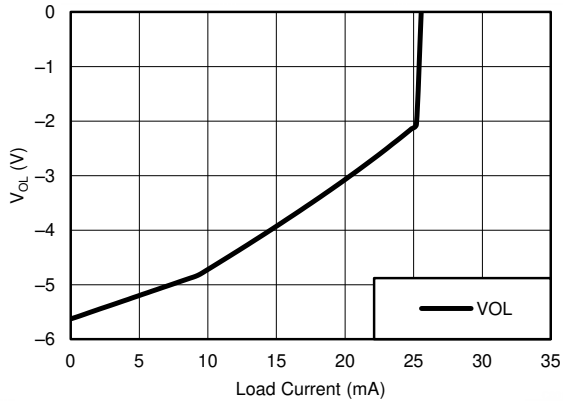
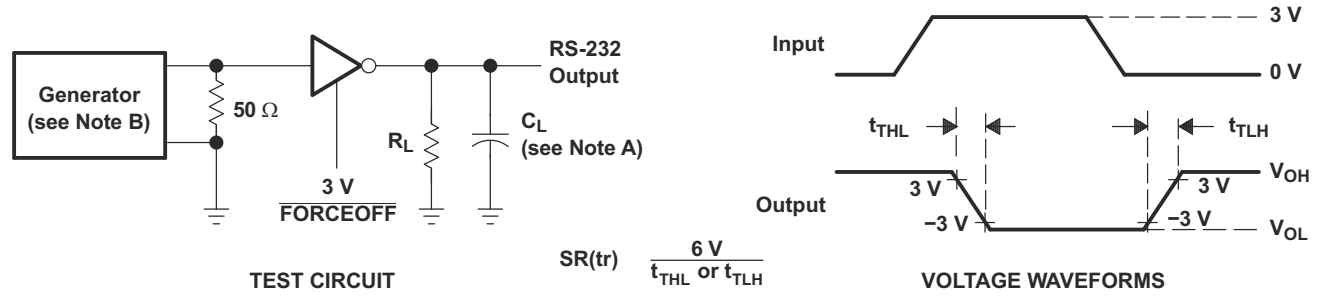


图 6-2. DOUT VOL vs Load Current

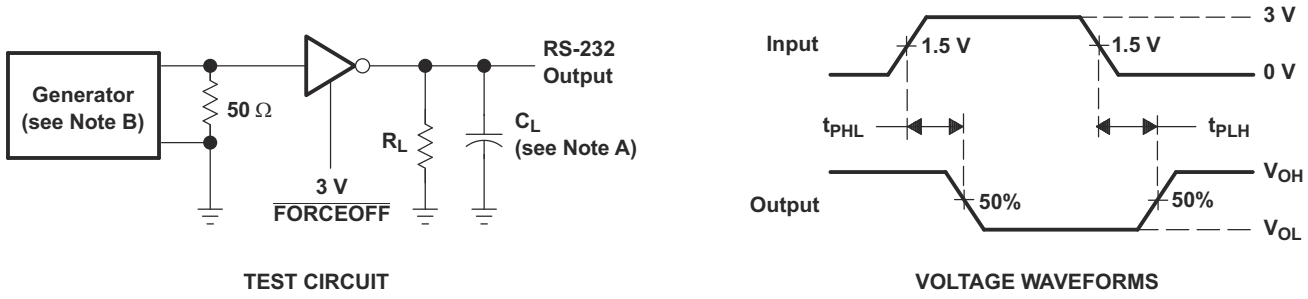
7 Parameter Measurement Information

7.1



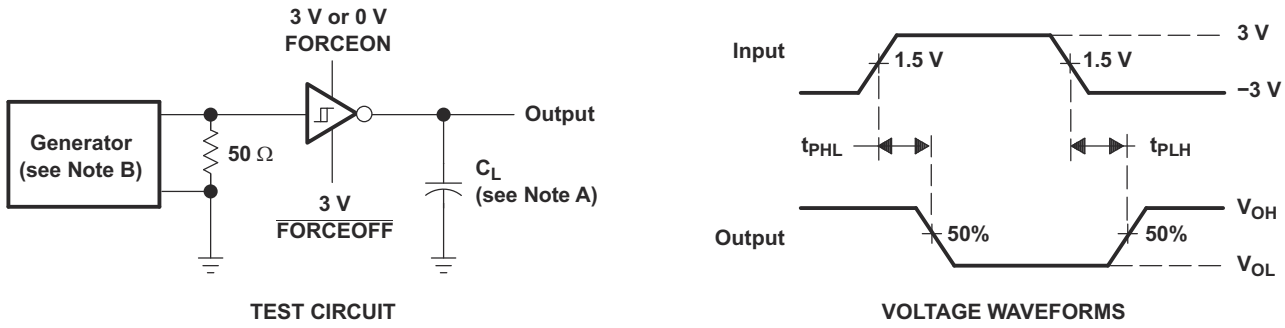
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s (MAX3243C/I) and 1 Mbit/s (MAX3243FC/I), Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

图 7-1. Driver Slew Rate



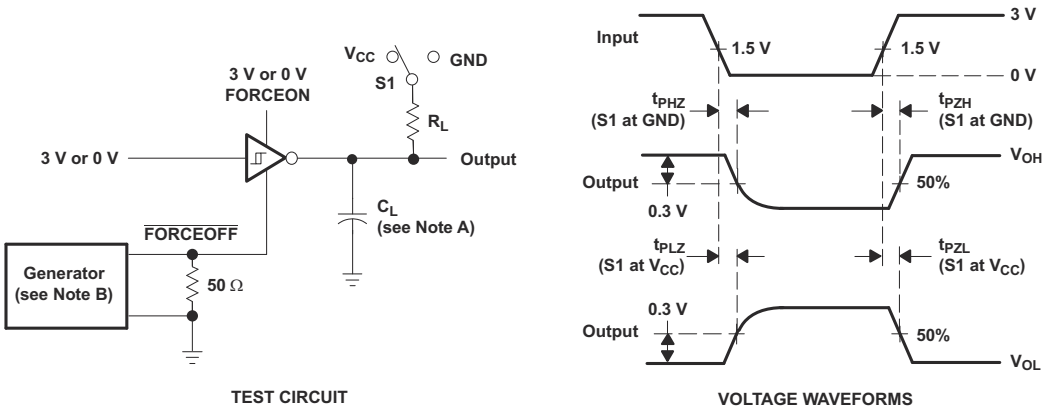
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s (MAX3243C/I) and 1 Mbit/s (MAX3243FC/I), Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

图 7-2. Driver Pulse Skew



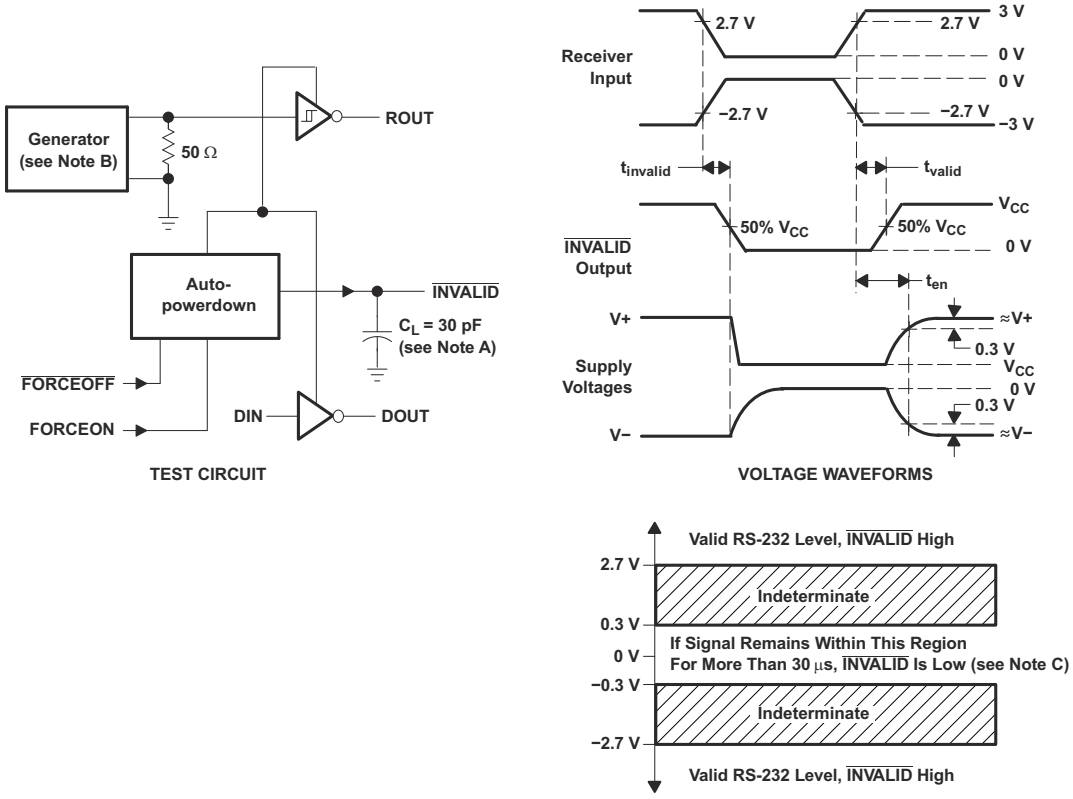
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

图 7-3. Receiver Propagation Delay Times



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

图 7-4. Receiver Enable and Disable Times



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.
C. Auto-powerdown disables drivers and reduces supply current to 1 µA.

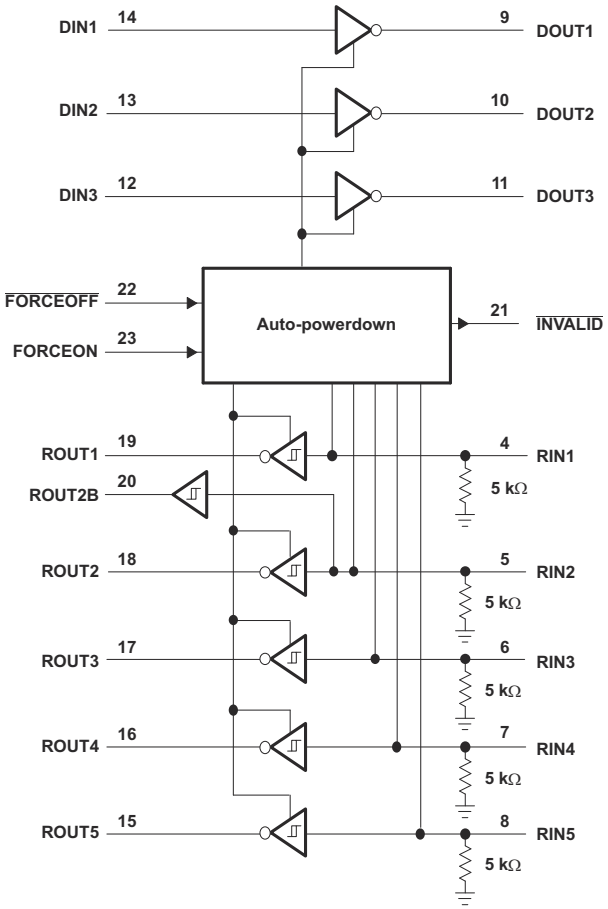
图 7-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

8 Detailed Description

8.1 Overview

The MAX3243 device consists of three line drivers, five line receivers, and a dual charge-pump circuit with ±15-kV ESD (HBM) protection pin to pin (serial- port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. This combination of drivers and receivers matches that needed for the typical serial port used in an IBM PC/AT, or compatible. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. Flexible control options for power management are available. when the serial port is inactive. The auto-power-down feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 µA. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur. Auto-powerdown can be disabled when FORCEON and FORCEOFF are high and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V or has been between –0.3 V and 0.3 V for less than 30 µs. INVALID is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 µs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Auto-Power-Down

Auto-Power-Down can be used to automatically save power when the receivers are unconnected or connected to a powered down remote RS232 port. FORCEON being high will override Auto power down and the drivers will be active. $\overline{\text{FORCEOFF}}$ being low will override FORCEON and will power down all outputs except for ROUT2B and $\overline{\text{INVALID}}$.

8.3.2 Charge Pump

The charge pump increases, inverts, and regulates voltage at V+ and V – pins and requires four external capacitors.

8.3.3 RS232 Driver

Three drivers interface standard logic level to RS232 levels. All DIN inputs must be valid high or low.

8.3.4 RS232 Receiver

Five receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

8.3.5 ROUT2B Receiver

ROUT2B is an always-active noninverting output of RIN2 input, which allows applications using the ring indicator to transmit data while the device is powered down.

8.3.6 Invalid Input Detection

The $\overline{\text{INVALID}}$ output goes active low when all RIN inputs are unpowered. The $\overline{\text{INVALID}}$ output goes inactive high when any RIN input is connected to an active RS232 voltage level.

8.4 Device Functional Modes

表 8-1. Each Driver(1)

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	YES	H	Normal operation with auto-powerdown enabled
H	L	H	YES	L	
X	L	H	NO	Z	Power off by auto-powerdown feature

(1) H = high level, L = low level, X = irrelevant, Z = high impedance, YES = any RIN valid, NO = all RIN invalid

表 8-2. Each Receiver(1)

INPUTS			OUTPUTS	RECEIVER STATUS
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	ROUT	
X	X	L	Z	Powered off
L	X	H	H	Normal operation
H	X	H	L	
Open	X	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

表 8-3. $\overline{\text{INVALID}}$ and ROUT2B Outputs(1)

INPUTS				OUTPUTS		OUTPUT STATUS
VALID RIN RS-232 LEVEL	RIN2	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{INVALID}}$	ROUT2B	
YES	L	X	X	H	L	Always Active
YES	H	X	X	H	H	
YES	OPEN	X	X	H	L	Always Active
NO	OPEN	X	X	L	L	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off),
OPEN = input disconnected or connected driver off, YES = any RIN valid, NO = all RIN invalid

9 Application and Implementation

备注

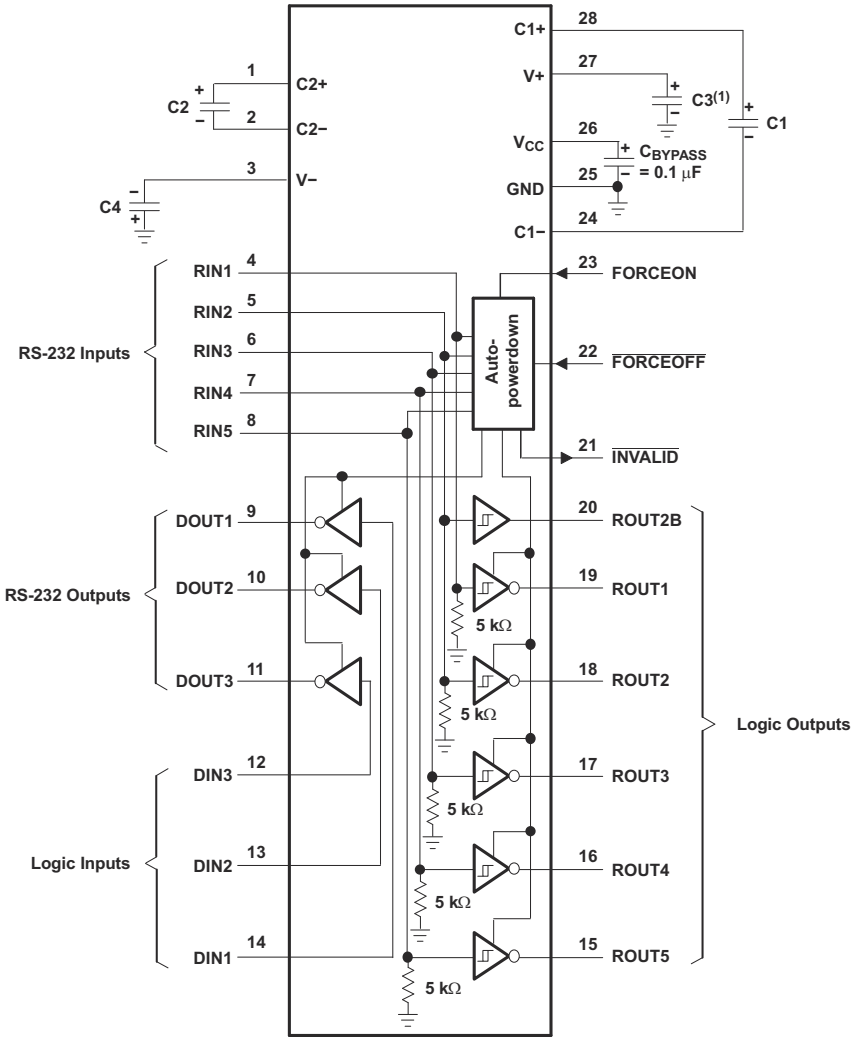
以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

It is recommended to add capacitors as shown in 图 9-1.

9.2 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. RIN and DOUT lines connect to a RS232 connector or cable.



(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

图 9-1. Typical Operating Circuit and Capacitor Values

9.2.1 Design Requirements

- V_{CC} minimum is 3 V and maximum is 5.5V.
- Maximum recommended bit rate is 250 kbit/s.

9.2.2 Detailed Design Procedure

- All DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels.
- Select capacitor values based on V_{CC} level for best performance.

9.2.3 Application Curves

V_{CC}= 3.3 V

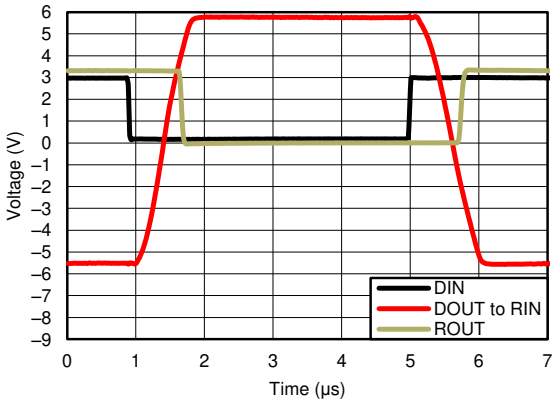


图 9-2. Driver to Receiver Loopback Timing Waveform

9.3 Power Supply Recommendations

V_{CC} should be between 3 V and 5.5 V. Charge pump capacitors should be chosen using table in 图 9-1.

9.4 Layout

9.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

In the *Layout Example* diagram, only critical layout sections are shown. Input and output traces will vary in shape and size depending on the customer application. FORCEON and $\overline{\text{FORCEOFF}}$ should be pulled up to VCC or GND via a pullup resistor, depending on which configuration the user desires upon power-up.

9.4.2 Layout Example

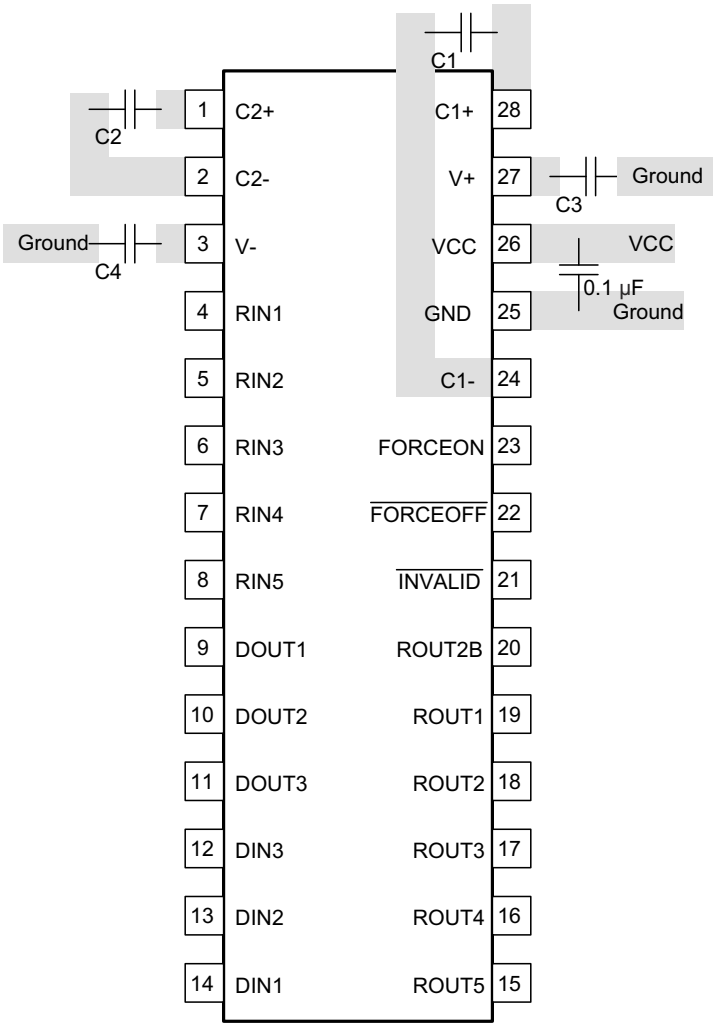


图 9-3. Layout Diagram

10 Device and Documentation Support

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

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10.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3243CDB	LIFEBUY	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C	
MAX3243CDBG4	LIFEBUY	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C	
MAX3243CDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C	Samples
MAX3243CDBRE4	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C	Samples
MAX3243CDBRG4	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C	Samples
MAX3243CDW	LIFEBUY	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C	
MAX3243CDWE4	LIFEBUY	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C	
MAX3243CDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C	Samples
MAX3243CDWRG4	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243C	Samples
MAX3243CPW	LIFEBUY	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3243C	
MAX3243CPWE4	LIFEBUY	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3243C	
MAX3243CPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3243C	Samples
MAX3243CPWRG4	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3243C	Samples
MAX3243IDB	LIFEBUY	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I	
MAX3243IDBG4	LIFEBUY	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I	
MAX3243IDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I	Samples
MAX3243IDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243I	Samples
MAX3243IDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	MAX3243I	Samples
MAX3243IPW	LIFEBUY	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3243I	
MAX3243IPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3243I	Samples
MAX3243IPWRE4	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3243I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF MAX3243 :

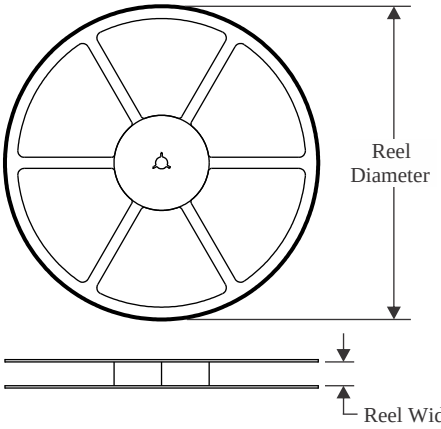
- Enhanced Product : MAX3243-EP

NOTE: Qualified Version Definitions:

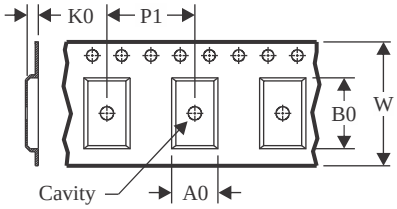
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

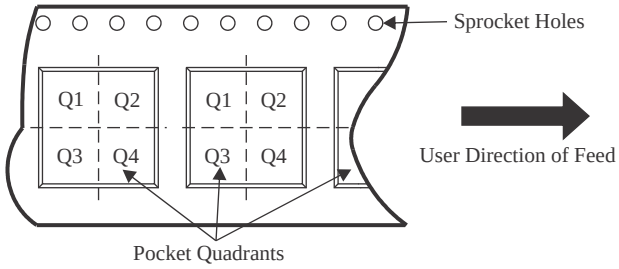


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

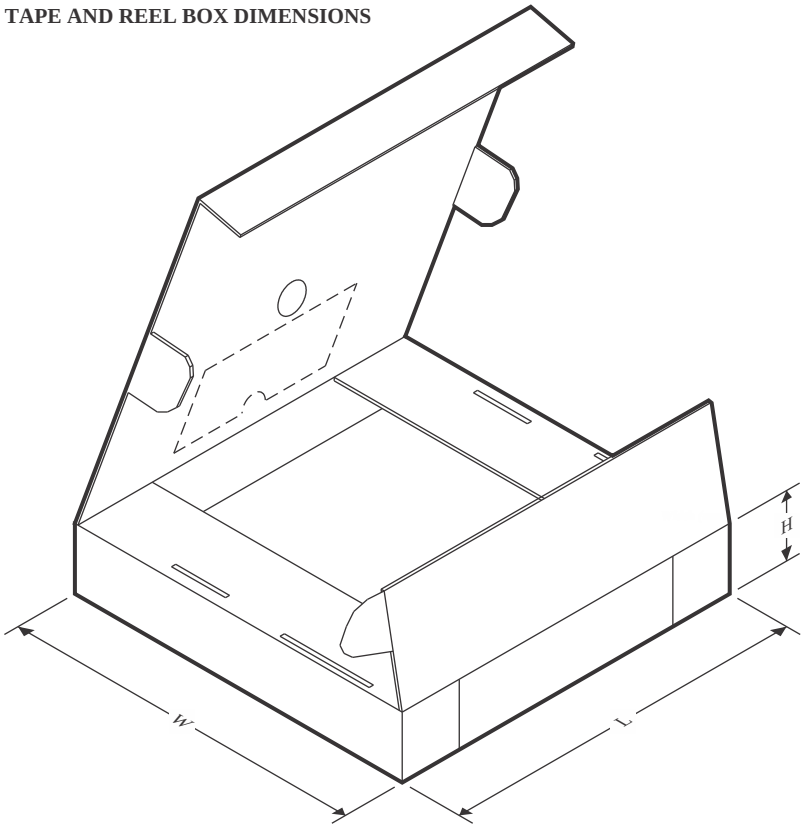
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3243CDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
MAX3243CDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MAX3243CPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MAX3243IDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
MAX3243IDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MAX3243IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

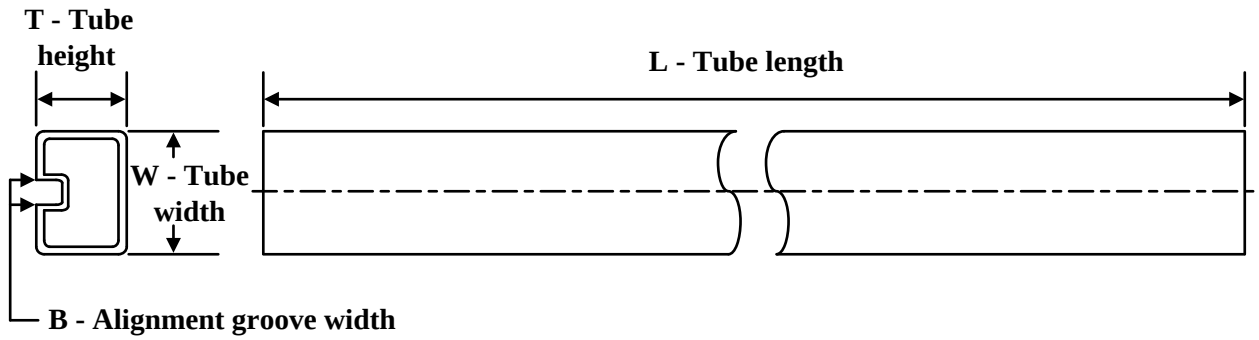
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3243CDBR	SSOP	DB	28	2000	356.0	356.0	35.0
MAX3243CDWR	SOIC	DW	28	1000	350.0	350.0	66.0
MAX3243CPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
MAX3243IDBR	SSOP	DB	28	2000	356.0	356.0	35.0
MAX3243IDWR	SOIC	DW	28	1000	350.0	350.0	66.0
MAX3243IPWR	TSSOP	PW	28	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

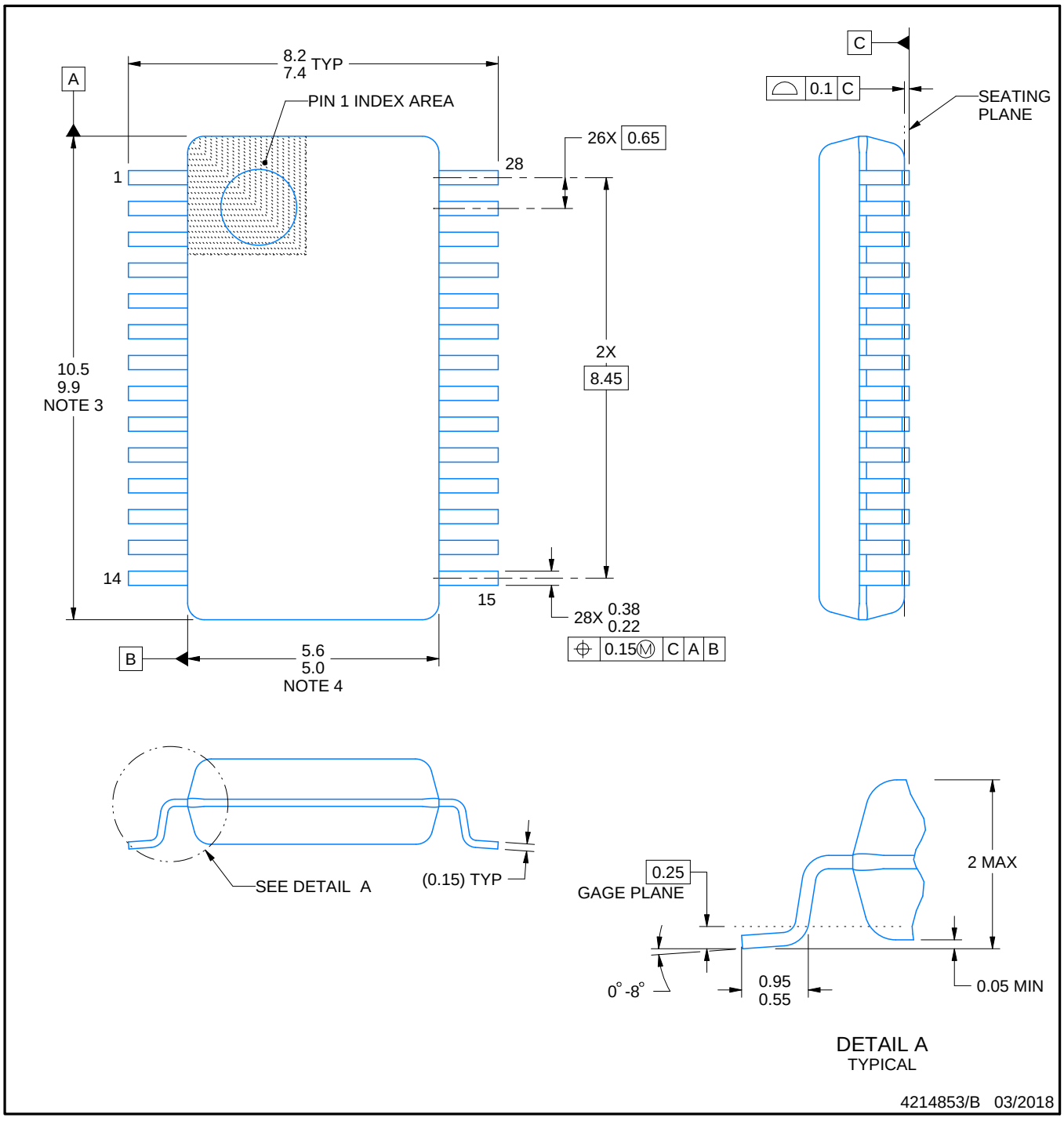
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MAX3243CDB	DB	SSOP	28	50	530	10.5	4000	4.1
MAX3243CDBG4	DB	SSOP	28	50	530	10.5	4000	4.1
MAX3243CDW	DW	SOIC	28	20	506.98	12.7	4826	6.6
MAX3243CDWE4	DW	SOIC	28	20	506.98	12.7	4826	6.6
MAX3243CPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243CPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243CPWE4	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243CPWE4	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243IDB	DB	SSOP	28	50	530	10.5	4000	4.1
MAX3243IDBG4	DB	SSOP	28	50	530	10.5	4000	4.1
MAX3243IDW	DW	SOIC	28	20	506.98	12.7	4826	6.6
MAX3243IPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243IPW	PW	TSSOP	28	50	530	10.2	3600	3.5

PACKAGE OUTLINE

DB0028A

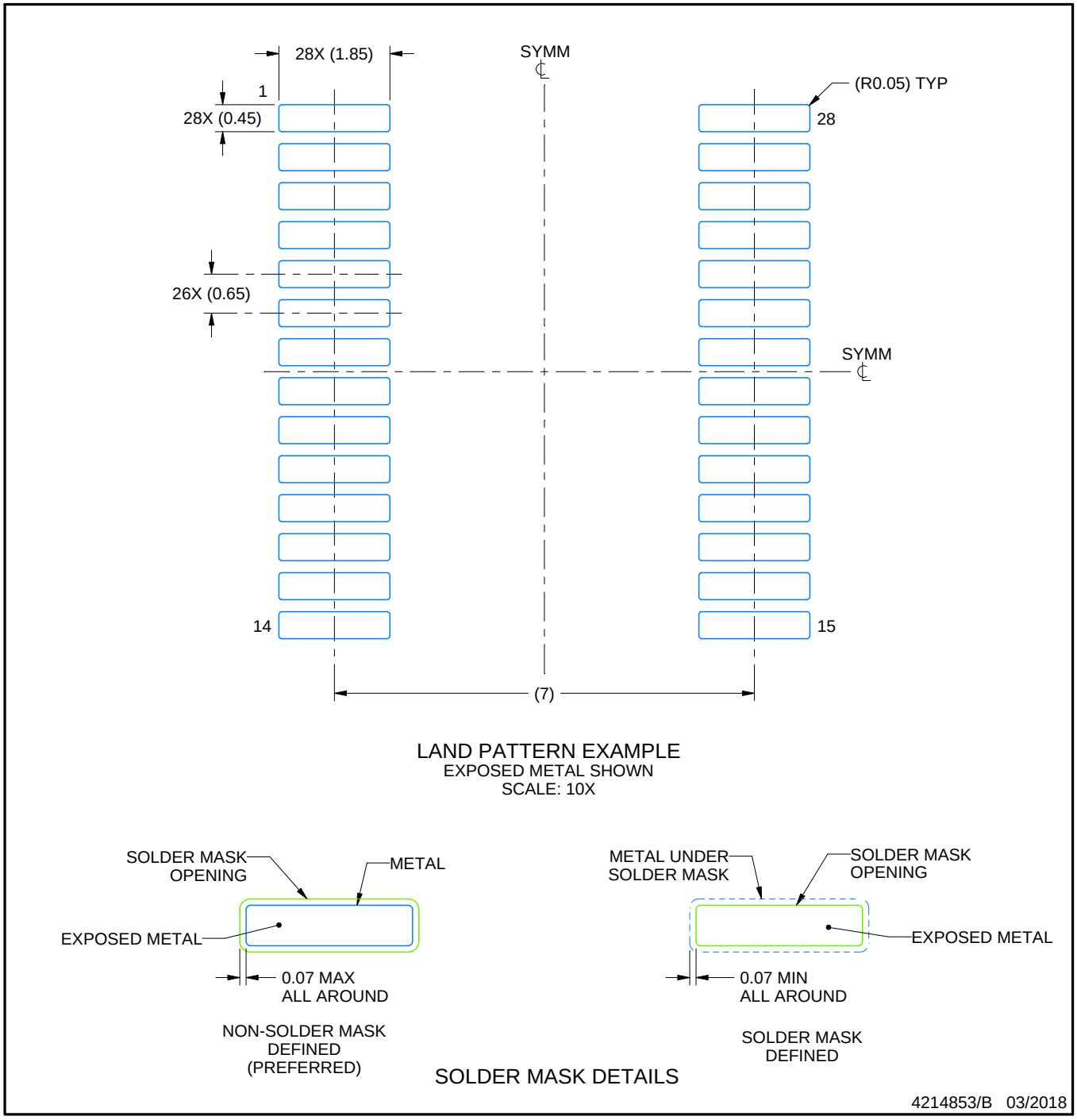
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



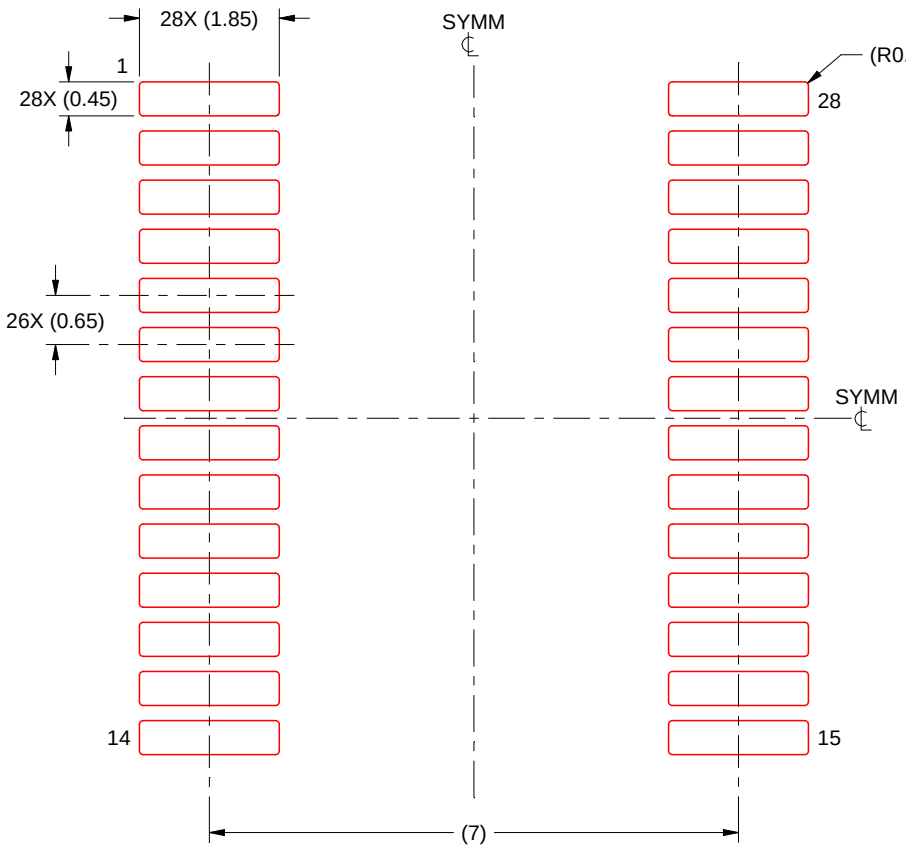
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



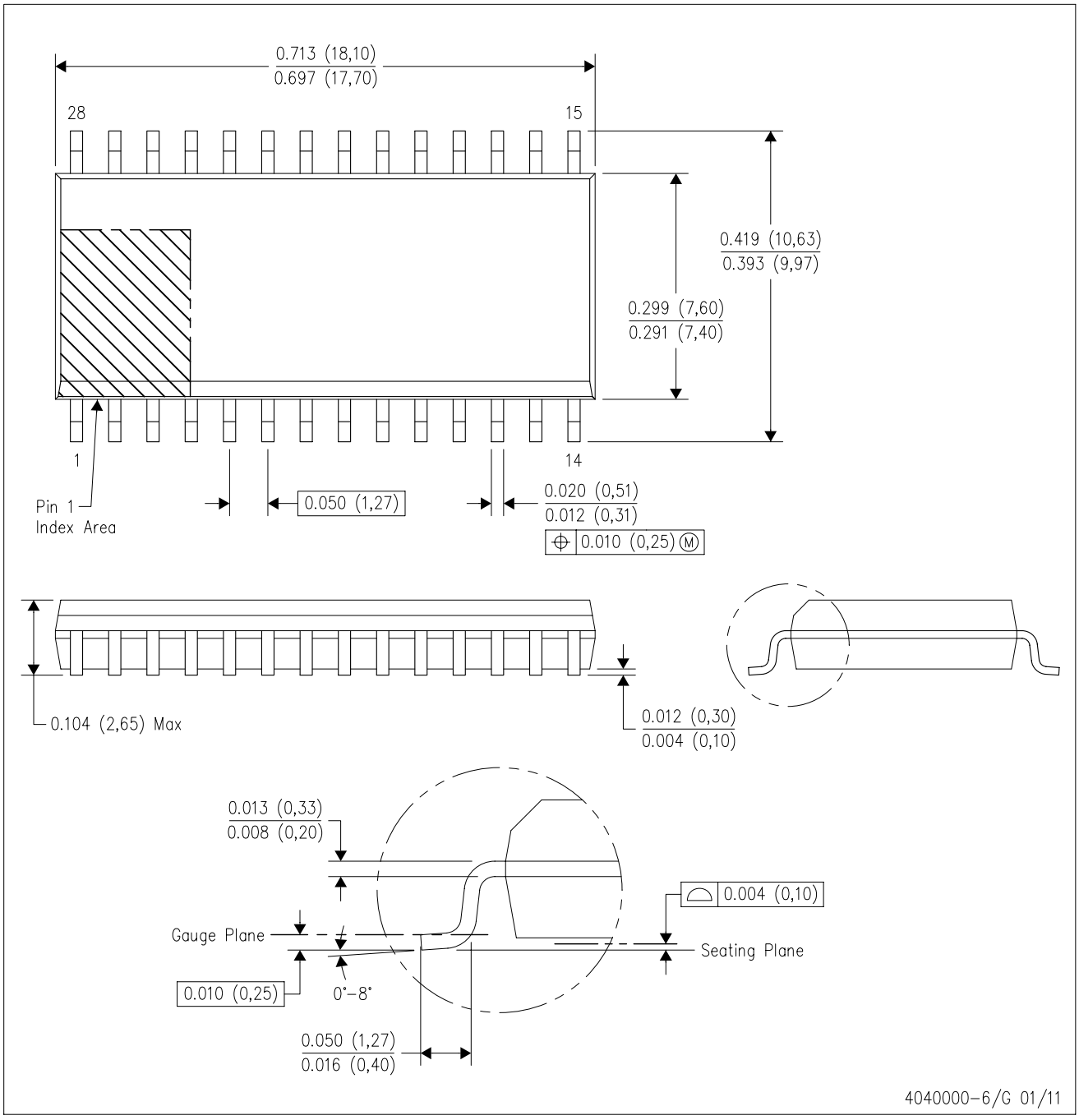
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

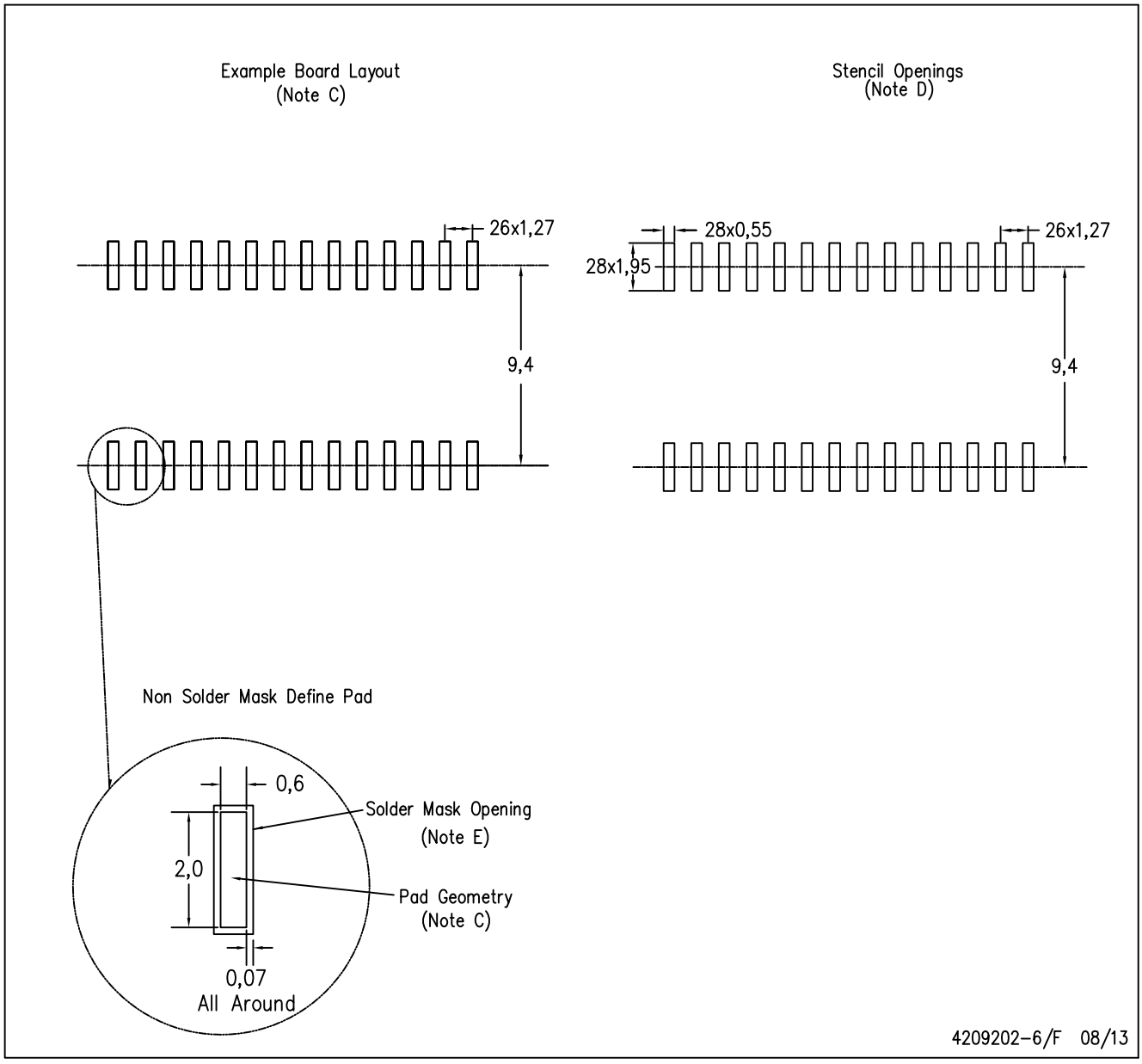
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



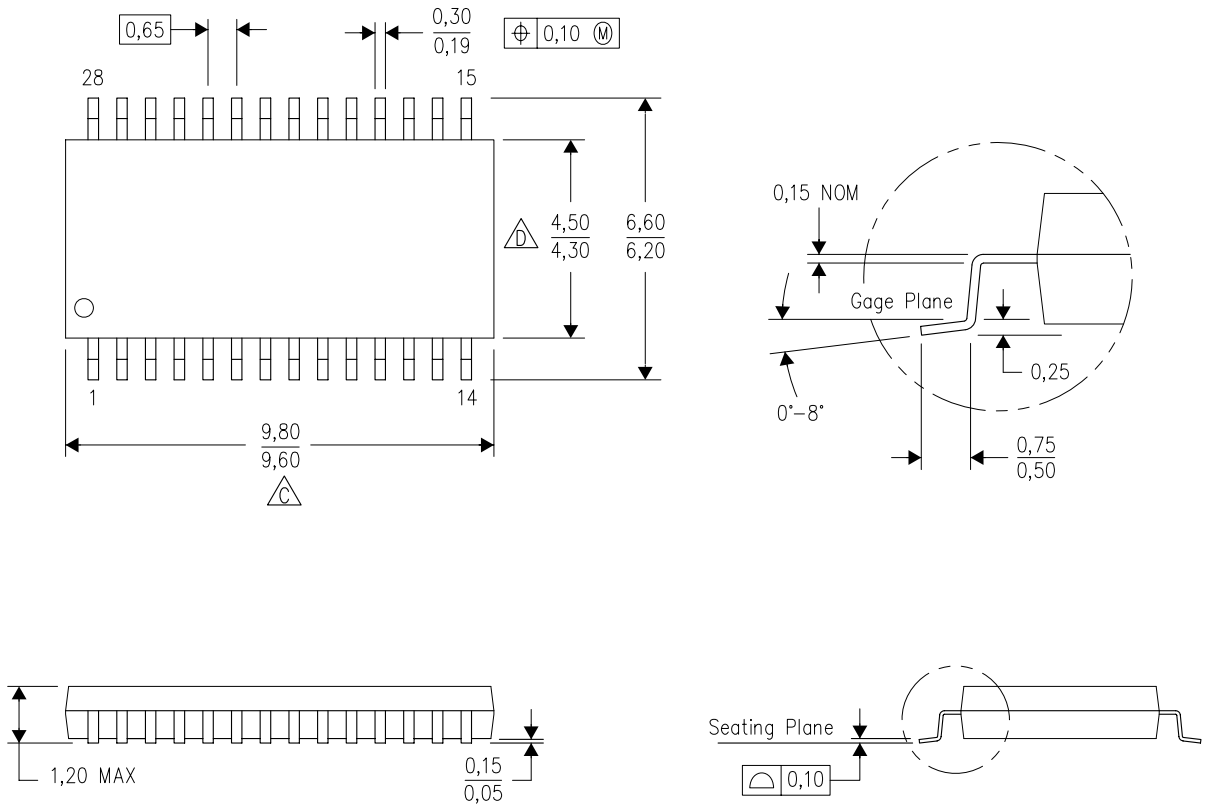
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

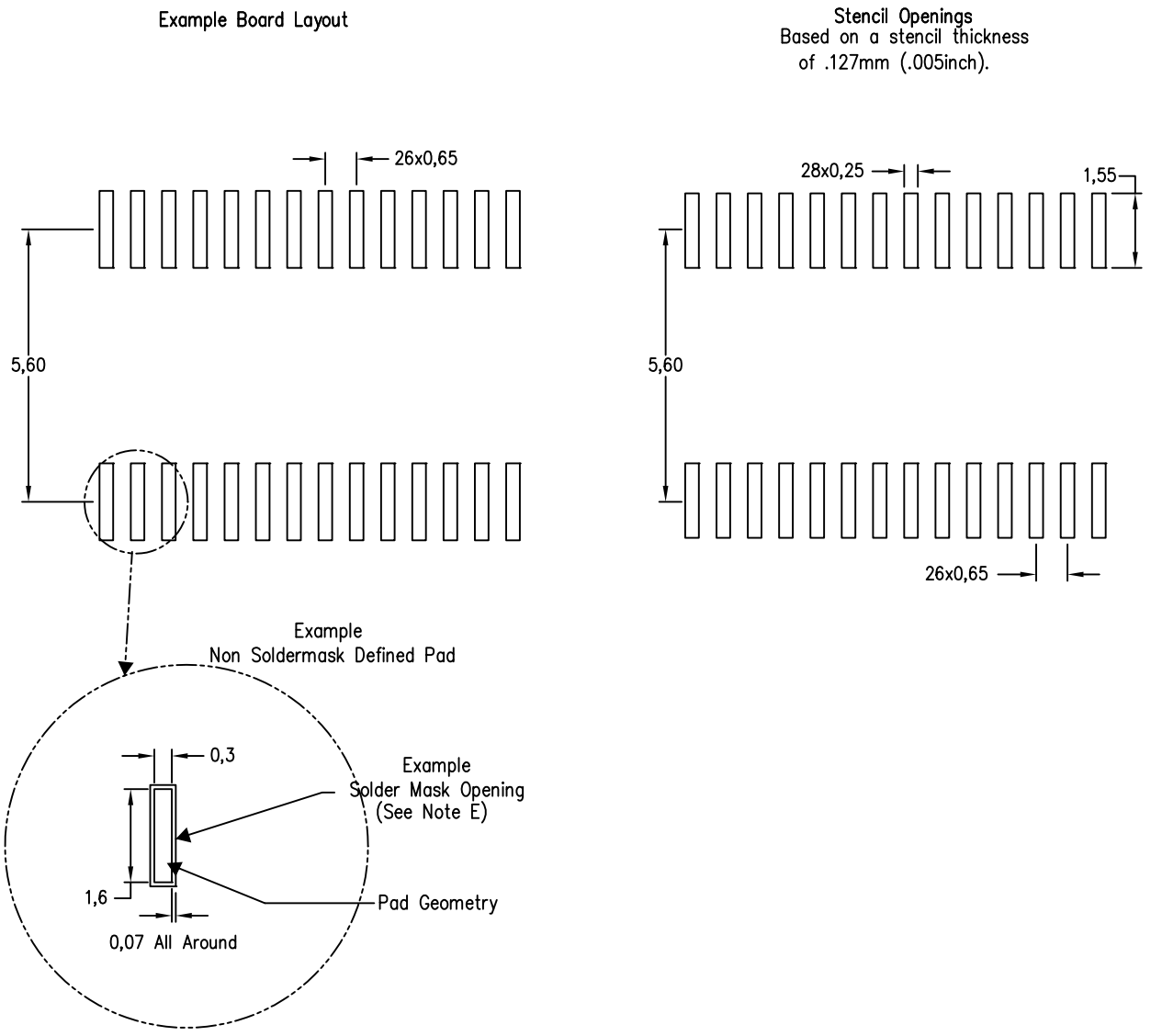
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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