aSC7512

DIGITAL TEMPERATURE SENSOR WITH INTEGRATED FAN CONTROL

PRODUCT SPECIFICATION

Fully Released Specification

Product Description

The aSC7512 has a two wire digital interface compatible with SMBus 2.0. Using a 10-bit ΣΔ- ADC, the aSC7512 measures the temperature of a remote diode connected transistor as well as its own die.

Using temperature information from these two zones, an automatic fan speed control algorithm is employed to minimize acoustic impact while achieving recommended CPU temperature under varying operational loads.

To set fan speed, the aSC7512 has a pulse width modulation (PWM) output that is controlled by one of two temperature zones. Both high- and low-frequency PWM ranges are supported. The aSC7512 also includes a digital filter that can be invoked to smooth temperature readings for better control of fan speed and minimum acoustic impact. The aSC7512 has a tachometer input to measure fan speed or alternatively, an alert pin that may be triggered by exceeding a temperature limit setting. Limit and status registers for all measured values are included to alert the system host that any measurements are outside of programmed limits.

Features

- 2-wire, SMBus 2.0 compliant, serial digital interface
- 10-bit ΣΔ-ADC
- Monitors internal and remote thermal diodes
- Programmable autonomous fan control based on temperature readings
- Noise filtering of temperature reading for fan control
- 0.25°C digital temperature sensor resolution
- PWM fan speed control output for 2-, 3- or 4-wire fans.
- Provides high and low PWM frequency ranges
- Fan tachometer input or $\overline{\text{ALERT}}$ output
- 8-lead MSOP or SOIC package

Measurement System

Temperature:

- 0.25°C resolution, ±1°C accuracy on remote diode
- 0.25°C resolution, ±3°C accuracy on local sensor
- Extended temperature measurement range on remote sensor –55°C to +125°C using or 2's complement coding.

Fan Tachometer:

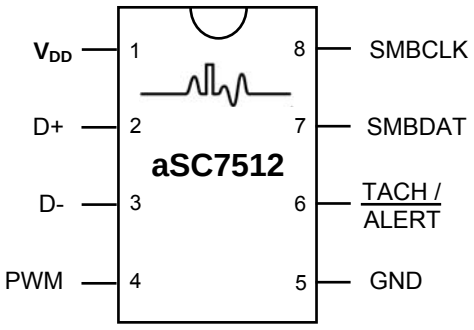
- 16-bit count of 90KHz clock periods

Limit alarms for all measured values

Applications

- Desktop Computers – Motherboards and Graphics Cards
- Laptop Computers
- Microprocessor based equipment (e.g. Base-stations, Routers, ATMs, Point of Sales)

Connection Diagram



Ordering Information

Part Number	Package	Temperature Range and Operating Voltage	Marking	How Supplied
aSC7512D8	8-lead SOIC	-40°C to +125°C, 3.3V	aSC7512 Ayww	2500 units Tape & Reel
aSC7512M8	8-lead MSOP	-40°C to +125°C, 3.3V	7512 Ayww	2500 units Tape & Reel

Ayww – Assembly site, year, workweek

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Block Diagram

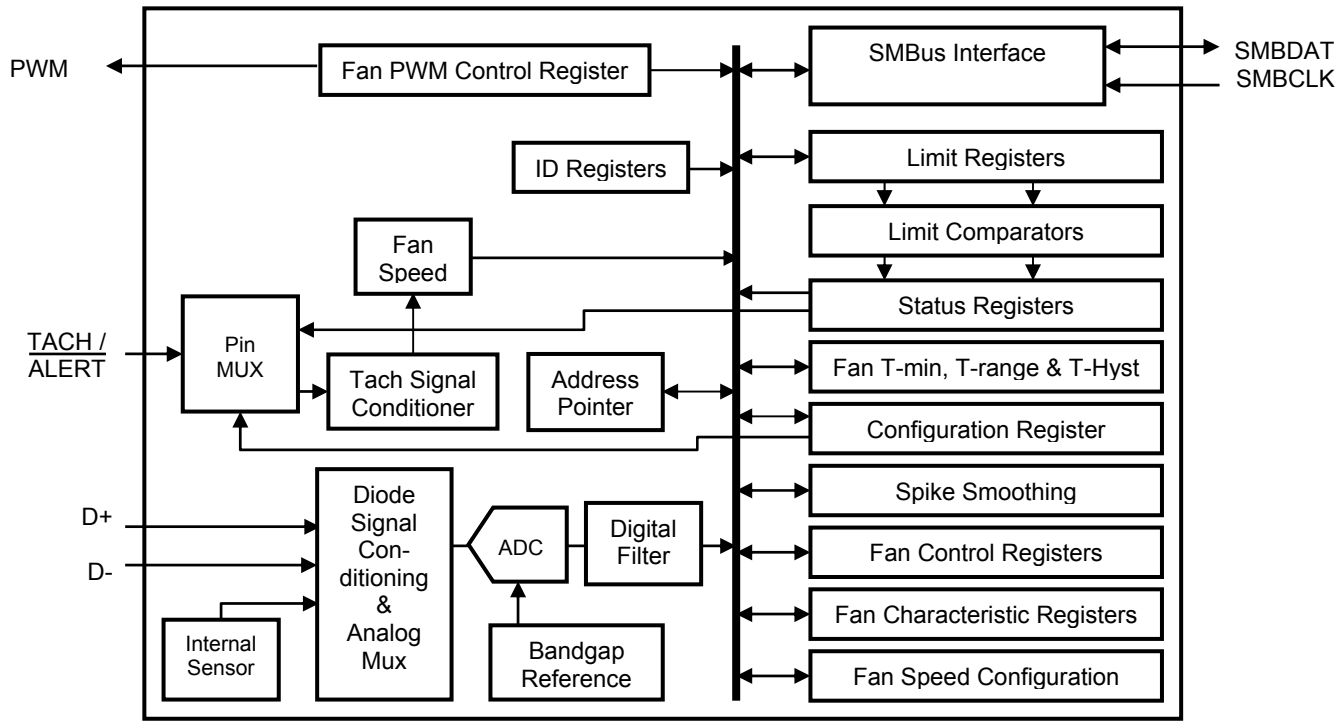


Figure 1 Block Diagram

Pin Descriptions

	Symbol	Pin	Type	Name and Function/Connection
SMBus	SMBDAT	7	Digital I/O (Open-Drain)	System Management Bus Data. Open-drain output. 5V tolerant, SMBus 2.0 compliant.
	SMBCLK	8	Digital Input	System Management Bus Clock. Tied to Open-drain output. 5V tolerant, SMBus 2.0 compliant.
Power	V_{DD}	1	POWER	+3.3V pin. Can be powered by +3.3V Standby power if monitoring in low power states is required. This pin should be bypassed with a 0.1μF capacitor in parallel with 100pF
	GND	5	GROUND	Ground for all analog and digital circuitry.
Remote	D+	2	Remote Thermal Diode Positive Input	Positive input (current source) from the remote thermal diode serves as the positive input into the A/D. Connected to the anode of a CPU thermal diode or the base-collector of a diode connected MMBT3904 NPN transistor.
	D-	3	Remote Thermal Diode Negative Input	Negative input (current sink) from the remote thermal diode serves as the negative input into the A/D. Connected to cathode of a CPU thermal diode or the emitter of a diode connected MMBT3904 NPN transistor.
Fan / Alert	TACH / $\overline{\text{ALERT}}$	6	Digital Input / Digital Open-Drain Output	Input for monitoring tachometer output of fan (default) or $\overline{\text{ALERT}}$ output selectable by configuration register 09h, bit 5.
	PWM	4	Digital Open-Drain Output	Fan speed control, Pulse Width Modulated.

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Absolute Maximum Ratings[1]

Parameter		Rating
Supply Voltage, V_{DD}		-0.5V to 6.0V
Voltage on Any Digital Input or Output Pin		-0.5V to 6.0V
Voltage on Remote +		-0.5V to (V_{DD} + 0.50V)
Current on Remote -		±1mA
Input Current on Any Pin[2]		±5mA
Package Input Current[2]		±20mA
Package Dissipation at T_A = 25°C		See (Note 3)
Storage Temperature		-65°C to +150°C
ESD[4]	Human Body Model	2500 V
	Machine Model	250 V

Operating Ratings[1]

Parameter	Rating
aSC7512 Operating Temperature Range	-40°C ≤ T_A ≤ +125°C
Remote Diode Temperature Range	-55°C ≤ T_D ≤ +125°C
Supply Voltage (3.3V nominal)	+3.0V to +3.6V
All Other Inputs	-0.05V to V_{DD} + 0.05V
Typical Supply Current	TBDmA

Notes:

1. Absolute maximum ratings are limits beyond which operation may cause permanent damage to the device. These are stress ratings only; functional operation at or above these limits is not implied.
2. When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_{DD}), the current at that pin should be limited to 5mA. The 20mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5mA to four. Parasitic components and/or ESD protection circuitry are present on the aSC7512 pins. Care should be taken not to forward bias the parasitic diode present on pins D+ and D-. Doing so by more than 50mV may corrupt temperature measurements.
3. Thermal resistance junction-to-ambient when attached to a double-sided printed circuit board with 1oz. foil is TBD°C/W
4. Human Body Model: 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Machine Model: 200pF capacitor discharged directly into each pin.

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DC Electrical Characteristics[5]

The following specifications apply for V_{DD} = 3.3V, and all analog input source impedance R_s = 50Ω unless otherwise specified in conditions. **Boldface limits apply for $T_A = T_J$ over T_{MIN} to 85°C**; all other limits $T_A = T_J$ = 25°C. T_A is the ambient temperature of the aSC7512; T_J is the junction temperature of aSC7512; T_D is the remote thermal diode junction temperature. Specifications subject to change without notice

Parameter		Conditions	Min	Typ	Max	Units
POWER SUPPLY CHARACTERISTICS						
Supply Current		Converting, Interface and Fans Inactive, Peak Current		1.8	**3.5**	mA(max)
		Converting, Interface and Fans inactive, Average Current		0.5		mA
Power-On Reset Threshold Voltage			**1.6**		**2.8**	V
TEMPERATURE TO DIGITAL CONVERTER CHARACTERISTICS						
Resolution				0.25 10		°C Bits
Local Sensor Accuracy[6]		-40°C≤T_A≤+100°C, 3V≤V_{DD}≤3.6V		±1	±3	°C
Remote Sensor Accuracy[7]		0°C≤T_A≤+100°C, -55°C≤T_D≤+125°C, 3V≤V_{DD}≤3.6V		±1	±2	°C
		-40°C≤T_A≤+120°C, -55°C≤T_D≤+125°C, 3V≤V_{DD}≤3.6V			±3	°C
External Diode Current Source	I_{DS}	High Level		96		µA
		Low Level		6		µA
External Diode Current Ratio				16		
DIGITAL OPEN-DRAIN OUTPUT: PWM						
Logic Low Sink Current	I_{OL}	V_{OL} = 0.4V	**8**			mA (min)
Logic Low Level	V_{OL}	I_{OUT} = +8mA			**0.4**	V (max)
SMBUS OPEN-DRAIN OUTPUT: SMBDAT						
Logic Low Output Voltage	V_{OL}	I_{OUT} = +4mA			**0.4**	V (max)
High Level Output Current	I_{OH}	V_{OUT} = V+		0.1	**10**	µA(max)
SMBUS INPUTS: SMBCLK, SMBDAT						
Logic Input High Voltage	V_{IH}		**2.1**			V (min)
Logic Input Low Voltage	V_{IL}				**0.8**	V (max)
Logic Input Hysteresis Voltage	V_{HYST}			300		mV
DIGITAL INPUTS: ALL						
Logic Input High Voltage	V_{IH}		**2.1**			V (min)
Logic Input Low Voltage	V_{IL}				**0.8**	V (max)
Logic Input Threshold Voltage	V_{TH}			1.5		V
Logic High Input Current	I_{IH}	V_{IN} = V+		0.005	**10**	µA(max)
Logic Low Input Current	I_{IL}	V_{IN} = GND		-0.005	**-10**	µA(max)
Digital Input Capacitance	C_{IN}			20		pF

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AC Electrical Characteristics

The following specifications apply for V_{DD} = 3.3V unless otherwise specified in conditions. **Boldface limits apply for $T_A = T_J$ over T_{MIN} to 85°C**; all other limits $T_A = T_J$ = 25°C.

Parameter		Conditions	Min	Typ	Max	Units
TACHOMETER						
Fan Full-Scale Count					**65535**	(max)
Fan Counter Clock Frequency				90		kHz
Fan Count Conversion Time				0.7	**1.46**	sec(max)
FAN PWM OUTPUT						
Frequency Range		Low-Frequency Range		10 94		Hz Hz
		High-Frequency Range		22.5 30		kHz kHz
Duty-Cycle Range					**0 to 100**	%(max)
Duty-Cycle Resolution (8-bits)				0.3906		%/count
Spin-Up Time Interval Range				0 4000		ms ms

Logic Electrical Characteristics

(T_A = 25 °C, V_{DD} = 3.3V unless otherwise noted)

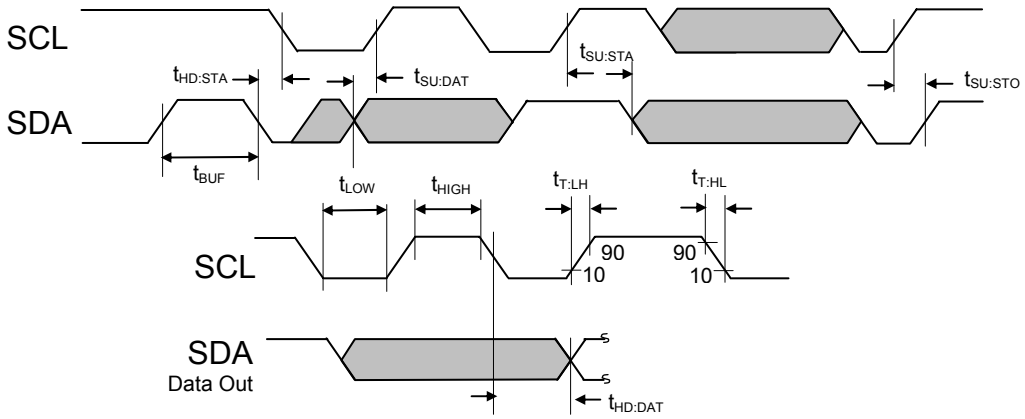
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Logic High	V_{IH}	$3V \le V_{DD} \le 3.6V$	2.1			V
Input Voltage Logic Low	V_{IL}	$3V \le V_{DD} \le 3.6V$			0.8	V
Output Voltage Logic Low ($\overline{\text{ALERT}}$)	V_{OL}	V_{DD}=5V, I_{OL}= -6mA			0.4	V
Output Low Sink Current ($\overline{\text{ALERT}}$)	I_{OL}	$\overline{\text{ALERT}}$ forced to 0.4V	6			mA
Input Leakage Current	I_{IN}	V_{IN} = 0V or 5.5V, $-40°C \le T_A \le +125°C$			±1.0	µA
SMBus Output Sink Current	I_{OL}	T_A = 25 °C, V_{OL} = 0.6V	6			mA
SMBus Logic Input Current	I_{IH}, I_{IL}		-1		+1	µA
Output Leakage Current	I_{OH}	$V_{OH} = V_{DD}$ = 5.5V		0.1	1	µA
Output Transition Time	t_F	C_L= 400pF, I_{OL} = -3mA			250	ns
Input Capacitance	C_{IN}	All Digital Inputs			5	pF

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Serial Port Timing

(T_A = 25 °C, V_{DD} = 3.3V unless otherwise noted, Guaranteed by design, not production tested)

Parameter	Symbol	Min	Typ	Max	Units
SCL Operating Frequency	f_{SCL}			400	kHz
SCL Clock Transition Time	$t_{T:LH}$, $t_{T:HL}$			300	ns
SCL Clock Low Period	t_{LOW}	1.3			µs
SCL Clock High Period	t_{HIGH}	0.6		50	µs
Bus free time between a Stop and a new Start Condition	t_{BUF}	1.3			µs
Data in Set-Up to SCL High	$t_{SU:DAT}$	100			ns
Data Out Stable after SCL Low	$t_{HD:DAT}$	300			ns
SCL Low Set-up to SDA Low (Repeated Start Condition)	$t_{SU:STA}$	600			ns
SCL High Hold after SDA Low (Start Condition)	$t_{HD:STA}$	600			ns
SDA High after SCL High (Stop Condition)	$t_{SU:STO}$	600			ns
Time in which aSC7512 must be operational after a power-on reset	t_{POR}			500	ms



5. These specifications are guaranteed only for the test conditions listed.
6. The accuracy of the aSC7512 is guaranteed when using the thermal diode of a processor or any thermal diode with a non-ideality of 1.008 and internal series resistance of 3.52Ω. When using a 2N3904 type transistor as a thermal diode the error band will be typically shifted depending on transistor characteristics.
7. Accuracy (expressed in °C) = Difference between the aSC7512 reported output temperature and the temperature being measured. Local temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the aSC7512 and the thermal resistance. See (Note 3) for the thermal resistance to be used in the self-heating calculation.
8. Holding the SMBDAT and/or SMBCLK lines Low for a time interval greater than $t_{TIMEOUT}$ will reset the aSC7512's SMBus state machine, therefore setting the SMBDAT pin to a high impedance state.

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Control Communication

SMBus

The aSC7512 is compatible with devices that are compliant to the SMBus 2.0 specifications. More information on this bus can be found at http://www.smbus.org/. Compatibility of SMBus2.0 to other buses is discussed in the SMBus 2.0 specification.

General Operation

Writing to and reading from the aSC7512 registers is accomplished via the SMBus-compatible two-wire serial interface. SMBus protocol requires that one device on the bus initiate and control all read and write operations. This device is called the "master" device. The master device also generates the SCL signal that is the clock signal for all other devices on the bus. All other devices on the bus are called "slave" devices. The aSC7512 is a slave device. Both the master and slave devices can send and receive data on the bus.

During SMBus operations, one data bit is transmitted per clock cycle. All SMBus operations follow a repeating nine clock-cycle pattern that consists of eight bits (one byte) of transmitted data followed by an acknowledge (ACK) or not acknowledge (NACK) from the receiving device. Note that there are no unused clock cycles during any operation—therefore there must be no breaks in the stream of data and ACKs / NACKs during data transfers.

For most operations, SMBus protocol requires the SDA line to remain stable (unmoving) whenever SCL is high — i.e. any transitions on the SDA line can only occur when SCL is low. The exceptions to this rule are when the master device issues a start or stop condition. Note that the slave device cannot issue a start or stop condition.

SMBus Definitions

The following are definitions for some general SMBus terms:

Start Condition: This condition occurs when the SDA line transitions from high to low while SCL is high. The master device uses this condition to indicate that a data transfer is about to begin.

Stop Condition: This condition occurs when the SDA line transitions from low to high while SCL is high. The master device uses this condition to signal the end of a data transfer.

Acknowledge and **Not Acknowledge:** When data are transferred to the slave device it sends an "acknowledge" (ACK) after receiving each byte. The receiving device sends an ACK by pulling SDA low for one clock. Following the last byte, a master device sends a "not acknowledge" (NACK) followed by a stop condition. A NACK is indicated by forcing SDA high during the clock after the last byte.

Slave Address

aSC7512 is designed to be used primarily in desktop systems that require only one monitoring device. The SMBus slave address is fixed at 58 hex (x 1 0 1 1 0 0 0 binary).

Writing to and Reading from the aSC7512

All read and write operations must begin with a start condition generated by the master device. After the start condition, the master device must immediately send a slave address (7-bits) followed by a R/$\overline{W}$ bit. If the slave address matches the address of the aSC7512, it sends an ACK by pulling the SDA line low for one clock. Read or write operations may contain one- or two-bytes. See Figures 2 through 6 for timing diagrams for all aSC7512 operations.

Setting the Register Address Pointer

For all operations, the address pointer stored in the address pointer register must be pointing to the register address that is going to be written to or read from. This register's content is automatically set to the value of the first byte following the R/$\overline{W}$ bit being set to 0.

After the aSC7512 sends an ACK in response to receiving the address and R/$\overline{W}$ bit, the master device must transmit an appropriate 8-bit address pointer value as explained in the Registers section of this data sheet. The aSC7512 will send an ACK after receiving the new pointer data.

The register address pointer set operation is illustrated in Figure 2. If the address pointer is not a valid address the aSC7512 will internally terminate the operation. Also recall that the address register retains the current address pointer value between operations. Therefore, once a register is being pointed to, subsequent read operations do not require another Address Pointer set cycle.

Writing to Registers

All writes must start with a pointer set as described previously, even if the pointer is already pointing to the desired register. The sequence is described in Figure 2.

Immediately following the pointer set, the master must begin transmitting the data to be written. After transmitting each byte of data, the master must release the SDA line for one clock to allow the aSC7512 to acknowledge receiving the byte. The write operation should be terminated by a stop condition from the master.

Reading from Registers

To read from a register other than the one currently being pointed to by the address pointer register, a pointer set sequence to the desired register must be done as described previously. Immediately following the pointer

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set, the master must perform a repeat start condition that indicates to the aSC7512 that a read is about to occur. It is important to note that if the repeat start condition does not occur, the aSC7512 will assume that a write is taking place, and the selected register will be overwritten by the upcoming data on the data bus. The read sequence is described in Figure 4. After the start condition, the master must again send the device address and read/write bit. This time the R/$\overline{W}$ bit must be set to 1 to indicate a read. The rest of the read cycle is the same as described in the previous paragraph for reading from a preset pointer location.

If the pointer is already pointing to the desired register, the master can read from that register by setting the R/$\overline{W}$ bit (following the slave address) to a 1. After sending an ACK, the aSC7512 will begin transmitting data during the following clock cycle. After receiving the 8 data bits, the master device should respond with a NACK followed by a stop condition.

If the master is reset while the aSC7512 is in the process of being read, the master should perform an SMBus reset. This is done by holding the data or clock low for more than 35ms, allowing all SMBus devices to be reset. This follows the SMBus 2.0 specification of 25-35ms.

When the aSC7512 detects an SMBus reset, it will prepare to accept a new start sequence and resume communication from a known state.

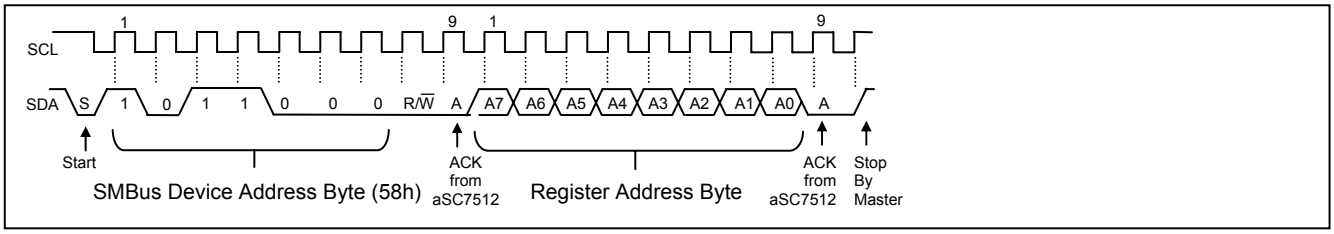


Figure 2 Register Address Pointer Set

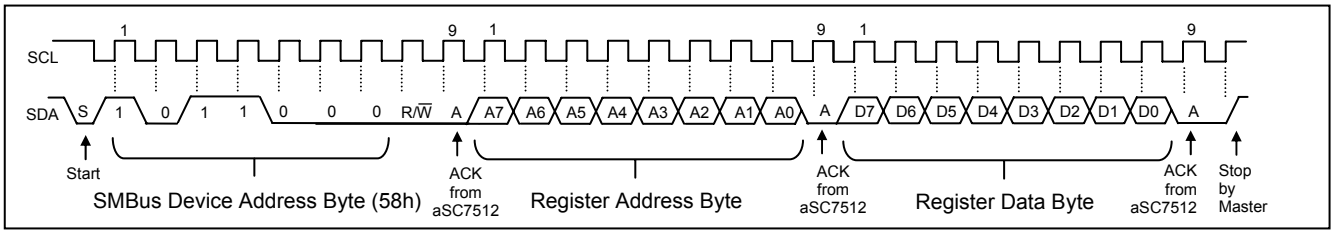


Figure 3 Register Write

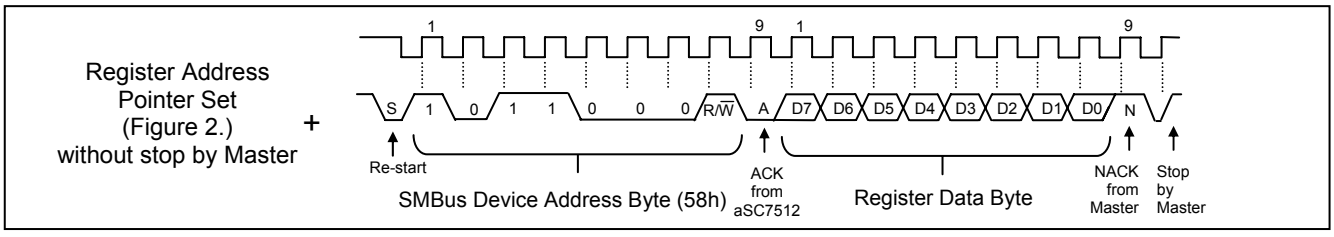


Figure 4 Register Read

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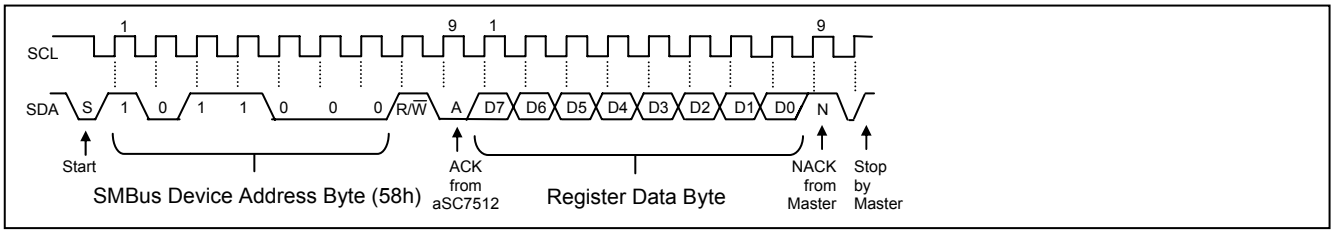


Figure 5 Register Read When Read Address Already Set

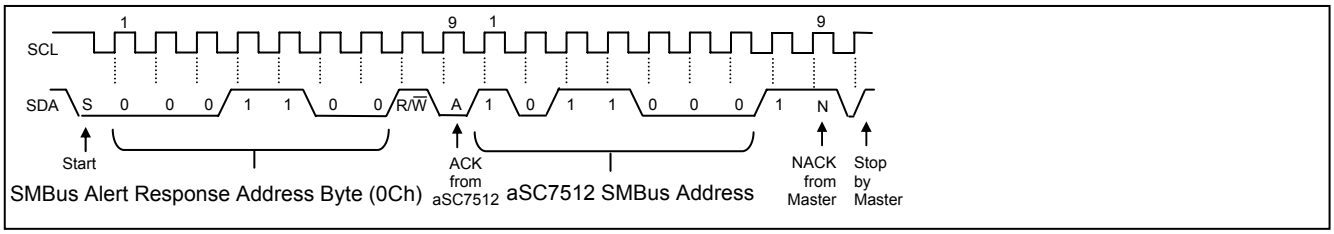


Figure 6 SMBus Alert Response

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Operation

$\overline{\text{ALERT}}$ Output

The aSC7512 has an emergency alarm function, $\overline{\text{ALERT}}$ that is optionally assigned to pin 6, the TACH / $\overline{\text{ALERT}}$ pin. $\overline{\text{ALERT}}$ is determined by both high and low limits and will also respond to a remote diode open circuit failure. These limits are settable separately for Zone 1 and Zone 2 sensors. Any alarm condition is reported individually in the status register and may be read at any time on the SMBus. Alarm conditions are logically combined and used to drive an open-drain output, the $\overline{\text{ALERT}}$ output, (pin 6).

This output pin may be used as an interrupt signal the CPU or to turn on remote drivers for fans or indicators. The $\overline{\text{ALERT}}$ pin will remain asserted until it has been reset by the host via the SMBus.

$\overline{\text{ALERT}}$ Limits

Figure 7 shows use of the $\overline{\text{ALERT}}$ high and low limits. The user sets up the alarm by writing the upper and lower limit temperatures into the limit registers over the SMBus. After each measurement, the comparator tests the readings against the programmed limits and if the measurement exceeds the high limit is or is equal to or less-than the low limit, it will assert the particular alarm bits in the status register and cause the $\overline{\text{ALERT}}$ pin to go low.

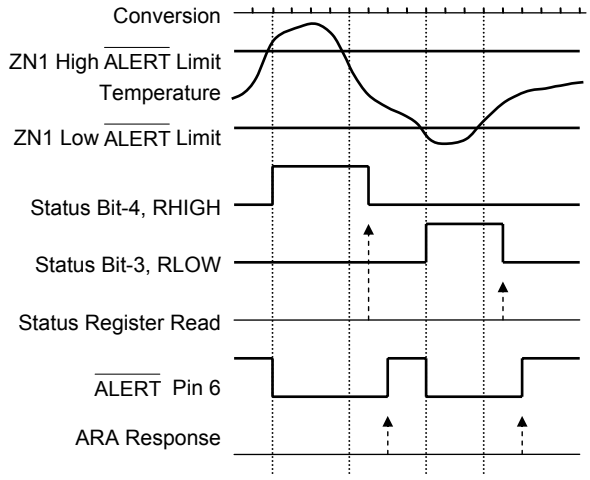


Figure 7 $\overline{\text{ALERT}}$ Limits and Responses

The status bits will remain high until the status register is read and then, if the condition is no longer present those bits will be reset, otherwise they will remain high until the conditions are no longer met and the register is read again. The same sequence applies to the local readings and limits.

The $\overline{\text{ALERT}}$ pin will remain low until the status bits have been reset and an Alert Response has been issued by the master and responded by the aSC7512. This flow is described below.

The user may mask-out or disable the $\overline{\text{ALERT}}$ signal pin should it be necessary to prevent a processor interrupt. This is controlled by setting bit 7 of the configuration register.

SMBus Alert Output

The $\overline{\text{ALERT}}$ pin may be used to signal an SMBus Alert to the host processor. This is a special mode of the SMBus interface that requires the SMBus host to send an Alert Response Address (ARA) to all slaves sharing the $\overline{\text{ALERT}}$ pin in order to isolate clear and service the alerting device. This sequence is described below and in Figure 6.

The sequence of servicing this interrupt is as follows:

1. $\overline{\text{ALERT}}$ is asserted by the aSC7512 driving pin 6 low.
2. The SMBus master begins a read operation with a start followed by the ARA response address, 0001 100. This is an SMBus General Call Address to be used only for requesting an alert response.
3. The device providing the $\overline{\text{ALERT}}$ signal responds to this by providing an ACK followed by its own bus address, an aSC7512 will provide, 101 1000, with the LSB of the data byte set to 1. A NACK response is expected from all devices not giving an $\overline{\text{ALERT}}$.
4. If more than one device responds, the device with the lowest device address will have priority and will be serviced first by the master.
5. The service routine must read the status register of the alerting device to determine the nature of the alert. If the alerting condition is still present, the status bit will remain set, continuing to activate the $\overline{\text{ALERT}}$ pin. If the condition is removed, the status bit will be cleared and an additional ARA will now de-assert the $\overline{\text{ALERT}}$ pin.

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Register Set

Register Address	R/W	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	De-fault Value (hex)	Lock
02h	R	Alert Status	BUSY	LHIGH	LLOW	RHIGH	RLOW	ROPEN	X	X	00	
09h	R/W	Configuration	Alert Mask	Run/ Stop	Alert/ Tach	RES	RES	RES	RES	RES	00	
0Ah	R/W	Conversion Rate	CONV7	CONV6	CONV5	CONV4	CONV3	CONV2	CONV1	CONV0	08	
0Bh	R/W	Zone 2 High Alert Limit	7	6	5	4	3	2	1	0	55	
0Ch	R/W	Zone 2 Low Alert Limit	7	6	5	4	3	2	1	0	00	
0Dh	R/W	Zone 1 High Alert Limit (MS byte)	9	8	7	6	5	4	3	2	55	
0Eh	R/W	Zone 1 Low Alert Limit (MS byte)	9	8	7	6	5	4	3	2	00	
0Fh	R/W	One shot Measurement	RES	RES	RES	RES	RES	RES	RES	RES	00	
10h	R	Zone 1 Temperature (LS Byte)	1	0	X	X	X	X	X	X	00	
11h	R/W	Zone 1 Offset (MS byte)	9	8	7	6	5	4	3	2	00	
12h	R/W	Zone 1 Offset (LS byte)	1	0	RES	RES	RES	RES	RES	RES	00	
13h	R/W	Zone 1 High Alert Limit (LS byte)	1	0	X	X	X	X	X	X	00	
14h	R/W	Zone 1 Low Alert Limit (LS byte)	1	0	X	X	X	X	X	X	00	
15h	R	Zone 2 Temperature (LS Byte)	1	0	X	X	X	X	X	X	00	
22h	R/W	Consecutive Alert	SMB Time-out	RES	RES	RES	Consec Alert 3	Consec Alert 2	Consec Alert 1	Consec Alert 0	01	
25h	R	Zone 1 Temperature	9	8	7	6	5	4	3	2	00	
26h	R	Zone 2 Temperature	9	8	7	6	5	4	3	2	00	
28h	R	Tach LSB	7	6	5	4	3	2	1	0	00	
29h	R	Tach MSB	15	14	13	12	11	10	9	8	00	
30h	R/W	Fan Current PWM Duty	7	6	5	4	3	2	1	0	FF	
3Ah	R/W	Tach Configuration	Tach1 Disable	3-Wire Enable	Meas Blank1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	
3Eh	R	Company ID	7	6	5	4	3	2	1	0	61	
3Fh	R	Version/ Stepping	VER3	VER2	VER1	VER0	STP3	STP2	STP1	STP0	62	
40h	R/W	Ready/Lock/ Start/Override	RES	RES	RES	RES	OVRID	READY	LOCK	START	00	

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Register Address	R/W	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	De-fault Value (hex)	Lock
41h	R	Interrupt Status Register 1	ERR	RES	ZN2	ZN1	RES	RES	RES	RES	00	
42h	R	Interrupt Status Register 2	RES	ERR1	RES	RES	RES	FAN	RES	RES	00	
4Eh	R/W	Zone 1 Low Temperature	7	6	5	4	3	2	1	0	81	
4Fh	R/W	Zone 1 High Temperature	7	6	5	4	3	2	1	0	7F	
50h	R/W	Zone 2 Low Temperature	7	6	5	4	3	2	1	0	81	
51h	R/W	Zone 2 High Temperature	7	6	5	4	3	2	1	0	7F	
54h	R/W	Tach Minimum LSB	7	6	5	4	3	2	1	0	FF	X
55h	R/W	Tach Minimum MSB	15	14	13	12	11	10	9	8	FF	X
5Ch	R/W	Fan Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62	X
5Fh	R/W	Fan Range/ Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X
60h	R/W	Zone 2 Range	RAN3	RAN2	RAN1	RAN0	RES	RES	RES	RES	C3	X
62h	R/W	Min/Off, Zone1 Spike Smoothing	RES	RES	OFF1	RES	ZN1E	ZN1-2	ZN1-1	ZN1-0	00	X
63h	R/W	Zone2 Spike Smoothing	ZN2E	ZN2-2	ZN2-1	ZN2-0	RES	RES	RES	RES	00	X
64h	R/W	Fan PWM Minimum	7	6	5	4	3	2	1	0	80	X
67h	R/W	Zone1 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
68h	R/W	Zone 2 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
6Ah	R/W	Zone 1 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Bh	R/W	Zone 2 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Dh	R/W	Zone 1, Zone 2 Hysteresis	H1-3	H1-2	H1-1	H1-0	H2-3	H2-2	H2-1	H2-0	44	X
75h	R/W	Fan Spin-up Mode	RES	RES	RES	RES	RES	RES	RES	PWM1SU	07	X

Note: Reserved bits will always return 0 when read, X-bits in readings are to be ignored.

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Temperature Measurement

Temperatures are measured with a precision Delta-V_{BE} methodology converted to a digital temperature reading by a 10-bit sigma-delta converter. The user may set limits on these readings to be continuously monitored and alarm bits set when they are exceeded. Separately, the measurements are also delivered to the automatic fan control system to adjust fan speed. The following registers contain the readings from the internal and remote sensors.

Registers 25-10h and 26-15h: Zone Temperature Reading (10-Bit, 2's Complement Reporting)

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
25h	R	Zone 1 Temperature	9	8	7	6	5	4	3	2	00
10h	R	Zone 1 Temperature (LS Byte)	1	0	X	X	X	X	X	X	00
26h	R	Zone 2 Temperature	9	8	7	6	5	4	3	2	00
15h	R	Zone 2 Temperature (LS Byte)	1	0	X	X	X	X	X	X	00

The Zone Temperature registers reflect the current temperature of the internal and remote diodes. Processor (Zone 1) Temp register reports the temperature measured by the thermal diode connected to the Remote - and Remote + pins. Internal (Zone 2) Temp register reports the temperature measured by the internal (junction) temperature sensor. Temperatures are represented as 10 bit, 2's complement, signed numbers, in Celsius, as shown below in Table 1.

The Temperature Reading register will return a value of 8000h if the remote diode pins are not used by the board designer or are not functioning properly. This reading will cause the zone limit bit (bit 4) in the Interrupt Status Register (41h) and the remote diode fault status bit (bit 6) in the Interrupt Status Register 2 (42h) to be set. These registers are read-only – a write to these registers has no effect.

Temperature	Digital Output (2's Complement)				
	High Byte		Low Byte		
	10-Bit Resolution			Ignore	
+125°C	0111	1101	00	XX	XXXX
+100°C	0110	0100	00	XX	XXXX
+50°C	0011	0010	00	XX	XXXX
+25°C	0001	1001	00	XX	XXXX
+10°C	0000	1010	00	XX	XXXX
+1.75°C	0000	0001	11	XX	XXXX
+0.25°C	0000	0000	01	XX	XXXX
0°C	0000	0000	00	XX	XXXX
-1.75°C	1111	1110	01	XX	XXXX
-55°C	1100	1001	00	XX	XXXX

Table 1 Relationship between Temperature and 2's Complement Digital Output, -55°C to +125°C

Temperature Measurement Configuration and ALERT Limits

Registers 09h, 0Ah, 0Fh, 22h: Conversion Rate and ALERT Configuration

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
09h	R/W	Configuration	Alert Mask	Run/ Stop	Alert/ Tach	RES	RES	RES	RES	RES	00
0Ah	R/W	Conversion Rate	CONV7	CONV6	CONV5	CONV4	CONV3	CONV2	CONV1	CONV0	08

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Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
0Fh	R/W	One shot Measurement	RES	RES	RES	RES	RES	RES	RES	RES	00
22h	R/W	Consecutive Alert	SMB Time-out	RES	RES	RES	Consec Alert 3	Consec Alert 2	Consec Alert 1	Consec Alert 0	01

These configuration register settings apply to measurements and alerts reported in registers 25h-10h and 26h-15h temperature readings (10-Bit 2's complement reporting). One-shot Measurement register address 0Fh initiates a temperature measurement when aSC7512 is in Stop mode and returns to that mode after both temperature measurements are complete.

Bit	Name	R/W	Default	Description
0:3	Reserved	R/W	0	Reserved
5	Alert/Tach	R/W	0	Selection between Tach input and ALERT output for pin 6, default is Tach input.
6	Run/Stop	R/W	0	Measurement system run(default) or stop, places aSC7512 in a low-power or standby mode.
7	Alert Mask	R/W	0	Mask alarm conditions from asserting ALERT pin 6 when ALERT function of pin 6 is enabled.

Table 2 Configuration Register [09h] bits

Bit	Name	R/W	Default	Description
3:0	Conversion Rate	R/W	08h	Temperature measurement rate for a set of internal and external readings.

Conversions per Second	Seconds per Conversion	Code (Hex)
0.0625	16	00
0.125	8	01
0.25	4	02
0.5	2	03
1	1	04
2	0.5	05
4	0.25	06
5	0.2	D0
8	0.125	07
16 (default)	0.0625	08
32	0.03125	09
64	0.015625	0A

Table 3 Conversion Rate Register [0Ah] bits

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Bit	Name	R/W	Default	Description
3:0	Consecutive Alert	R/W	000	The number of consecutive out-of-limit measurements required to set the ALERT pin. 1: 000 2: 001 3: 011 4: 111
6	Reserved	R/W	0	Reserved
7	SMBTimeout	R/W	0	Enables a reset of the aSC7512 SMBus interface if it detects SMBus clock stuck low for more than 35 milli-seconds.

Table 4 Consecutive Alert Register [22h] bits

Register 0B-0Eh and 11-14h: ALERT Temperature Limits (Compared to Registers 25h-14h, 26h-15h)

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
0Bh	R/W	Zone 2 High Alert Limit	7	6	5	4	3	2	1	0	55
0Ch	R/W	Zone 2 Low Alert Limit	7	6	5	4	3	2	1	0	00
0Dh	R/W	Zone 1 High Alert Limit (MS byte)	9	8	7	6	5	4	3	2	55
13h	R/W	Zone 1 High Alert Limit (LS byte)	1	0	X	X	X	X	X	X	00
0Eh	R/W	Zone 1 Low Alert Limit (MS byte)	9	8	7	6	5	4	3	2	55
14h	R/W	Zone 1 Low Alert Limit (LS byte)	1	0	X	X	X	X	X	X	00

These limits are compared Zone 1 and Zone 2 registers and trigger the optional $\overline{\text{ALERT}}$ signal pin and status bits that may be enabled in Register 09h, Bit-5. The limits are in binary temperature format representing values from 0 to +127 degrees.

Status Registers

Register 02h: Alert Status Register

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
02h	R	Alert Status	BUSY	LHIGH	LLOW	RHIGH	RLOW	ROPEN	RES	RES	00

The Alert Status Register is a read-only register for reporting the state of the aSC7512's alarms. It is a read-only register located at 02h. When any high or low Zone 1 (remote) limits or high or low Zone 2 (local) limits are exceeded, bits 3 through 6 are set accordingly and the $\overline{\text{ALERT}}$ pin 6 will be driven low. If the remote sensor is open-circuit, bit 2 will be set and the $\overline{\text{ALERT}}$ will be asserted. Reading the status register will re-set these flags if the alerted condition has been removed, however, the $\overline{\text{ALERT}}$ pin will remain asserted until the master has serviced the SMBus alert. This register is read-only – a write to this register has no effect.

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Bit	Name	R/W	Default	Description
1:0	RESERVED	R	0	RESERVED
2	ROPEN	R	0	ZONE 1 (REMOTE) SENSOR OPEN-CIRCUIT
3	RLOW	R	0	ZONE 1 (REMOTE) SENSOR ≤ LOW LIMIT
4	RHIGH	R	0	ZONE 1 (REMOTE) SENSOR > HIGH LIMIT
5	LLOW	R	0	ZONE 2 (LOCAL) SENSOR ≤ LOW LIMIT
6	LHIGH	R	0	ZONE 2 (LOCAL) SENSOR > HIGH LIMIT
7	BUSY	R	0	CONVERTER IN PROCESS OF CONVERSION

Table 5 Alert Status Register

Register 41h: Interrupt Status Register 1

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
41h	R	Interrupt Status 1	ERR	RES	ZN2	ZN1	RES	RES	RES	RES	00

The Interrupt Status Register 1 bits will be automatically set, by the aSC7512, whenever a fault condition is detected. A fault condition is detected whenever a measured value is outside the window set by its limit registers. ZN1 bit will be set when a diode fault condition, such as an open or short, is detected. More than one fault may be indicated in the interrupt register when read. The register will hold a set bit(s) until the event is read by software. The contents of this register will be cleared (set to 0) automatically by the aSC7512 after it is read by software, if the fault condition no longer exists. Once set, the Interrupt Status Register 1 bits will remain set until a read event occurs, even if the fault condition no longer exists. This register is read-only – a write to this register has no effect.

Bit	Name	R/W	Default	Description
3:0	RES	R	0	Reserved
4	Zone 1 Limit Exceeded	R	0	The aSC7512 automatically sets this bit to 1 when the temperature input measured by the Remote1- and Remote1+ inputs is less than or equal to the limit set in the Processor (Zone 1) Low Temp register or more than the limit set in the Processor (Zone 1) High Temp register. This bit will be set when a diode fault is detected.
5	Zone 2 Limit Exceeded	R	0	The aSC7512 automatically sets this bit to 1 when the temperature input measured by the internal temperature sensor is less than or equal to the limit set in the thermal (Zone2) Low Temp register or greater than the limit set in the Internal (Zone2) High Temp register.
6	RES	R	0	Reserved
7	Error in Status Register 2	R	0	If there is a set bit in Status Register 2, this bit will be set to 1.

Table 6 Interrupt Status Register 1

Register 42h: Interrupt Status Register 2

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
42h	R	Interrupt Status 2	RES	ERR1	RES	RES	RES	FAN	RES	RES	00

The Interrupt Status Register 2 bits will be automatically set, by the aSC7512, whenever a fault condition is detected. Interrupt Status Register 2 identifies faults caused by temperature sensor error, fan speed dropping below minimum set by the tachometer minimum register. Interrupt Status Register 2 will hold a set bit until the event is read by software. The contents of this register will be cleared (set to 0) automatically by the aSC7512 after it is read by software, if fault condition no longer exists. Once set, the Interrupt Status Register 2 bits will remain set until a read event occurs, even if the fault no longer exists. This register is read-only – a write to this register has no effect.

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Bit	Name	R/W	Default	Description
0:1	RES	R	0	Reserved
2	FAN STALLED	R	0	The aSC7512 automatically sets this bit to 1 when the TACH1 input reading is above the count value set in the Tach1 Minimum MSB and LSB registers.
5:3	RES	R	0	Reserved
6	Remote Diode Fault	R	0	The aSC7512 automatically sets this bit to 1 when there is an open circuit fault on the Remote1+ or Remote1- thermal diode input pins. A diode fault will also set bit 4 Diode 1 Zone Limit bit, of Interrupt Status Register 1.
7	RES	R	0	Reserved

Table 7 Interrupt Status Register 2

Tachometer Measurement and Configuration

Register 28-29h: Fan Tachometer Reading

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
28h	R	Tach LSB	7	6	5	4	3	2	1	0	N/A
29h	R	Tach MSB	15	14	13	12	11	10	9	8	N/A

The Fan Tachometer Reading registers contains the number of 11.111μs periods (90 kHz) between full fan revolutions. The results are based on the time interval of two tachometer pulses, since most fans produce two tachometer pulses per full revolution. These registers will be updated at least once every second.

The value, for each fan, is represented by a 16-bit unsigned number.

The Fan Tachometer Reading registers will always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional, however, if PWM command (register 30h) is zero, tach measurements are suspended and the last reading may remain in the register.

FF FFh indicates that the fan is not spinning, or that the tachometer input is not connected to a valid signal. These registers are read-only – a write to these registers has no effect.

When the LSByte of the aSC7512 16-bit register is read, the other byte (MSByte) is latched at the current value until it is read. At the end of the MSByte read the Fan Tachometer Reading registers are updated. During spin-up, the PWM duty cycle reported is 0%.

Register 3Ah: Fan Tachometer Measurement Configuration

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
3Ah	R/W	Tach1 Configuration	Tach1 Disable	3-Wire Enable	Meas Blank 1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36

The Fan Tachometer Configuration registers contain the settings that define the modes of measurement of the Tachometer input signal. The user is allowed to disable a tachometer measurement or to request PWM stretching, in the case of a 3-wire fan. Also, the rate, start-up and period of measurements within a fan rotation cycle may be selected. The table below describes the controls.

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Bit	Name	R/W	Default	Description
1:0	Measurement Duration	R/W	10	The amount of fan rotation used for the tach measurement. Assumes 2 pulse periods per rotation of fan. 00: ¼ Rotation – Tach Count x4 = Reported Value 01: ½ Rotation – Tach Count x2 = Reported Value 10: 1 Rotation – Tach Count x1 = Reported Value (default) 11: 2 Rotation – Tach Count x1 = Reported Value
3:2	Measurement Dwell	R/W	01	Delay between Tach Measurements 00: 100 ms 01: 300 ms (default) 10: 500 ms 11: 728 ms
5:4	Measurement Blank	R/W	11	In 3-wire fan mode, a delay is needed to assure that the tach input has stabilized after the PWM has been set to 100% 00: 11.1 µs 01: 22.2 µs 10: 33.3 µs 11: 44.4 µs (default)
6	3-Wire Enable	R/W	0	When high, forces the PWM to stay high for the duration of a tach measurement for a 3-wire fan. This will result in increasing the PWM on-time percentage vs. the value in the PWM register.
7	Tach Disable	R/W	0	Suspends the 90KHz clock for power savings when high.

Table 8 Tachometer Configuration Register

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Automatic Fan Control

Auto Fan Control Operating Mode

The aSC7512 includes the circuitry for automatic fan control. In Auto Fan Mode, the aSC7512 will automatically adjust the PWM duty cycle of the PWM output. PWM outputs are assigned to a thermal zone based on the fan configuration registers. At any time, the temperature of a zone exceeds its absolute limit, all PWM outputs will go to 100% duty cycle to provide maximum cooling to the system.

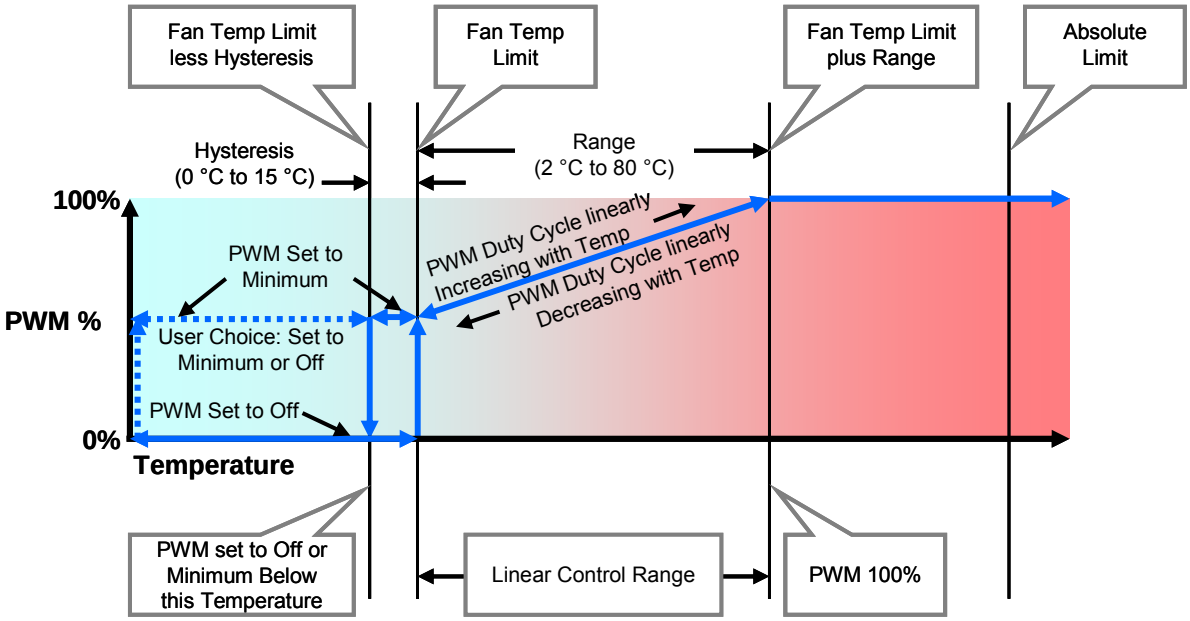


Figure 8 Automatic Fan Speed Control Example

Example for PWM1 assigned to Zone 1:

- Zone 1 Fan Temp Limit (Register 67h) is set to 50°C (32h).
- Zone 1 Range (Register 5Fh) is set to 8°C (6xh).
- Fan PWM Minimum (Register 64h) is set to 50% (32h).

In this case, the PWM duty cycle will be 50% at 50°C.

Since (Zone 1 Fan Temp Limit) + (Zone 1 Range) = 50°C + 8°C = 58°C, the fan will run at 100% duty cycle when the temperature of the Zone 1 sensor reaches 58°C.

Since the midpoint of the fan control range is 54°C, and the median duty cycle is 75% (Halfway between the PWM Minimum and 100%), PWM1 duty cycle would be 75% at 54°C.

Above (Zone 1 Fan Temp Limit) + (Zone 1 Range), the duty cycle will be 100%.

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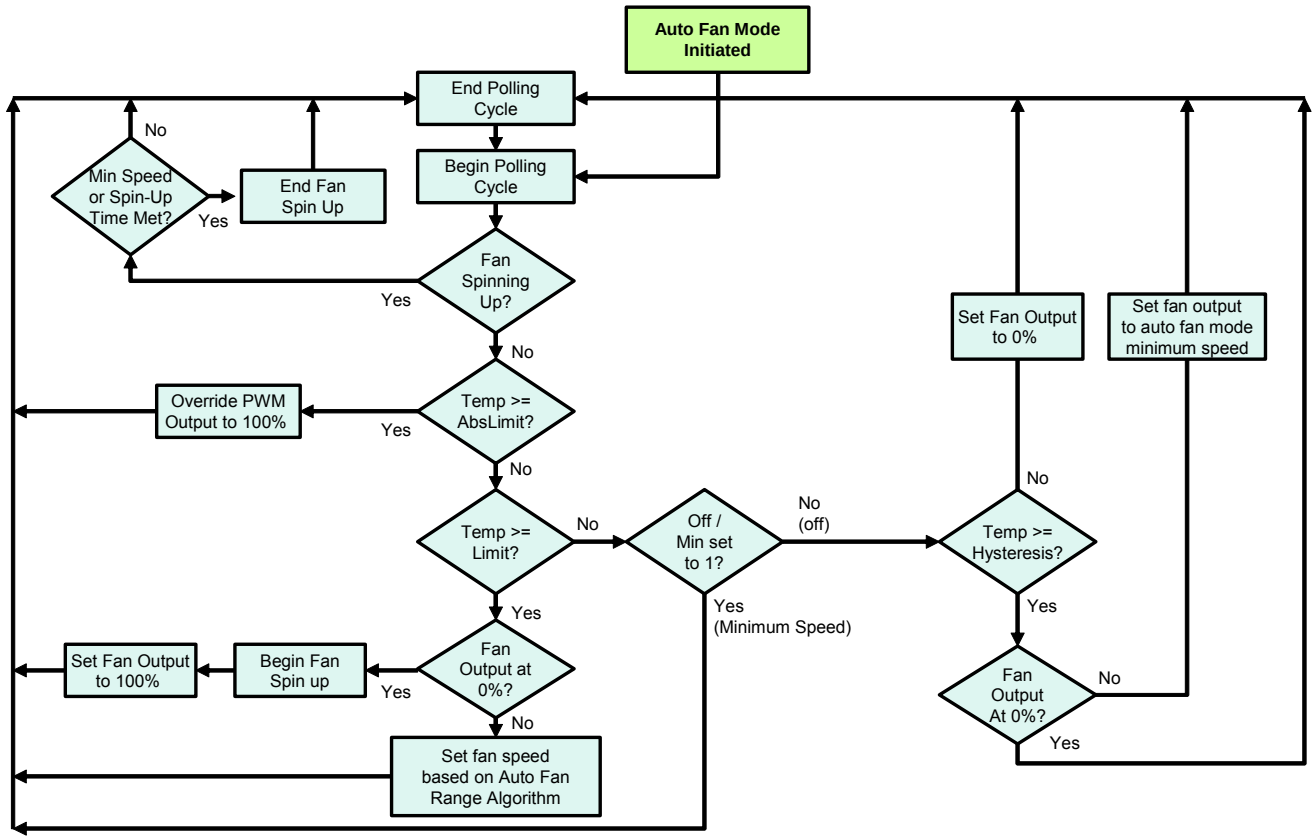


Figure 9 Automatic Fan Control Algorithm

Fan Register Device Set-Up

The BIOS will follow the following steps to configure the fan registers on the aSC7512. The registers corresponding to each function are listed. All steps may not be necessary if default values are acceptable. Regardless of all changes made by the BIOS to the fan limit and parameter registers during configuration, the aSC7512 will continue to operate based on default values until the START bit (bit 0), in the Ready/Lock/Start/Override register (address 40h), is set. Once the fan mode is updated, by setting the START bit to 1, the aSC7512 will operate using the values that were set by the BIOS in the fan control limit and parameter registers (address in the range 5Ch through 6Dh).

1. Set limits and parameters (not necessarily in this order):
   - [5F-60h] Set PWM frequency for the fan and auto fan control range for each zone.
   - [62-63h] Set spike smoothing and min/off.
   - [5Ch] Set the fan spin-up delay.
   - [75h] Set PWM spin-up mode to terminate after time set in [5Ch]. Value = 00h instead of default 01h.
   - [5Ch] Match fan with a corresponding thermal zone.
   - [67-68h] Set the fan temperature limits.
   - [6A-6Bh] Set the temperature absolute limits.
   - [64h] Set the PWM minimum duty cycle.
   - [6Dh] Set the temperature hysteresis values.
2. [40h] Set bit 0 (START) to update fan control and limit register values and start fan control based on these new values.

[40h] (Optional) Set bit 1 (LOCK) to lock the fan limit and parameter registers. **WARNING:** this is a **non-reversible** change in state and locks out further change in critical fan control parameters until power is removed from the aSC7512.

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Register 5F-60h: Auto Fan Speed Range, PWM Frequency

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
5Fh	R/W	Zone 1 Range Fan1 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X
60h	R/W	Zone 2 Range	RAN3	RAN2	RAN1	RAN0	RES	RES	RES	RES	C3	X

In Auto Fan Mode, when the temperature for a zone is above the Temperature Limit (Registers 67-69h) and below its Absolute Temperature Limit (Registers 6A-6Bh), the speed of a fan assigned to that zone is determined as follows:

When the temperature reaches the Fan Temp Limit for a zone, the PWM output assigned to that zone will be Fan PWM Minimum. Between Fan Temp Limit and (Fan Temp Limit + Range), the PWM duty cycle will increase linearly according to the temperature as shown in the figure below. The PWM duty cycle will be 100% at (Fan Temp Limit + Range).

PWM frequency - FRQ[3:0] and HLFRQ

The PWM frequency bits [3:0] determine the PWM frequency for the fan. The aSC7512 has high and low frequency ranges for the PWM outputs that are controlled by the HLFRQ bit.

PWM Frequency Selection (Default = 0011 = 30.04 Hz).

HLFRQ	FRQ [2:0]	PWM Frequency
0	000	10.01 Hz
0	001	15.02 Hz
0	010	23.14 Hz
0	011	30.04 Hz (Default)
0	100	38.16 Hz
0	101	47.06 Hz
0	110	61.38 Hz
0	111	94.12 Hz
1	000	22.5 kHz
1	001	24 kHz
1	010	25.7 kHz
1	011	25.7 kHz
1	100	27.7 kHz
1	101	27.7 kHz
1	110	30 kHz
1	111	30 kHz

Table 9 Register Setting vs PWM Frequency

RAN[3:0]	Linear Control Range (°C)
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16

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RAN[3:0]	Linear Control Range (°C)
1010	20
1011	26.67
1100	32 (default)
1101	40
1110	53.33
1111	80

Table 10 Zone Range Setting, RAN[3:0]

This register becomes Read-Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

Register 40h: Ready/Lock/Start/Override

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
40h	R/W	Ready/Lock/Start/ Override	RES	RES	RES	RES	OVRID	READY	LOCK	START	00

Bit	Name	R/W	Default	Description
0	START	R/W	0	When software writes a 1 to this bit, the aSC7512 fan monitoring and PWM output control functions will use the values set in the fan control limit and parameter registers (address 5Ch through 6Eh). Before this bit is set, the aSC7512 will not update the used register values, the default values will remain in effect. Whenever this bit is set to 0, the aSC7512 fan monitoring and PWM output control functions use the default fan limits and parameters, regardless of the current values in the limit and parameter registers (5C through 6E). The aSC7512 will preserve the values currently stored in the limit and parameter registers when this bit set or cleared. This bit is not affected by the state of the Lock bit. It is expected that all limit and parameter registers will be set by BIOS or application software prior to setting this bit.
1	LOCK	R/W	0	Setting this bit to 1 locks specified limit and parameter registers. **WARNING:** Once this bit is set, limit and parameter registers become read-only and will remain locked **until the device is powered off**. This register bit becomes read-only once it is set.
2	READY	R	0	The aSC7512 sets this bit automatically after the part is fully powered up, has completed the power-up-reset process, and after all A/D converters are properly functioning.
3	OVRID	R/W	0	If this bit is set to 1, all PWM outputs will go to 100% duty cycle regardless of whether or not the lock bit is set. The OVRID bit has precedence over the disabled mode. Therefore, when OVRID is set the PWM will go to 100% even if the PWM is in the disabled mode.
4-7	RESERVED	R	0	Reserved

Table 11 READY / LOCK / START / OVRID Settings

Register 30h: Current PWM Duty Cycle

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
30h	R/W	Fan Current PWM Duty	7	6	5	4	3	2	1	0	N/A

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The Current PWM Duty registers store the current duty cycle at each PWM output. At initial power-on, the PWM duty cycle is 100% and thus, when read, this register will return FFh. After the Ready/Lock/Start/Override register Start bit is set, this register and the PWM signals will be updated based on the algorithm described in the Auto Fan Control Operating Mode section.

When read, the Current PWM Duty registers return the current PWM duty cycle. These registers are read-only unless the fan is in manual (test) mode, in which case a write to these registers will directly control the PWM duty cycle for each fan. The PWM duty cycle is represented as shown in Table 12.

If a 3-wire fan is being used and the option to enable 3-wire tach measurement is selected, the effective PWM duty cycle will be impacted by this feature. The 3-wire Enable setting will hold the PWM signal high for the period taken to make a tachometer reading. This period depends on the RPM and various tachometer measurement parameters. Overall impact is that lower PWM commands will be effectively increased and there may be acoustic effects.

Current PWM %	Register Value		
	Binary		Hex
0%	0000	0000	00
~25%	0100	0000	40
~50% (Default)	1000	0000	80
~75%	1100	0000	C0
100%	1111	1111	FF

Table 12 Current PWM Duty Cycle Setting

Register 4E-51h: Thermal Zone Temperature Limit Registers

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
4Eh	R/W	Zone 1 Low Temp	7	6	5	4	3	2	1	0	81
4Fh	R/W	Zone 1 High Temp	7	6	5	4	3	2	1	0	7F
50h	R/W	Zone 2 Low Temp	7	6	5	4	3	2	1	0	81
51h	R/W	Zone 2 High Temp	7	6	5	4	3	2	1	0	7F

If an external temperature input or the internal temperature sensor either exceeds the value set in the corresponding high limit register or falls below the value set in the corresponding low limit register, the corresponding bit will be set automatically by the aSC7512 in the Interrupt Status Register 1 (41h). For example, if the temperature read from the Remote - and Remote + inputs exceeds the Zone 1 High Temp register limit setting, Interrupt Status Register 1 ZN1 bit will be set. The temperature limits in these registers are represented as 8 bit 2's complement, signed numbers in Celsius, as shown below in Table 13. Setting the Ready/Lock/Start/Override register Lock bit has no effect on these registers.

Temperature	Temperature Limit (2's Complement)	
>127°C	0111	1111
+127°C (Default High)	0111	1111
+125°C	0111	1101
+90°C	0101	1010
+50°C	0011	0010
+25°C	0001	1001
0°C	0000	0000
-50°C	1100	1110
-127°C (Default Low)	1000	0001

Table 13 Zone Temperature High- and Low-Limit Registers - 8-Bit Two's Complement

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Register 54-55h: Fan Tachometer Minimum Limits

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
54h	R/W	Tach Minimum LSB	7	6	5	4	3	2	1	0	FF
55h		Tach Minimum MSB	15	14	13	12	11	10	9	8	FF

The Fan Tachometer Low Limit registers indicate the tachometer reading under which the corresponding bit will be set in the Interrupt Status Register 2 register. In Auto Fan Control mode, the fan can run at low speeds, so care should be taken in software to ensure that the limit is high enough not to cause sporadic alerts. The fan tachometer will not cause a bit to be set in Interrupt Status Register 2 if the current value in Current PWM Duty registers is 00h or if the fan 1 disabled via the Fan Configuration Register. Interrupts will never be generated for a fan if its minimum is set to FF FFh.

Given the relative insignificance of Bit 0 and Bit 1 of Tach Minimum LSB, these bits could be programmed to designate the physical location of the fan generating the tachometer signal, as follows:

Register Name	Bit 1	Bit 0 (LSB)
CPU Cooler	0	0
Memory Controller	0	1
Chassis Front	1	0
Chassis Rear	1	1

Table 14 Fan Location

Setting the Ready/Lock/Start/Override register Lock bit has no effect on these registers.

Register 5Ch: Fan Thermal Zone Assignment and Spin-up Mode

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
5Ch	R/W	Fan Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62	X

This register becomes Read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

Bits [7:5] Zone/Mode

Bits [7:5] of the Fan Configuration registers associate each fan with a temperature sensor. When in Auto Fan Mode the fan will be assigned to a zone, and its PWM duty cycle will be adjusted according to the temperature of that zone. If “Hottest” option is selected (110), the fan will be controlled by the the hotter of zones 1, or 2. To determine the “hotter zone”, the PWM level for each zone is calculated then the zone with the higher PWM value (not temperature) is selected. When in manual control mode, the Current PWM duty register (30h) become Read/Write. It is then possible to control the PWM outputs with software by writing to these registers. When the fan is disabled (100) the corresponding PWM output should be driven low (or high, if inverted).

Zone 1: External Diode (processor)

Zone 2: Internal Sensor

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Fan Configuration	ZON[2:0]
Fan on Zone 1 auto	000
Fan on Zone 2 auto	001
Reserved	010
Fan always on full	011
Fan disabled	100
Fan on Zone 2 auto	101
Fan controlled by hotter of zones 1 or 2	110
Fan manually controlled (Test Mode)	111

Table 15 Fan Zone Setting

Bit [4] PWM Invert

Bit [4] inverts the PWM output. If set to 0, 100% duty cycle will yield an output that is always high. If set to 1, 100% duty cycle will yield an output that is always low.

Bit [3] Reserved

Bit [2:0] Spin Up

Bits [2:0] specify the 'spin up' time for the fan. When a fan is being started from a stationary state, the PWM output is held at 100% duty cycle for the time specified in the table below before scaling to a lower speed.

Spin Up Time	SPIN[2:0]
0 ms	000
100 ms	001
250 ms	010
400 ms	011
700 ms	100
1000 ms	101
2000 ms	110
4000 ms	111

Table 16 Fan Spin-Up Register

Register 62, 63h: Min/Off, Spike Smoothing

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
62h	R/W	Min/Off, Zone1 Spike Smoothing	RES	RES	OFF	RES	ZN1E	ZN1-2	ZN1-1	ZN1-0	00	X
63h	R/W	Zone2 Spike Smoothing	ZN2E	ZN2-2	ZN2-1	ZN2-0	RES	RES	RES	RES	00	X

The Off/Min Bit 5 specifies whether the duty cycle will be 0% or Minimum Fan Duty when the measured temperature falls below the Temperature LIMIT register setting (see Table 18 below).

If the Remote pins are connected to a processor or chipset, instantaneous temperature spikes may be sampled by the aSC7512. Fan speed algorithm has two phases of filtering on temperature zone readings. First, a "No-Spike" value is created from the current temperature and three previous readings. This is an average of the two remaining values when the high and low values are removed. This is the temperature used to determine PWM and is always running.

The second phase is a user specified filter and coefficient. This filter determines a smoothed temperature value, Smooth T_i, by taking the No-Spike T_i, subtracting the previous smoothed temperature, Smooth T_{i-1}, divided by 2^N and adding that to the previously smoothed temperature. N is a user selectable coefficient, in the range 1 to 8, designated ZN1-2:ZN1-0 for Zone 1 and ZN2-2:ZN2-0 for Zone 2.

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For the current temperature reading T_i:

No-Spike T_i = (Discard min and max of (T_i, T_{i-1}, T_{i-2}, T_{i-3}))/2

Smooth T_i = (No-Spike T_i - Smooth T_{i-1})/2^N + Smooth T_{i-1}

If these spikes are not filtered, the CPU fan (if connected to aSC7512) may turn on prematurely or produce unpleasant noise. For this reason, any zone that is connected to a chipset or processor should have spike smoothing enabled. Individual system characteristics will determine how large this coefficient should be.

When spike smoothing is enabled, the temperature reading registers will still reflect the current value of the temperature – not the "smoothed out" value.

ZN1E and ZN2E enable temperature smoothing for zones 1 and 2 respectively.

ZN1-2, ZN1-1 and ZN1-0 control smoothing time for Zone 1.

ZN2-2, ZN2-1 and ZN2-0 control smoothing time for Zone 2.

These registers become read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to these registers shall have no effect.

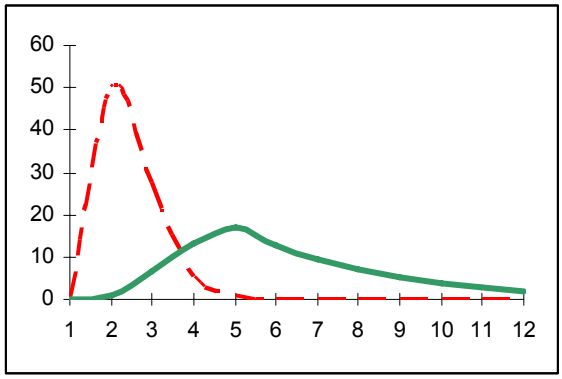


Figure 10 Representation of What Temperature Is Passed to the aSC7512 Auto Fan Control with (green) and without (red dashed) Spike Smoothing

Spike Smoothing Filter Coefficient	ZNn-[2:0]
8	000
7	001
6	010
5	011
4	100
3	101
2	110
1	111

Table 17 Spike Smoothing

PWM Action	Off/Min Bit
At 0% duty below LIMIT	0
At Min PWM Duty below LIMIT	1

Table 18 PWM Output Below Limit Depending on Value of Off/Min

Register 64h: Minimum PWM Duty Cycle

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
64h	R/W	Fan PWM Minimum	7	6	5	4	3	2	1	0	80	X

This register specifies the minimum duty cycle that the PWM will output when the measured temperature reaches the Temperature LIMIT register setting.

This register becomes Read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

Minimum PWM %	Register Value		
	Binary		Hex
0%	0000	0000	00
~25%	0100	0000	40
~50% (Default)	1000	0000	80
~75%	1100	0000	C0
100%	1111	1111	FF

Table 19 Minimum PWM Duty Cycle Setting

Register 67-68h: Temperature Limit

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
67h	R/W	Zone1 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
68h	R/W	Zone2 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X

These are the temperature limits for the individual zones. When the current temperature equals this limit, the fan will be turned on if it is not already. When the temperature exceeds this limit, the fan speed will be increased according to the algorithm set forth in the Auto Fan Range, PWM Frequency register description, Default = 90°C = 5Ah

This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

Temperature	Fan Temp Limit (2's Complement)	
>127°C	0111	1111
+127°C	0111	1111
+125°C	0111	1101
+90°C (default)	0101	1010
+50°C	0011	0010
+25°C	0001	1001
0°C	0000	0000
-50°C	1100	1110
-127°C	1000	0001

Table 20 Fan Temperature Limit Register - 8-Bit Two's Complement

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Register 6A-6Bh: Temperature Limit

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
6Ah	R/W	Zone 1 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Bh	R/W	Zone 2 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X

In the Auto Fan mode, if a zone exceeds the temperature set in the Absolute Temperature Limit register, all of the PWM outputs will increase its duty cycle to 100%. This is a safety feature that attempts to cool the system if there is a potentially catastrophic thermal event. If set to 80h (-128°C), the feature is disabled. Default = 100 C = 64h.

These registers become read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to these registers shall have no effect. After power up the default values are used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to these registers are possible.

Temperature	Absolute Limit (2's Complement)	
>127°C	0111	1111
+127°C	0111	1111
+125°C	0111	1101
+100°C (default)	0110	0100
+50°C	0011	0010
+25°C	0001	1001
0°C	0000	0000
-50°C	1100	1110
-127°C	1000	0001
-128°C (Disable)	1000	0000

Table 21 Absolute Temperature Limit Register - 8-Bit Two's Complement

Register 6Dh: Thermal Zone Hysteresis

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
6Dh	R/W	Zone 1 and Zone 2 Hysteresis	H1-3	H1-2	H1-1	H1-0	H2-3	H2-2	H2-1	H2-0	44	X

If the temperature is above Fan Temp Limit, then drops below Fan Temp Limit, the following will occur:

- The fan will remain on, at Fan PWM Minimum, until the temperature goes a certain amount below Fan Temp Limit.
- The Hysteresis registers control this amount. See below table for details.

This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to these registers shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

Temperature	Zone Hysteresis Hn-[3:0]
0°C	0000
1°C	0001
4°C (default)	0100
10°C	1010
15°C	1111

Table 22 Zone Hysteresis Register Format

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Register 75h: Fan Spin-Up Mode

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
75h	R/W	Fan Spin-Up Mode	RES	RES	RES	RES	RES	RES	RES	PWM SU	07	X

The PWM SU bit configures the PWM spin-up mode. If PWM SU is cleared the spin-up time will terminate after time programmed by the Fan Configuration register has elapsed. When set to 1, the spin-up time will terminate early if the TACH reading exceeds the Tach Minimum value or after the time programmed by the Fan Configuration register has elapsed, which ever occurs first.

This register becomes Read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect. After power up the default value is used whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

Miscellaneous Registers

Register 3Eh, FEh: Company ID

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
3Eh	R	Company ID	7	6	5	4	3	2	1	0	61

The company ID register contains the company identification number. For Andigilog this is 61h. This number is assigned by Intel and is a method for uniquely identifying the part manufacturer. This register is read-only – a write to this register has no effect.

Register 3Fh: Version/Stepping

Register Address	Read/ Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
3Fh	R	Version/Stepping	VER3	VER2	VER1	VER0	STP3	STP2	STP1	STP0	62

The four least significant bits of the Version/Stepping register [3:0] contain the current stepping of the aSC7512 silicon. The four most significant bits [7:4] reflect the aSC7512 base device number when set to a value of 0110b. For the aSC7512, this register will read 01101000b (62h).

The register is used by application software to identify which device in the hardware monitor family has been implemented in the given system. Based on this information, software can determine which registers to read from and write to. Further, application software may use the current stepping to implement work-around for bugs found in a specific silicon stepping.

This register is read-only – a write to this register has no effect.

Register 70-7Fh: Vendor Specific Registers

These registers are for vendor specific features, including test registers. They will not default to a specific value on power up.

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Applications Information

Remote Diodes

The aSC7512 is designed to work with a variety of remote sensors in the form of the substrate thermal diode of a CPU or graphics controller or a diode-connected transistor. Actual diodes are not suited for these measurements.

There is some variation in the performance of these diodes, described in terms of its departure from the ideal diode equation. This factor is called diode non-ideality, nf.

The equation relating diode temperature to a change in thermal diode voltage with two driving currents is:

$$\Delta V_{BE} = (nf)\frac{KT}{q}ln(N)$$

where:

nf = diode non-ideality factor, (nominal 1.008).
K = Boltzman's constant, (1.38 x 10^{-23}).
T = diode junction temperature in Kelvins.
q = electron charge (1.6 x 10^{-19} Coulombs).
N = ratio of the two driving currents (16).

The aSC7512 is designed and trimmed for an expected nf value of 1.008, based on the typical value for the Intel Pentium™ III and AMD Athlon™. There is also a tolerance on the value provided. The values for other CPUs and the 2N3904 may have different nominal values and tolerances. Consult the CPU or GPU manufacturer's data sheet for the nf factor. Table 23 gives a representative sample of what one may expect in the range of non-ideality. The trend with CPUs is for a lower value with a larger spread.

When thermal diode has a non-ideality factor other than 1.008 the difference in temperature reading at a particular temperature may be interpreted with the following equation:

$$T_{actual} = T_{reported}\left(\frac{1.008}{n_{actual}}\right)$$

where:

$T_{reported}$ = reported temperature in temperature register.
T_{actual} = actual remote diode temperature.
n_{actual} = selected diode's non-ideality factor, nf .
Temperatures are in Kelvins or °C + 273.15.

This equation assumes that the series resistance of the remote diode is the same for each. This resistance is given in the data sheet for the CPU and may vary from 2.5Ω to 4.5Ω.

Although the temperature error caused by non-ideality difference is directly proportional to the difference from 1.008, but a small difference in non-ideality results in a relatively large difference in temperature reading. For example, if there were a ±1% tolerance in the non-Ideality of a diode it would result in a ±2.7 degree difference (at 0°C) in the result (0.01 x 273.15).

This difference varies with temperature such that a fixed offset value may only be used over a very narrow range. Typical correction method required when measuring a wide range of temperature values is to scale the temperature reading in the host firmware.

Part	nf Min	nf Nom	nf Max	Series Res
Pentium™ III (CPUID 68h)	1.0057	1.008	1.0125	
Pentium 4, 130nM	1.001	1.002	1.003	3.64
Pentium 4, 90nM		1.011		3.33
Intel Pentium M	1.0015	1.0022	1.0029	3.06
AMD Athlon™ Model 6	1.002	1.008	1.016	
AMD Duron™ Models 7 and 8	1.002	1.008	1.016	
AMD Athlon Models 8 and 10	1.0000	1.0037	1.0090	
2N3904	1.003	1.0046	1.005	

Table 23 Representative CPU Thermal Diode and Transistor Non-Ideality Factors

CPU or ASIC Substrate Remote Diodes

A substrate diode is a parasitic PNP transistor that has its collector tied to ground through the substrate and the base (D-) and emitter (D+) brought out to pins. Connection to these pins is shown in Figure 11. The non-ideality figures in Table 23 include the effects of any package resistance and represent the value seen from the CPU socket. The temperature indicated will need to be compensated for the departure from a non-ideality of 1.008.

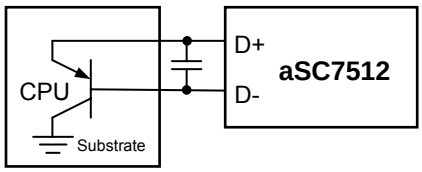


Figure 11 CPU Remote Diode Connection

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Series Resistance

Any external series resistance in the connections from the aSC7512 to the CPU pins should be accounted for in interpreting the results of a measurement.

The impact of series resistance on the measured temperature is a result of measurement currents developing offset voltages that add to the diode voltage. This is relatively constant with temperature and may be corrected with a fixed value in the offset register. To determine the temperature impact of resistance is as follows:

$$\Delta T_R = R_S \times \Delta I_D / T_V$$

or,

$$\Delta T_R = R_S \times \frac{90\mu A}{230\mu V/°C} = R_S \times 0.391°C/\Omega$$

where:

ΔT_R = difference in the temperature reading from actual.

R_S = total series resistance of interconnect (both leads).

ΔI_D = difference in the two diode current levels (90µA).

T_V = scale of temperature vs. V_{BE} (230µV/°C).

For example, a total series resistance of 10Ω would give an offset of +3.9°C.

Discrete Remote Diodes

When sensing temperatures other than the CPU or GPU substrate, an NPN or PNP transistor may be used. Most commonly used are the 2N3904 and 2N3906. These have characteristics similar to the CPU substrate diode with non-ideality around 1.0046. They are connected with base to collector shorted as shown in Figure 12.

While it is important to minimize the distance to the remote diode to reduce high-frequency noise pickup, they may be located many feet away with proper shielding. Shielded, twisted-pair cable is recommended, with the shield connected only at the aSC7512 end as close as possible to the ground pin of the device.

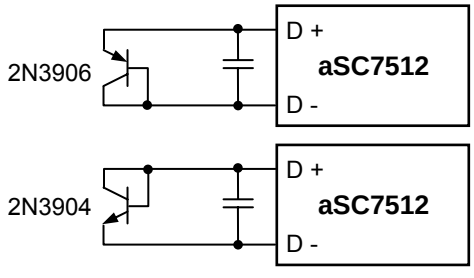


Figure 12 Discrete Remote Diode Connection

As with the CPU substrate diode, the temperature reported will be subject to the same errors due to non-ideality variation and series resistance. However, the transistor's die temperature is usually not the temperature of interest and care must be taken to minimize the thermal resistance and physical distance between that temperature and the remote diode. The offset and response time will need to be characterized by the user.

Board Layout Considerations

The distance between the remote sensor and the aSC7512 should be minimized. All wiring should be defended from high frequency noise sources and a balanced differential layout maintained on D+ and D-.

Any noise, both common-mode and differential, induced in the remote diode interconnect may result in an offset in the temperature reported. Circuit board layout should follow the recommendation of Figure 13. Basically, use 10-mil lines and spaces with grounds on each side of the differential pair. Choose the ground plane closest to the CPU when using the CPU's remote diode.



Figure 13 Recommended Remote Diode Circuit Board Interconnect

Noise filtering is accomplished by using a bypass capacitor placed as close as possible to the aSC7512 D+ and D- pins. A 1.0nF ceramic capacitor is recommended, but up to 3.3nF may be used. Additional filtering takes place within the aSC7512.

It is recommended that the following guidelines be used to minimize noise and achieve highest accuracy:

1. Place a 0.1µF bypass capacitor to digital ground as close as possible to the power pin of the aSC7512.
2. Match the trace routing of the D+ and D- leads and use a 1.0nF filter capacitor close to the aSC7512. Use ground runs along side the pair to minimize differential coupling as in Figure 13.
3. Place the aSC7512 as close to the CPU or GPU remote diode leads as possible to minimize noise and series resistance.
4. Avoid running diode connections close to or in parallel with high-speed busses, staying at least 2cm away.
5. Avoid running diode connections close to on-board switching power supply inductors.
6. PC board leakage should be minimized by maintaining minimum trace spacing and covering traces over their full length with solder mask.

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Thermal Considerations

The temperature of the aSC7512 will be close to that of the PC board on which it is mounted. Conduction through the leads is the primary path for heat flow. The reported local sensor is very close to the circuit board temperature and typically between the board and ambient.

In order to measure PC board temperature in an area of interest, such as the area around the CPU where voltage regulator components generate significant heat, a remote diode-connected transistor should be used. A surface-mount SOT-23 or SOT-223 is recommended. The small size is advantageous in minimizing response time because of its low thermal mass, but at the same time it has low surface area and a high thermal resistance to ambient air. A compromise must be achieved between minimizing thermal mass and increasing the surface area to lower the junction-to-ambient thermal resistance.

In order to sense temperature of air-flows near board-mounted heat sources, such as memory modules, the sensor should be mounted above the PC board. A TO-92 packaged transistor is recommended.

The power consumption of the aSC7512 is relatively low and should have little self-heating effect on the local sensor reading. At the highest measurement rate the dissipation is less than 2mW, resulting in only a few tenths of a degree rise.

Evaluation Board

The aSC7511/aSC7512EVB provides a platform for evaluation of the operational characteristics of the aSC7511 and aSC7512. The board features a graphical user interface (GUI) to control and monitor all activities and readings of the aSC7511. The provided software will run on a Windows XP™-based desktop or laptop PC with a USB port.

In addition to being a self-contained fan speed control demonstration, it may be connected into an operating PC's fan and CPU diode to evaluate various settings under real operating conditions without the need to adjust BIOS code. After optimization, the settings may be programmed into the system.

Features:

- Interactive GUI for setting limits and operational configuration
- aSC7512 Automatic Fan Control
- Powered and operated from the USB port
- Graphical readouts:
  - Temperature and alarms
  - Fan RPM
  - Automatic fan control state
- Selectable on-board 2N3904 or wired remote diode
- Headers for 2-, 3- and 4-wire fans
- Customizable Log file of readings
- Saving of register setting configurations
- LED indicator of pin state
- Optional use of external 12V fan power for higher current fans
- Optional connection to off-board SMBus clients

Application Diagrams

The aSC7512 may be easily adapted to two-, three- or 4-wire fans for precise, wider-range fan speed control when compared to variable DC drive. Pin 6 may optionally be used as $\overline{\text{ALERT}}$, pulled up to 3.3V with a 10K resistor to warn the system of an extreme condition needing immediate attention in any fan configuration.

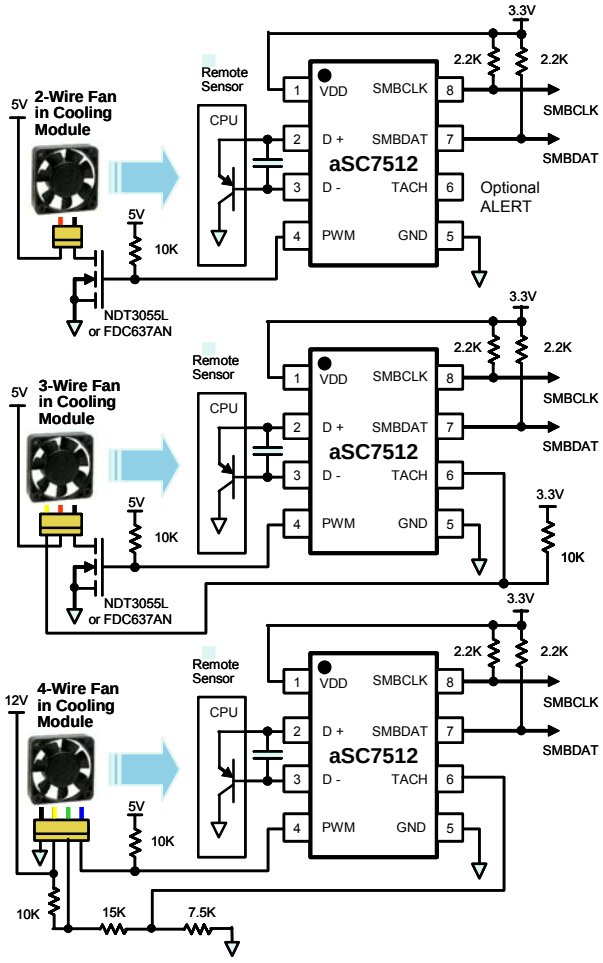


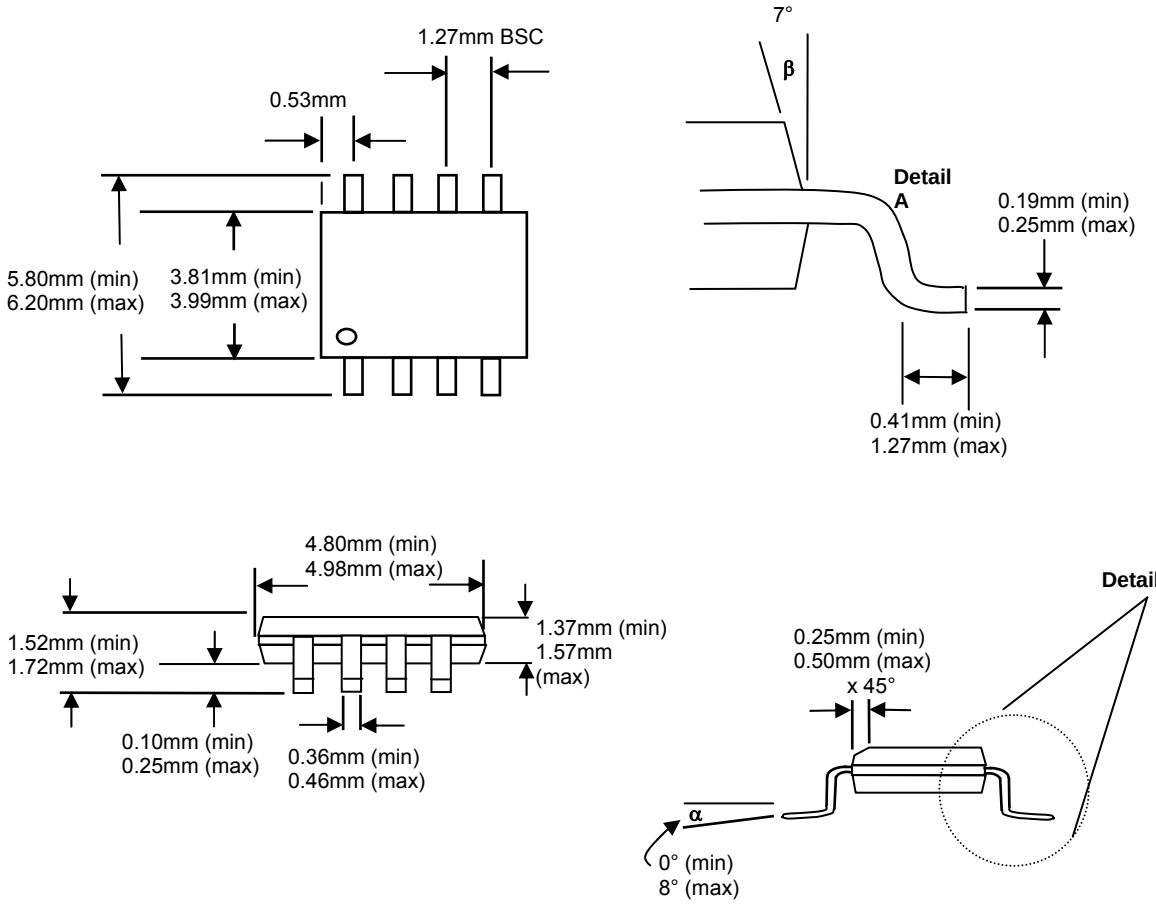
Figure 14 aSC7512 2-, 3- and 4-Wire Fan Connections

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Physical Dimensions in millimeters unless otherwise noted:

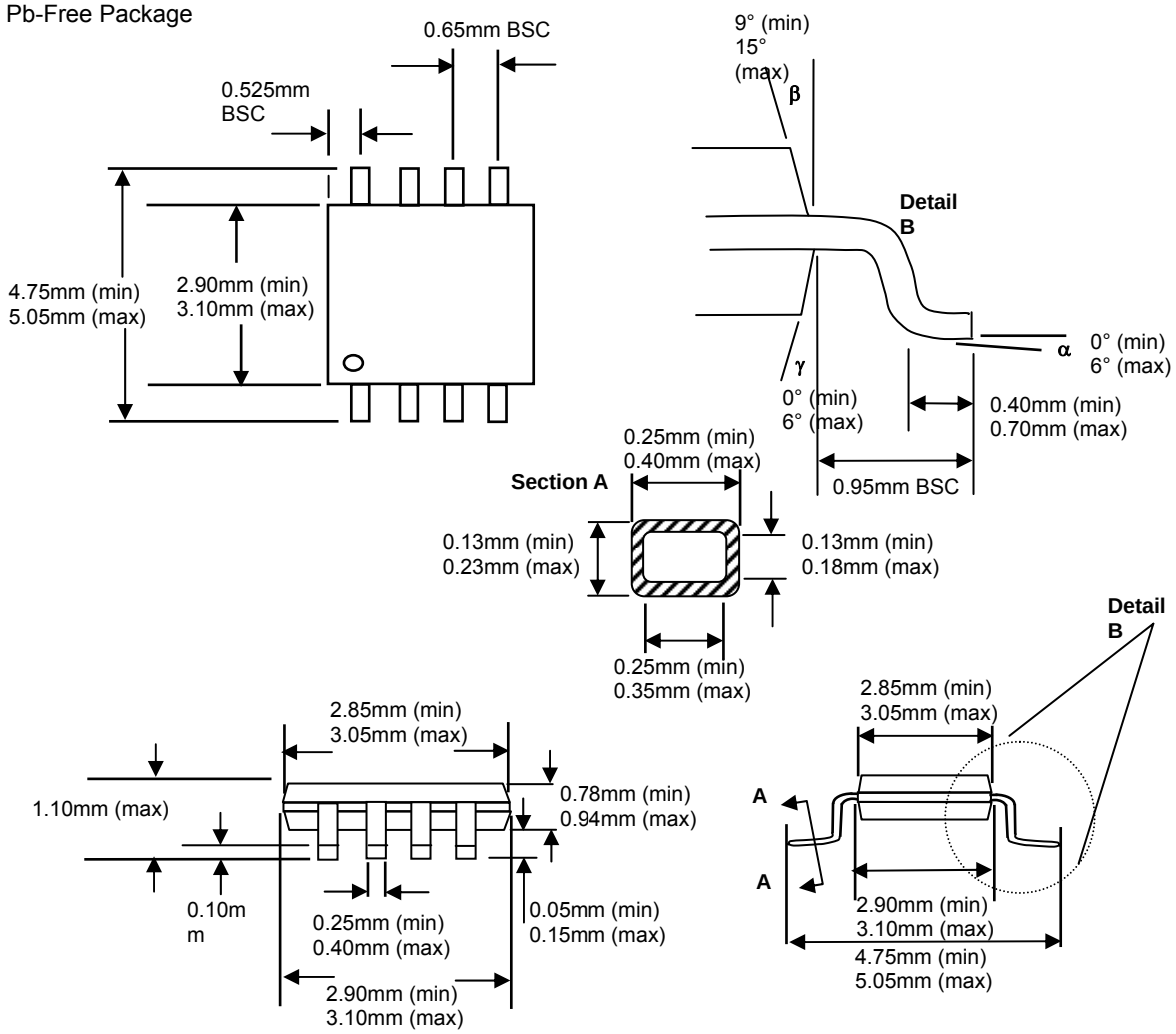
D8 Package – 8-Lead SOP Package Dimensions

Pb-Free Package



M8 Package – 8-Lead MSOP Package Dimensions

Pb-Free Package



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Data Sheet Classifications

Preliminary Specification

This classification is shown on the heading of each page of a specification for products that are either under development (design and qualification), or in the formative planning stages. Andigilog reserves the right to change or discontinue these products without notice.

New Release Specification

This classification is shown on the heading of the first page only of a specification for products that are either under the later stages of development (characterization and qualification), or in the early weeks of release to production. Andigilog reserves the right to change the specification and information for these products without notice.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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