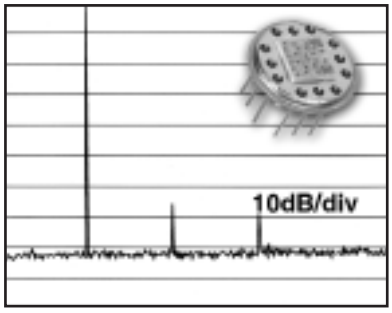
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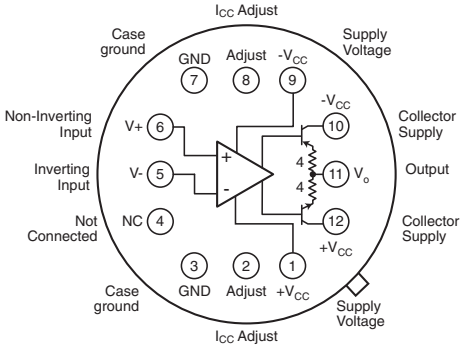
KH232
Low Distortion Wideband Op Amp

Features
- -69dBc 2nd and 3rd harmonics at 20MHz
- -3dB bandwidth of 270MHz
- 0.05% settling in 15ns
- 3000V/µs slew rate
- 1mV input offset voltage, 10µV/°C drift
- ±10V, 100mA max output
- Direct replacement for CLC232

Applications
- Flash A/D drivers
- DAC current-to-voltage conversion
- Wide dynamic range IF amps
- VCO drivers
- DDS postamps
- Radar/communication receivers
- Precision line drivers



Bottom View



Pins 2 and 8 are used to adjust the supply current or to adjust the offset voltage (see text). These pins are normally left unconnected.

General Description
The KH232 is a wideband low distortion operational amplifier designed specifically for high speed, low gain applications requiring wide dynamic range. Utilizing a current feedback architecture, the KH232 offers high speed performance while maintaining DC precision.

The KH232 offers precise gains from ±1 to ±5 with a true 0.1% linearity and provides stable, oscillation-free operation across the entire gain range without external compensation. The KH232, a pin compatible enhanced version of the KH231, reduces 2nd and 3rd harmonic distortion to an extremely low -69dBc at 20MHz ($2V_{pp}$, R_L = 100Ω). Additional features provided by the KH232 include a small signal bandwidth of 270MHz, a large signal bandwidth of 95MHz and a 3000V/µs slew rate. The input offset voltage is typically 1mV with an input offset drift of 10µV/°C.

The KH232 combines these high performance features with its 0.05% settling time of 15ns and its 100mA drive capability to provide high speed, high resolution A/D and D/A converter systems with an attractive solution for driving and buffering. Wide dynamic range systems such as radar and communication receivers requiring low harmonic distortion and low noise will find the KH232 to be an excellent choice. As a line driver, the KH232 set at a gain of 2 cancels matched line losses.

The KH232 is constructed using thin film resistor/bipolar transistor technology, and is available in the following versions:

KH232AI	-25°C to +85°C	12-pin TO-8 can
KH232AK	-55°C to +125°C	12-pin TO-8 can, features burn-in & hermetic testing
KH232AM	-55°C to +125°C	12-pin TO-8 can, environmentally screened and electrically tested to MIL-STD-883
KH232HXC	-55°C to +125°C	SMD#: 5962-9166501HXC
KH232HXA	-55°C to +125°C	SMD#: 5962-9166501HXA

Typical Performance

	Gain Setting						
Parameter	1	2	5	-1	-2	-5	**Units**
-3dB bandwidth	430	270	135	220	175	110	MHz
rise time (2V)	1.8	2.0	2.5	2.0	2.2	2.9	ns
slew rate	2.5	3.0	3.0	3.0	3.0	3.0	V/ns
settling time (to 0.1%)	12	12	12	12	12	15	ns

KH232 Electrical Characteristics (T_A = +25°C, A_V = +2V, V_{CC} = ±15V, R_L = 100Ω, R_f = 250Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MIN & MAX RATINGS			UNITS	SYM
Ambient Temperature	KH232AI	+25°C	-25°C	+25°C	+85°C		
Ambient Temperature	KH232AK/AM/HXC/HXA	+25°C	-55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
† -3dB bandwidth (note 2)	V_o ≤0.63V_{pp}	270	>200	>200	>200	MHz	SSBW
	V_o ≤2V_{pp}	165	>145	>145	>120	MHz	SSBW
large-signal bandwidth	V_o ≤10V_{pp}	95	>80	>80	>60	MHz	FPBW
gain flatness (note 2)	V_o ≤0.63V_{pp}						
† peaking	0.1 to 50MHz	0.1	<0.6	<0.3	<0.6	dB	GFPL
† peaking	>50MHz	0.1	<1.5	<0.3	<0.8	dB	GFPH
† rolloff	at 100MHz	0.4	<0.6	<0.6	<1.0	dB	GFR
group delay	to 100MHz	3.5 ± 0.5	–	–	–	ns	GD
linear phase deviation	to 100MHz	0.5	<2.0	<2.0	<2.0	°	LPD
reverse isolation							
non-inverting		53	>43	>43	>43	dB	RINI
inverting		36	>26	>26	>26	dB	RIIN
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.0	<2.4	<2.3	<2.7	ns	TRS
	10V step	5.0	<7.0	<6.5	<6.5	ns	TRL
settling time to 0.05%	5V step	15	–	–	–	ns	TS
to 0.1%	2.5V step	12	<22	<17	<22	ns	TSP
overshoot	5V step	5	<15	<10	<15	%	OS
slew rate (overdriven input)		3.0	>2.5	>2.5	>1.8	V/ns	SR
overload recovery	<1% error						
<50ns pulse, 200% overdrive		120	–	–	–	ns	OR
NOISE AND DISTORTION RESPONSE							
† 2nd harmonic distortion	$2V_{pp}$, 20MHz	-69	<-64	<-64	<-56	dBc	HD2
† 3rd harmonic distortion	$2V_{pp}$, 20MHz	-69	<-64	<-64	<-64	dBc	HD3
equivalent input noise							
voltage	>100kHz	2.8	<3.2	<3.2	<3.5	nV/√Hz	VN
inverting current	>100kHz	20	<23	<23	<25	pA/√Hz	ICN
non-inverting current	>100kHz	2.3	<2.6	<2.6	<2.9	pA/√Hz	NCN
noise floor	>100kHz	-155	<-154	<-154	<-153	dBm(1Hz)	SNF
integrated noise	1kHz to 200MHz	57	<64	<64	<72	µVrms	INV
integrated noise	5MHz to 200MHz	57	<64	<64	<72	µVrms	INV
STATIC, DC PERFORMANCE							
* input offset voltage		1	<4.0	<2.0	<4.5	mV	VIO
average temperature coefficient		10	<25	<25	<25	µV/°C	DVIO
* input bias current	non-inverting	5.0	<29	<21	<31	µA	IBN
average temperature coefficient		50	<125	<125	<125	nA/°C	DIBN
* input bias current	inverting	10	<31	<15	< 35	µA	IBI
average temperature coefficient		125	<200	<200	<200	nA/°C	DIBI
* power supply rejection ratio		50	>45	>45	>45	dB	PSRR
common mode rejection ratio		46	>40	>40	>40	dB	CMRR
* supply current	no load	25	<27	<27	<29	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance	DC	400	>100	>200	>400	kΩ	RIN
non-inverting input capacitance		1.3	<2.5	<2.5	<2.5	pF	CIN
output impedance	@ 100MHz	5, 37	–	–	–	Ω, nH	RO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{CC}	±20V
I_o	±100mA
common mode input voltage, V_o	$\|V_{CC}\|$ >15V ±(30-$\|V_{CC}\|$)V
	$\|V_{CC}\|$ ≤15V ±$\|V_{CC}\|$V
differential input voltage	±3V
thermal resistance	(see thermal model)
junction temperature	+175°C
operating temperature	AI: -25°C to +85°C
	AK/AM/HXC/HXA: -55°C to +125°C
storage temperature	-65°C to +150°C
lead temperature (soldering 10s)	+300°C

Recommended Operating Conditions

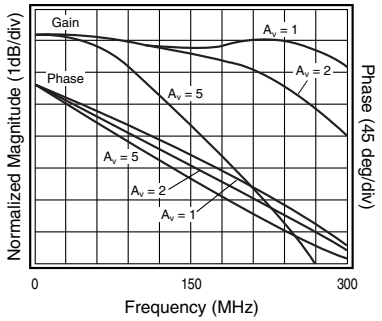
V_{CC}	±5V to ±15V
I_o	±75mA
common mode input voltage	±($\|V_{CC}\|$ -5)V
gain range	±1 to ±5

note 1: * AI/AK/AM/HXC/HXA 100% tested at +25°C
† AK/AM/HXC/HXA 100% tested at +25°C and sample tested at -55°C and +125°C
† AI sample tested at +25°C

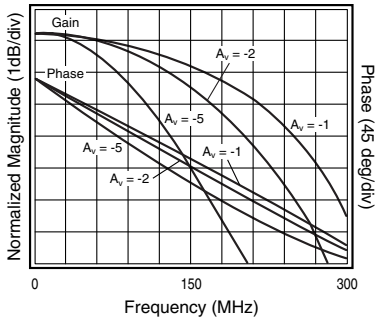
note 2: The output amplitude used in testing is 0.63V_{pp}. Performance is guaranteed for conditions listed.

KH232 Typical Performance Characteristics (T_A = +25°C, A_v = +2, V_{CC} = ±15V, R_L = 100Ω, R_f = 250Ω; unless specified)

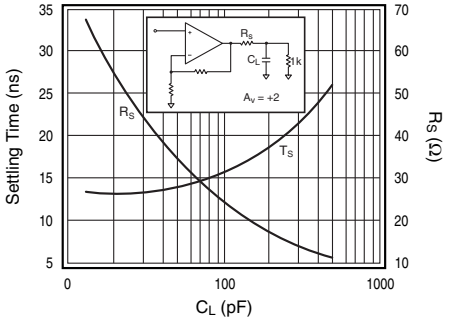
Non-Inverting Frequency Response



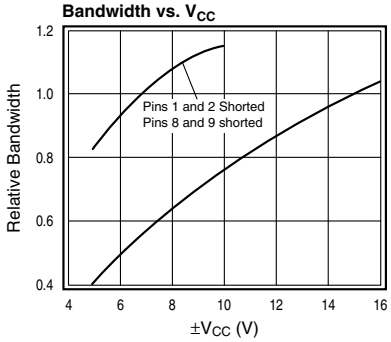
Inverting Frequency Response



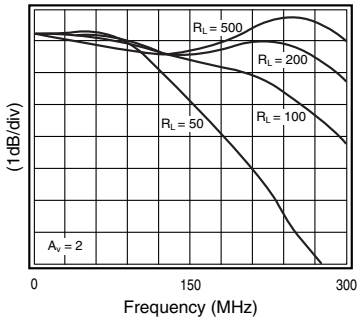
Settling Time vs. C_L



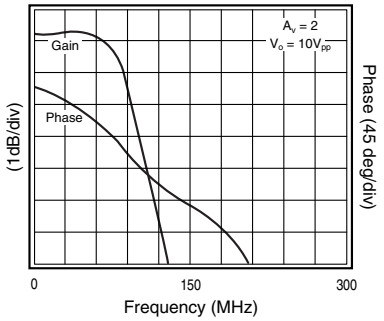
Bandwidth vs. V_{CC}



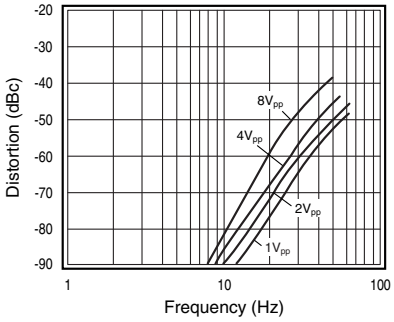
Frequency Response vs. R_L



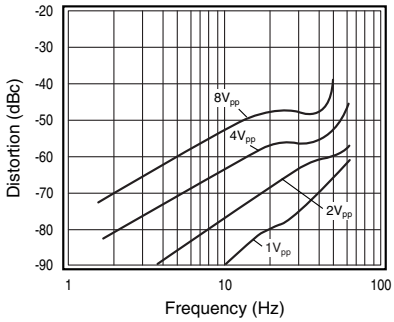
Large Signal Non-Inverting Gain & Phase



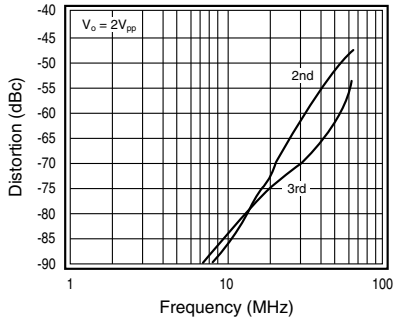
2nd Harmonic Distortion



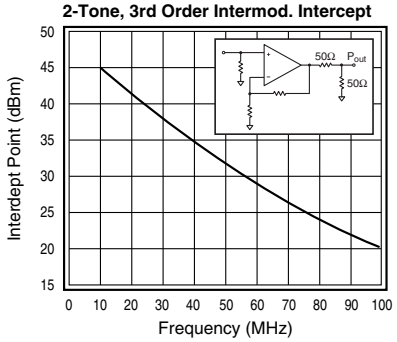
3rd Harmonic Distortion



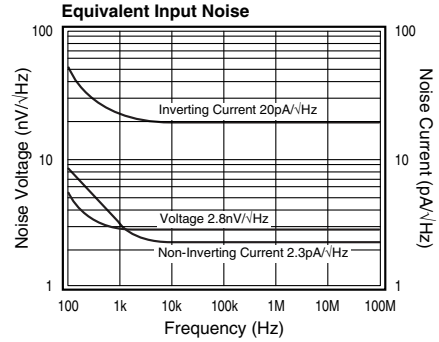
2nd and 3rd Harmonic Distortion



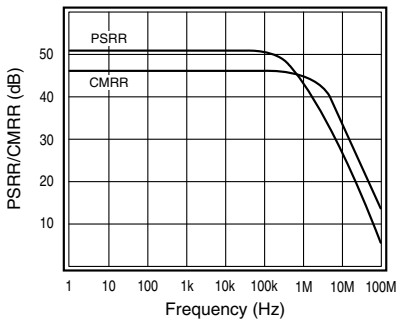
2-Tone, 3rd Order Intermod. Intercept



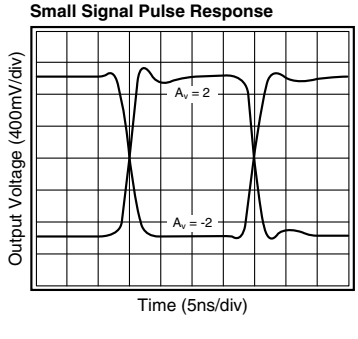
Equivalent Input Noise



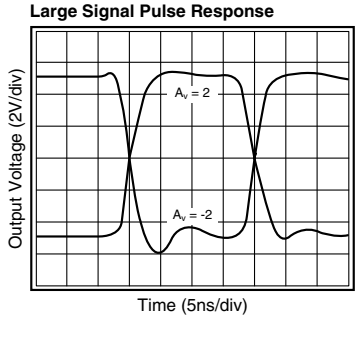
CMRR and PSRR



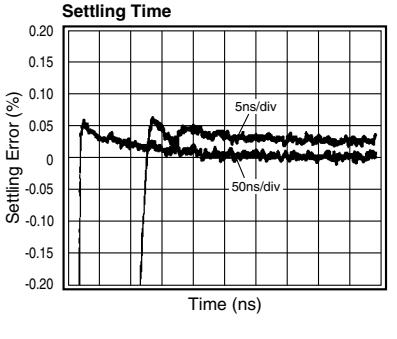
Small Signal Pulse Response



Large Signal Pulse Response



Settling Time



Operation

The KH232 is based on the current feedback op amp topology, a design that uses current feedback instead of the usual voltage feedback.

The use of the KH232 is basically the same as that of the conventional op amp (see Figures 1 and 2). Since the device is designed specifically for low gain applications, the best performance is obtained when the circuit is used at gains between ±1 and ±5. Additionally, performance is optimum when a 250Ω feedback resistor is used.

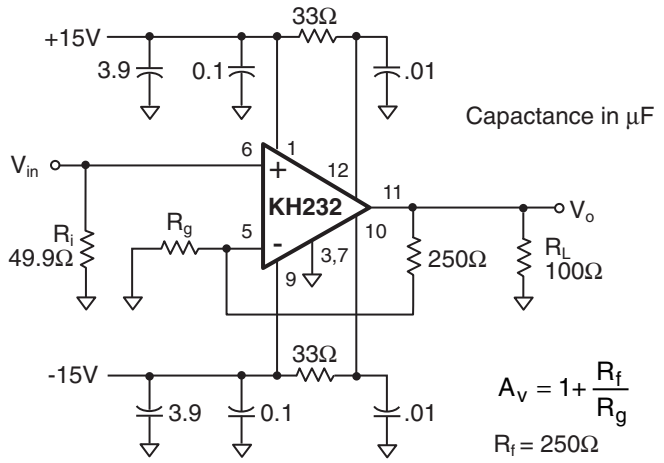


Figure 1: Recommended non-inverting gain circuit

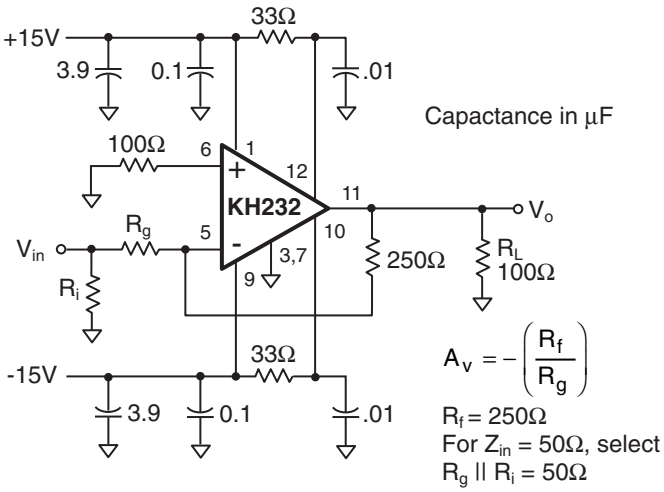


Figure 2: Recommended inverting gain circuit

Layout Considerations

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial bread-boarding of the circuit use direct point to point wiring, keeping the lead lengths to less than 0.25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

During pc board layout keep all traces short and direct The resistive body of R_g should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of 0.01 to 0.1µf (with short leads) should be less than 0.15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins. V_{CC} connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in figures 1 and 2. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip or coaxial cable when the signal must traverse more than a few inches.

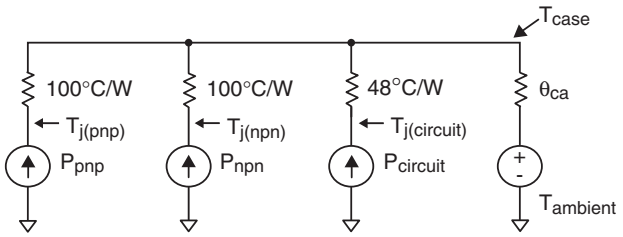
Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase. Evaluation boards designed for either inverting or non-inverting gains are available.

Offset Voltage Adjustment

If trimming of the input offset voltage ($V_{os} = V_{ni} - V_{in}$) is desired, a resistor value of 10kΩ to 1MΩ placed between pins 8 and 9 will cause V_{os} to become more negative by 8mV to 0.2mV respectively. Similarly, a resistor placed between pins 1 and 2 will cause V_{os}, to become more positive.

Thermal Considerations

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. Use the thermal model on the previous page to determine junction temperatures. Many styles of heat sinks are available for TO-8 packages; the Thermalloy 2240 and 2268 are good examples. Some heat sinks are the radial fin type which cover the pc board and may interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance. For use of these heat sinks with conventional components, a 0.1" high spacer can be inserted under the TO-8 package to allow sufficient clearance.



$P_{(circuit)} = (I_{CC})((+V_{CC}) - (V_{CC}))$ where I_{CC} = 14mA at ±15V

$P_{(xxx)} = [(\pm V_{CC}) - V_{out} - (I_{col})\ (R_{col} + 4)]\ (I_{col})\ (\%Duty)$

For positive V_o and V_{CC}, this is the power in the npn device. For negative V_o and V_{CC}, this is the power in the pnp device.

$I_{col} = V_o/R_L$ or 12mA, whichever is greater. (Include feedback R in R_L.)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{CC}$.

The limiting factor for output current and voltage is junction temperature. Of secondary importance is $I_{(out)}$, which should not exceed 150mA.

$T_{j(pnp)} = P_{(pnp)}\ (100 + \theta_{ca}) + (P_{(cir)} + P_{(npn)})(\theta_{ca}) + T_a$, similar for $T_{j(npn)}$.

$T_{j(cir)} = P_{(cir)}(48 + \theta_{ca}) + (P_{(pnp)} + P_{(npn)})(\theta_{ca}) + T_a$.

θ_{ca} = 65°C/W for the KH232 without heat sink in still air.
35°C/W for the KH232 with a Thermalloy 2268A heat sink in still air.
15°C/W for the KH232 with a Thermalloy 2268A heat sink at 300 ft/min air.
(Thermalloy 2240A works equally as well.)

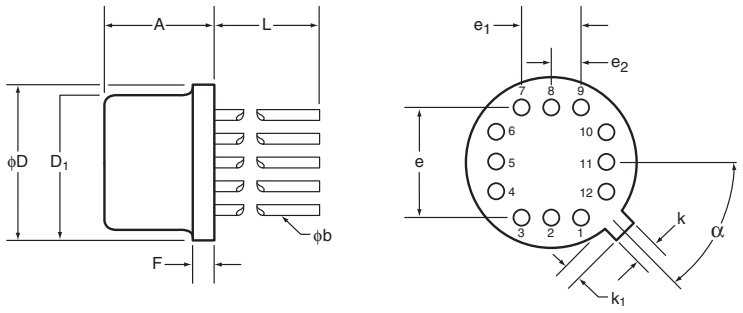
For example, with the KH232 operating at ±15V while driving a 100Ω load at $15V_{pp}$ output (50% duty cycle pulse waveform, DC = 0), $P_{(npn)} = P_{(pnp)}$ = 190mW (R_{col} = 33) and $P_{(cir)}$ = 0.42W. Then with the Thermalloy 2268 heat sink and air flow of 300 ft/min the output transistors' T_j is 31°C above ambient and worst case T_j in the rest of the circuit is 32°C above ambient. In still air, however, the rise in T_j is 47°C and 48°C, respectively. With no heat sink, the rise in T_j is 71°C and 72°C, respectively! Under most conditions, **HEAT SINKING IS REQUIRED**.

Other methods of heat sinking may be used, but for best results, make contact with the base of the KH232 package, use a large thermal capacity heat sink and use forced air convection.

Low V_{CC} Operation: Supply Current Adjustment

The KH232 is designed to operate on supplies as low as ±5V. In order to improve full bandwidth at reduced supply voltages, the supply current (I_{CC}) must be increased. The plot of Bandwidth vs. V_{CC}, shows the effect of shorting pins 1 and 2 and pins 8 and 9; this will increase both bandwidth and supply current. Care should be taken to not exceed the maximum junction temperatures; for this reason this technique should not be used with supplies exceeding ±10V. For intermediate values of V_{CC}, external resistors between pins 1 and 2 and pins 8 and 9 can be used.

KH232 Package Dimensions



TO-8				
SYMBOL	INCHES		MILIMETERS	
	Minimun	Maximum	Minimum	Maximum
A	0.142	0.181	3.61	4.60
ϕb	0.016	0.019	0.41	0.48
ϕD	0.595	0.605	15.11	15.37
ϕD_1	0.543	0.555	13.79	14.10
e	0.400 BSC		10.16 BSC	
e_1	0.200 BSC		5.08 BSC	
e_2	0.100 BSC		2.54 BSC	
F	0.016	0.030	0.41	0.76
k	0.026	0.036	0.66	0.91
k_1	0.026	0.036	0.66	0.91
L	0.310	0.340	7.87	8.64
α	45° BSC		45° BSC	

NOTES:

Seal: cap weld
Lead finish: gold per MIL-M-38510
Package composition:
Package: metal
Lid: Type A per MIL-M-38510

Life Support Policy
Cadeka's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Cadeka Microcircuits, Inc. As used herein:

1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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