LM96080 System Hardware Monitor with 2-Wire Serial Interface

Check for Samples: LM96080

FEATURES

- **Local Temperature Sensing**
- **7 Positive Voltage Inputs with 10-bit Resolution**
- **2 Programmable Fan Speed Monitoring Inputs**
- **2.5 mV LSb and 2.56V Input Range**
- **Chassis Intrusion Detector Input**
- **WATCHDOG Comparison of All Monitored Values**
- **Separate Input to Show Status in Interrupt Status Register of Additional External Temperature Sensors Such as the LM26/27, LM56/57, LM73, or LM75**
- **I^2C Serial Bus Interface Compatibility, Supports Standard Mode, 100 kbits/s, and Fast Mode, 400 kbits/s**
- **Shutdown Mode to Minimize Power Consumption**
- **Programmable $\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ Pin: $\overline{\text{RST\_OUT}}$ Provides a Reset Output; $\overline{\text{OS}}$ Provides an Interrupt Output Activated by an Overtemperature Shutdown Event**
- **Software and Pin Compatible with the LM80**

APPLICATIONS

- **Communications Infrastructure**
- **System Thermal and Hardware Monitoring for Servers**
- **Electronic Test Equipment and Instrumentation**
- **Office Electronics**

KEY SPECIFICATIONS

- **Total Unadjusted Error ±1 %FS (Max)**
- **Differential Non-Linearity ±1 Lsb (Max)**
- **Supply Voltage Range +3.0 V to +5.5 V**
- **Supply Current (Operating) 0.370 mA Typ**
- **Supply Current (Shutdown) 0.330 mA Typ**
- **ADC Resolution 10 Bits**
- **Temperature Resolution 0.5°C/0.0625°C**
- **Temperature Accuracy ±3°C (Max)**

DESCRIPTION

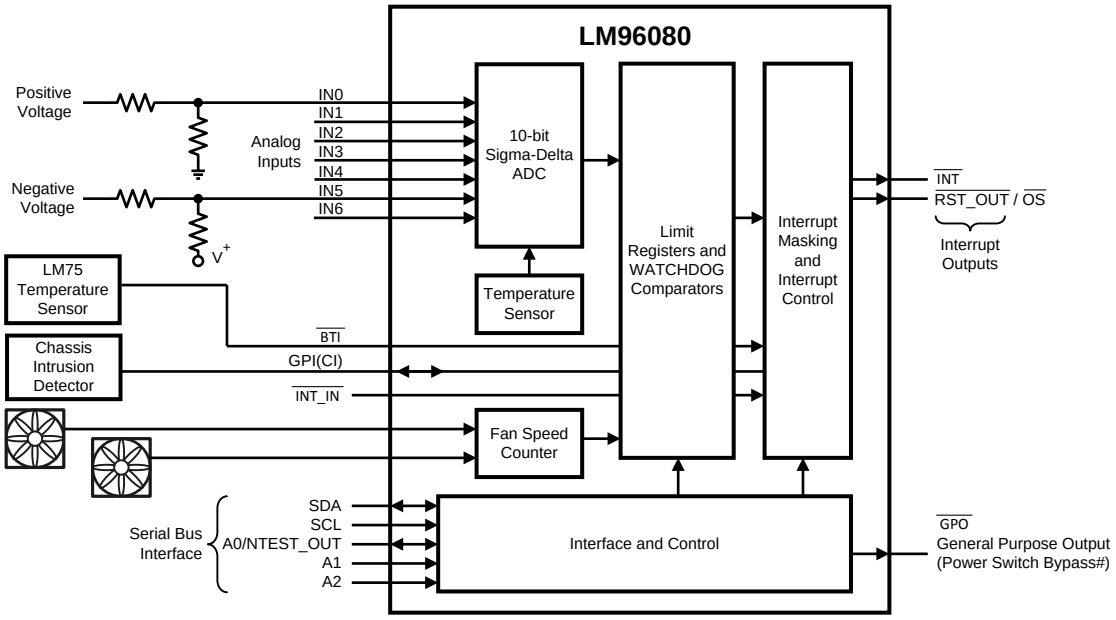
LM96080, compatible to LM80, is a hardware monitor that contains a 10-bit delta-sigma ADC capable of measuring 7 positive voltages and local temperature. The LM96080 also measures the speed of two fans and includes other hardware monitoring on an I^2C® interface. The LM96080 includes a sequencer that performs WATCHDOG window comparisons of all measured values and its interrupt outputs become active when any values exceed the programmed limits.

The LM96080 is especially suited to interface to both linear and digital temperature sensors. The 2.5 mV LSb (least significant bit) and 2.56 volt input range is ideal for accepting inputs from a linear sensor such as the LM94022. The $\overline{\text{BTI}}$ is used as an input from either digital or thermostat sensors such as LM73, LM75, LM56, LM57, LM26, LM27, LM26LV, or other LM96080.

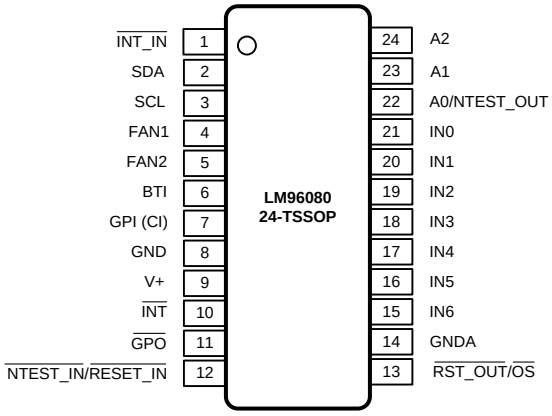
The LM96080 supports Standard Mode (Sm, 100 kbits/s) and Fast Mode (Fm, 400 kbits/s) I^2C interface modes of operation. LM96080 includes an analog filter on the I^2C digital control lines that allows improved noise immunity and supports TIMEOUT reset function on SDA and SCL that prevents I^2C bus lockup. Three I^2C device address pins allow up to 8 parts on a single bus.

The LM96080's 3.0V to 5.5V supply voltage range, low supply current, and I^2C interface make it ideal for a wide range of applications. Operation is ensured over the temperature range of $(-40)°C \le T_A \le +125°C$. The LM96080 is available in a 24-pin TSSOP package.

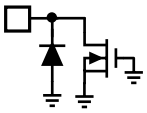
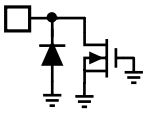
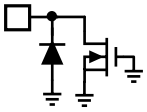
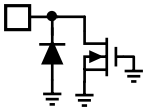
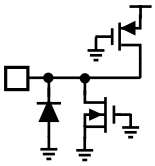
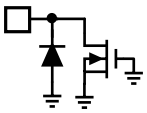
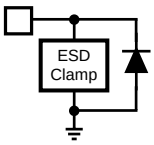
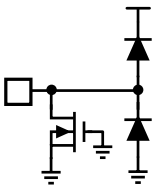
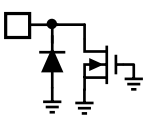
Typical Application



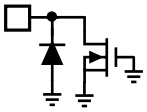
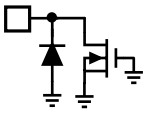
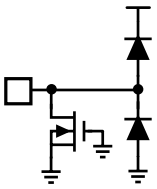
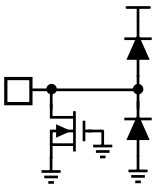
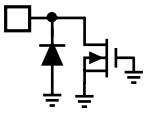
Connection Diagram



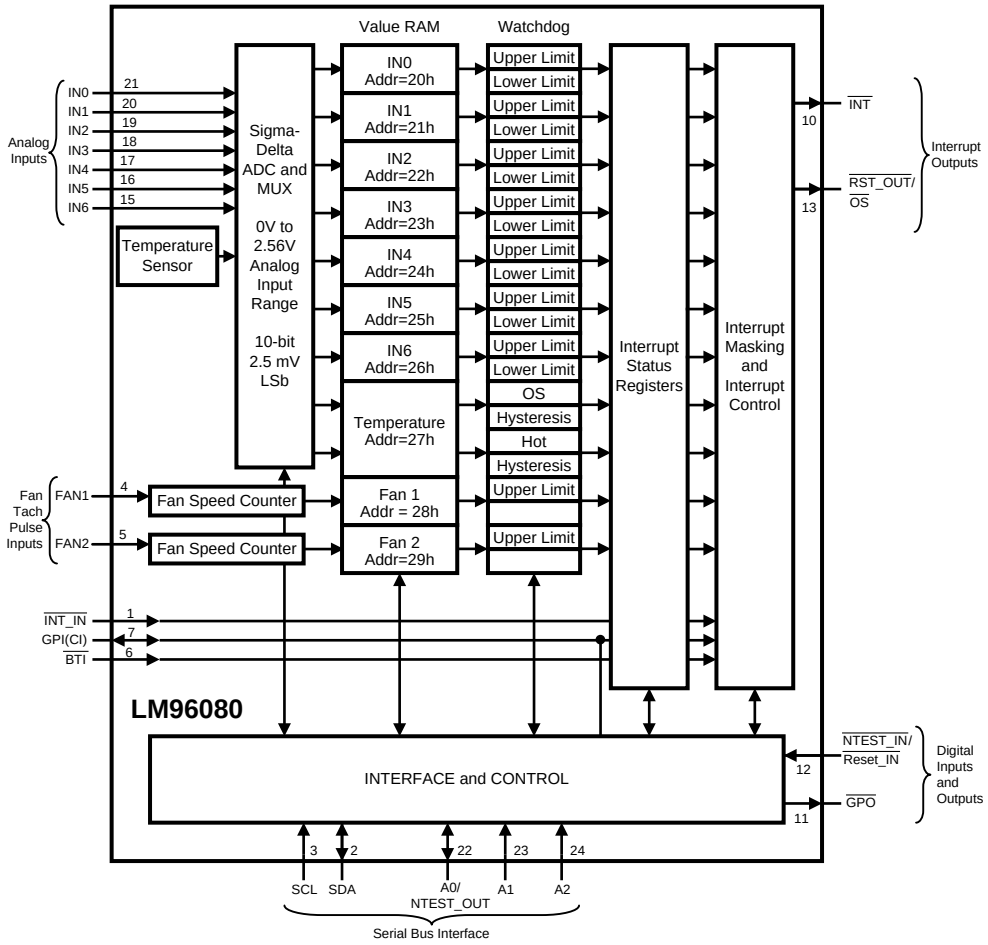
PIN DESCRIPTIONS

Pin Number	Pin Name(s)	ESD Structure	Type	Description
1	$\overline{\text{INT\_IN}}$		Digital Input	Interrupt Input Bar. This is an active low input that propagates the $\overline{\text{INT\_IN}}$ signal to the $\overline{\text{INT}}$ output of the LM96080.
2	SDA		Digital I/O	Serial Bus Bidirectional Data. NMOS open-drain output.
3	SCL		Digital Input	Serial Bus Clock.
4-5	FAN1, FAN2		Digital Inputs	Fan tachometer inputs.
6	$\overline{\text{BTI}}$		Digital Input	Board Temperature Interrupt driven by Overtemperature Shutdown (O.S.) outputs of additional temperature sensors such as LM75. This pin provides internal pull-up of 10 kΩ.
7	GPI (Chassis Intrusion)		Digital I/O	General Purpose Input pin. GPI can be used as an additional active high interrupt input pin or as an active high input from an external circuit which latches a Chassis Intrusion event.
8	GND		GROUND	Internally connected to all of the digital circuitry.
9	V^+		POWER	+3.0V to +5.5V power. Bypass with the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors.
10	$\overline{\text{INT}}$		Digital Output	Non-Maskable Interrupt (Active High, PMOS, open-drain) or Interrupt Request (Active Low, NMOS, open-drain). Whenever $\overline{\text{INT\_IN}}$, $\overline{\text{BTI}}$, or GPI interrupts, this output pin becomes active.
11	$\overline{\text{GPO}}$ ($\overline{\text{Power Switch}}$ $\overline{\text{Bypass}}$)		Digital Output	General Purpose Output pin is an active low NMOS open drain output intended to drive an external power PMOS for software power control or can be utilized to control power to a cooling fan.

PIN DESCRIPTIONS (continued)

Pin Number	Pin Name(s)	ESD Structure	Type	Description
12	$\overline{\text{NTEST\_IN}}$/ $\overline{\text{RESET\_IN}}$		Digital Input	An active-low input that enables NAND Tree board-level connectivity testing. Whenever NAND Tree connectivity is enabled, the LM96080 resets to its power on state.
13	$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$		Digital Output	This pin is an NMOS open drain output. $\overline{\text{RST\_OUT}}$ provides a master reset to devices connected to this line. $\overline{\text{OS}}$ is dedicated to the temperature reading WATCHDOG.
14	GNDA		GROUND	Internally connected to all analog circuitry. The ground reference for all analog inputs. This pin needs to be taken to a low noise analog ground plane for optimum performance.
15-21	IN6-IN0		Analog Inputs	0V to 2.56V full scale range Analog Inputs.
22	A0/NTEST_OUT		Digital I/O	The lowest order bit of the Serial Bus Address. This pin also functions as an output when doing a NAND Tree test.
23-24	A1-A2		Digital Inputs	The two highest order bits of the Serial Bus Address.

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3]

Supply Voltage (V^+)		6.0V
Voltage on SCL, SDA, $\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$, GPI (CI), $\overline{\text{GPO}}$, $\overline{\text{NTEST\_IN}}$/$\overline{\text{RESET\_IN}}$, $\overline{\text{INT\_IN}}$, FAN1 and FAN2		(−0.3)V to +6.0V
Voltage on Other Pins		(−0.3)V to (V^+ + 0.3V) and ≤ 6.0V
(GND - GNDA)		±300 mV
Input Current at Any Pin[4]		±5 mA
Package Input Current[4]		±30 mA
Maximum Junction Temperature (T_J max)		150°C
ESD Susceptibility[5]	Human Body Model	3000V
	Machine Model	300V
	Charged Device Model	1000V
Storage Temperature		(−65)°C to +150°C
For soldering specifications, see http://www.ti.com/lit/SNOA549[6]		

(1) All voltages are measured with respect to GND, unless otherwise specified
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN}< (GND or GNDA) or V_{IN}>V^+), the current at that pin should be limited to 5 mA. The 30 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to six pins. Parasitic components and/or ESD protection circuitry are shown in the Pin Descriptions table.
(5) Human body model (HBM) is a charged 100 pF capacitor discharged into a 1.5 kΩ resistor. Machine model (MM), is a charged 200 pF capacitor discharged directly into each pin. Charged Device Model (CDM) simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.
(6) Reflow temperature profiles are different for packages containing lead (Pb) than for those that do not..

Operating Ratings[1][2]

Supply Voltage (V^+)	+3.0V to +5.5V
Voltage on SCL, SDA, $\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$, GPI (CI), $\overline{\text{GPO}}$, $\overline{\text{NTEST\_IN}}$/$\overline{\text{RESET\_IN}}$, $\overline{\text{INT\_IN}}$, FAN1 and FAN2	(−0.05)V to +5.5V
Voltage on Other Pins	(−0.05)V to (V^+ + 0.05)V and ≤ 5.5V
|GND − GNDA|	≤ 100 mV
V_{IN} Voltage Range	(−0.05)V to (V^+ + 0.05)V
Temperature Range for Electrical Characteristics	(−40)°C ≤ T_A ≤ +125°C
Operating Temperature Range	(−40)°C ≤ T_A ≤ +125°C
Junction to Ambient Thermal Resistance (θ_{JA}[3])	
Package Number: PW	95°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND, unless otherwise specified
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J$max, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J\text{max} - T_A)/\theta_{JA}$.

DC Electrical Characteristics

The following specifications apply for +3.0 V_{DC} ≤ V^+ ≤ +5.5 V_{DC} , IN0-IN6, R_S = 25Ω, unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.(1)

Symbol	Parameter	Conditions	Typical(2)	Limits(3)	Units (Limits)
POWER SUPPLY CHARACTERISTICS					
V^+	Supply Voltage		+3.3 +5.0	**+3.0** **+5.5**	V (min) V(max)
I^+	Supply Current (Interface Inactive). (See SUPPLY CURRENT (I^+) for the I^+ equation).	Round robin conversion, V^+= 5.5V	0.430	**0.580**	mA (max)
		Round robin conversion, V^+= 3.8V	0.370	**0.520**	mA (max)
		Shutdown mode, V^+= 5.5V	0.400	**0.540**	mA (max)
		Shutdown mode, V^+= 3.8V	0.330	**0.480**	mA (max)
TEMPERATURE-to-DIGITAL CONVERTER CHARACTERISTICS					
	Temperature Error	(−40)°C ≤ T_A ≤ +125°C (−25)°C ≤ T_A ≤ +100°C		**±3** **±2**	°C (max) °C (max)
	Resolution			**0.0625**	°C (min)
ANALOG-to-DIGITAL CONVERTER CHARACTERISTICS					
n	Resolution (10 bits with full-scale at 2.56V)		2.5		mV
TUE	Total Unadjusted Error	See(4)		**±1**	% (max)
DNL	Differential Non-Linearity	See(5)		**±1**	LSb (max)
PSS	Power Supply Sensitivity		±0.05		% / V
t_C	Total Monitoring Cycle Time	See(6)	728	**662** **810**	ms (min) ms (max)
MULTIPLEXER/ADC INPUT CHARACTERISTICS					
R_{ON}	On Resistance		2	**10**	kΩ (max)
I_{ON}	Input Current (On Channel Leakage Current)		±0.005		µA
I_{OFF}	Off Channel Leakage Current		±0.005		µA
FAN RPM-to-DIGITAL CONVERTER					
	Fan RPM Error	(–40)°C ≤ T_A ≤ +125°C		**±10**	% (max)
	Internal Clock Frequency	(–40)°C ≤ T_A ≤ +125°C	22.5	**20.2** **24.8**	kHz (min) kHz (max)
	FAN1 and FAN2 Nominal Input RPM (See FAN INPUTS)	Divisor = 1, Fan Count = 153(7)	8800		RPM
		Divisor = 2, Fan Count = 153(7)	4400		RPM
		Divisor = 3, Fan Count = 153(7)	2200		RPM
		Divisor = 4, Fan Count = 153(7)	1100		RPM
	Full-scale Count			**255**	(max)
DIGITAL OUTPUTS: A0/NTEST_OUT, $\overline{INT}$					
$V_{OUT(1)}$	Logical “1” Output Voltage	I_{OUT} = +5.0 mA at V^+ = +4.5V, I_{OUT} = +3.0 mA at V^+ = +3.0V		**2.4**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{OUT} = +5.0 mA at V^+ = +4.5V, I_{OUT} = +3.0 mA at V^+ = +3.0V		**0.4**	V (max)

(1) Each input and output is protected by an ESD structure to GND, as shown in the Pin Descriptions table. Input voltage magnitude up to 0.3V above V^+ or 0.3V below GND will not damage the LM96080. There are parasitic diodes that exist between some inputs and the power supply rails. Errors in the ADC conversion can occur if these diodes are forward biased by more than 50 mV. As an example, if V^+ is 4.50 V_{DC}, input voltage must be ≤ 4.55 V_{DC}, to ensure accurate conversions.
(2) Typicals are at T_J= T_A= 25°C and represent most likely parametric norm.
(3) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(4) TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC.
(5) Limit is Specified by Design.
(6) Total Monitoring Cycle Time includes temperature conversion, 7 analog input voltage conversions and 2 tachometer readings. For more information on the conversion rates, refer to the description of bit 0, register 07h in REGISTERS AND RAM.
(7) The total fan count is based on 2 pulses per revolution of the fan tachometer output.

DC Electrical Characteristics (continued)

The following specifications apply for +3.0 V_{DC} ≤ V^+ ≤ +5.5 V_{DC} , IN0-IN6, R_S = 25Ω, unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.(1)

Symbol	Parameter	Conditions	Typical(2)	Limits(3)	Units (Limits)
OPEN DRAIN OUTPUTS: $\overline{GPO}$, $\overline{RST\_OUT}$ / $\overline{OS}$, GPI (CI)					
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{OUT} = +5.0 mA at V^+ = +4.5V, I_{OUT} = +3.0 mA at V^+ = +3.0V		**0.4**	V (min)
I_{OH}	High Level Output Current	V_{OUT} = V^+	0.005	**1**	µA (max)
	$\overline{RST\_OUT}$/$\overline{OS}$, GPI (CI) Pulse Width		22.5	10	ms (min)
OPEN DRAIN SERIAL BUS OUTPUT: SDA					
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{OUT} = +3.0 mA at V^+ = +3.0V		**0.4**	V (min)
I_{OH}	High Level Output Current	V_{OUT} = V^+	0.005	**1**	µA (max)
DIGITAL INPUTS: A0/NTEST_Out, A1-A2, $\overline{BTI}$, GPI (Chassis Intrusion), $\overline{INT\_IN}$, and $\overline{NTEST\_IN}$ / $\overline{Reset\_IN}$					
$V_{IN(1)}$	Logical “1” Input Voltage			**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage			**0.8**	V (max)
VHYST	Hysteresis Voltage	V^+ = +3.3V	0.23		V
		V^+ = +5.5V	0.33		V
SERIAL BUS INPUTS (SCL, SDA)					
$V_{IN(1)}$	Logical “1” Input Voltage			**0.7 × V^+**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage			**0.3 × V^+**	V (max)
V_{HYST}	Hysteresis Voltage	V^+ = +3.3V	0.67		V
		V^+ = +5.5V	1.45		V
FAN TACH PULSE INPUTS (FAN1, FAN2)					
$V_{IN(1)}$	Logical “1” Input Voltage			**0.7 × V^+**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage			**0.3 × V^+**	V (max)
V_{HYST}	Hysteresis Voltage	V^+ = +3.3V	0.35		V
		V^+ = +5.5V	0.5		V
ALL DIGITAL INPUTS Except for $\overline{BTI}$					
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = V^+	−0.005	**−1**	µA (min)
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0 V_{DC}	0.005	**1**	µA (max)
C_{IN}	Digital Input Capacitance		20		pF
$\overline{BTI}$ Digital Input					
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = V^+	−1	**−10**	µA (min)
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0 V_{DC}, V^+= +5.5 V	1	**2**	mA
C_{IN}	Digital Input Capacitance		20		pF

AC Electrical Characteristics

The following specifications apply for +3.0 V_{DC} ≤ V^+ ≤ +5.5 V_{DC} , unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.(1)

Symbol	Parameter	Conditions	Typical(2)	Limits(3)	Units (Limits)
SERIAL BUS TIMING CHARACTERISTICS					
t_1	SCL (Clock) Period			**2.5** **100**	µs (min) µs (max)
t_2	Data In Setup Time to SCL High			**100**	ns (min)
t_3	Data Out Stable After SCL Low			**0**	ns (min)
t_4	SDA Low Setup Time to SCL Low (start)			**100**	ns (min)
t_5	SDA High Hold Time After SCL High (stop)			**100**	ns (min)
$t_{TIMEOUT}$	SCL or SDA time low for I^2C bus reset			**25** **35**	ms (min) ms (max)
t_{RSDA}	Minimum $\overline{\text{NTEST\_IN}}$/$\overline{\text{Reset\_IN}}$ rising edge to SDA falling edge		2		µs
t_{RSCL}	Minimum $\overline{\text{NTEST\_IN}}$/$\overline{\text{Reset\_IN}}$ rising edge to SCL falling edge		13		µs

(1) Timing specifications are tested at the Serial Bus Input logic levels, $V_{IN(0)}$ = 0.3 × V^+ for a falling edge and $V_{IN(1)}$ = 0.7 × V^+ for a rising edge when the SCL and SDA edge rates are similar.
(2) Typicals are at T_J= T_A= 25°C and represent most likely parametric norm.
(3) Reflow temperature profiles are different for packages containing lead (Pb) than for those that do not..

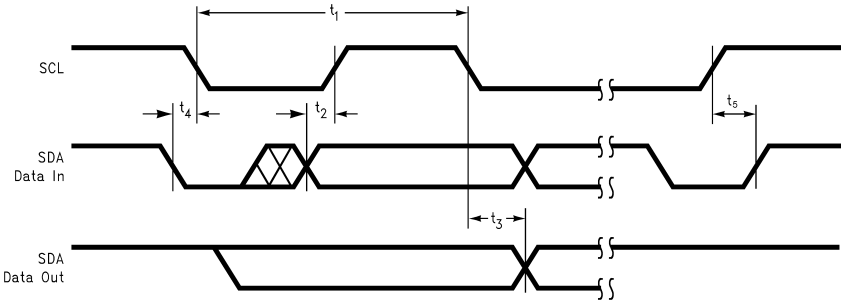


Figure 1. Serial Bus Timing Diagram

Typical Performance Characteristics

The following specifications apply for +3.0 V_{DC} ≤ V^+ ≤ +5.5 V_{DC} , unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.(1)

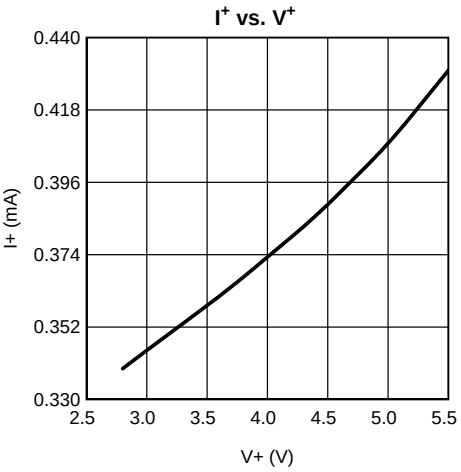


Figure 2.

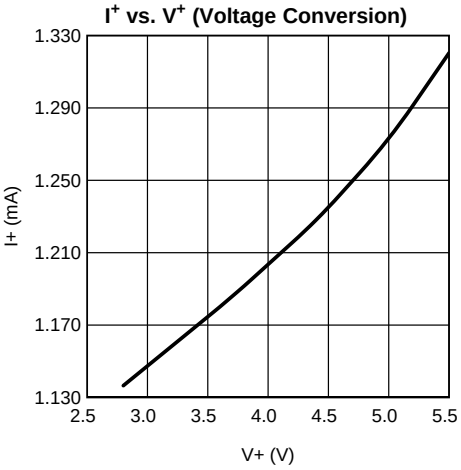


Figure 3.

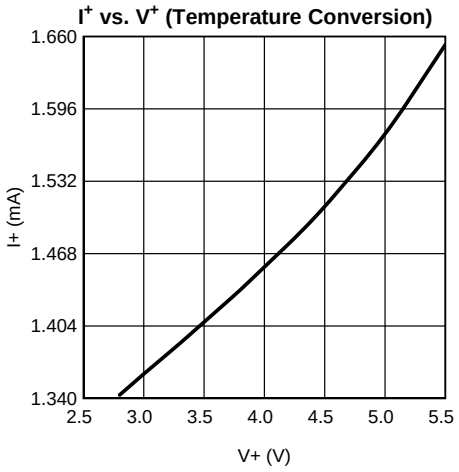


Figure 4.

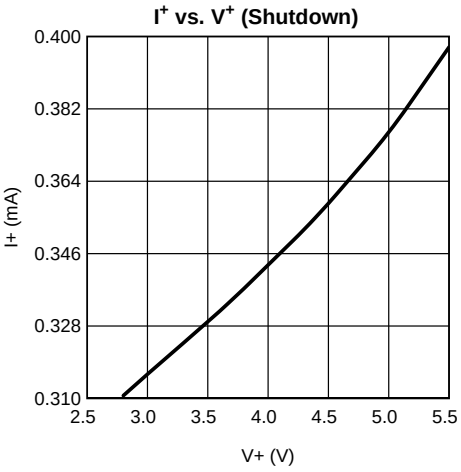


Figure 5.

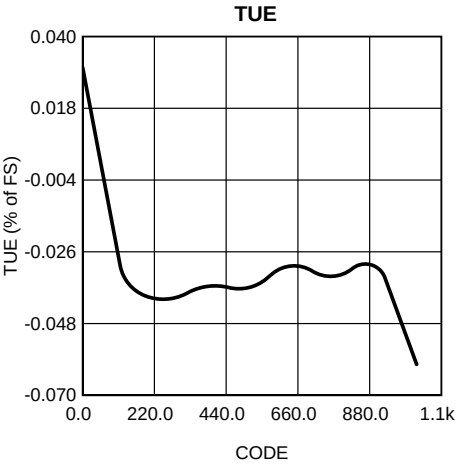


Figure 6.

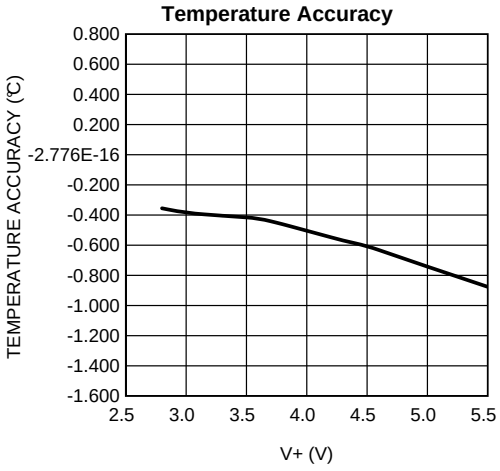


Figure 7.

(1) Timing specifications are tested at the Serial Bus Input logic levels, $V_{IN(0)}$ = 0.3 × V^+ for a falling edge and $V_{IN(1)}$ = 0.7 × V^+ for a rising edge when the SCL and SDA edge rates are similar.

FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

The LM96080 provides 7 analog inputs, a temperature sensor, a delta-sigma ADC (Analog-to-Digital Converter), 2 fan speed counters, WATCHDOG registers, and a variety of inputs and outputs on a single chip. A two wire Serial Bus interface is also provided. The LM96080 can perform power supply, temperature and fan monitoring for a variety of computer systems. The LM96080 is pin and software backwards compatible with the LM80.

The LM96080 continuously converts analog inputs to 10-bit resolution with a 2.5 mV LSb (Least Significant bit) weighting, yielding input ranges of 0 to 2.56V. The Analog Inputs, IN0 - IN6, are intended to be connected to the several power supplies present in a typical communications infrastructure system. Temperature can be converted to a 9-bit or 12-bit two's complement word with resolutions of 0.5°C LSb or 0.0625°C LSb, respectively.

Fan inputs can be programmed to accept either fan failure indicator or tachometer signals. Fan failure signals can be programmed to be either active high or active low. Fan inputs measure the period of tachometer pulses from the the fans, providing a higher count for lower fan speeds. The fan inputs are digital inputs with transition levels according to the Fan Tach Pulse Inputs in the Electrical Characteristics table. Full scale fan counts are 255 (8-bit counter), which represent a stopped or very slow fan. Nominal speeds, based on a count of 153, are programmable from 1100 to 8800 RPM. Signal conditioning circuitry is included to accommodate slow rise and fall times.

The LM96080 provides a number of internal registers. These include:

- **Configuration Register:** Provides control and configuration.
- **Interrupt Status Registers:** Two registers to provide status of each WATCHDOG limit or Interrupt event.
- **Interrupt Mask Registers:** Allows masking of individual Interrupt sources, as well as separate masking for each of both hardware Interrupt outputs.
- **Fan Divisor/$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ Registers:** Bits 0-5 of this register contain the divisor bits for FAN1 and FAN2 inputs. Bits 6-7 control the function of the $\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ output.
- **$\overline{\text{OS}}$ Configuration/Temperature Resolution Register:** The configuration of the $\overline{\text{OS}}$ (Overtemperature Shutdown) is controlled by the lower 3 bits of this register. Bit 3 enables 12-bit temperature conversions. Bits 4-7 reflect the lower four bits of the temperature reading for a 12-bit resolution.
- **Conversion Rate Register:** Controls the conversion rate of the round robin cycle to either continuous or 728 ms.
- **Voltage/Temperature Channel Disable Register:** Allows voltage inputs and the local temperature conversion to be disabled.
- **Value RAM:** The monitoring results: temperature, voltages, fan counts, and Fan Divisor/$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ Register limits are all contained in the Value RAM. The Value RAM consists of a total of 32 bytes. The first 10 bytes are all of the results, the next 20 bytes are the Watchdog Register limits, and the last two bytes are at the upper locations for Manufacturers ID and Device Stepping/Die Revision ID.

The LM96080 is compatible with Standard Mode (Sm, 100 kbits/s) and Fast Mode (Fm, 400 kbits/s) I^2C interface modes of operation. LM96080 includes an analog filter on the I^2C digital control lines that allows improved noise immunity and supports TIMEOUT reset function on SDA and SCL that prevents I^2C bus lockup. Three address pins, A0 - A2, allow up to 8 parts on a single bus.

When enabled, the LM96080 starts by cycling through each measurement in sequence, and it continuously loops through the sequence based on the Conversion Rate Register (address 07h) setting. Each measured value is compared to values stored in WATCHDOG, or Limit Registers (addresses 2Ah - 2Dh). When the measured value violates the programmed limit, the LM96080 will set a corresponding Interrupt in the Interrupt Status Registers (addresses 01h - 02h).

Two output Interrupt lines, $\overline{\text{INT}}$ and $\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$, are available. $\overline{\text{INT}}$ is fully programmable with masking of each Interrupt source, and masking of each output. $\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ is dedicated to the temperature reading WATCHDOG registers. In addition, the Fan Divisor register has control bits to enable or disable the hardware Interrupts.

Additional digital inputs are provided for daisy chaining the Interrupt output pin, $\overline{\text{INT}}$. This is done by connecting multiple external temperature sensors (i.e. LM75 or LM73) to the $\overline{\text{BTI}}$ (Board Temperature Interrupt) input and/or the GPI (Chassis Intrusion) input. The Chassis Intrusion input is designed to accept an active high signal from an external circuit that latches, such as when the cover is removed from the computer.

INTERFACE

Internal Registers of the LM96080

Table 1. The internal registers and their corresponding internal LM96080 address are as follows:

Register	LM96080 Internal Address (Hex)	Power on Value (Binary)	Notes
Configuration Register	00h	0000 1000	
Interrupt Status Register 1	01h	0000 0000	
Interrupt Status Register 2	02h	0000 0000	
Interrupt Mask Register 1	03h	0000 0000	
Interrupt Mask Register 2	04h	0000 0000	
Fan Divisor/$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ Register	05h	0001 0100	FAN1 and FAN2 divisor = 2 (count of 153 = 4400 RPM)
$\overline{\text{OS}}$/ Configuration/ Temperature Resolution Register	06h	0000 0001	
Conversion Rate Register	07h	0000 0000	
Voltage/Temperature Channel Disable Register	08h	0000 0000	Allows voltage monitoring inputs to be disabled
Value RAM	20h - 29h	Indeterminate	Input and FAN readings
Value RAM	2Ah - 3Dh	Indeterminate	Limit Registers
Value RAM	3Eh	0000 0001	Manufacturer's ID
Value RAM	3Fh	0000 1000	Stepping/Die Revision ID

Serial Bus Interface/Serial Bus Timings

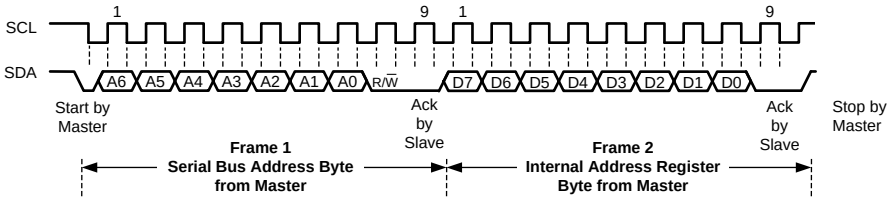


Figure 8. Internal Address Register Set Only

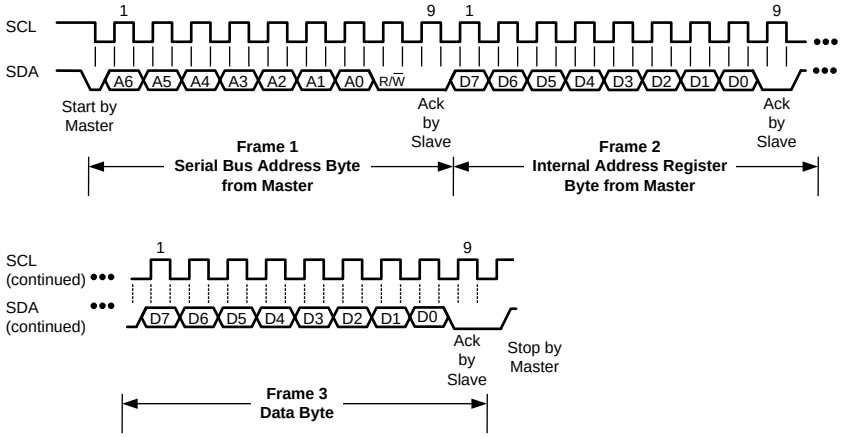


Figure 9. Internal Address Register Set with Data Byte Write

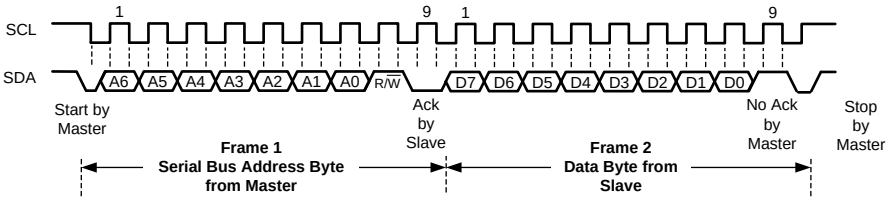


Figure 10. Single Byte Read from Register with Preset Internal Address Register

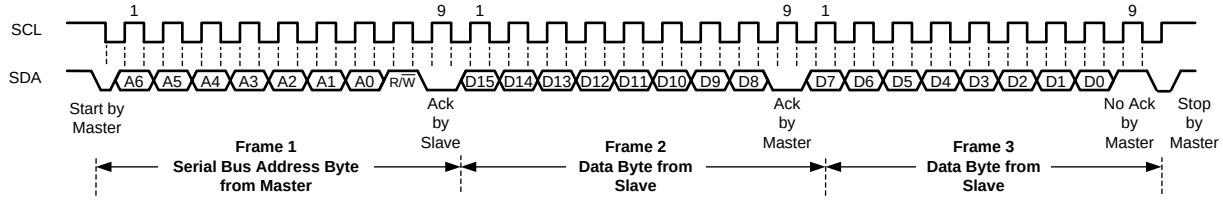


Figure 11. Double Byte Read from Register with Preset Internal Address Register

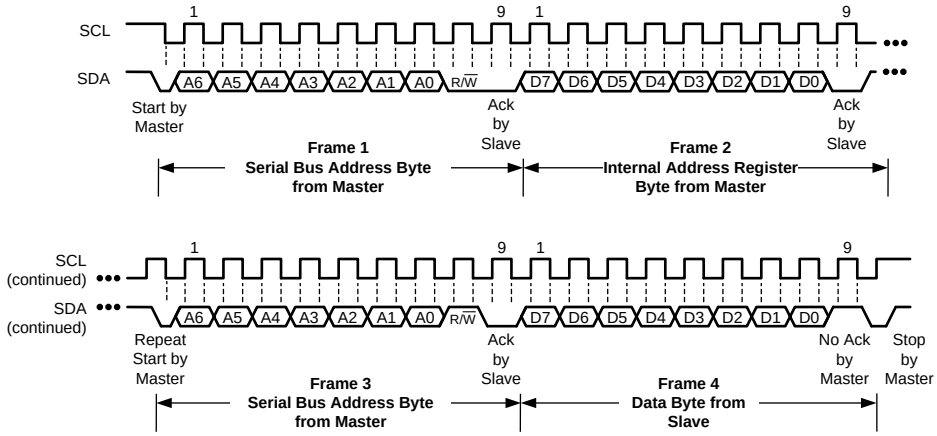


Figure 12. Single Byte Read from Register with Internal Address Set using a Repeat Start

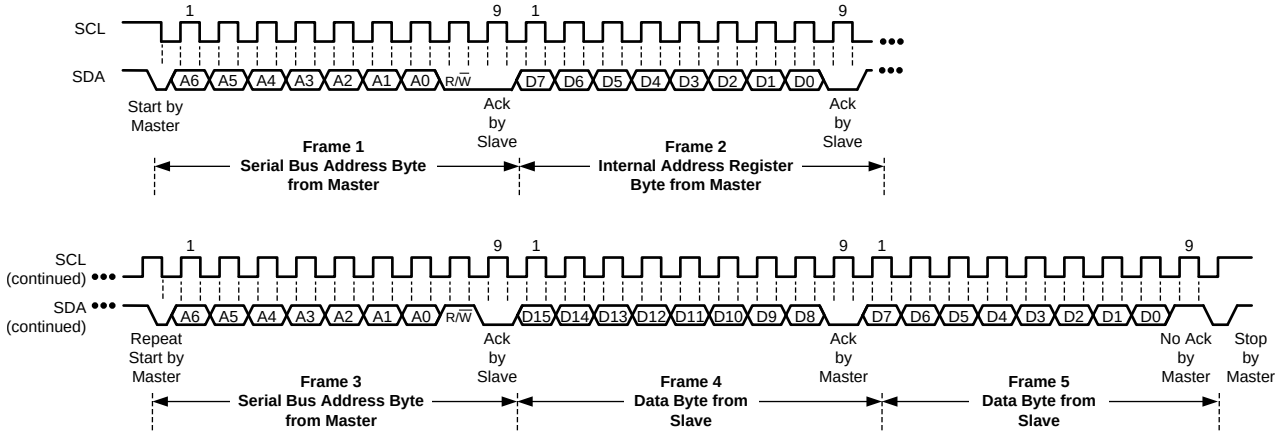


Figure 13. Double Byte Read from Register with Internal Address Set using a Repeat Start

The Serial Bus control lines include the SDA (serial data), SCL (serial clock), and A0-A2 (address) pins. The LM96080 can only operate as a slave. The SCL line only controls the serial interface, all other clock functions within LM96080 such as the ADC and fan counters are done with a separate asynchronous internal clock.

When using the Serial Bus Interface, a write will always consists of the LM96080 Serial Bus Interface Address byte, followed by the Internal Address Register byte, then the data byte.

There are two cases for a read:

1. If the Internal Address Register is known to be at the desired Address, simply read the LM96080 with the Serial Bus Interface Address byte, followed by the data byte read from the LM96080.
2. If the Internal Address Register value is unknown, write to the LM96080 with the Serial Bus Interface Address byte, followed by the Internal Address Register byte. Then restart the Serial Communication with a Read consisting of the Serial Bus Interface Address byte, followed by the data byte read from the LM96080.

The default power on Serial Bus address for the LM96080 is 0101(A2)(A1)(A0) binary, where A0-A2 are the Serial Bus Address.

All of the combinations of communications supported by the LM96080 are depicted in the Serial Bus Interface Timing Diagrams as shown in Figure 13.

USING THE LM96080

Power On

When power is first applied, the LM96080 performs a “power on reset” on several of its registers. The power on condition of registers is shown in Table 1. Registers whose power on values are not shown have power on conditions that are indeterminate (this includes the value RAM and WATCHDOG limits). In most applications, usually the first action after power-on would be to write WATCHDOG limits into the Value RAM.

Resets

Configuration Register INITIALIZATION bit (address 00h, bit 7) accomplishes the same function as power on reset. The Value RAM conversion results (addresses 20h - 29h) and Value RAM WATCHDOG limits (addresses 2Ah - 3Dh) are not reset and will be indeterminate immediately after power on. If the Value RAM contains valid conversion results and/or Value RAM WATCHDOG limits have been previously set, they will not be affected by the Configuration Register INITIALIZATION (except for addresses 3Eh and 3Fh). Power on reset or Configuration Register INITIALIZATION bit clear or initialize the following registers (the initialized values are shown in Table 1):

1. Configuration Register
2. Interrupt Status Register 1
3. Interrupt Status Register 2
4. Interrupt Mask Register 1
5. Interrupt Mask Register 2
6. Fan Divisor/$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ Register
7. $\overline{\text{OS}}$ Configuration/Temperature Resolution Register
8. Conversion Rate Register
9. Voltage/Temperature Channel Disable Register
10. Value RAM Registers (only addresses 3Eh and 3Fh)

Configuration Register INITIALIZATION is accomplished by setting bit 7 of the Configuration Register (address 00h) high. This bit automatically clears after being set.

The LM96080 can be reset to its “power on state” by taking $\overline{\text{NTEST\_IN}}$/$\overline{\text{Reset\_IN}}$ pin low for at least 50 ns.

The time it takes for $\overline{\text{NTEST\_IN}}$/$\overline{\text{Reset\_IN}}$ rising edge to SDA falling edge is at least t_{RSDA}, and for $\overline{\text{NTEST\_IN}}$/$\overline{\text{Reset\_IN}}$ rising edge to SCL falling edge is at least t_{RSCL}. Refer to the AC Electrical Characteristics for more information on t_{RSDA} and t_{RSCL}.

Using the Configuration Register

The Configuration Register (address 00h) provides control for the LM96080. At power on, the ADC is stopped and INT_Clear (bit 3) is asserted, clearing the $\overline{INT}$ and $\overline{RST\_OUT}$/$\overline{OS}$ hardwire outputs. The Configuration Register starts and stops the LM96080, enables and disables $\overline{INT}$ outputs, clears and sets GPI (CI) and $\overline{GPO}$ I/O pins, initiates reset pulse on $\overline{RST\_OUT}$/$\overline{OS}$ pin, and provides the reset function described in the AC Electrical Characteristics section.

Bit 0 of the Configuration Register, START, controls the monitoring loop of the LM96080. Setting bit 0 low stops the LM96080 monitoring loop and puts the LM96080 in shutdown mode, reducing power consumption. Serial Bus communication is possible with any register in the LM96080 although activity on these lines will increase consumption current. Taking bit 0 high starts the monitoring loop, described in more detail subsequently.

Bit 1 of the Configuration Register, $\overline{INT}$ Enable, enables the $\overline{INT}$ Interrupt hardwire output when this bit is taken high.

Bit 2 of the Configuration Register, $\overline{INT}$ Polarity Select, defines whether the $\overline{INT}$ pin is NMOS or PMOS open drain.

Bit 3, INT_Clear, clears the $\overline{INT}$ output when taken high. The LM96080 monitoring function will stop until bit 3 is taken low. The content of the Interrupt Status Registers (addresses 01h - 02h) will not be affected.

Bit 4, $\overline{RESET}$, when taken high, will initiate a 10 ms RESET signal on the $\overline{RST\_OUT}$/$\overline{OS}$ output when $\overline{OS}$ Pin Enable (address 05h, bit 6) = 0 and $\overline{RST}$ Enable (address 05h, bit 7) = 1.

When bit 5, Chassis Clear, is taken high, the GPI (Chassis Intrusion) pin is driven low for 10 ms.

Bit 6 of the configuration register, $\overline{GPO}$, sets or clears the $\overline{GPO}$ output. This pin can be used in software power control by activating an external power control MOSFET.

Starting Conversions

Start the monitoring function (Analog inputs, temperature, and fan speeds) in the LM96080 by writing to the Configuration Register and setting INT_Clear (bit 3) low and Start (bit 0) high. The LM96080 then performs a round-robin monitoring of all analog inputs, temperature, and fan speed inputs. The sequence of items being monitored corresponds to locations in the Value RAM (except for the Temperature reading) as follows:

1. Temperature
2. IN0
3. IN1
4. IN2
5. IN3
6. IN4
7. IN5
8. IN6
9. Fan 1
10. Fan 2

Reading Conversion Results

The conversion results are available in the Value RAM (addresses 20h - 29h). Conversions can be read at any time and will provide the result of the last conversion. If a conversion is in progress while a communication is started, that conversion will be completed, and the internal register(s) will not be updated until the communication is complete.

A typical sequence of events upon power on of the LM96080 would consist of:

1. Set WATCHDOG Limits
2. Set Interrupt Masks
3. Start the LM96080 monitoring process

ANALOG INPUTS

The 10-bit ADC has a 2.5 mV ($2.56/2^{10}$) LSb , yielding a 0V to 2.5575V (2.56 - 1 LSb) input range. This is true for all analog inputs. In most monitoring applications, these inputs would most often be connected to power supplies. The 2.5, 3.3, ±5 and ±12 volt inputs should be attenuated with external resistors to any desired value within the input range. Care should be taken not to exceed V^+ at any time.

A typical application, such as is shown in Figure 14, might select the input voltage divider to provide 1.9V at the analog inputs of the LM96080. This is sufficiently high for good resolution of the voltage, yet leaves headroom for upward excursions from the supply of about 25%. To simplify the process of resistor selection, set the value of R2 first. Select a value for R2 or R4 between 10 kΩ and 100 kΩ. This is low enough to avoid errors due to input leakage currents yet high enough to protect both the inputs under overdrive conditions as well as minimize loading of the source. Then select R1 or R3 to provide a 1.9V input as show in Figure 14.

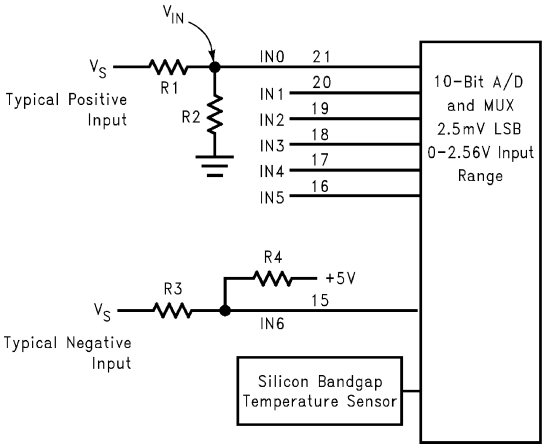


Figure 14. Input Examples. Resistor values shown in table provide approximately 1.9V at the analog inputs.

Table 2. V_{IN} = 1.9V for Different R Values

Voltage Measure-ments (V_S)	R1 or R3	R2 or R4	Voltage at Analog Inputs (ADC code 760)
+2.5V	23.7 kΩ	75 kΩ	+1.9V
+3.3V	22.1 kΩ	30 kΩ	+1.9V
+5.0V	24 kΩ	14.7 kΩ	+1.9V
+12V	160 kΩ	30.1 kΩ	+1.9V
−12V	160 kΩ	35.7 kΩ	+1.9V
−5V	36 kΩ	16.2 kΩ	+1.9V

For positive input voltages, the equation for calculating R1 is as follows:

$$R1 = [(V_S - V_{IN}) / V_{IN}] R2 \quad (1)$$

For negative input voltages, the equation for calculating R3 is as follows:

$$R3 = [(V_S - V_{IN}) / (V_{IN} - 5V)] R4 \quad (2)$$

External resistors should be included to limit input currents to the values given in the ABSOLUTE MAXIMUM RATINGS for Input Current At Any Pin. Inputs with the attenuator networks will usually meet these requirements. If it is possible for inputs without attenuators to be turned on while LM96080 is powered off, additional resistors of about 10 kΩ should be added in series with the inputs to limit the input current.

SUPPLY CURRENT (I^+)

The measured supply current (I^+) in the Electrical Characteristics are only for the round robin conversion and the shutdown mode at a certain supply voltage. To calculate the supply current I^+ in the round robin mode at different supply voltages, use the equation below.

$$I+ = \frac{(1293 \times I^+_{TEMP}) + (1116 \times 7 \times I^+_{VOLTAGE}) + (253037 \times I^+_{SHUTDOWN})}{262{,}142} \quad (3)$$

The I^+_{TEMP}, $I^+_{VOLTAGE}$, and $I^+_{SHUTDOWN}$ values can be obtained from the plots shown in Typical Performance Characteristics.

LAYOUT AND GROUNDING

Analog inputs will provide best accuracy when referred to the AGND pin or a supply with low noise. A separate, low-impedance ground plane for analog ground, which provides a ground point for the voltage dividers and analog components, will provide best performance but is not mandatory. Analog components such as voltage dividers should be located physically as close as possible to the LM96080.

The power supply bypass, a parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors connected between V^+, pin 9, and ground, should also be located as close as possible to the LM96080.

FAN INPUTS

Inputs are provided for signals from fans equipped with tachometer outputs. These are logic-level inputs set according to the Fan Tach Pulse Inputs in the Electrical Characteristics table. Signal conditioning in the LM96080 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 to +5.5V. In the event these inputs are supplied from fan outputs which exceed 0 to +5.5V, either resistive division or diode clamping must be included to keep inputs within an acceptable range. R2 is selected so that it does not develop excessive error voltage due to input leakage. R1 is selected based on R2 to provide a minimum input of 2V and a maximum of 5.5V. R1 should be as low as possible to provide the maximum possible input up to 5.5V for best noise immunity. Alternatively, use a shunt reference or zener diode to clamp the input level.

If fans can be powered while the power to the LM96080 is off, the LM96080 inputs must be protected to meet the Absolute Maximum Ratings section. In most cases, open collector outputs with pull-up resistors inherently limit this current. If this maximum current could be exceeded, either a larger pull up resistor should be used or resistors connected in series with the fan inputs.

The Fan Inputs gate an internal 22.5 kHz oscillator for one period of the Fan signal into an 8-bit counter (maximum count = 255). The default divisor is set to 2 (choices are 1, 2, 4, and 8) providing a nominal count of 153 for a 4400 RPM fan with two pulses per revolution. Typical practice is to consider 70% of normal RPM a fan failure, at which point the count will be 219.

Determine the fan count according to:

$$\text{Count} = \frac{1.35 \times 10^6}{\text{RPM} \times \text{Divisor}} \quad (4)$$

For example, if the frequency of the tachometer were 150 Hz, the RPM would be 4,500 [RPM = (freq) × (60 seconds/min) / (2 pulses/revolution)]. Since the default divisor is 2, the count would be 150 according to the equation above.

Note that Fan 1 and Fan 2 Divisors are programmable via the Fan Divisor/$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ Register (address 05h).

FAN1 and FAN2 inputs can also be programmed to be level sensitive interrupt inputs.

Fans that provide only one pulse per revolution would require a divisor set twice as high as fans that provide two pulses, thus maintaining a nominal fan count of 153. Therefore, the divisor should be set to 4 for a fan that provides 1 pulse per revolution with a nominal RPM of 4400.

Alternatives for Fan Inputs

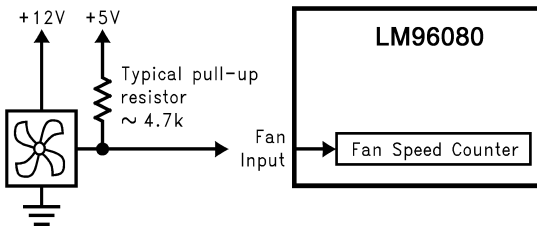


Figure 15. Fan with Tach Pull-Up to +5V

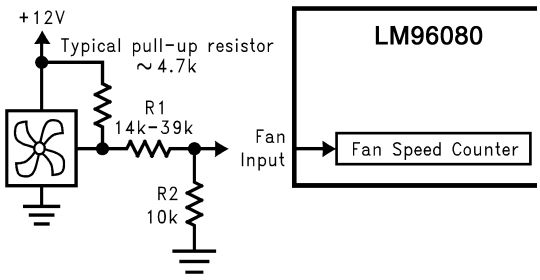


Figure 16. Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Resistor Attenuator

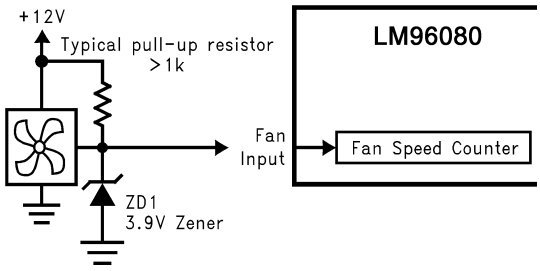


Figure 17. Fan with Tach Pull-Up to +12V and Diode Clamp

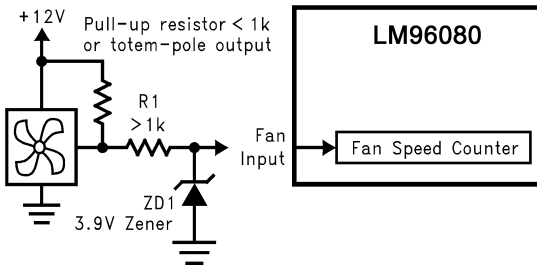


Figure 18. Fan with Strong Tach Pull-Up or Totem Pole Output and Diode Clamp

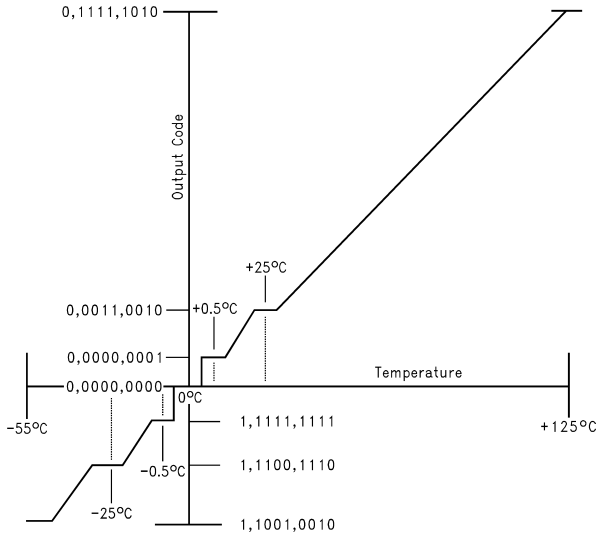
The table below shows example calculation for Count with different divisor and frequency. Counts are based on 2 pulses per revolution tachometer outputs.

RPM	Time per Revolution	Counts for "Divide by 2"	Comments
		(Default) in Decimal	
4400	13.64 ms	153 counts	Typical RPM
3080	19.48 ms	219 counts	70% RPM
2640	22.73 ms	255 counts	60% RPM
		(maximum counts)	

Mode Select	Nominal RPM	Time per Revolution	Counts for the Given Speed in Decimal	70% RPM	Time per Revolution for 70% RPM
Divide by 1	8800	6.82 ms	153	6160	9.74 ms
Divide by 2	4400	13.64 ms	153	3080	19.48 ms
Divide by 4	2200	27.27 ms	153	1540	38.96 ms
Divide by 8	1100	54.54 ms	153	770	77.92 ms

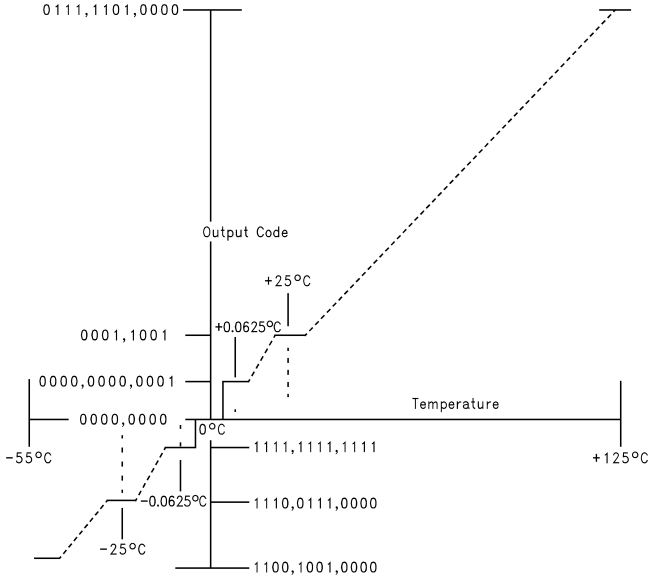
TEMPERATURE MEASUREMENT SYSTEM

The LM96080 delta-V_{BE} type temperature sensor and sigma-delta ADC perform 9-bit or a 12-bit two's-complement conversions of the temperature. An 8-bit digital comparator is also incorporated that compares the readings to the user-programmable Hot and Overtemperature setpoints, and Hysteresis values.



(Non-Linear Scale for Clarity)

Figure 19. 9-bit Temperature-to-Digital Transfer Function



(Non-Linear Scale for Clarity)

Figure 20. 12-bit Temperature-to-Digital Transfer Function

Temperature Data Format

Temperature data can be read from the Temperature Reading Register (address 27h). Temperature limits can be read from and written to the Hot Temperature, Hot Temperature Hysteresis, $\overline{OS}$ Temperature, and $\overline{OS}$ Temperature Hysteresis Limit Registers (addresses 38h - 3Bh). These limits are also referred to as T_{hot}, $T_{hot\ hyst}$, T_{os} , and $T_{os\ hyst}$ respectively. Each limit is represented by an 8-bit, two's complement word with an LSb (Least Significant Bit) equal to 1°C:

Temperature	Digital Output	
	Binary	Hex
+125°C	0111 1101	7Dh
+25°C	0001 1001	19h
+1.0°C	0000 0001	01h
+0°C	0000 0000	00h
−1.0°C	1111 1111	FFh
−25°C	1110 0111	E7h
−55°C	1100 1001	C9h

By default, Temperature Reading Register is represented by a 9-bit two's complement digital word with the LSb having a resolution of 0.5°C:

Temperature	Digital Output	
	Binary	Hex
+125°C	0 1111 1010	0 FAh
+25°C	0 0011 0010	0 32h
+1.5°C	0 0000 0011	0 03h
+0°C	0 0000 0000	0 00h
−0.5°C	1 1111 1111	1 FFh
−25°C	1 1100 1110	1 CEh
−55°C	1 1001 0010	1 92h

Temperature Register data can also be represented by a 12-bit two's complement digital word with a LSb of 0.0625°C:

Temperature	Digital Output	
	Binary	Hex
+125°C	0111 1101 0000	7 D0h
+25°C	0001 1001 0000	1 90h
+1.0°C	0000 0001 0000	0 10h
+0.0625°C	0000 0000 0001	0 01h
0°C	0000 0000 0000	0 00h
(−0.0625)°C	1111 1111 1111	F FFh
(−1.0)°C	1111 1111 0000	F F0h
(−25)°C	1110 0111 0000	E 70h
(−55)°C	1100 1001 0000	C 90h

When using a single byte read, the 8 MSbs of the Temperature reading can be found at Value RAM (address 27h). The remainder of the Temperature reading can be found in the $\overline{OS}$ Configuration/Temperature Resolution Register (address 06h), bits 4-7. In 9-bit format, bit 7 is the only valid bit. In addition, all 9 or 12 bits can be read using a double byte read at register address 27h.

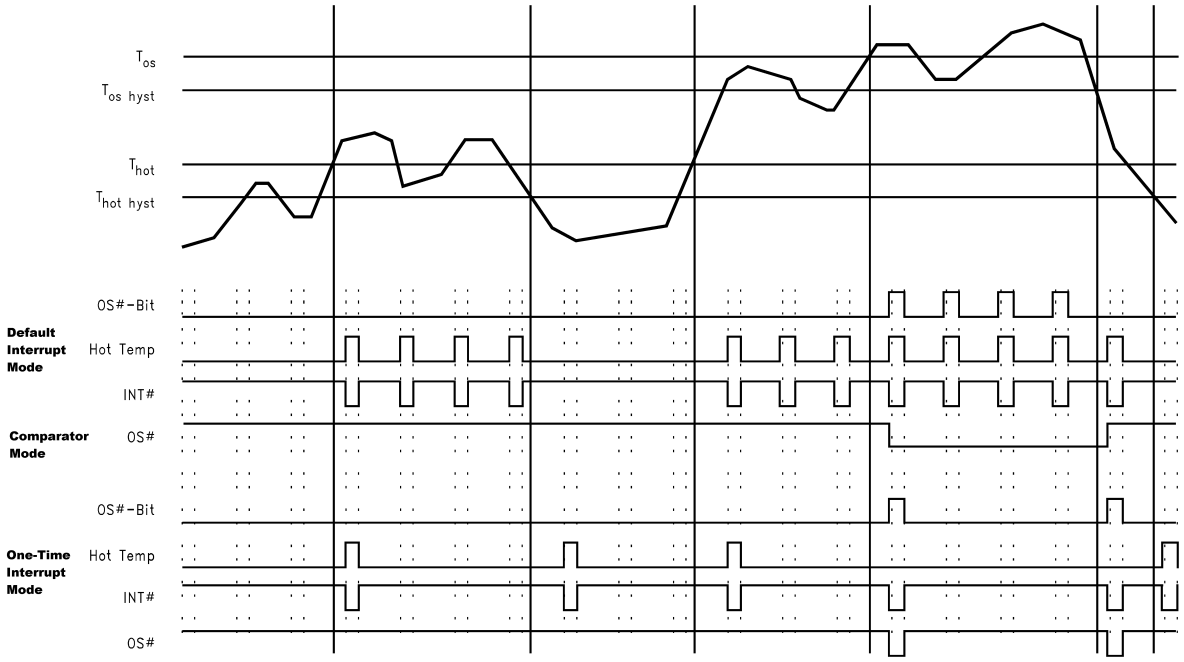
Temperature Interrupts

There are four Value RAM WATCHDOG limits for the Temperature reading that affect the $\overline{INT}$ and $\overline{OS}$ outputs of the LM96080. They are: T_{hot}, $T_{hot\ hyst}$, T_{os} , and $T_{os\ hyst}$ Limit Registers (addresses 38h - 3Bh). There are three interrupt modes of operation: "Default Interrupt" mode, "One-Time Interrupt" mode, and "Comparator Mode". The $\overline{OS}$ output of the LM96080 can be programmed for "One-Time Interrupt" mode and "Comparator" mode. $\overline{INT}$ can be programmed for "Default Interrupt" mode and "One-Time" Interrupt. These modes are explained below and shown in Figure 21.

"Default Interrupt mode" operates in the following way: Exceeding T_{hot} causes an Interrupt that will remain active indefinitely until reset by reading Interrupt Status Register 1 (address 01h) or cleared by the INT_Clear bit in the Configuration register (address 00h, bit 3). Once an Interrupt event has occurred by crossing T_{hot}, then reset, an Interrupt will occur again once the next temperature conversion has completed. The interrupts will continue to occur in this manner until the temperature goes below $T_{hot\ hyst}$, at which time the Interrupt output will automatically clear.

"One-Time Interrupt" mode operates in the following way: Exceeding T_{hot} causes an Interrupt that will remain active indefinitely until reset by reading Interrupt Status Register 1 or cleared by the INT_Clear bit in the Configuration register. Once an Interrupt event has occurred by crossing T_{hot}, then reset, an Interrupt will not occur again until the temperature goes below $T_{hot\ hyst}$.

"Comparator" mode operates in the following way: Exceeding T_{os} causes the $\overline{OS}$ output to go Low (default). $\overline{OS}$ will remain Low until the temperature goes below $T_{os\ hyst}$. Once the temperature goes below $T_{os\ hyst}$, $\overline{OS}$ will go high.



A. This diagram does not reflect all the possible variations in the operation of the $\overline{OS}$ and $\overline{INT}$ outputs nor the $\overline{OS}$ and Hot Temp bits. The interrupt outputs are cleared by reading the appropriate Interrupt Status Registers (addresses 01h - 02h).

Figure 21. Temperature Interrupt Response Diagram

THE LM96080 INTERRUPT STRUCTURE

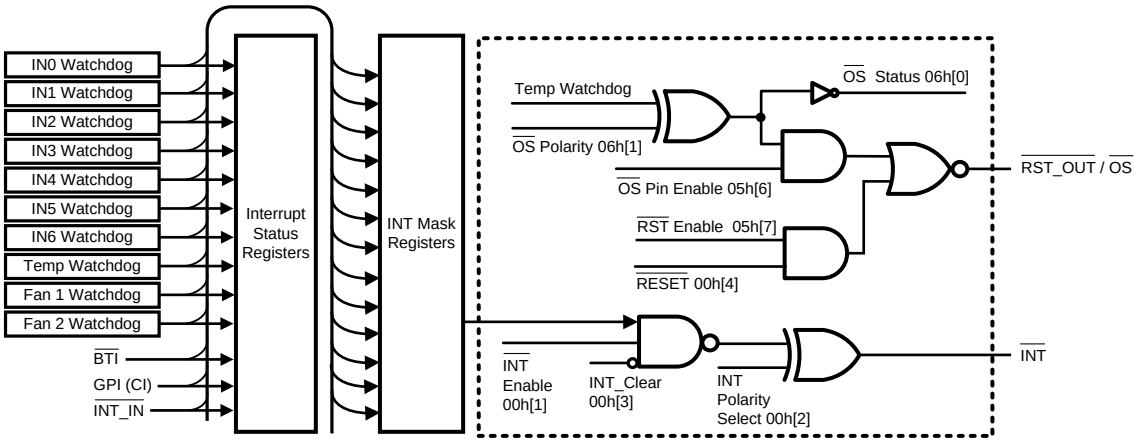


Figure 22. Interrupt Structure

Figure 22 depicts the Interrupt Structure of the LM96080. Note that the number next to each input of the gate represents a register and bit address. For example, INT_Clear 00h[3] refers to bit 3, INT_Clear, of register address 00h. The LM96080 can generate Interrupts as a result of each of its internal WATCHDOG registers on the analog, temperature, and fan inputs.

Interrupt Inputs

External Interrupts can come from the following sources. While the label suggests a specific type or source of Interrupt, this label is not a restriction of its usage, and it could come from any desired source:

- **BTI (Board Temperature Interrupt) -** This is an active low Interrupt intended to come from the Overtemperature Shutdown (O.S.) output of LM75 temperature sensors. The LM75 O.S. output goes active when its temperature exceeds a programmed threshold. Up to 8 LM75's can be connected to a single serial bus with their O.S. output's wire or'ed to the BTI input of the LM96080. If the temperature of any LM75 exceeds its programmed limit, BTI is driven low. This generates an Interrupt via bit 1 of the Interrupt Status Register 2 (address 02h) to notify the host of a possible overtemperature condition. To disable this feature, set bit 1 of the Interrupt Mask Register 2 (address 04h) high. This pin also provides an internal pull-up resistor of 10 kΩ.
- **GPI (Chassis Intrusion) -** This is an active high interrupt from any type of device that detects and captures chassis intrusion violations. This could be accomplished mechanically, optically, or electrically, and circuitry external to the LM96080 is expected to latch the event. Read this Interrupt using bit 4 of the Interrupt Status Register 2 (address 02h), and disable it using bit 4 of the Interrupt Mask Register 2 (address 04h). The design of the LM96080 allows this input to go high even with no power applied to the LM96080, and no clamping or other interference with the line will occur. This line can also be pulled low for at least 10 ms by the LM96080 to reset a typical Chassis Intrusion circuit. Accomplish this reset by setting bit 5 of Configuration Register (address 00h) high; this bit is self-clearing.
- **INT_IN -** This active low Interrupt provides a way to chain the INT (Interrupt) from other devices through the LM96080 to the processor. If this pin is pulled low, then bit 7 of the Interrupt Status Register 1 (address 01h) will go high indicating this Interrupt detection. Setting bit 1 of the Configuration Register (address 00h) will also allow the output INT pin to go low when INT_IN goes low. To disable this feature, set bit 7 of the Interrupt Mask Register 1 (address 03h) high.

Interrupt Outputs

All Interrupts are indicated in the two Interrupt Status Registers.

- **INT -**an output pin, not to be confused with the input INT_IN pin. This pin becomes active whenever INT_IN, BTI, or GPI interrupts. As described in Using the Configuration Register, INT is enabled when bit 1 of the Configuration Register (address 00h) is set high. Bits 2 and 3 of the Configuration Register are also used to set the polarity and state of the INT Interrupt line.
- **OS -**dedicated to the Temperature reading WATCHDOG. In the Fan Divisor/RST_OUT/OS Register (address

05h), the $\overline{OS}$ enable bit (bit 6), must be set high and the $\overline{RST}$ enable bit (bit 7) must be set low to enable the $\overline{OS}$ function on the $\overline{RST}\_OUT/\overline{OS}$ pin. $\overline{OS}$ pin has two modes of operation: "One-Time Interrupt" and "Comparator". "One-Time Interrupt" mode is selected by taking bit 2 of the $\overline{OS}$ Configuration/Temperature Resolution Register (address 06h) high. If bit 2 is taken low, "Comparator" mode is selected. Unlike the $\overline{OS}$ pin, the $\overline{OS}$ bit in Interrupt Status Register 2 (address 02h, bit 5) functions in "Default Interrupt" and "One-Time Interrupt" modes. The $\overline{OS}$ bit can be masked to $\overline{INT}$ pin by taking bit 5 in the Interrupt Mask Register 2 (address 04h) low. A description of "Comparator", "Default Interrupt", and "One-Time Interrupt" modes can be found in Temperature Data Format.

Interrupt Clearing

Reading an Interrupt Status Registers (addresses 01h - 02h) will output the contents of the Register and reset the Register. The Interrupt Status Registers clear upon being read. When the Interrupt Status Registers clear, the $\overline{INT}$ output pin is also cleared until the Registers are updated by the monitoring loop. The $\overline{INT}$ output pin is cleared with the INT_Clear bit (address 00h, bit 3), without affecting the contents of the Interrupt Status Registers. When this bit is high, the LM96080 monitoring loop will stop and will resume when the bit is low.

$\overline{RST}\_OUT$ and $\overline{GPO}$ OUTPUTS

In PC applications, the open drain $\overline{GPO}$ provides a gate drive signal to an external PMOS power switch. This external MOSFET would keep the power turned on regardless of the state of the front panel power switches when software power control is used. In any given application, this signal is not limited to the function described by its label. For example, since the LM96080 incorporates temperature sensing, the $\overline{GPO}$ output could also be utilized to control power to a cooling fan. Take $\overline{GPO}$ active low by setting bit 6 in the Configuration Register (address 00h) high.

$\overline{RST}\_OUT$ is intended to provide a master reset to devices connected to this line. $\overline{RST}$ Enable, bit 7 of address 05h, is the $\overline{RST}\_OUT/\overline{OS}$ control bit that must be set high to enable this function. Setting bit 4, $\overline{RESET}$, in the Configuration Register (address 00h) high outputs a low pulse of at least 10 ms on this line, at the end of which bit 4 in the Configuration Register automatically clears. Again, the label for this pin is only its suggested use. In applications where the $\overline{RST}\_OUT$ capability is not needed, it can be used for any type of digital control that requires a 10 ms active low open drain output.

NAND TREE TESTS

A NAND tree is provided in the LM96080 for Automated Test Equipment (ATE) board level connectivity testing. If the user applies a logic zero to the $\overline{NTEST}\_IN/\overline{Reset}\_IN$ input pin, the device will be in the NAND tree test mode. A0/NTEST_OUT will become the NAND tree output pin. To perform a NAND tree test, all pins included in the NAND tree should be driven to 1. Beginning with IN0 and working clockwise around the chip, each pin can be toggled and a resulting toggle can be observed on A0/NTEST_OUT. The following pins are excluded from the NAND tree test: GNDA (analog ground), GND (digital ground), V^+ (power supply), A0/NTEST_OUT, $\overline{NTEST}\_IN/\overline{Reset}\_IN$ and $\overline{RST}\_OUT/\overline{OS}$. Allow for a typical propagation delay of 500 ns.

REGISTERS AND RAM

Address Register

The bit designations for a register are as follows:

Bit	Name	Read/Write	Description
7-0	Address Pointer	Read/Write	Address of RAM and Registers. See the tables below for detail.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address Pointer (Power On default 00h)							
A7	A6	A5	A4	A3	A2	A1	A0

Address Pointer Index (A7–A0)

Registers and RAM	A7–A0 in Hex	Power On Value of Registers: <7:0> in Binary
Configuration Register	00h	0000 1000
Interrupt Status Register 1	01h	0000 0000
Interrupt Status Register 2	02h	0000 0000
Interrupt Mask Register 1	03h	0000 0000
Interrupt Mask Register 2	04h	0000 0000
Fan Divisor/$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$	05h	0001 0100
$\overline{\text{OS}}$ Configuration/Temperature Resolution Register	06h	0000 0001
Conversion Rate Register	07h	0000 0000
Channel Disable Register	08h	0000 0000
Value RAM	20h – 3Fh	Register 3Eh defaults to 0000 0001 Register 3Fh defaults to 0000 1000

Configuration Register—Address 00h

Power on default <7:0> = 00001000 binary

Bit	Name	Read/Write	Description
0	Start	Read/Write	A one enables startup of monitoring operations, a zero puts the part in shutdown mode. **Note:** Unlike the "INT_Clear" bit, the outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred. At startup, limit checking functions and scanning begin. Note, all limits should be set in the Value RAM before setting this bit HIGH.
1	$\overline{\text{INT}}$ Enable	Read/Write	A one enables the $\overline{\text{INT}}$ Interrupt output.
2	$\overline{\text{INT}}$ Polarity Select	Read/Write	A one selects an active high open source output while a zero selects an active low open drain output.
3	INT_Clear	Read/Write	A one disables the $\overline{\text{INT}}$ output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
4	$\overline{\text{RESET}}$	Read/Write	A one outputs at least a 10 ms active low reset signal at $\overline{\text{RST\_OUT}}$, if bit 7 and bit 6 in the Fan Divisor/$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ Register (address 05h) = 1 and = 0, respectively. This bit is cleared once the pulse has gone inactive.
5	Chassis Clear	Read/Write	A one clears the GPI (Chassis Intrusion) pin. This bit clears itself after 10 ms.
6	$\overline{\text{GPO}}$	Read/Write	A one drives the $\overline{\text{GPO}}$ (General Purpose Output) pin low.
7	INITIALIZATION	Read/Write	A one restores power on default value to the Configuration Register, Interrupt Status Registers, Interrupt Mask Registers, Fan Divisor/$\overline{\text{RST\_OUT}}$/$\overline{\text{OS}}$ Register, the $\overline{\text{OS}}$ Configuration/Temperature Resolution Register, Conversion Rate, Channel Disable, Manufacturers ID and Stepping/Die revision ID registers. This bit clears itself. The power-on default is zero.

Interrupt Status Register 1—Address 01h

Power on default <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0	IN0	Read Only	A one indicates a High or Low limit has been exceeded.
1	IN1	Read Only	A one indicates a High or Low limit has been exceeded.
2	IN2	Read Only	A one indicates a High or Low limit has been exceeded.
3	IN3	Read Only	A one indicates a High or Low limit has been exceeded.
4	IN4	Read Only	A one indicates a High or Low limit has been exceeded.
5	IN5	Read Only	A one indicates a High or Low limit has been exceeded.
6	IN6	Read Only	A one indicates a High or Low limit has been exceeded.
7	$\overline{\text{INT\_IN}}$	Read Only	A one indicates that a Low has been detected on the $\overline{\text{INT\_IN}}$.

Interrupt Status Register 2—Address 02h

Power on default <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0	Hot Temperature	Read Only	A one indicates a High or Low limit has been exceeded. Only “One-Time Interrupt” and “Default Interrupt” modes are supported (see Temperature Interrupts and Interrupt Outputs). The mode is set by bit-6 of the Interrupt Mask Register 2 (address 04h).
1	$\overline{\text{BTI}}$	Read Only	A one indicates that an interrupt has occurred from the Board Temperature Interrupt ($\overline{\text{BTI}}$) input pin. $\overline{\text{BTI}}$ can be tied to the OS output of multiple LM75 chips.
2	FAN1	Read Only	A one indicates that a fan count limit has been exceeded.
3	FAN2	Read Only	A one indicates that a fan count limit has been exceeded.
4	GPI (Chassis Intrusion)	Read Only	A one indicates GPI (Chassis Intrusion) has gone high.
5	$\overline{\text{OS}}$ bit	Read Only	A one indicates a High or a Low $\overline{\text{OS}}$ Temperature limit has been exceed. Only “One-Time Interrupt” and “Default Interrupt” modes are supported (see Temperature Interrupts and Interrupt Outputs). The mode is set by bit 7 of the Interrupt Mask Register 2.
6	Reserved	Read Only	
7	Reserved	Read Only	

Interrupt Mask Register 1—Address 03h

Power on default <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0	IN0	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
1	IN1	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
2	IN2	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
3	IN3	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
4	IN4	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
5	IN5	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
6	IN6	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
7	$\overline{\text{INT\_IN}}$	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.

Interrupt Mask Register 2—Address 04h

Power on default <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0	Hot Temperature	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
1	$\overline{\text{BTI}}$	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
2	FAN1	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
3	FAN2	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
4	GPI (Chassis Intrusion)	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
5	$\overline{\text{OS}}$ bit	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{INT}}$ interrupt.
6	Hot Temperature Interrupt Mode Select	Read/Write	A zero selects the default interrupt mode which gives the user an interrupt if the temperature goes above the hot limit. The interrupt will be cleared once the status register is read, but it will again be generated when the next conversion has completed. It will continue to do so until the temperature goes below the hysteresis limit. A one selects the one time interrupt mode which only gives the user one interrupt when it goes above the hot limit. The interrupt will be cleared once the status register is read. Another interrupt will not be generated until the temperature goes below the hysteresis limit. It will also be cleared if the status register is read. No more interrupts will be generated until the temperature goes above the hot limit again. The corresponding bit will be cleared in the status register every time it is read but may not set again when the next conversion is done. (Refer to Figure 21).

Bit	Name	Read/Write	Description
7	$\overline{OS}$ Bit Interrupt Mode Select	Read/Write	A zero selects the default interrupt mode which gives the user an interrupt if the temperature goes above the OS limit. The interrupt will be cleared once the status register is read, but it will again be generated when the next conversion has completed. It will continue to do so until the temperature goes below the hysteresis limit. A one selects the one time interrupt mode which only gives the user one interrupt when it goes above the OS limit. The interrupt will be cleared once the status register is read. Another interrupt will not be generated until the temperature goes below the hysteresis limit. It will also be cleared if the status register is read. No more interrupts will be generated until the temperature goes above the OS limit again. The corresponding bit will be cleared in the status register every time it is read but may not set again when the next conversion is done. (Refer to Figure 21).

Fan Divisor/$\overline{RST\_OUT}$/$\overline{OS}$ Register —Address 05h

Power on – <7:0> is 0001 0100

Bit	Name	Read/Write	Description
0	FAN1 Mode Select	Read/Write	A one selects the level sensitive input mode while a zero selects Fan count mode for the FAN1 input pin.
1	FAN2 Mode Select	Read/Write	A one selects the level sensitive input mode while a zero selects Fan count mode for the FAN2 input pin.
2-3	FAN1 RPM Control	Read/Write	FAN1 Speed Control. <3:2> = 00 - divide by 1; <3:2> = 01 - divide by 2; <3:2> = 10 - divide by 4; <3:2> = 11 - divide by 8. If level sensitive input is selected: <2> = 1 selects and active-low input (An interrupt will be generated if the FAN1 input is Low), <2> = 0 selects an active-high input (an interrupt will be generated if the FAN1 input is High).
4-5	FAN2 RPM Control	Read/Write	FAN2 Speed Control. <5:4> = 00 - divide by 1; <5:4> = 01 - divide by 2; <5:4> = 10 - divide by 4; <5:4> = 11 - divide by 8. If level sensitive input is selected: <4> = 1 selects and active-low input (An interrupt will be generated if the FAN2 input is Low), <4> = 0 selects an active-high input (an interrupt will be generated if the FAN2 input is High).
6	$\overline{OS}$ Pin Enable	Read/Write	A one enables $\overline{OS}$ mode on the $\overline{RST\_OUT}$/$\overline{OS}$ output pin, while bit 7 of this register is set to zero. If bits 6 and 7 of this register are set to zero, the $\overline{RST\_OUT}$/$\overline{OS}$ pin is disabled.
7	$\overline{RST}$ Enable	Read/Write	A one sets the $\overline{RST\_OUT}$/$\overline{OS}$ pin in the $\overline{RST\_OUT}$ mode instead of the $\overline{OS}$ mode. If bits 6 and 7 of this register are set to zero, the $\overline{RST\_OUT}$/$\overline{OS}$ pin is disabled.

$\overline{OS}$ Configuration/Temperature Resolution Register—Address 06h

Power on default <7:0> = 0000 0001 binary

Bit	Name	Read/Write	Description
0	$\overline{OS}$ Status	Read only	Status of the $\overline{OS}$. This bit mirrors the state of the $\overline{RST\_OUT}$/$\overline{OS}$ pin when in the $\overline{OS}$ mode.
1	$\overline{OS}$ Polarity	Read/Write	A zero selects $\overline{OS}$ to be active-low, while a one selects $\overline{OS}$ to be active high. $\overline{OS}$ is an open-drain output.
2	$\overline{OS}$ Mode Select	Read/Write	A one selects the one time interrupt mode for $\overline{OS}$, while a zero selects comparator mode for $\overline{OS}$. (See Temperature Data Format)
3	Temperature Resolution Control	Read/Write	A zero selects the default 8-bit plus sign resolution temperature conversions, while a one selects 11-bit plus sign resolution temperature conversions.

Bit	Name	Read/Write	Description
4-7	Temp [3:0]	Read/Write	The lower nibble (4 LSbs) of the 11-bit plus sign temperature data: <4> = Temp [0] (nibble LSb, 0.0625°C), <5> = Temp [1], <6> = Temp [2], <7> = Temp [3] (nibble MSb, 0.5°C). For 8-bit plus sign temperature resolution: <7> = Temp [0] (LSb, 0.5°C) <4:6> are undefined

Conversion Rate Register—Address 07h

Power on default <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0	CR1	Read/Write	Controls conversion rate: 0 = 728ms (typical) 1 = Continuous Conversion. Note: — Each voltage channel conversion takes 3 ms typical. — Temperature conversion takes 3.6 ms typical for 9 - bit resolution and 23.5 ms typical for 12 - bit resolution. — Each fan tachometer input is monitored for 2 pulses, the time interval for two pulses is added to the round robin time for each fan tach input that is enabled.
1-7	Reserved	Read only	Reserved — will always report zero.

Voltage/Temperature Channel Disable Register—Address 08h

Power on default <7:0> = 0000 0000 binary

Bit	Name	Read/Write	Description
0	IN0	Read/Write	When set to "1", IN0: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
1	IN1	Read/Write	When set to "1", IN1: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
2	IN2	Read/Write	When set to "1", IN2: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
3	IN3	Read/Write	When set to "1", IN3: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
4	IN4	Read/Write	When set to "1", IN4: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
5	IN5	Read/Write	When set to "1", IN5: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
6	IN6	Read/Write	When set to "1", IN6: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
7	Temp	Read/Write	When set to "1", Temperature: conversions are skipped and disabled value register readings will be 0 error events will be suppressed

Value RAM—Address 20h–3Fh(1)

Address A7–A0	Description
20h	IN0 reading (10-bit)
21h	IN1 reading (10-bit)
22h	IN2 reading (10-bit)
23h	IN3 reading (10-bit)
24h	IN4 reading (10-bit)
25h	IN5 reading (10-bit)
26h	IN6 reading (10-bit)
27h	Temperature reading (9-bit or 12-bit for easy read-back)
28h	FAN1 reading **Note:** This location stores the number of counts of the internal clock per revolution.
29h	FAN2 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Ah	IN0 High Limit
2Bh	IN0 Low Limit
2Ch	IN1 High Limit
2Dh	IN1 Low Limit
2Eh	IN2 High Limit
2Fh	IN2 Low Limit
30h	IN3 High Limit
31h	IN3 Low Limit
32h	IN4 High Limit
33h	IN4 Low Limit
34h	IN5 High Limit
35h	IN5 Low Limit
36h	IN6 High Limit
37h	IN6 Low Limit
38h	Hot Temperature Limit (High)
39h	Hot Temperature Hysteresis Limit (Low)
3Ah	$\overline{OS}$ Temperature Limit (High)
3Bh	$\overline{OS}$ Temperature Hysteresis Limit (Low)
3Ch	FAN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Dh	FAN2 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Eh	Manufacturer's ID always defaults to 0000 0001; this register is writable and can be reset to the default value by the INITIALIZATION bit in the Configuration Register (address 00h, bit 7).
3Fh	Stepping/Die Revision ID always defaults to 0000 1000; this register is writable and can be reset to the default value by the INITIALIZATION bit in the Configuration Register.

(1) Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will **never** be generated except the case when voltages go below the low limits.
For voltage input high limits, the device is doing a greater than comparison. For low limits, however, it is doing a less than or equal to comparison.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	28

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM96080CIMT/NOPB	ACTIVE	TSSOP	PW	24	61	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM96080 CIMT	Samples
LM96080CIMTX/NOPB	ACTIVE	TSSOP	PW	24	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM96080 CIMT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

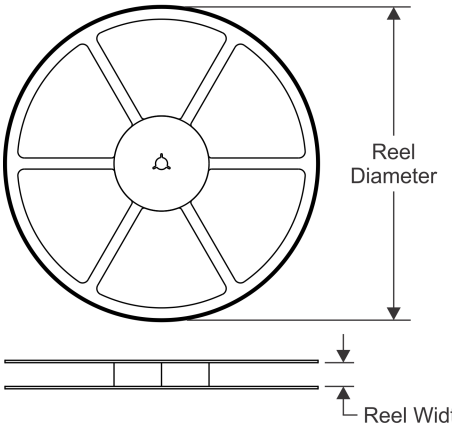
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

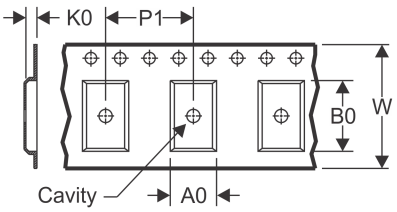
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

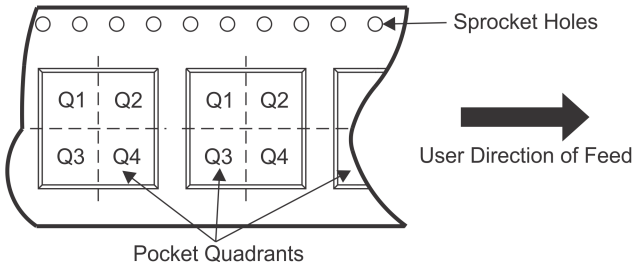


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

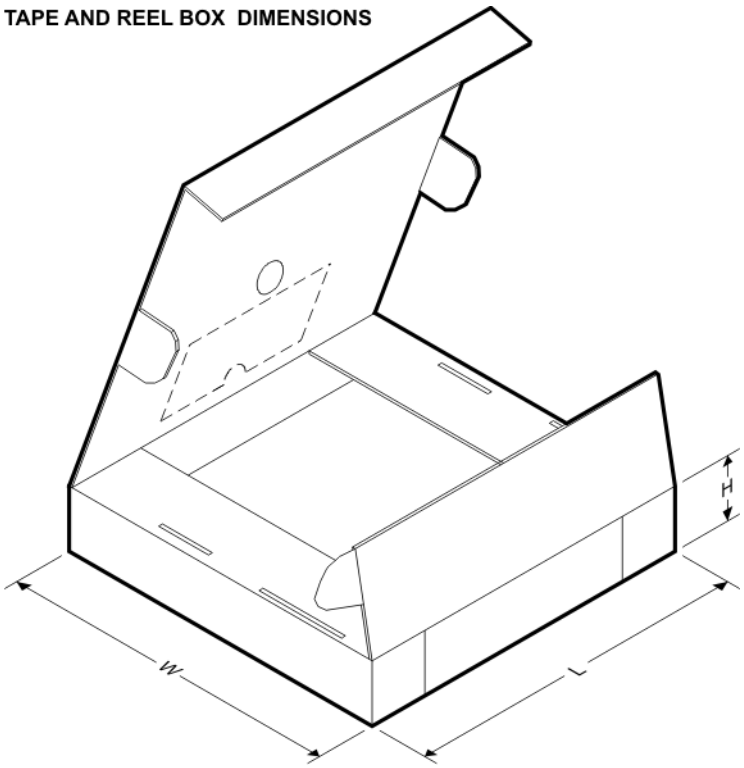
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM96080CIMTX/NOPB	TSSOP	PW	24	2500	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

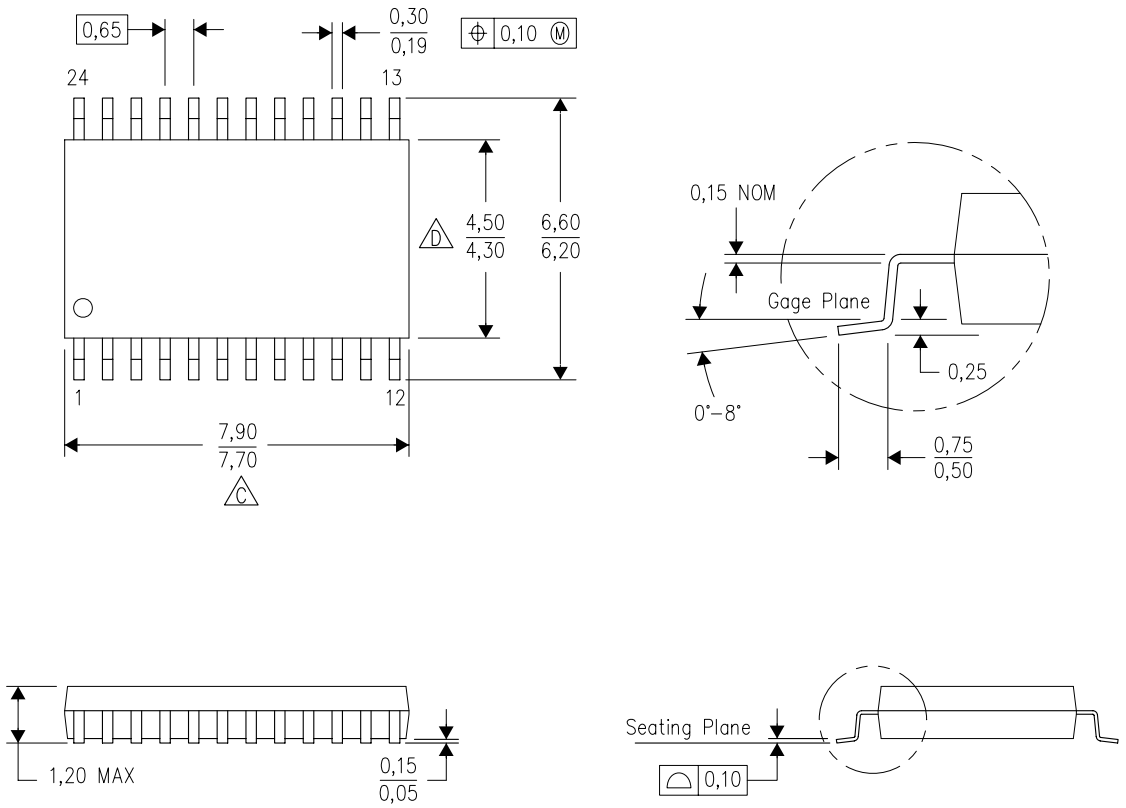
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM96080CIMTX/NOPB	TSSOP	PW	24	2500	367.0	367.0	35.0

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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