Features

- PLL with quartz stabilized VCXO
- Crystal output jitter less than 20ps
- Dual redundant reference input clocks with loss of signal detection
- Manual or automatic switch over between reference input clocks
- VCXO provides smooth output transition during switch over of input clocks
- Lock detection
- Selectable metal mask options for phase detectors, op. Amps, and charge pump
- Loss of signals alarm
- Return to nominal clock upon LOS
- Input data rates from 8 kb/s to 40 Mb/s
- Tri-state output
- User defined PLL loop response
- NRZ data compatible
- +3.3 and +5.0V supply voltage

Description

The device is composed of phase-lock loop with integrated VCXO for use in clock recovery, data re-timing, frequency translation and clock smoothing applications in telecom and datacom systems.

Crystal Frequencies Supported: 12.624~38.880MHz.

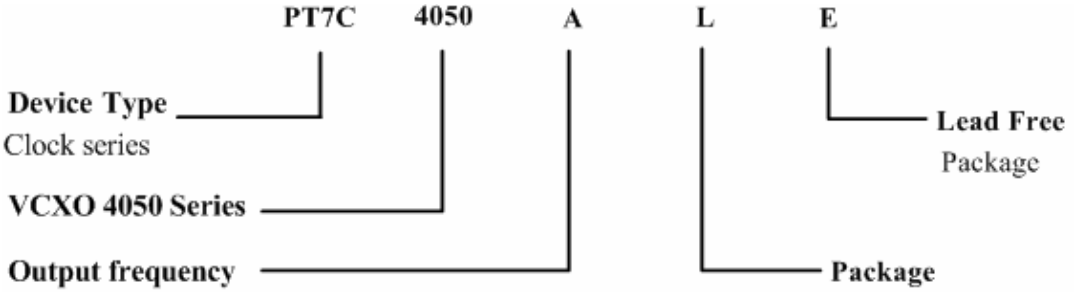
Ordering Information

Part Number	Package
PT7C4050xDE	Die form
PT7C4050xLE	Lead free 28-Pin TSSOP

Note: Pls see below specification of part no.

Applications

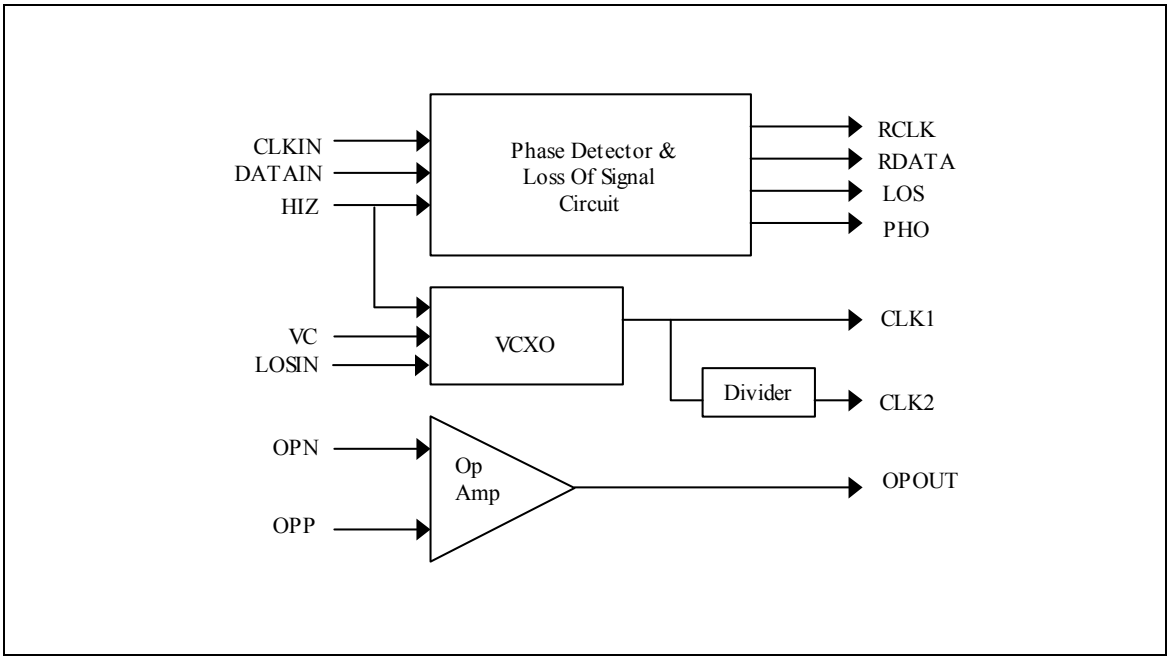
- Frequency translation
- Clock Smoothing, Clock Switching
- NRZ Clock Recovery
- Optical Switching/Routing, Base Station



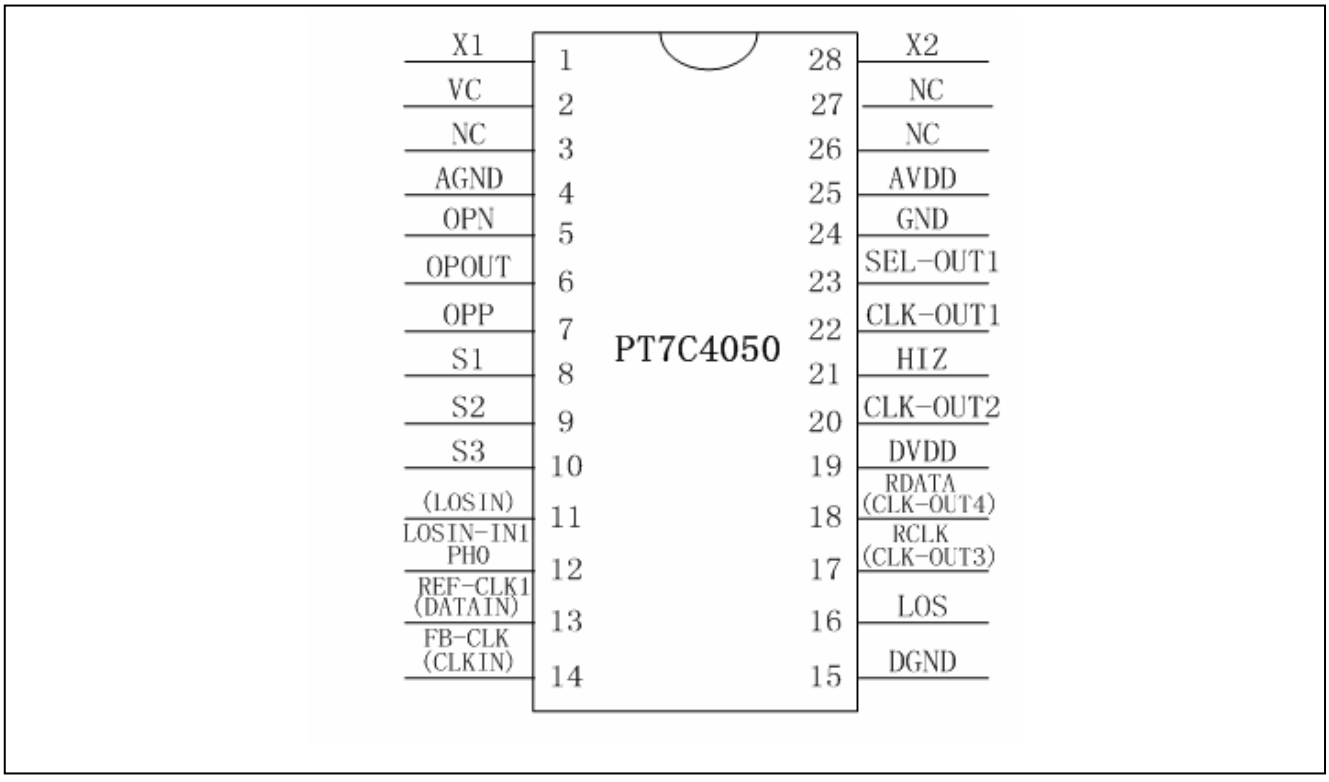
Freq. range	Symbol
10~30MHz	Retain "A"
30~40MHz	Omit "A"

Crystal Freq. Used
12.624 MHz
16.384 MHz
19.440 MHz
20.000 MHz
24.704 MHz
32.768 MHz
38.880 MHz

Block Diagram



Pin Configuration

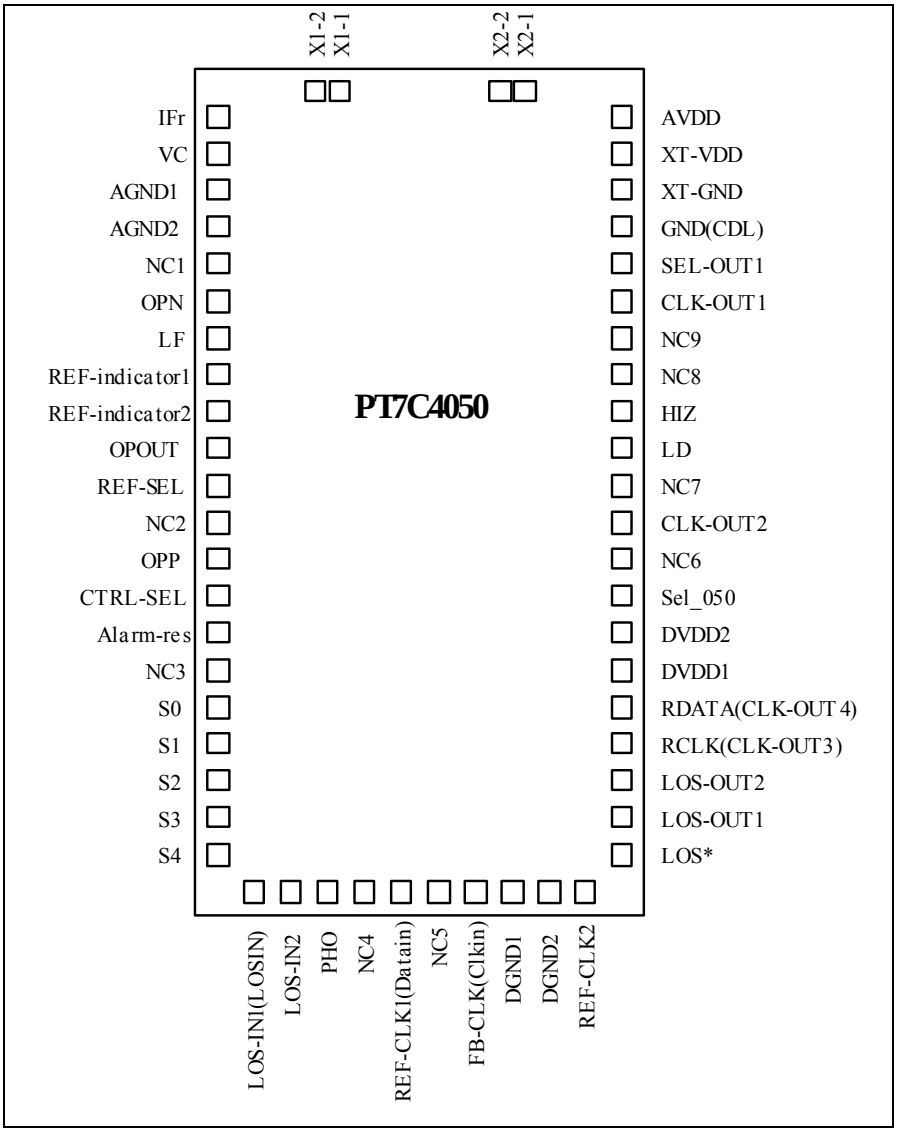


Pin Description

Pin	Sym	Description
1	X1	Crystal oscillator connected between X1 and X2
2	VC	**Control voltage input.** It controls crystal oscillator (VCXO).
3	NC	**Not connected.**
4	AGND	**Analog ground.**
5	OPN	**Negative input.** terminal to internal operational amplifier.
6	OPOUT	**Output.** terminal of internal operational amplifier.
7	OPP	**Positive input.** terminal to internal operational amplifier.
8	S1	S1, S2, S3 Options for selectable divider N
9	S2	
10	S3	
11	LOS-IN1 (LOSIN)	**TTL input.** Internal pull down. Normally this pin is connected to OUT1 and selects REF-CLK1 input
12	PHO	**Output.** signal produced by phase detector of data.
13	REF-CLK1 (DATAIN)	**Input clock signal.** to phase detector (TTL switching thresholds for recovering DATAIN)
14	FB-CLK (CLKIN)	**TTL switching thresholds input.** Connected to external feedback clock.
15	DGND	**Digital ground.**
16	LOS	**Loss of signal detection.** for DATAIN input. Refer to LOS detection description.
17	RCLK (CLK-OUT3)	**Output recovered clock.**
18	RDATA (CLK-OUT4)	**Output recovered data stream.**
19	DVDD	**Digital power supply.**
20[*1]	CLK-OUT2	**Output clock** of internal VCXO frequency controlled by S3, S2, S1 while S4 set logic high
21	HIZ	**TTL input.** When set to a logic low, output pins CLK-OUT1, CLK-OUT2, RCLK, and RDATA buffers are set to high-impedance state. When set to logic high or no connection, the device functions and output pins CLK-OUT1, CLK-OUT2, RCLK, and RDATA etc. are active. This input has an internal pull-up resistor.
22	CLK-OUT1	**Output clock.** of internal VCXO or half VCXO frequency, controlled by SEL-OUT1.
23[*2]	SEL-OUT1	**CMOS input.** 'LO' selects half of internal VCO frequency. 'HI' selects internal VCO frequency. Internal pull up.
24	GND	**Ground.**
25	AVDD (XT-VDD)	**Analog power supply.**
26	NC	**Not connected.**
27	NC	**Not connected.**
28	X2	Crystal oscillator connected between X1 and X2

Note:
*[1]: S3, S2, S1 option for selectable divider N, Please refer to Table 1
*[2]: SEL-OUT1 option for VCXO or half VCXO output freq. Please refer to Table 2
( ): For pin11/13/14/17/18/25, die option

Pad Location



Die size: 2190×3401μm(Including scribe line).
Die thickness: 300μm(no coating).

Table 1 Bonding Options for selectable divider N

S3	S2	S1	Divider N
1	1	1	2
1	1	0	4
1	0	1	8
1	0	0	16
0	1	1	32
0	1	0	64
0	0	1	128
0	0	0	256

Table 2 Bonding Options for CLK-OUT1

SEL-OUT1	CLK-OUT1 frequency
1	Internal VCXO frequency
0	Half of internal VCXO frequency

Function Description

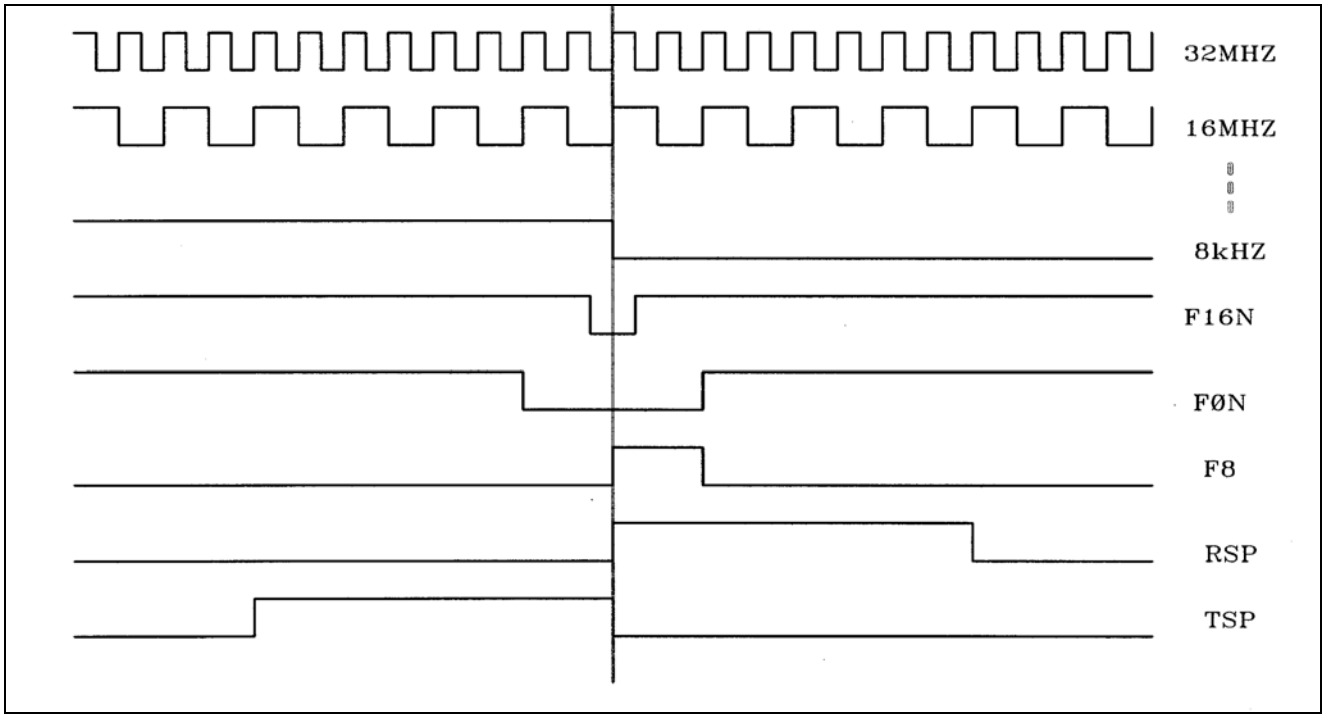
LOS detection

LOS-OUT1 provides output alarm flag when REF-CLK1 is lost. The LOS output is set to logic high after 256 consecutive FB-CLK (CLKIN) periods with no REF-CLK1 (DATAIN) transitions. As soon as a transition occurs at REF-CLK1 (DATAIN), LOS is reset to a logic low.

Divider output signals

The internal divider N is 2,4,8, ------, 8192, and creates 5 kinds of 8KHZ frame signals: F0N, F8, F16N, RSP, TSP. F0N outputs to CLK-OUT3 pin, F16N outputs to CLK-OUT4 pin. The F8, TSP, RSP can be selected by S4:1 (bond option) and output to CLK-OUT2 pin.

8KHZ frame signals' generator based on 32MHZ VCXO frequency. All signals are compatible with 4409 DPLL product.



Maximum Rating

Storage Temperature……- 65°C to +150°C
Core supply voltage…….- 0.5 to +7.0V
I/O supply voltage……... - 0.5 to +7.0V
DC Input Voltage ……- 0.5 to +7.0V
Input ESD protection ……...2000V

Note: Stresses greater than those listed under MAXIMUMRATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

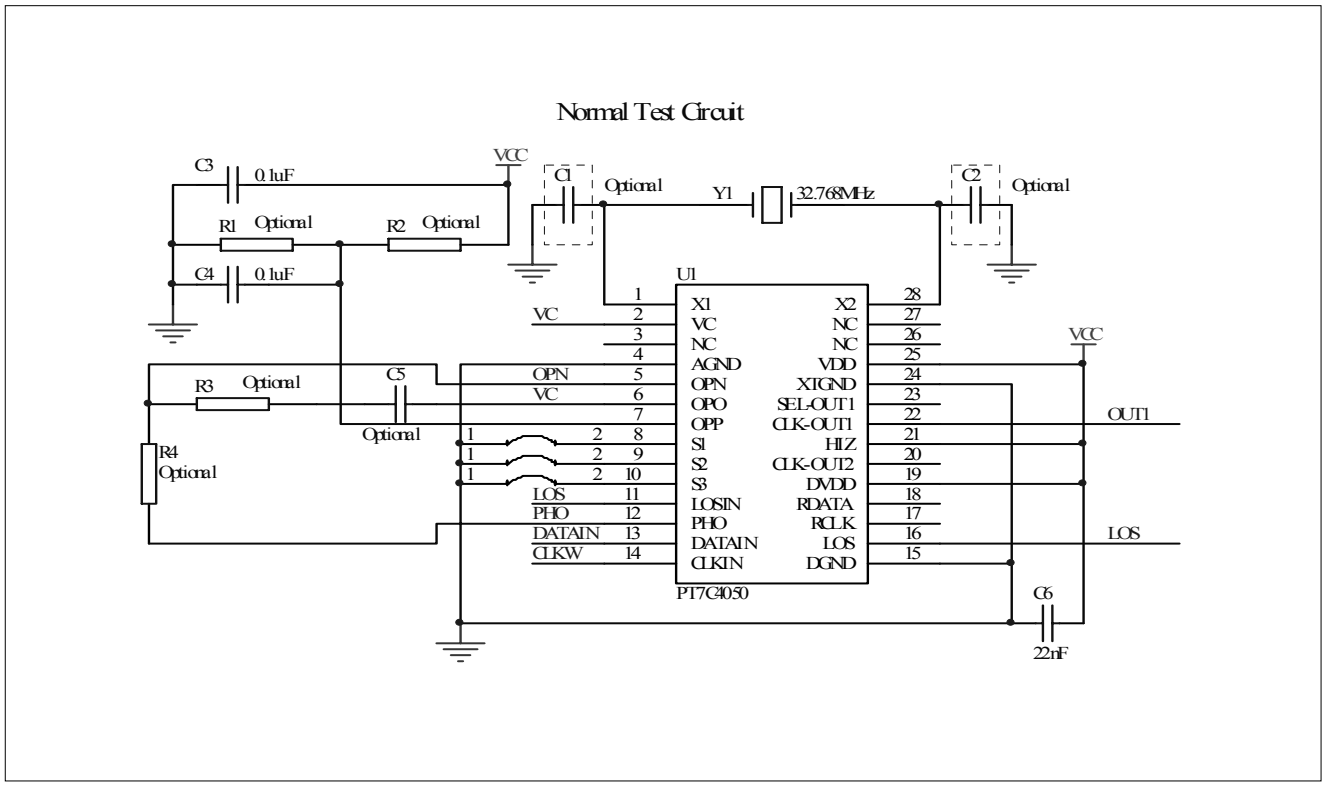
DC Characteristics

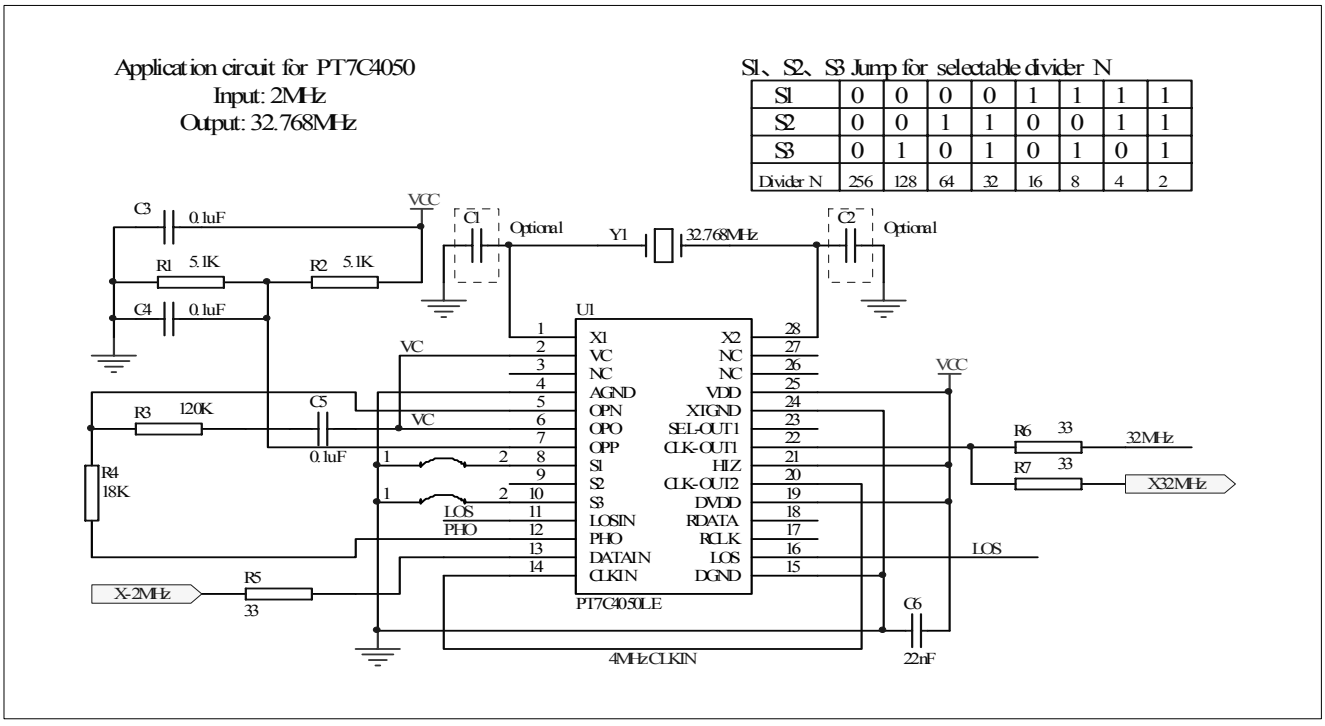
Sym	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	-	4.5	-	5.5	V
		-	3.0		3.6	
I_{LEAK}	Input Leakage Current	-	-10	-	10	µA
V_{TIH}	TTL Input High Voltage	-	2	-	-	V
V_{TIL}	TTL Input Low Voltage	-	-	-	0.8	V
V_{CIH}	CMOS Input High Voltage	-	$0.7V_{DD}$	-	-	V
V_{CIL}	CMOS Input Low Voltage	-	-	-	$0.3V_{DD}$	V
V_{OH1}	Output High Voltage for CLK-OUT1/2/3/4	Ioh = 8mA	2.4	-	-	V
V_{OL1}	Output Low Voltage for CLK-OUT1/2/3/4	Iol = 8mA	-	-	0.4	V
$I_{PULLUP1}$	Input Pull up Current for HIZ	-	-160	-	-	µA
$I_{PULLUP2}$	Input Pull up Current for S4:0, Test	$V_i = 0V$	-50	-	-	
$I_{PULLDOWN}$	Input Pull down Current for LOS-IN1	$V_i = V_{DD}$	-	-	50	
I_{CC}	Maximum Supply Current	Full Active	-	-	60	mA
T_A	Ambient Temperature	-	-40	-	85	°C

AC Characteristics

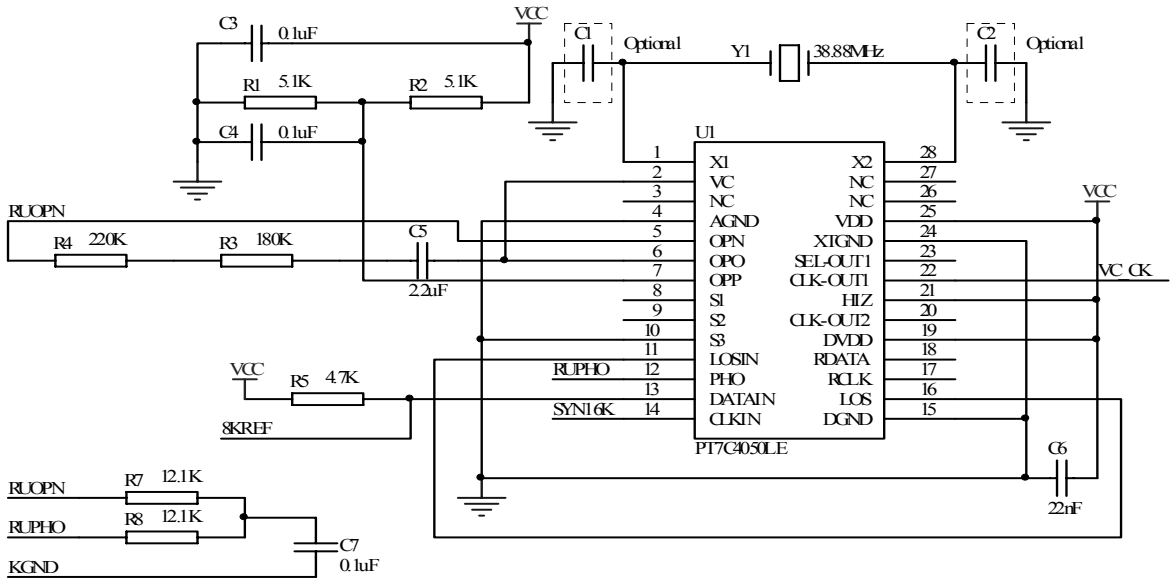
Sym	Parameter	Test Condition	Min	Typ	Max	Unit
DATAIN	Input NRZ Data Rates	-	0.008	-	65.536	Mb/s
REF-CLK	Input RZ Data and Clock Rates	-	0.008	-	32.768	Mb/s
OUT1	Nominal Output Frequency CLK-OUT1	-	12.0	-	61.44	MHz
OUT2	Nominal Output Frequency CLK-OUT2	-	out1 /8192	-	out1 /2	MHz
t_R	Rise Time	0.5V to 2.5V	0.5	-	5	ns
t_F	Fall Time	2.5V to 0.5V	0.5	-	5	ns
SYM 1	CLK-OUT1 (Symmetry or Duty cycle)	VC = 1.4V	40	-	60	%
SYM 2	CLK-OUT2 (Symmetry or Duty cycle)	VC = 1.4V	45	-	55	%
RCLK	RCLK (Symmetry or Duty cycle)	VC = 1.4V	40	-	60	%
BW	Control Voltage Bandwidth	-3 dB, VC = 1.65 V	-	25	-	kHz
ΔF/ΔV C	Sensitivity	VC = Vdd/2	-	-	100	ppm/V
NR	VCXO Negative Resistor	-	-	-	-40	Ohm
OUT1	Nominal Output Frequency on Loss of Signal: CLK-OUT1/2	-	-75	-	75	ppm from fo 1
OUT2			-75	-	75	ppm from fo 2
KD	Phase Detector Gain	Internal design value	-	-	0.53 x Data Density	V/rad
	Phase Detector Gain offset	Internal design value, DATAIN and CLKIN is "0" degree phase difference, OP-Amp gain=2/3	-	-	TDB	V
GB	Loop Filter Op-Amp Unity Gain Band Width	Internal design VALUE.	-	750	-	KHz

Application Circuit

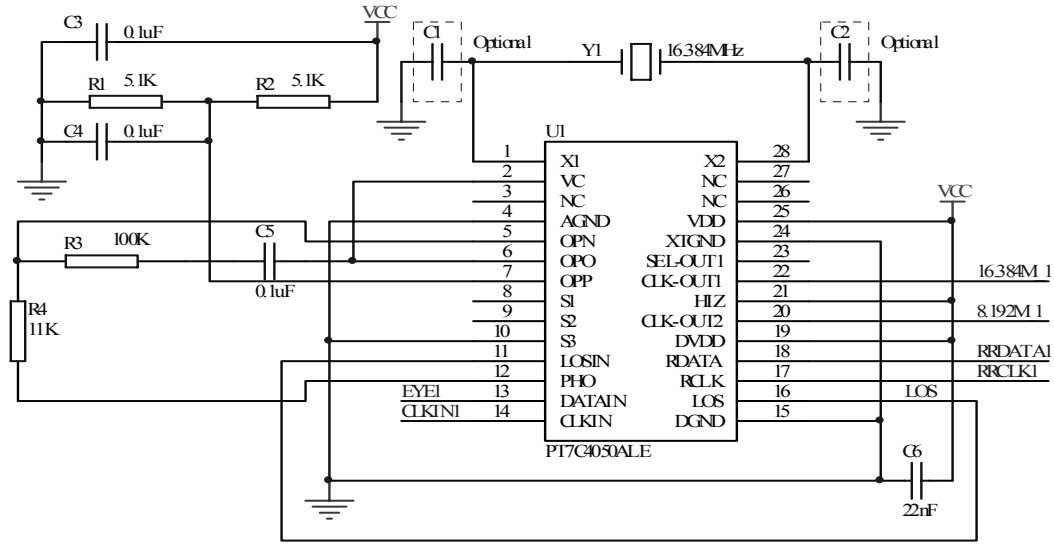




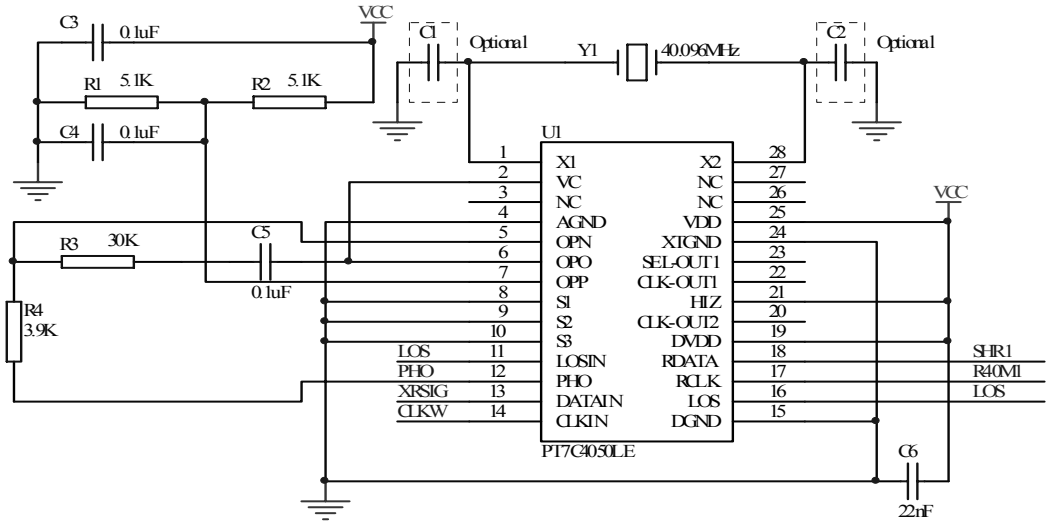
38.88/19.44



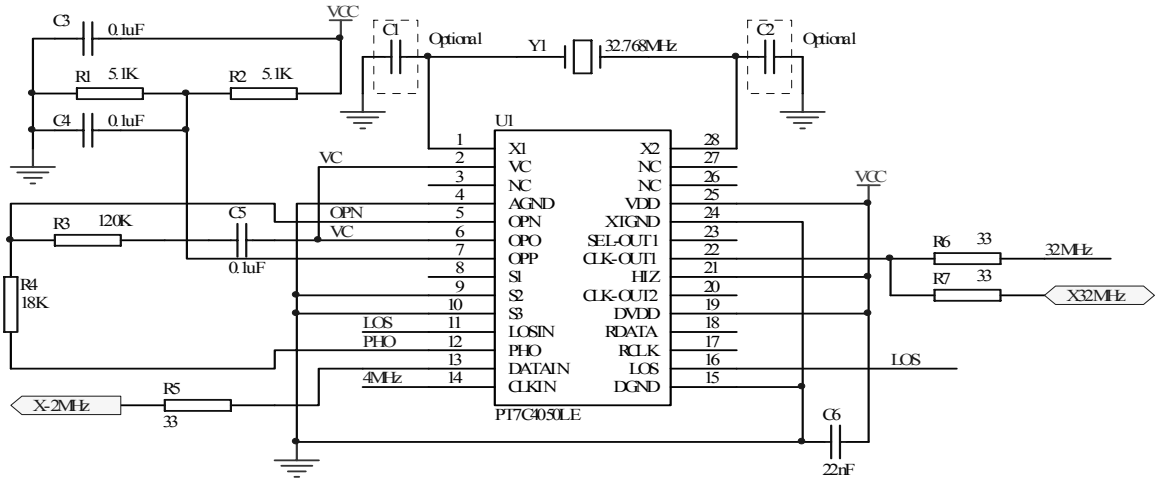
16.384/8.192

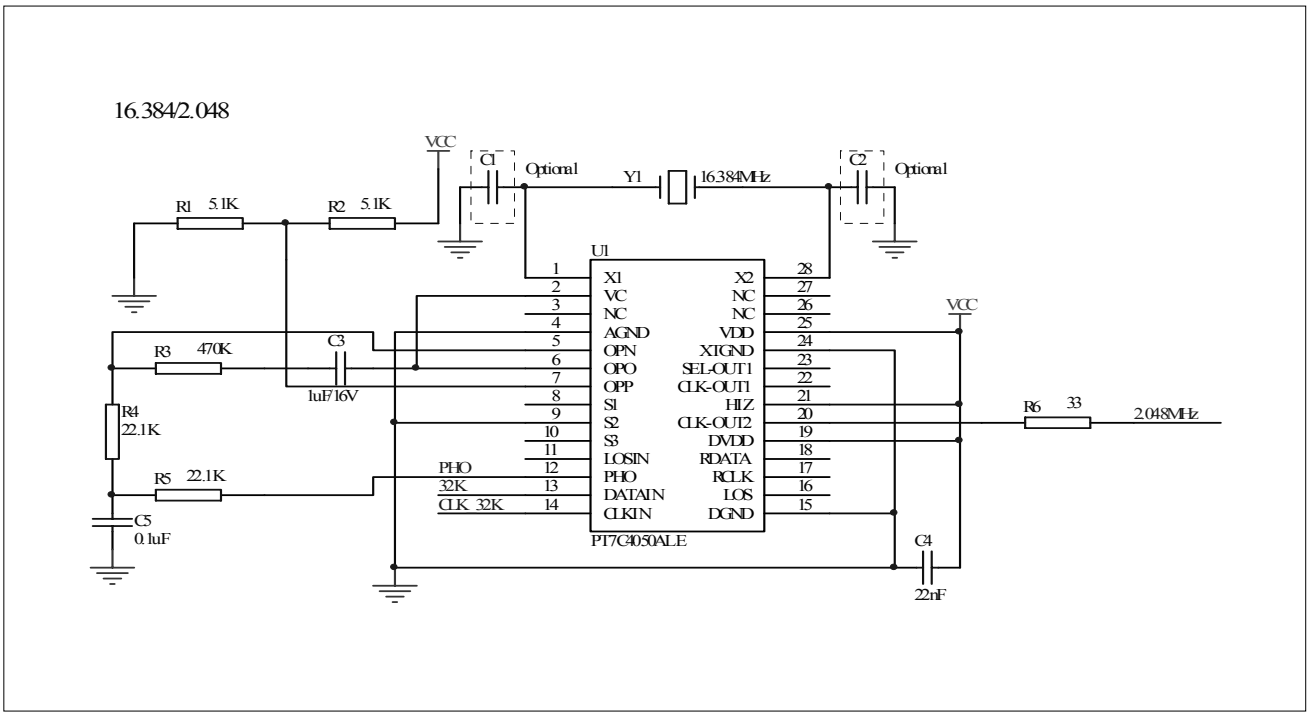


40.096/2.560



32.768/2.048





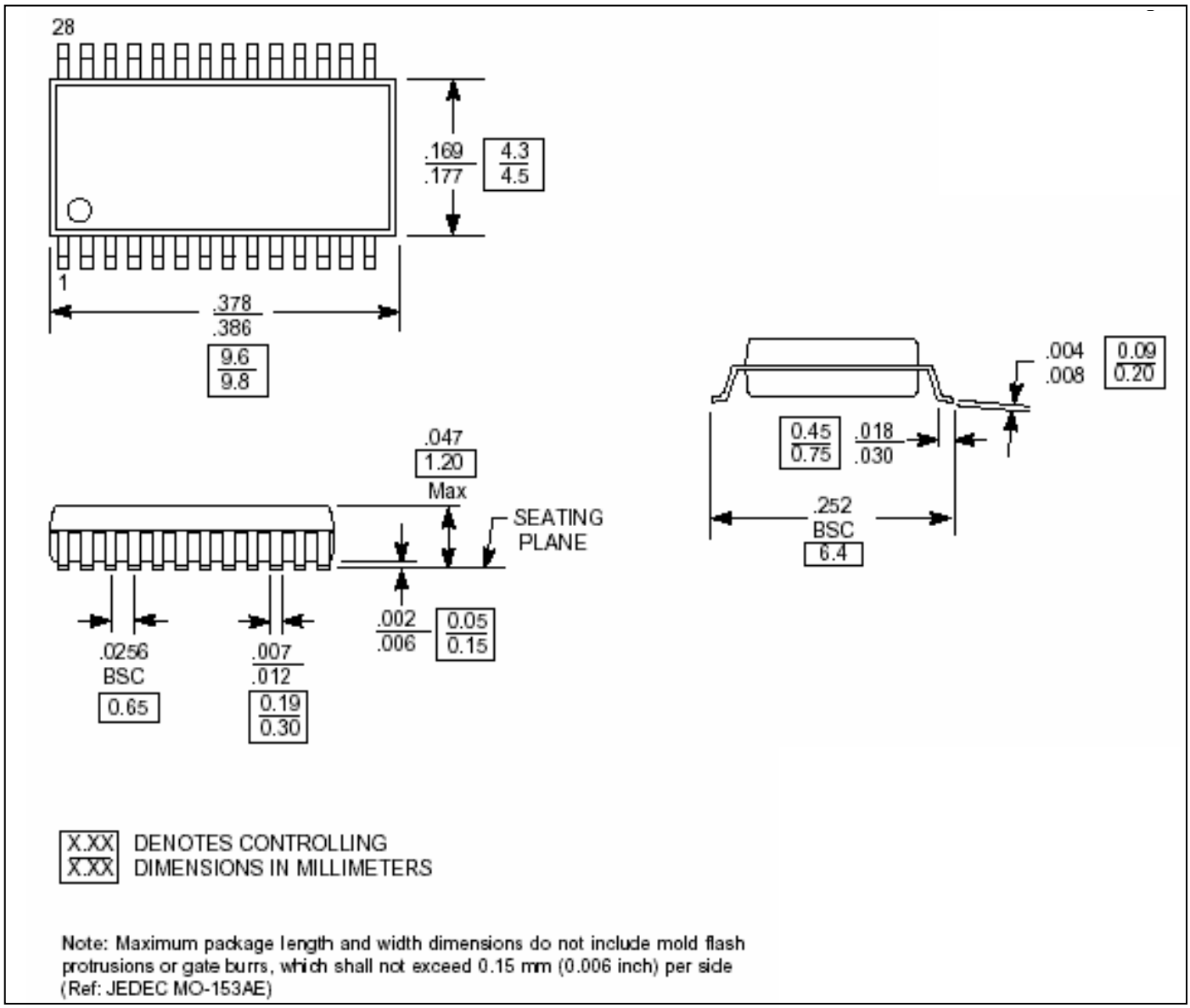
Recommended Crystal Specifications

Description	Crystal
Mode of Oscillation	Fundamental, AT cut
Frequency Range	12.0000 to 41.0000MHz
Frequency Tolerance	±20ppm (Max, 25℃)
Operating Temperature	-40℃ to 85℃
Load Capacitance (C_L)	12pF

Frequency Range (MHz)	Motional Capacitance	Shunt Capacitance	R_R max
12.0000 – 13.0000	11 fF	2.4 pF	50 Ω
13.0001 – 15.0000	12 fF	2.6 pF	50 Ω
15.0001 – 17.0000	13 fF	3.0 pF	40 Ω
17.0001 – 20.0000	14 fF	3.2 pF	40 Ω
20.0001 – 23.0000	15 fF	3.5 pF	30 Ω
23.0001 – 26.0000	16 fF	4.0 pF	30 Ω
26.0001 – 41.0000	17 fF	4.5 pF	25 Ω

Mechanical Information

LE (28-Pin TSSOP)



Notes

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