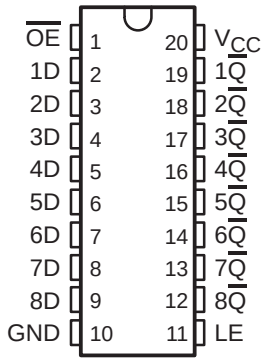
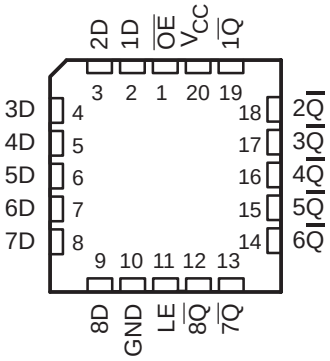
- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages**

**SN54ALS563B . . . J OR W PACKAGE**
**SN74ALS563B . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54ALS563B . . . FK PACKAGE**
**(TOP VIEW)**




## description

These 8-bit D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the complements of data (D) inputs. When LE is taken low, the outputs are latched at the inverses of the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high logic level provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS563B is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS563B is characterized for operation from 0°C to 70°C.

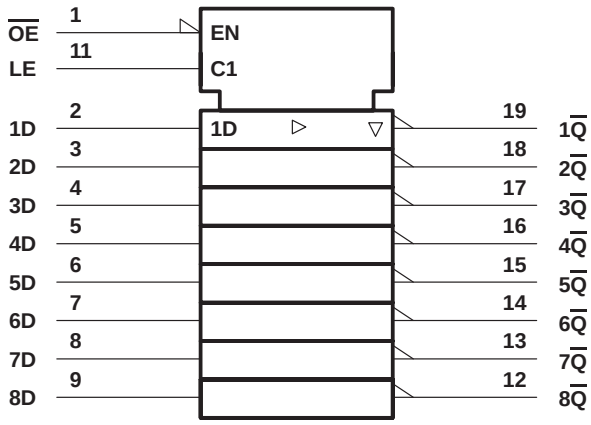
**FUNCTION TABLE**
**(each latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | $\overline{Q}$ |
| L | H | H | L |
| L | H | H | H |
| L | L | X | $Q_0$ |
| H | X | X | Z |

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

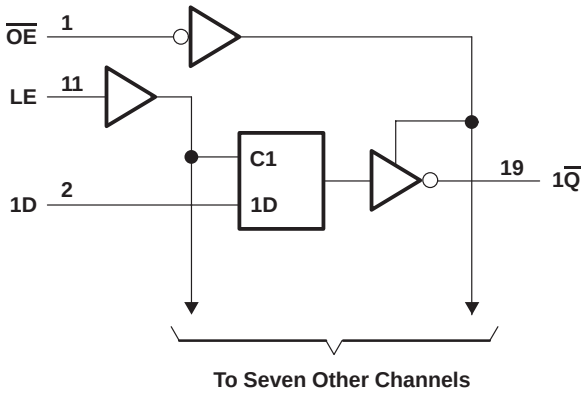
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## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, $T_A$: SN54ALS563B . . . . . –55°C to 125°C
SN74ALS563B . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | SN54ALS563B | | | SN74ALS563B | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | –1 | | | –2.6 | mA |
| $I_{OL}$ | Low-level output current | | | 12 | | | 24 | mA |
| $t_w$ | Pulse duration, LE high | 15 | | | 15 | | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 20 | | | 10 | | | ns |
| $t_h$ | Hold time, data after LE↓ | 12 | | | 10 | | | ns |
| $T_A$ | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54ALS563B | | | SN74ALS563B | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –0.4 mA | $V_{CC}$ –2 | | | $V_{CC}$ –2 | | | V |
| | $V_{CC}$ = 4.5 V | $I_{OH}$ = –1 mA | 2.4 | 3.3 | | | | | |
| | | $I_{OH}$ = –2.6 mA | | | | 2.4 | 3.2 | | |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{OZL}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | –20 | | | –20 | µA |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.1 | | | –0.1 | mA |
| $I_O$‡ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –20 | | –112 | –30 | | –112 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | Outputs high | | 10 | 17 | | 10 | 17 | mA |
| | | Outputs low | | 16 | 26 | | 16 | 26 | |
| | | Outputs disabled | | 17 | 29 | | 17 | 29 | |

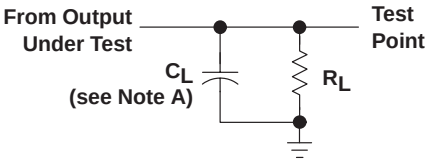
† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

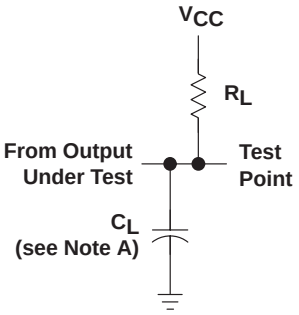
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54ALS563B | | SN74ALS563B | | |
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | $\overline{Q}$ | 3 | 26 | 3 | 18 | ns |
| $t_{PHL}$ | | | 3 | 15 | 3 | 14 | |
| $t_{PLH}$ | LE | $\overline{Q}$ | 8 | 29 | 6 | 22 | ns |
| $t_{PHL}$ | | | 4 | 22 | 6 | 21 | |
| $t_{PZH}$ | $\overline{OE}$ | $\overline{Q}$ | 4 | 25 | 3 | 18 | ns |
| $t_{PZL}$ | | | 4 | 21 | 4 | 18 | |
| $t_{PHZ}$ | $\overline{OE}$ | $\overline{Q}$ | 2 | 12 | 1 | 10 | ns |
| $t_{PLZ}$ | | | 3 | 22 | 1 | 15 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

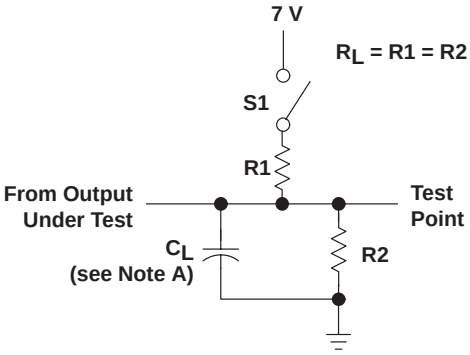
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



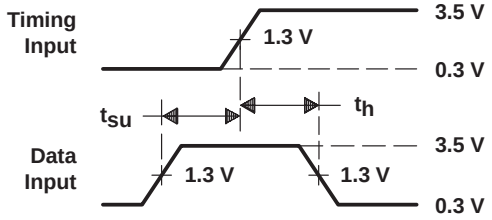

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



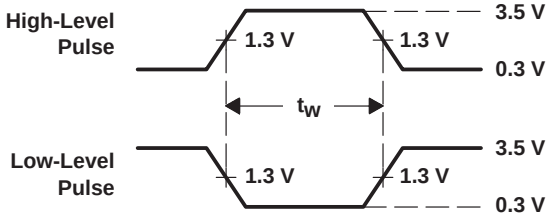

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



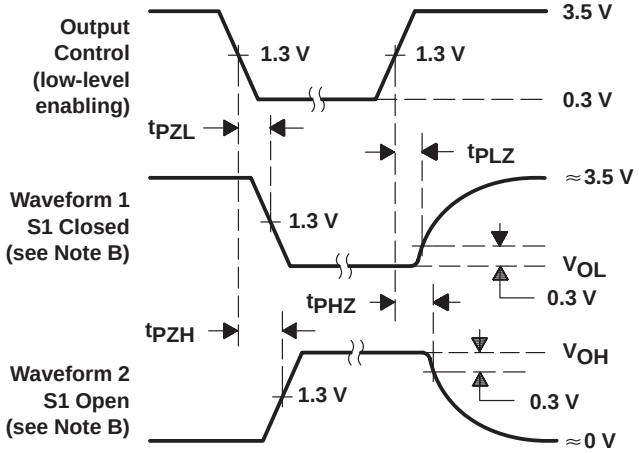

LOAD CIRCUIT
FOR 3-STATE OUTPUTS



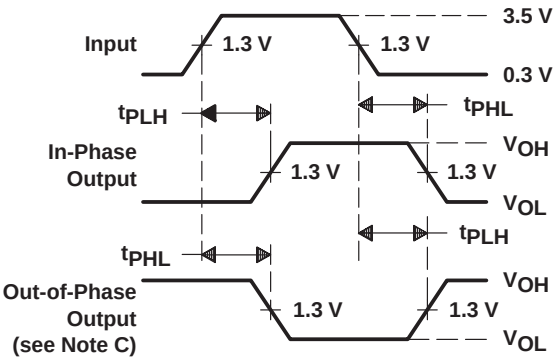

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

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