TPDxE05U06-Q1 1 and 4 Channel ESD Protection Diodes for SuperSpeed (Up to 6 Gbps) Interface

1 Features

- AEC-Q101 Qualified
  - Device HBM Classification Level H3B
  - Device CDM Classification Level C5
  - Device Temperature Range: –40°C to +125°C
- IEC 61000-4-2 Level 4 ESD Protection (See the *ESD Ratings—IEC Specification Table*)
  - ±12-kV Contact Discharge
  - ±15-kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 2.5 A (8/20 µs)
- I/O Capacitance 0.42 pF to 0.5 pF (Typical)
- DC Breakdown Voltage 6.4 V (Minimum)
- Ultra Low Leakage Current 10 nA (Maximum)
- Low ESD Clamping Voltage (14 V at 5-A TLP)
- Easy Flow-Through Routing Packages

2 Applications

- End Equipment
  - Head Unit
  - Rear Seat Entertainment
  - Telematics
  - USB Hub
  - Navigation Module
  - Media Interface
- Interfaces
  - USB 2.0
  - USB 3.0
  - HDMI 1.4/2.0
  - LVDS
  - DisplayPort
  - SIM Card

3 Description

The TPDxE05U06-Q1 is a family of unidirectional Transient Voltage Suppressor (TVS) Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. They are rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 level 4 international standard. The ultra-low loading capacitance makes these devices ideal for protecting any high-speed signal applications up to 6 Gbps.

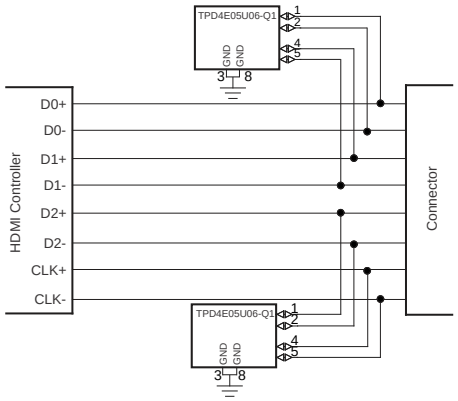
These devices are also available without automotive qualification: TPDxE05U06.

Device Information[1]

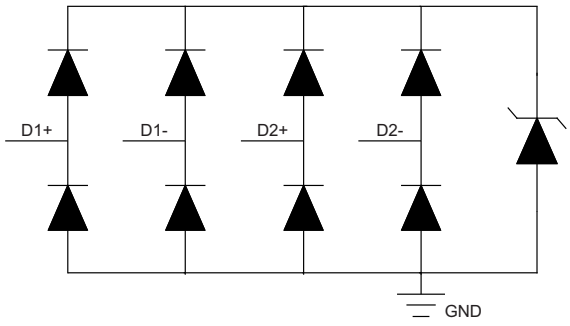
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4E05U06-Q1	USON (10)	2.50 mm × 1.00 mm
TPD1E05U06-Q1	X1SON (2)	0.60 mm x 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

TPD4E05U06-Q1 Simplified Schematic



TPD4E05U06-Q1 Block Diagram



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4 Revision History

Changes from Revision A (August 2014) to Revision B **Page**

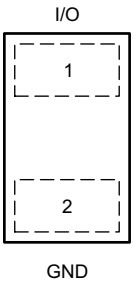
- Added 1-channel (TPD1E05U06-Q1) package ... 1
- Added DPY package information in *Thermal Information* table ... 4
- Added DPY package Dynamic resistance in *Electrical Characteristics* table ... 5
- Added DPY package Line capacitance in *Electrical Characteristics* table ... 5

Changes from Original (August 2014) to Revision A **Page**

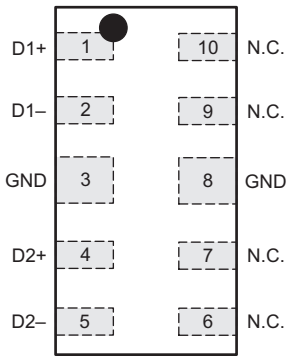
- Added (See the *ESD Ratings—IEC Specification Table*) to Feature: IEC 61000-4-2 Level 4 ESD Protection ... 1

5 Pin Configuration and Functions

DPY Package
2-Pin X1SON
Top View



DQA Package
10-Pin USON
Top View



Pin Functions TPD1E05U06-Q1 DPY

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	I/O	I/O	ESD Protected Channel(1)
2	GND	Ground	Ground; Connect to ground

(1) Place as close to the connector as possible.

Pin Functions TPD4E05U06-Q1 DQA

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	D1+	I/O	ESD Protected Channel(1)
2	D1–	I/O	ESD Protected Channel(1)
4	D2+	I/O	ESD Protected Channel(1)
5	D2–	I/O	ESD Protected Channel(1)
6, 7, 9, 10	NC	NC	Not Connected; Used for optional straight-through routing. Can be left floating or grounded
3, 8	GND	Ground	Ground; Connect to ground

(1) Place as close to the connector as possible.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-4 (5/50 ns)		80	A
Peak pulse	IEC 61000-4-5 Current (tp – 8/20 µs)		2.5	A
	IEC 61000-4-5 Power (tp – 8/20 µs) - TPD4E05U06-Q1 (3)		40	W
	IEC 61000-4-5 Power (tp – 8/20 µs) - TPD1E05U06-Q1 (3)		30	W
T_A	Operating temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are with respect to GND unless otherwise noted.
(3) Measured at 25°C

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (1)	Human-body model (HBM), per AEC Q100-002 (2)	±8000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
V(ESD)	Electrostatic Discharge	IEC 61000-4-2 contact discharge - TPD4E05U06-Q1 (1)	±12000	V
		IEC 61000-4-2 contact discharge - TPD1E05U06-Q1	±12000	
		IEC 61000-4-2 air-gap discharge	±15000	

(1) Measured at 25°C, per IEC 61000.4.2 Ed. 2.0 Section 7.2.4.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	0	5.5	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC (1)		TPD1E05U06-Q1	TPD4E05U06-Q1	UNIT
		DPY (X1SON)	DQA (USON)	
		2 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	697.3	327	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	471	189.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	575.9	257.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	175.7	60.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	575.1	257	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT – OUTPUT RESISTANCE								
V_{RWM}	Reverse stand-off voltage		I_{IO} < 10 µA				5.5	V
V_{BR}	Break-down voltage		I_{IO} = 1 mA		6.4		8.7	V
V_{CLAMP}	Clamp voltage		I_{PP} = 1 A, TLP, from I/O to GND (1)			10		V
			I_{PP} = 5 A, TLP, from I/O to GND (1)			14		
			I_{PP} = 1 A, TLP, from GND to I/O (1)			3		
			I_{PP} = 5 A, TLP, from GND to I/O (1)			7.5		
I_{LEAK}	Leakage current		V_{IO} = 2.5 V			1	10	nA
R_{DYN}	Dynamic resistance	DPY package	I/O to GND (2)			0.8		Ω
			GND to I/O (2)			0.7		
		DQA package	I/O to GND (2)			0.96		
			GND to I/O (2)			0.9		
CAPACITANCE								
C_L	Line capacitance		V_{IO} = 2.5 V, f = 1 MHz, I/O to GND	TPD1E05U06-Q1 DPY package		0.42		pF
				TPD4E05U06-Q1 DQA package		0.5		
$\Delta C_{IO\text{-}TO\text{-}GND}$	Variation of input capacitance		GND Pin = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, Channel x pin to GND – channel y pin to GND			0.05	0.08	pF
C_{CROSS}	Channel to channel input capacitance		GND Pin = 0 V, f = 1 MHz, V_{BIAS} = 2.5 V, between channel pins			0.04	0.08	pF

(1) Transition line pulse with 100 ns width, 200 ps rise time.
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 5 A and I = 10 A.

6.7 Typical Characteristics

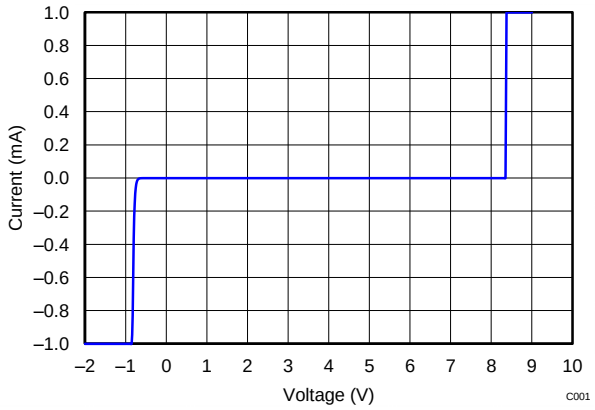


Figure 1. Current vs Voltage
Current vs Voltage DC Voltage Sweep I-V Curve

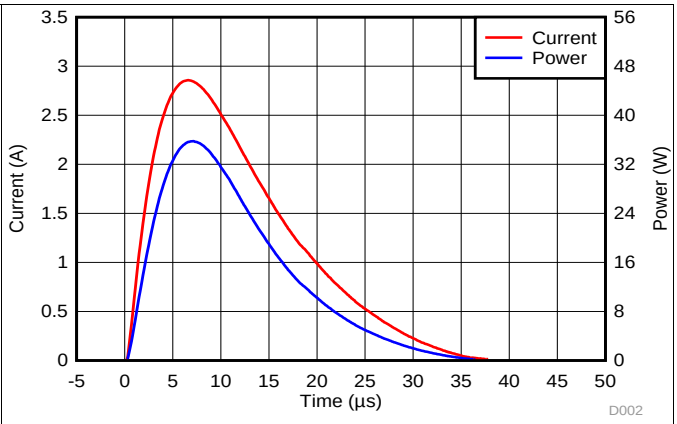


Figure 2. Current and Power vs Time
Surge Curve (tp = 8/20 µs), Pin I/O to GND

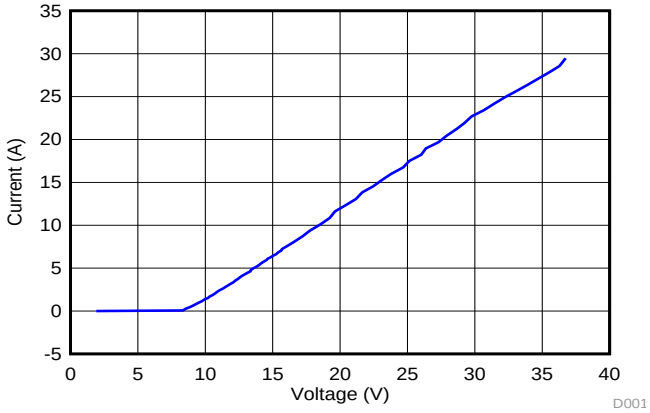


Figure 3. Current vs Voltage
Positive TLP Plot I/O to GND

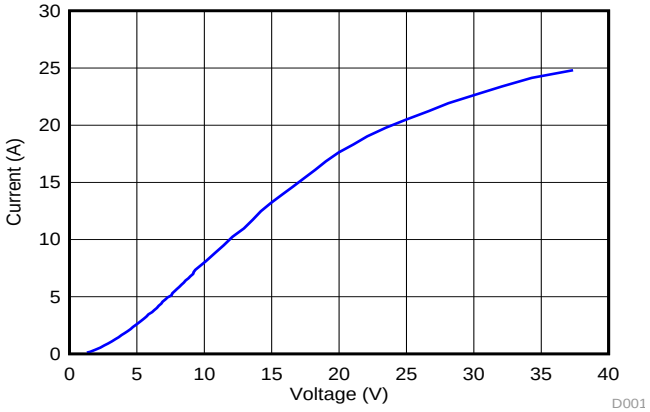


Figure 4. Current vs Voltage
Negative TLP Plot I/O to GND

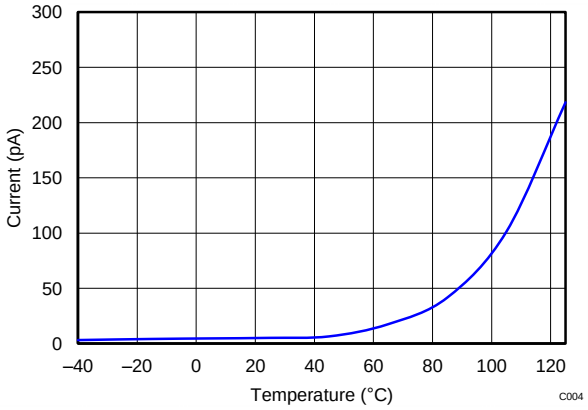


Figure 5. Leakage Current vs Temperature

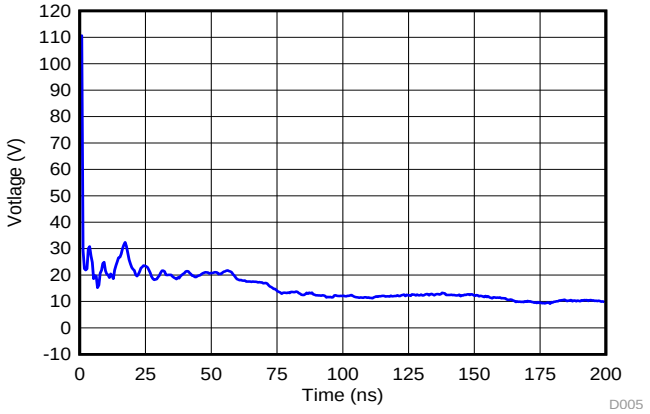


Figure 6. Voltage vs Time 8-kV IEC Waveform

Typical Characteristics (continued)

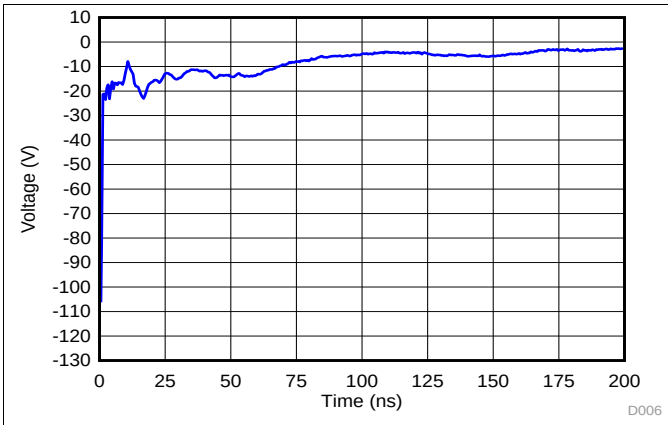


Figure 7. Voltage vs Time –8-kV IEC Waveform

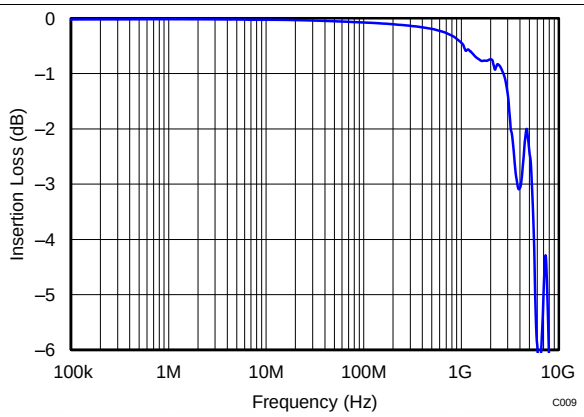


Figure 8. Insertion Loss vs Frequency

7 Detailed Description

7.1 Overview

The TPDxE05U06-Q1 is a family of unidirectional TVS ESD protection diode arrays with ultra-low capacitance between 0.42 pF and 0.5 pF. They are rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 level 4 international standard (12-kV contact, 15-kV air gap). The ultra-low loading capacitance makes them ideal for protecting any high-speed signal applications up to 6 Gbps.

7.2 Functional Block Diagram

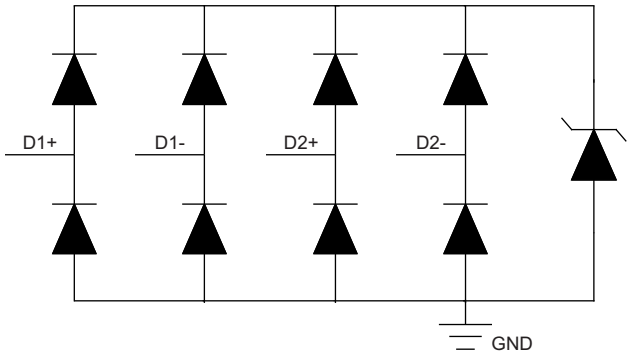


Figure 9. TPD4E05U06-Q1 Block Diagram

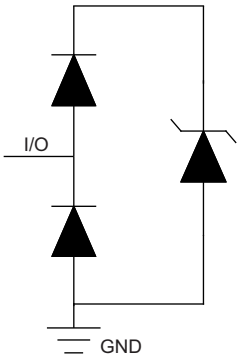


Figure 10. TPD1E05U06-Q1 Block Diagram

7.3 Feature Description

7.3.1 AEC-Q101 Qualification

These devices are qualified to AEC-Q101 standards. They pass HBM H3B (±8 kV) and CDM C5 (±1 kV) ESD ratings and are qualified to operate from –40°C to +125°C.

7.3.2 IEC 61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to ±12-kV contact and ±15-kV air. An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

Feature Description (continued)

7.3.4 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 40 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.5 I/O Capacitance

The capacitance between each I/O pin to ground is 0.5 pF. These capacitances support data rates up to 5 Gbps.

7.3.6 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.4 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5 V.

7.3.7 Ultra-Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (Maximum) with a bias of 2.5 V.

7.3.8 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 10 V (I_{PP} = 1 A).

7.3.9 Easy Flow-Through Routing

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPDxE05U06-Q1 are passive integrated circuits that triggers when voltages are above V_{BR} or below the lower diodes V_f (–0.6 V). During ESD events, voltages as high as ±15 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPDxE05U06-Q1 (usually within 10s of nano-seconds) the devices reverts to passive.

8 Application and Implementation

8.1 Application Information

The TPD4E05U06-Q1 is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

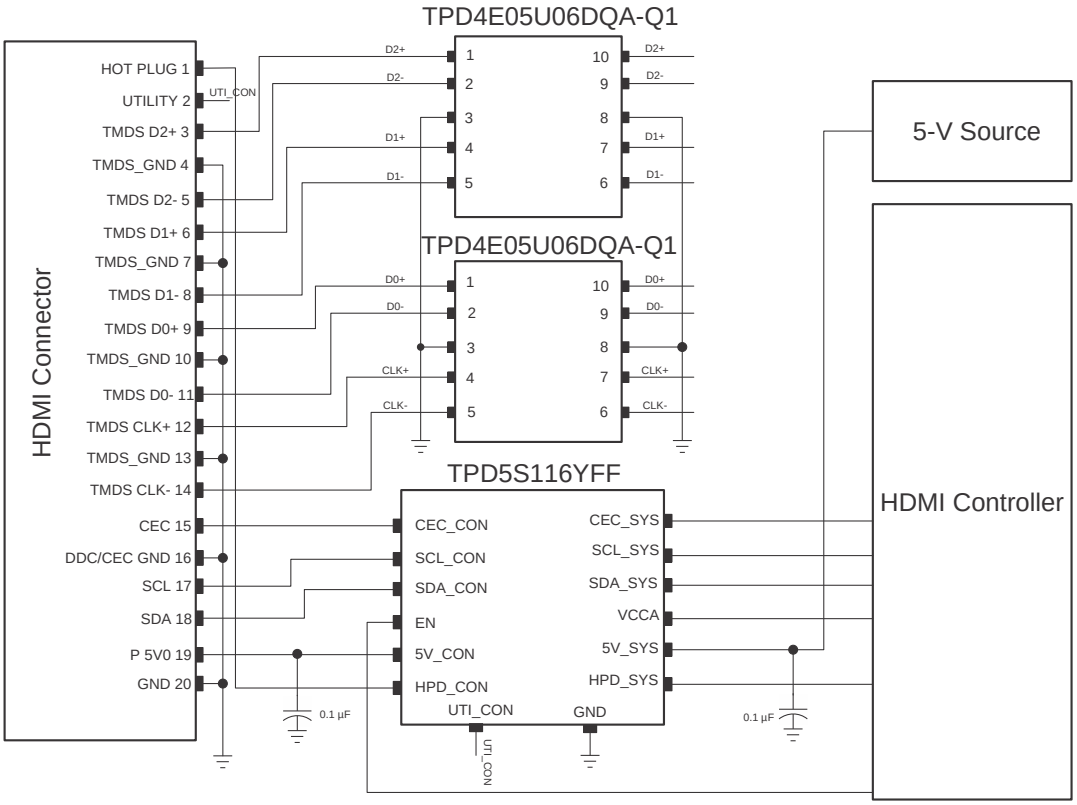


Figure 11. HDMI 1.4 Application

8.2.1 Design Requirements

For this design example, two TPD4E05U06-Q1 devices, and a TPD5S116 are being used in an HDMI 1.4 application. This provides a complete port protection scheme.

Given the HDMI 1.4 application, the parameters in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on pins 1, 2, 4, or 5	0 V to 5 V
Operating frequency	1.7 GHz

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

8.2.2.1 Signal Range on Pin 1, 2, 4, or 5

The TPD4E05U06-Q1 has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 I/O channels protect which signal lines. Any I/O will support a signal range of 0 to 5.5 V.

8.2.2.2 Operating Frequency

The TPD4E05U06-Q1 has a capacitance of 0.5 pF (Typical), supporting HDMI 1.4 data rates.

8.2.3 Application Curve

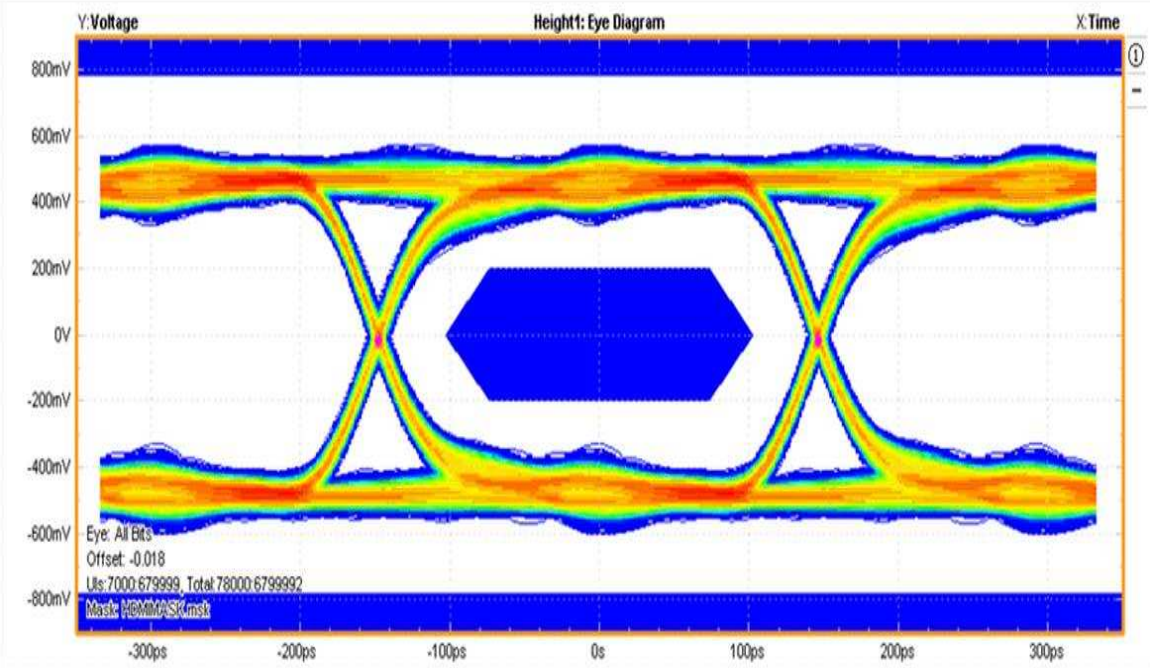


Figure 12. 3.4 Gbps HDMI Eye Diagram

9 Layout

9.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

9.2 Layout Example

This application is typical of an HDMI 1.4 layout.

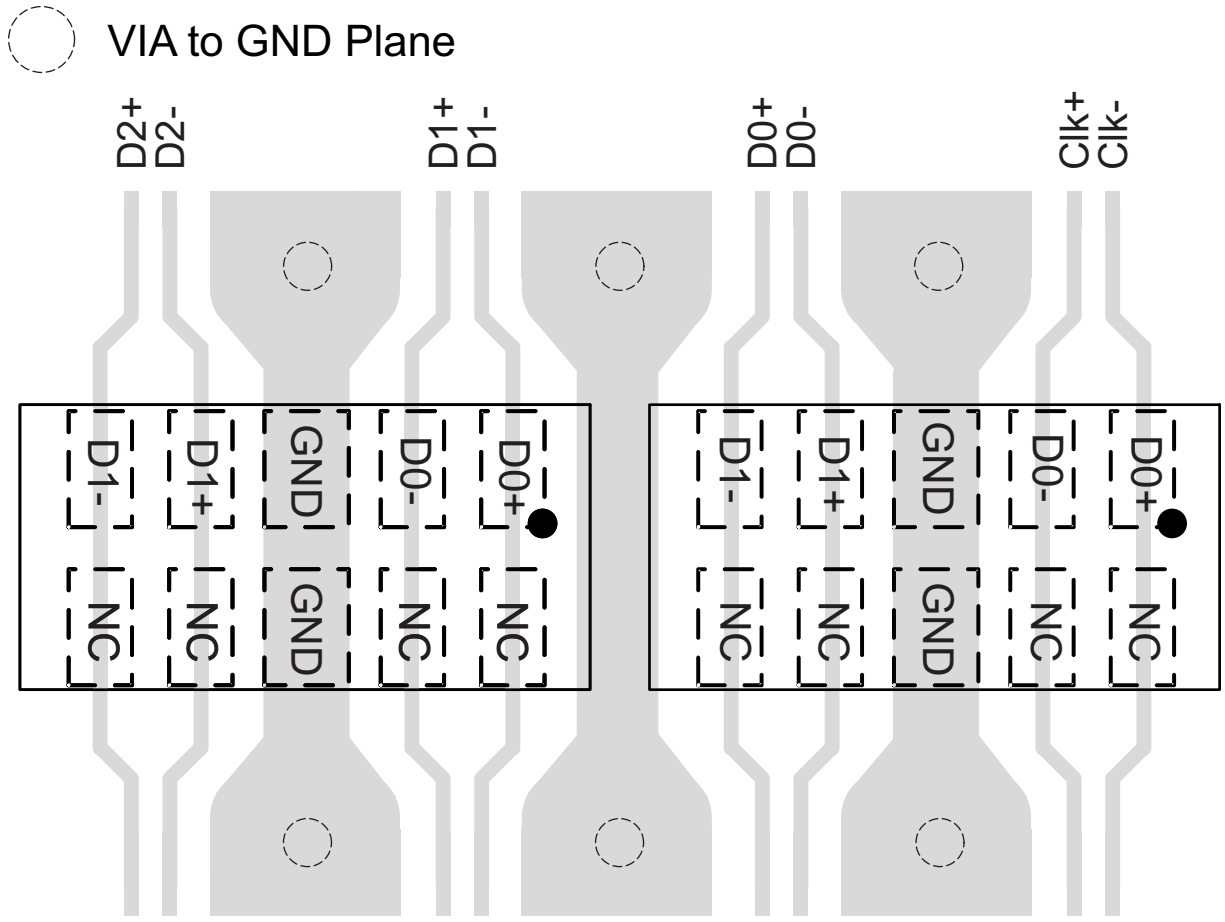


Figure 13. TPD4E05U06-Q1 Layout

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- *TPD1E05U06-Q1 Evaluation Module User's Guide*
- *Reading and Understanding an ESD Protection Datasheet*
- *ESD Layout Guide*
- *TPD4E05U06DQA EVM User's Guide*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPD4E05U06-Q1	Click here	Click here	Click here	Click here	Click here
TPD1E05U06-Q1	Click here	Click here	Click here	Click here	Click here

10.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E05U06QDPYRQ1	PREVIEW	X1SON	DPY	2	10000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	4O	
TPD4E05U06QDQARQ1	ACTIVE	USON	DQA	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BRH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPD4E05U06-Q1 :

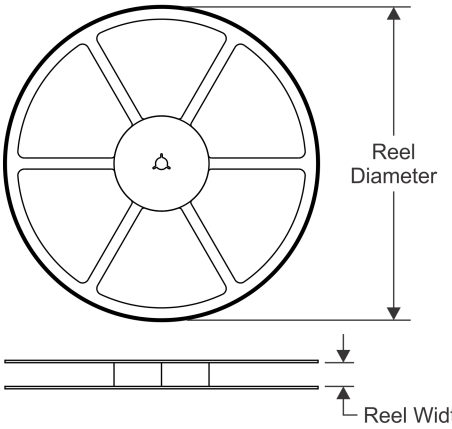
- Catalog: TPD4E05U06

NOTE: Qualified Version Definitions:

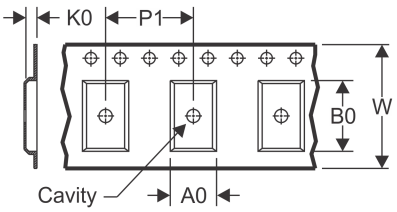
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

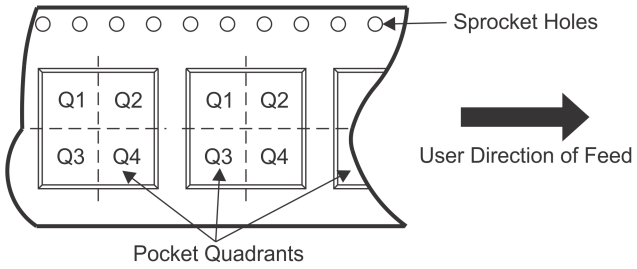


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

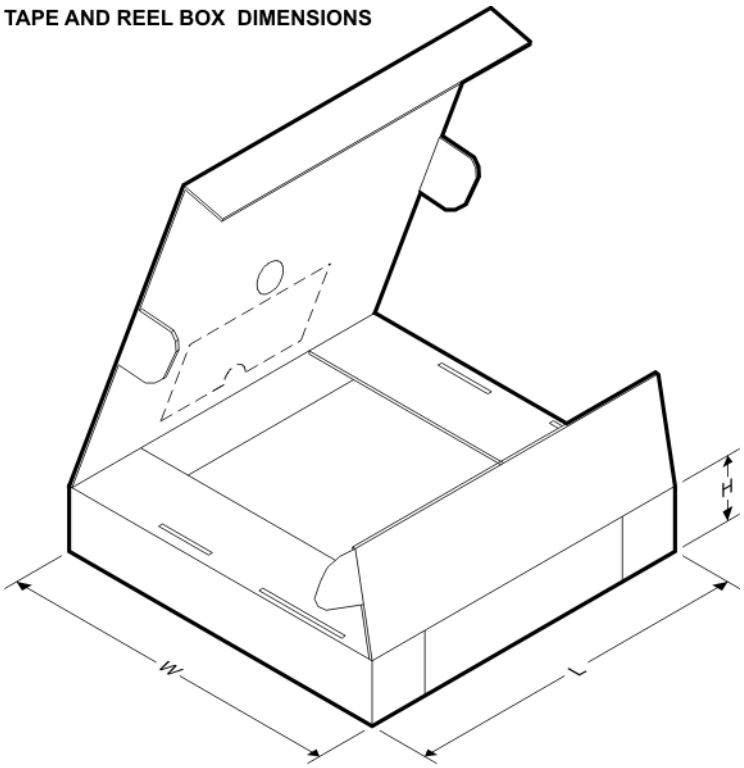
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E05U06QDQARQ1	USON	DQA	10	3000	180.0	8.4	1.3	2.83	0.65	4.0	8.0	Q1

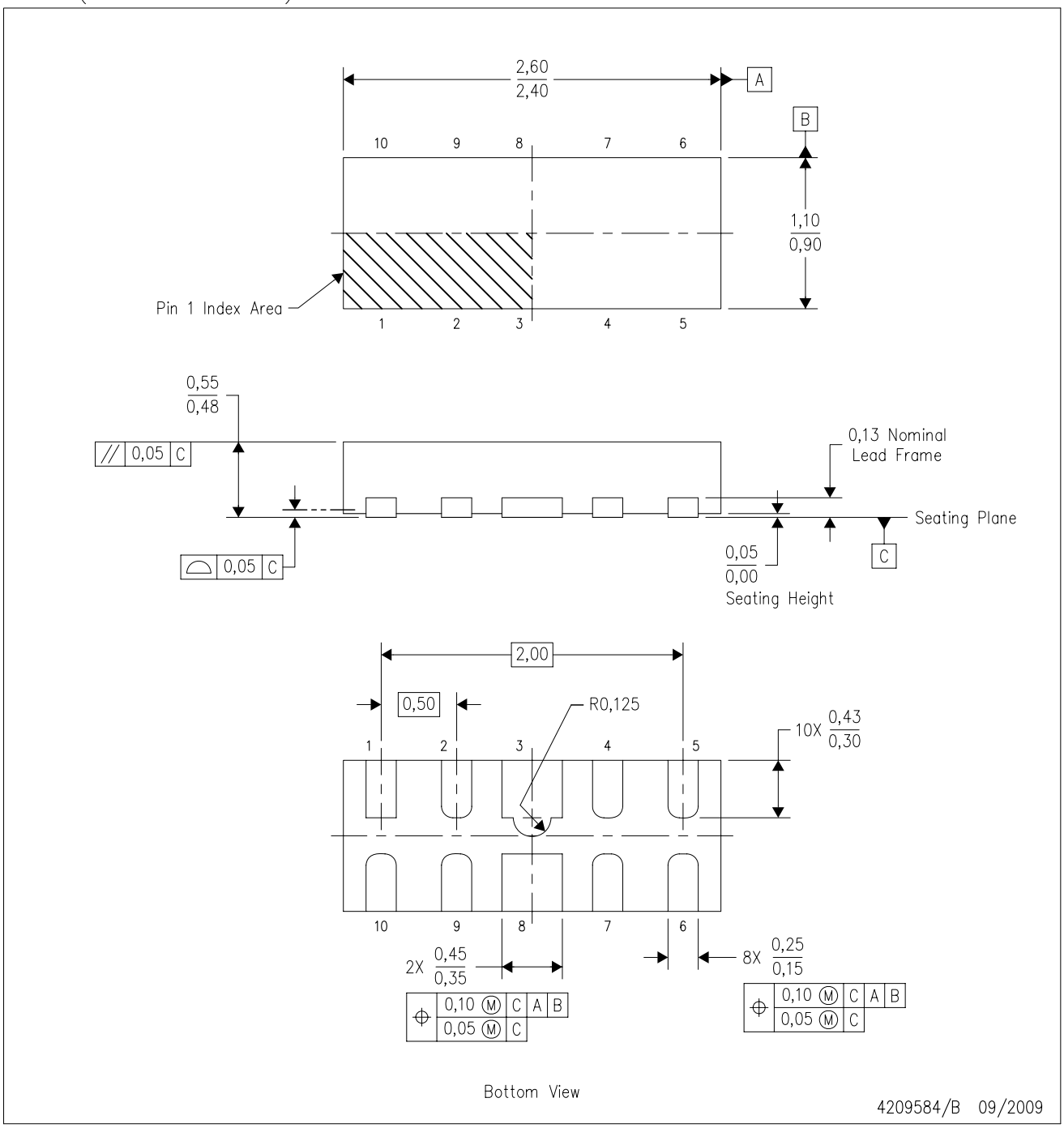
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

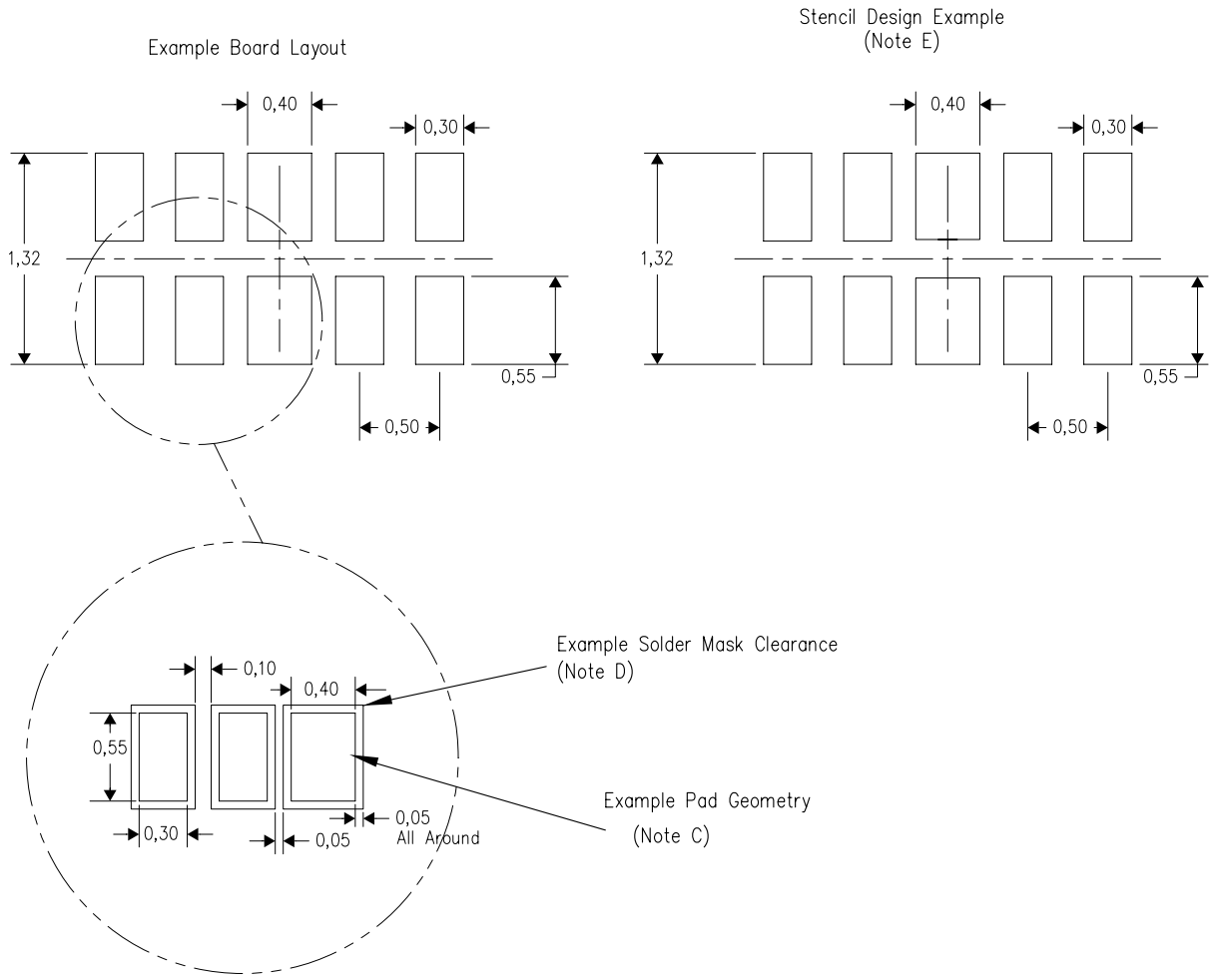
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E05U06QDQARQ1	USON	DQA	10	3000	223.0	270.0	35.0

DQA (R–PSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



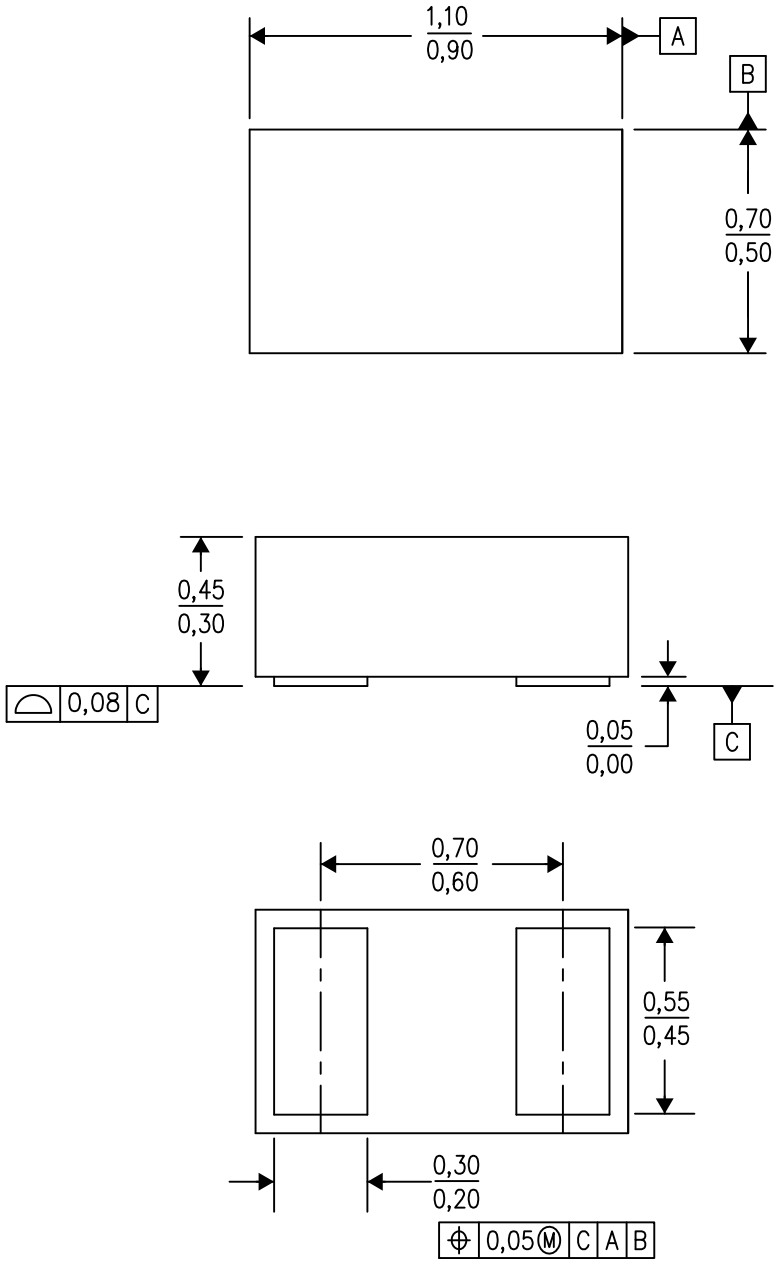
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

DQA (R–PUSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

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