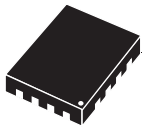
STG5683

Low voltage dual SPDTswitch with negative rail capability

Features

- Distortion-free negative signal throughput down to V_{CC}-5.5V
- Wide operating voltage range: V_{CC} (Opr) = 1.65V to 4.5V single supply
- Ultra low power dissipation: I_{CC} = 0.2µA (Max.) at t_A = 85°C
- Low "ON" resistance V_{IN} = 0V: R_{ON} = 0.5Ω (max. t_A = 25°C) at V_{CC} = 4.3V
- 4.3V tolerant and 1.8V compatible threshold on digital control input at V_{CC} = 1.65 to 3.0V
- Latch-up performance exceeds 300mA (JESD 17)
- ESD performance exceeds JESD22
- 2000-V human-body model (A114-A)



QFN16L (2.6mm x 1.8mm)

Description

The STG5683 is a high-speed CMOS low voltage dual analog S.P.D.T. (Single Pole Dual Throw) SWITCH or 2:1 Multiplexer /Demultiplexer Switch fabricated in silicon gate C^2MOS technology. It is designed to operate from 1.65V to 4.5V, making this device ideal for portable applications.

Additional key features are fast switching speed, Break Before Make Delay Time and Ultra Low Power Consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Figure 1. Device summary

Order code	Package	Packaging
STG5683QTR	QFN16L (2.6mm x 1.8mm)	Tape and reel

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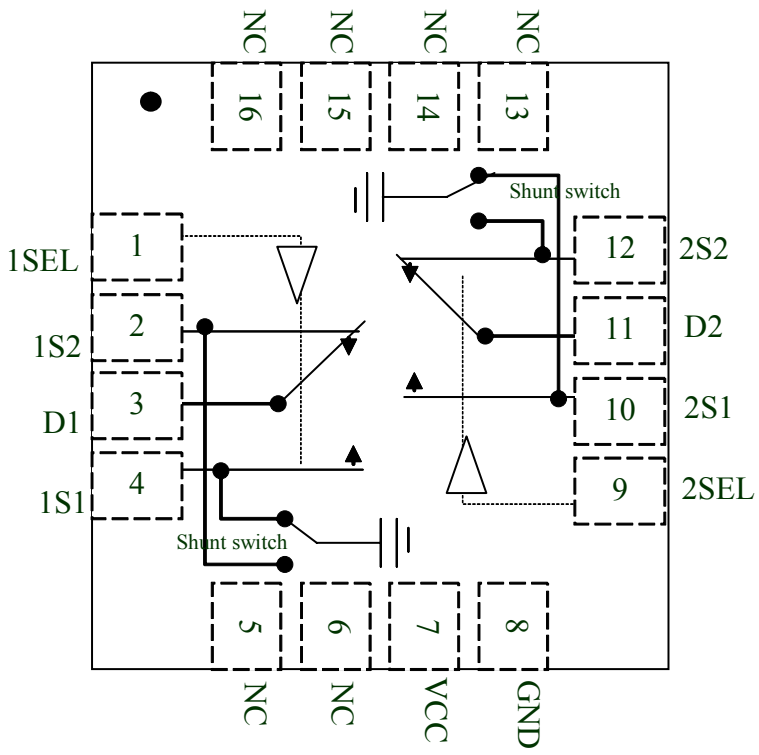
1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top through view)



1.2 Pin description

Table 1. Pin description

Pin N°	Symbol	Name and function
4, 2, 10, 12	1S1, 1S2, 2S1, 2S2	Independent channels
3, 11	D1, D2	Common channel
1, 9	1SEL, 2SEL	Control
7	V_{CC}	Positive supply voltage
8	GND	Ground (0V)
5,6,13,14,15,16	NC	No connect

2 Device summary

Figure 3. Input equivalent circuit

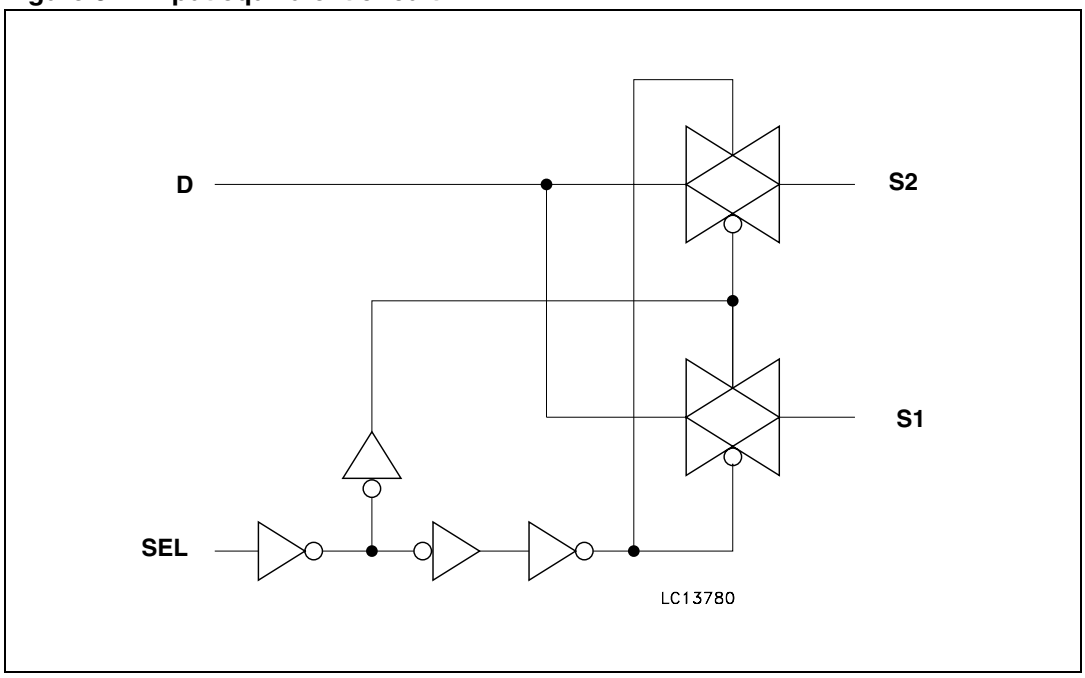


Table 2. Truth table

SEL	Switch S1	Switch S2
H	ON	OFF (1)
L	OFF (1)	ON

1. Shorted to ground by the shunt switch

3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to 5.5	V
V_I	DC input voltage	- (V_{CC} - 6.0V) to V_{CC} + 0.5	V
V_{IC}	DC control input voltage	-0.5 to 5.5	V
V_O	DC output voltage	- (V_{CC} - 6.0V) to V_{CC} + 0.5	V
I_{IKC}	DC input diode current on control pin (V_{SEL}<0V)	-50	mA
I_{IK}	DC input diode current (V_{SEL}<0V)	±50	mA
I_{OK}	DC output diode current	±20	mA
I_O	DC output current	±150	mA
I_{OP}	DC output current peak (pulse at 1ms, 10% duty cycle)	±400	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at T_A = 70°C (1)	1120	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 sec)	300	°C

1. Derate above 70ºC by 18.5mW/C

3.1 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage[1]		1.65 to 4.5	V
V_I	Input voltage		V_{CC} -5.5 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.5	V
V_O	Output voltage		V_{CC} -5.5 to V_{CC}	V
T_{op}	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	V_{CC} = 1.65V to 2.7V	0 to 20	ns/V
		V_{CC} = 3.0 to 4.3V	0 to 10	

1. Truth Table guaranteed: 1.2V to 4.3V

4 Electrical characteristics

Table 5. DC specifications

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
V_{IH}	High level input voltage	1.65 -1.95		0.65V_{CC}			0.65V_{CC}		V
		2.3-2.5		1.0			1.4		
		2.7-3.0		1.1			1.5		
		3.3-4.3		1.3			1.6		
V_{IL}	Low level input voltage	1.65-1.95				0.5		0.5	V
		2.3-2.5				0.5		0.4	
		2.7-3.0				0.6		0.5	
		3.3-4.3				0.7		0.6	
R_{ON}	Switch ON resistance	1.8	V_S = V_{CC} -5.5V to V_{CC}; I_S = 100mA		3.20	4.0			Ω
		2.7			0.77	0.90			
		3.0			0.64	0.80			
		3.6			0.51	0.65			
		4.3			0.45	0.55			
ΔR_{ON}	ON resistance match between channels (1)	1.8	V_S @ R_{ON} Max I_S = 100mA		50				mΩ
		2.7			20				
		3.0			15				
		3.6			15				
		4.3			15				
R_{FLAT}	ON resistance flatness (2)	1.8	V_S = V_{CC} -5.5V to V_{CC}; I_S = 100mA		3.0				Ω
		2.7			0.50				
		3.0			0.40				
		3.6			0.25				
		4.3			0.16				
R_{SH}	Shunt switch resistance	2.7	S1 or S2 = 10mA		70	100			Ω
I_{ON}	Sn ON State Leakage Current	4.3	V_S = -1.2 to 4.3V V_D = Open	-0.1		0.1	-1	1	µA

Table 5. DC specifications (continued)

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
I_D	D ON State Leakage Current	4.3	V_S = Open V_D = 4.3 to -1.2V	-0.1		0.1	-1	1	µA
I_{IH},I_{IL}	SEL Leakage Current	4.3	V_{SEL}=4.3V or GND	-0.1		0.1	-1	1	µA
I_{CCLV}	Quiescent Supply Current Low Voltage Driving	4.3	V_{1SEL}, V_{2SEL} = 1.65V		±37	±50		±100	µA
			V_{1SEL}, V_{2SEL} = 1.80V		±33	±40		±50	
			V_{1SEL}, V_{2SEL} = 2.60V		±12	±20		±30	
I_{CC}	Quiescent Supply Current	4.3	V_{SEL}= V_{CC} or GND			±50		±200	nA

1. Note 1: ΔRon = max |mSN-nSN|, where m = 1..4 and n = 1..4, N = 1..2
2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 6. AC electrical characteristics (C_L = 35pF, R_L = 50Ω, $t_r = t_f \leq$ 5ns)

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation delay	1.65-1.95			0.45				ns
		2.3-2.7			0.40				
		3.0-3.3			0.30				
		3.6-4.3			0.25				
t_{ON}	Turn-ON time	1.65-1.95	V_S = 0.8V		180	220			ns
		2.3-2.7	V_S = 1.5V		100	130			
		3.0-3.3			72	95			
		3.6-4.3			58	80			
t_{OFF}	Turn-OFF time	1.65-1.95	V_S = 0.8		64	80			ns
		2.3-2.7	V_S = 1.5V		41	60			
		3.0-3.3			34	50			
		3.6-4.3			33	50			
t_D	Break before make time delay	1.65-1.95	C_L = 35pF R_L = 50Ω $V_S = V_{CC}\backslash 2$	1	110				ns
		2.3-2.7		1	58				
		3.0-3.3		1	40				
		3.6-4.3		1	23				
Q	Charge injection	1.65-1.95	C_L = 100pF V_{GEN} = 0V		16				pC
		2.3-2.7			25				
		3.0-3.3			34				
		3.6-4.3			46				

Table 7. Analog switch characteristics (C_L = 5pF, R_L = 50Ω, T_A = 25°C)

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T_A = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
OIRR	OFF Isolation (1)	2.7 - 4.3	$V_S = 1V_{RMS}$, f = 100kHz		-55				dB
Xtalk	Crosstalk	2.7 - 4.3	$V_S = 1V_{RMS}$, f = 100kHz		-60				dB
THD	Total harmonic distortion	2.7 - 4.3	R_L = 32Ω $V_{IN} = 0.5V_{PP}$ DC Bias = 0 f = 20Hz to 20 kHz		0.01				%
BW	-3dB bandwidth	2.7 - 4.3	R_L = 50Ω Signal = 0dBm		33				MHz
C_{IN}	Control pin input capacitance	3.3			6				pF
C_D	D Port capacitance when switch is enabled	3.3	f = 1MHz		290				

1. Off Isolation = 20Log10 (V_D/V_S), V_D = output. V_S = input to off switch.

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 8. QFN16L (2.6x1.8mm) mechanical data

Dim.	mm.		
	Min	Typ	Max
A	0.45	0.55	0.60
A1	0	0.02	0.05
b	0.15	0.20	0.25
D	2.50	2.60	2.70
E	1.70	1.80	1.90
e		0.40	
L	0.35	0.40	0.45

Note: 1 VFQFPN - Standard for thermally enhanced vey fine pitch quad flat package no leads.

2 The leads size is comprehensive of the thickness of the leads finishing material.

3 Dimensions do not include mold protusion.

4 Package outline exclusive of metal burrs dimensions.

5 Shipping media tape and reel units: 3000

Figure 4. Foot print recommendation

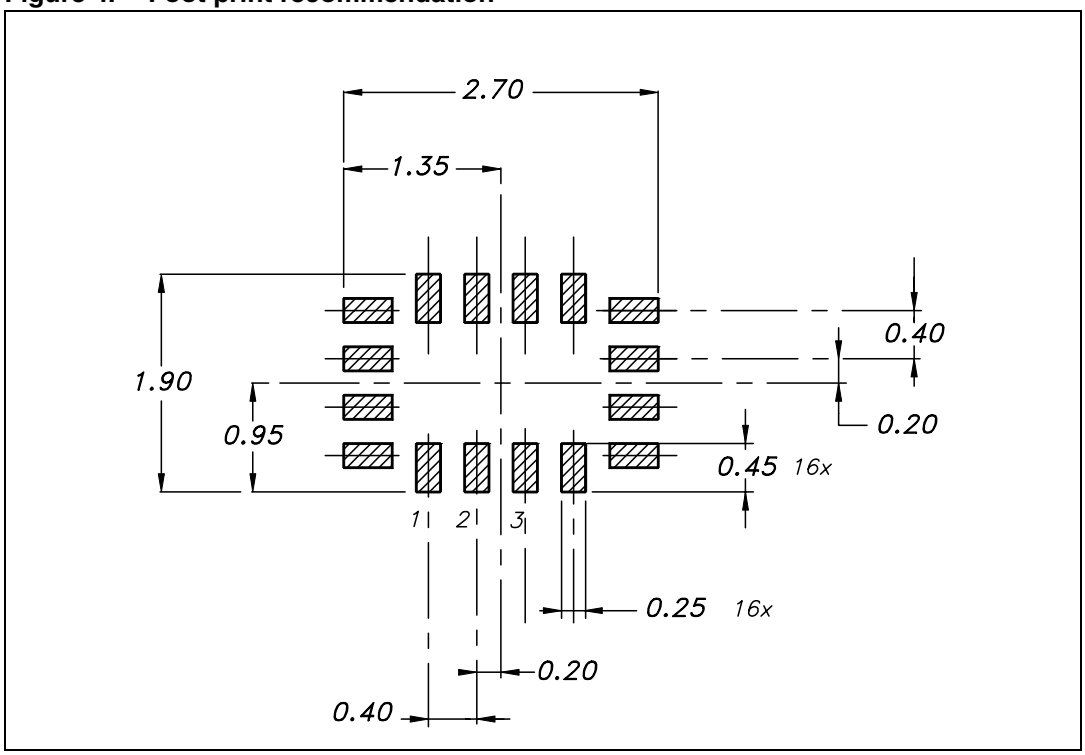


Figure 5. Package information

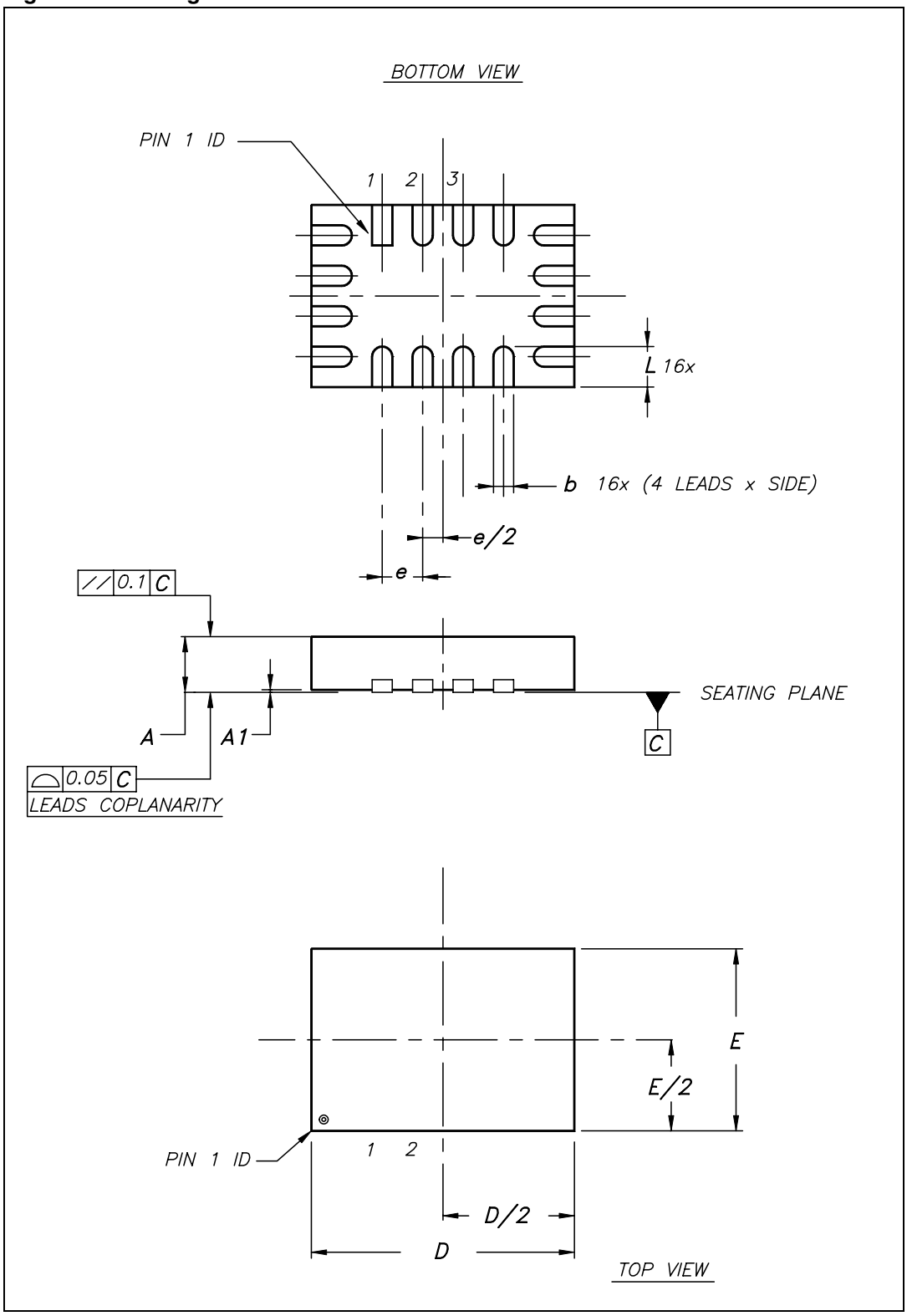
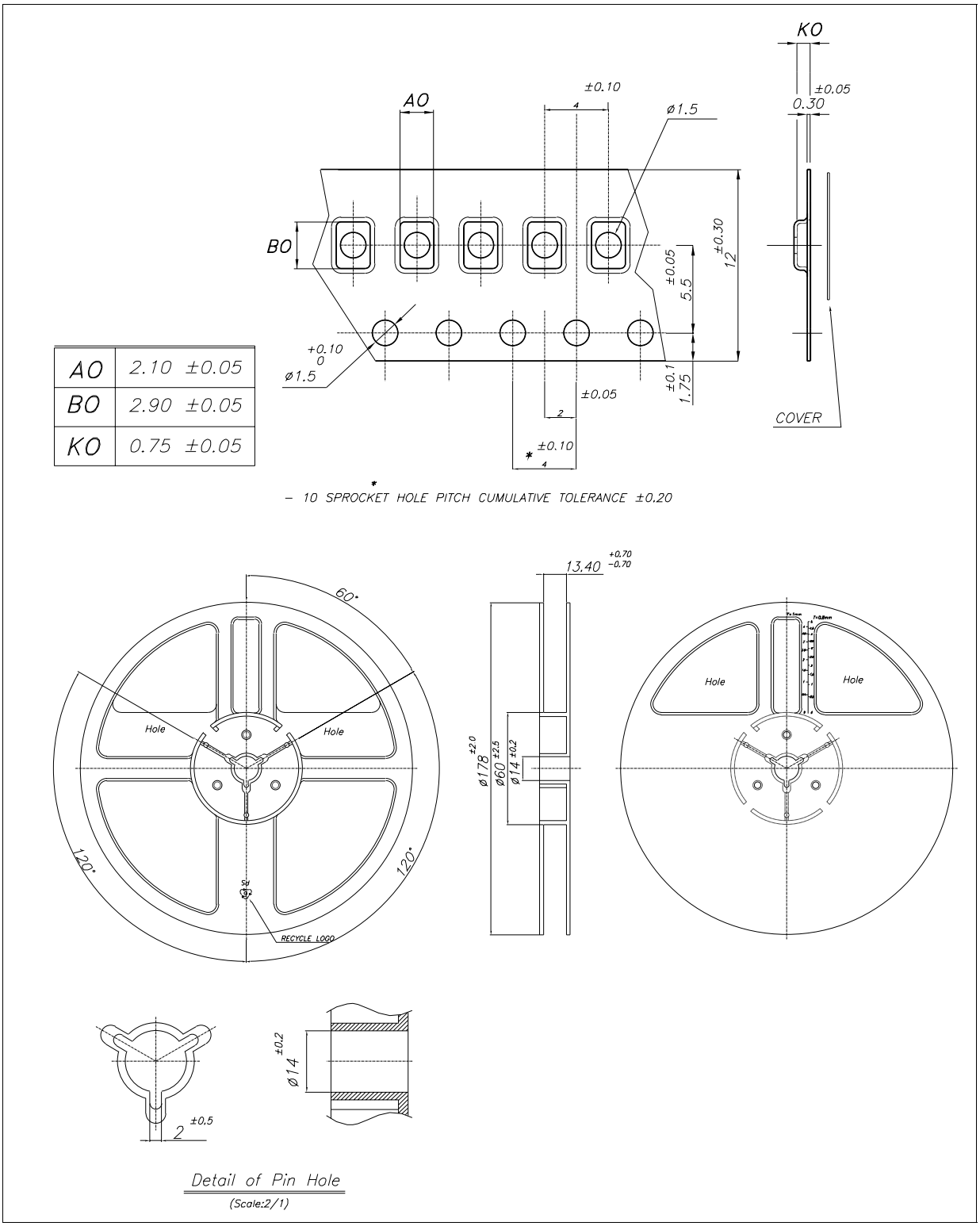


Figure 6. QFN16L (2.6mmx1.8mm) tape & reel



AO	2.10 ±0.05
BO	2.90 ±0.05
KO	0.75 ±0.05

6 Revision history

Table 9. Revision history

Date	Revision	Changes
27-Apr-2007	1	First release
04-May-2007	2	Typo in cover page
05-Jul-2007	3	*Table 5 on page 7* updated

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