AN1317
APPLICATION NOTE

NON ISOLATED POWER SUPPLIES IN BUCK AND INVERTER CONFIGURATION USING VIPer20 DEVICE

A. Bailly - S. Luciano

INTRODUCTION

The VIPer20 is a full integrated switching device. It replaces the conventional PWM driver circuit, its associated high voltage Power MOSFET switch and a full set of other passive components, and provide a high level of performance thanks to its current mode structure and standby operation capability.

1. SCOPE

The VIPer20 is initially designed to be used at the primary side of any off line power supplies in isolated flyback configuration but it is also the right solution for different types of not isolated power supplies applications where low power (1W to 5W), wide input voltage range and low prices are required. In this case, a simple two pins inductor can replace an expensive safety transformer. The basic principle of this type of supplies is to convert a high voltage source to a low voltage one by the only way of the switching frequency and duty cycle management.

The applications like home appliances (microwave oven, washing machine, triac drivers...), industrial applications (motors control,...) do not require galvanic isolation between the mains lines and the low voltage load, especially when one of the low voltage outputs must be connected to one of the mains lines.

All these applications will take benefits from VIPer20 features:

- Full integrated PWM start up current source and high voltage Power MOSFET, allow to build simple, robust, cost effective and compact power supplies.
- Built in overtemperature and overcurrent protection provide a safe control in overload conditions.

This application note gives all the elements to enable the designer to start the development of his own non isolated power supply using the VIPer20. It defines the key components, and highlights the differences between the Buck and the Inverter (also called Buck-Boost) topologies.

2. NOT ISOLATED TOPOLOGIES

2.1 VIPer20 In Buck Topology

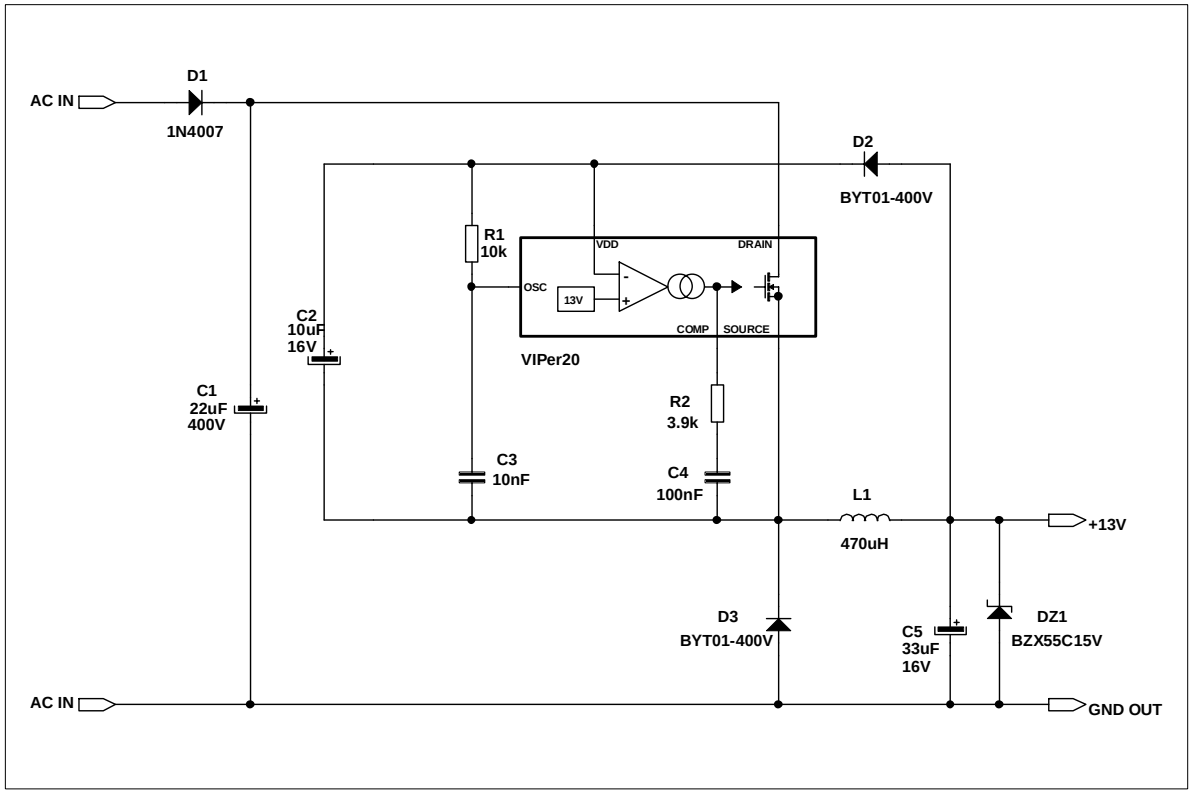
The basic schematic of a VIPer20 in Buck topology delivering 2W typical, with a fixed output voltage, is given fig. 1. The Buck structure is composed here by the on chip Power MOSFET, the inductor L1, the free wheeling diode D3, the output filtering capacitor C5 and the output load itself.

In this topology, the VIPer20 switching duty cycle is very low (a few percent) because of the very high difference between the input and the output voltages. Its value would be at the maximum equal to the voltages ratio, when in continuous mode and even less in discontinuous mode. If the switching frequency is too high, the Power MOSFET conduction time will decrease accordingly, which may result in early burst mode operation if lower than the minimum turn on time of the device. In practice, the chosen

switching frequency will be comprised between 20 kHz and 30 kHz, just above audible values.

During the start up phase, the VIPer20 is in standby mode and its on chip high voltage current source sources a current on the V_{DD} pin until the voltage across the capacitor C2 reaches the V_{DDon} threshold. Then, this current source is turned off and the device starts switching. After a transition phase during which the output voltage grows up, the V_{DD} supply of the VIPer20 is provided by the capacitor C2 and finally, from the positive output through the diode D2 when the output voltage becomes higher than the current V_{DD} value.

Figure 1: 2W typical single output not isolated power supply with Buck topology



In normal operation, the output voltage regulation is achieved by the VIPer20 error amplifier which accurately compares the V_{DD} value to the internal 13V voltage reference. The forward voltage across the diode D2 is here partially compensated by the forward voltage across the diode D3. So, the output voltage and the on chip voltage reference values are equal, except for diode forward voltage differences due to different diodes current: It is generally higher in the free wheeling diode D3, resulting in a slightly lower output voltage.

A typical characteristic of the Buck is that the inductor charge and discharge paths are exclusively done through the output load. It is a slight advantage in normal operation because the energy is transferred to the load during both turn on and turn off cycles, but in very low or no load conditions, it has two drawbacks:

• The charge of the start up tank capacitor C2 is impossible, especially when the input voltage is slowly

increased. If no protection is foreseen, it is possible to apply the input voltage directly on the output, with large overvoltages.

• Once started, overvoltages may also occur at the output, mainly for low input voltage values.

The root cause of the last phenomenon resides in the duty cycle increase at low input voltage, together with a low output load. Fig. 2 shows the drain current shape for two input voltages. The lower is the input voltage, and the higher is the turn on. As a consequence, the turn off phase during which the energy is sent to C2 through D2 is reduced, and the device is increasing its drain current to maintain a correct regulated voltage on the V_{DD} pin at 13 V. If the load is not able to absorb the corresponding current during the on phase, overvoltage is resulting on the output.

Figure 2: Drain current for two input voltages in low load conditions

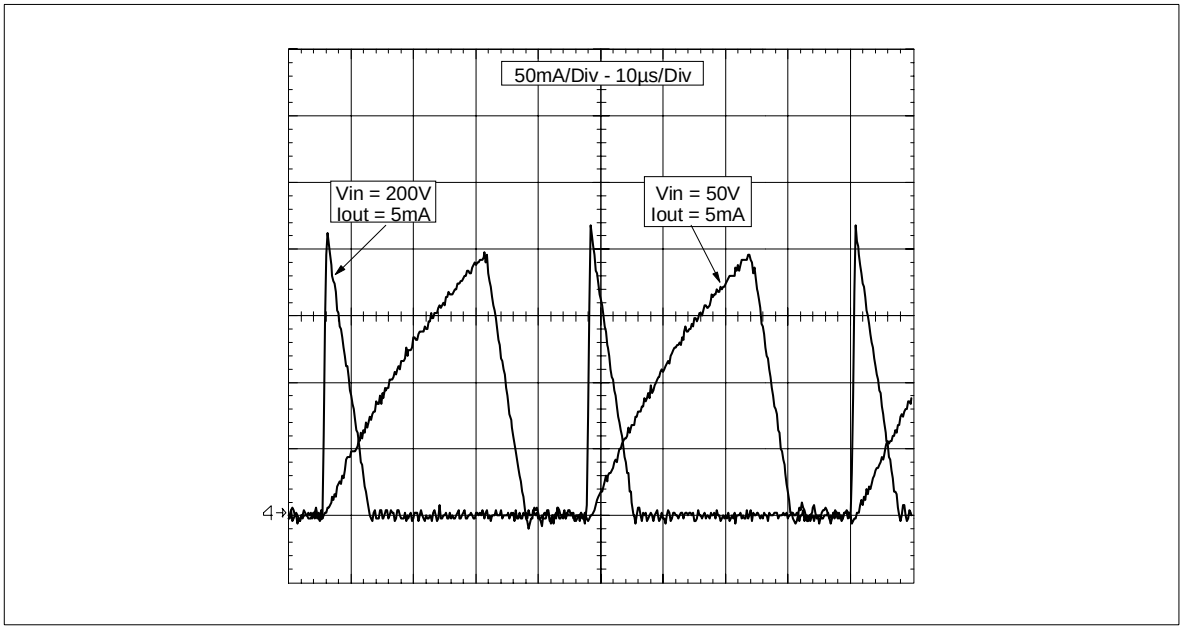
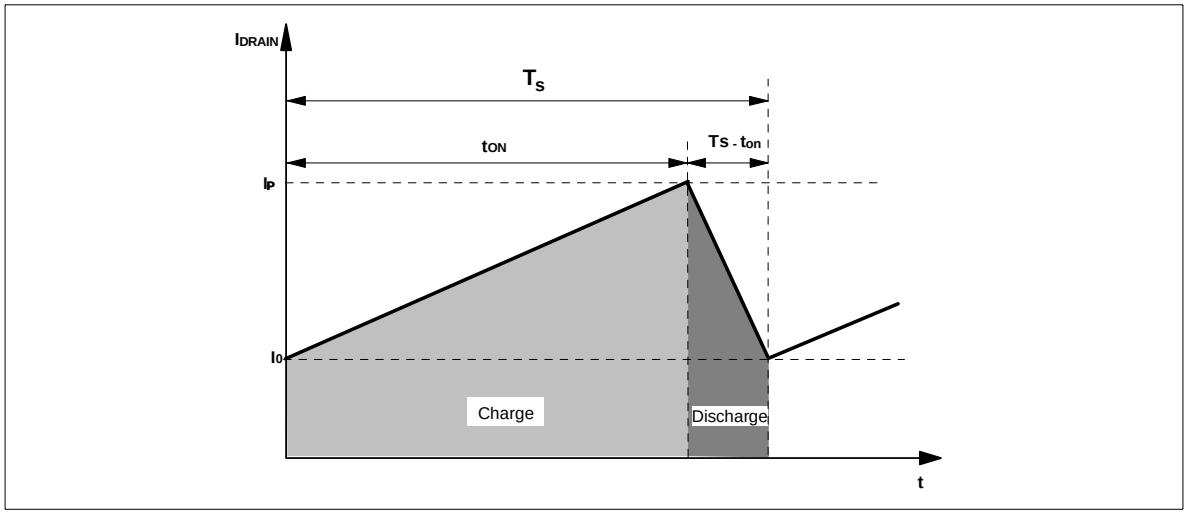


Fig. 3 shows an extreme case where the phenomenon reaches its critical phase, with a continuous mode of operation. The following computation demonstrates the risk of overvoltage and/or overcurrent on the output.

Figure 3: Switching cycle in continuous mode in low input voltage condition



The average currents consumed by the VIPer20 I_{DD} and the output current I_{out} can be expressed as:

$$I_{DD} = \frac{1}{2 \cdot T_s} \cdot (I_P + I_0) \cdot (T_S - t_{on})$$

and

$$I_{out} = \frac{1}{2 \cdot T_s} \cdot (I_p + I_0) \cdot t_{on}$$

By using these two equations:

$$I_{out} = t_{on} \cdot \frac{I_{DD}}{T_s - t_{on}}$$

Finally, by introducing the duty cycle expression in continuous mode: $d = \frac{t_{on}}{T_s} = \frac{V_{in}}{V_{out}}$

The minimum output current mandatory to keep the output voltage under control is given by:

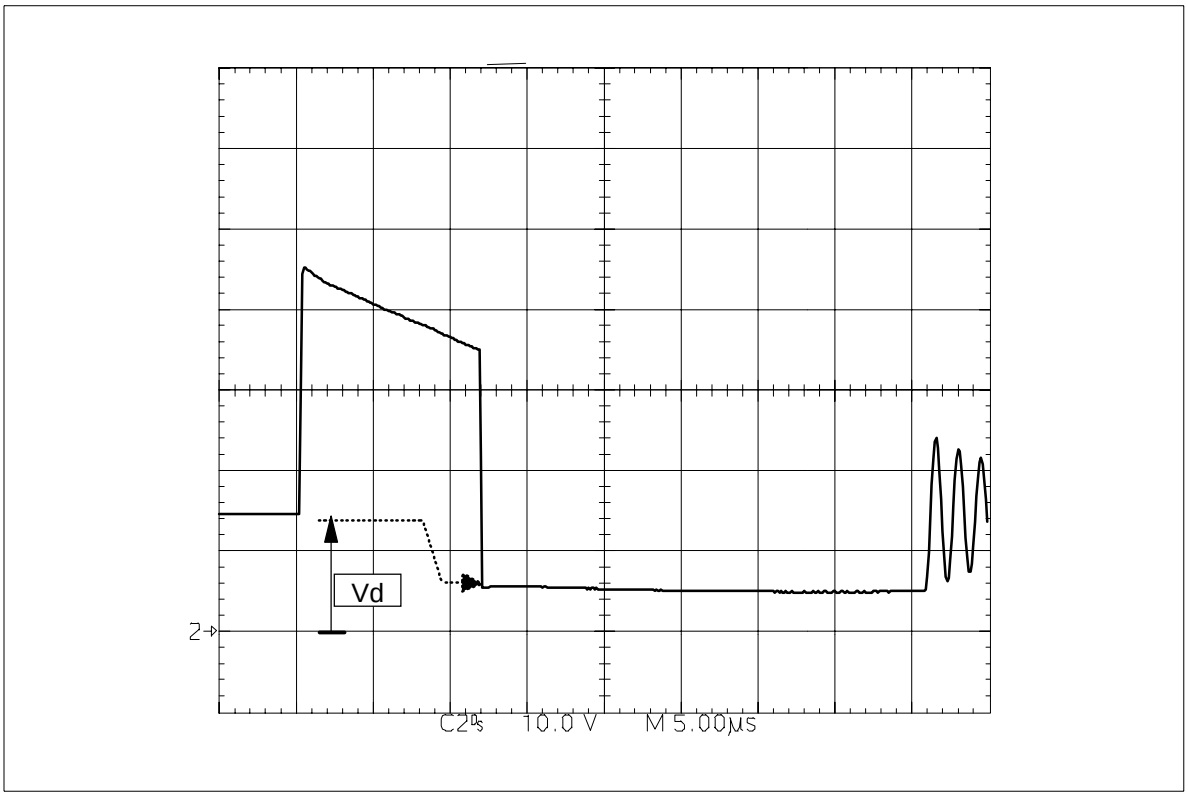
$$I_{out} = I_{DD} \cdot \frac{V_{out}}{V_{in} - V_{out}}$$

To prevent these disturbances resulting in possible output overvoltage or incorrect start up, a 15V zener diode DZ1 is added. It allows a current to flow at the output, insuring a correct start up and clamps any possible overvoltage. Nevertheless, as shown in the above last formula, the current flowing in this zener can be very high when the input voltage approaches the output one. Section 5 describes a schematic modification to overcome this issue.

Fig. 4 presents the operation of the free wheeling diode in this condition: Actually it is always blocked, as the voltage on the cathode never becomes negative. Also on this figure, it can be observed that the voltage drop V_d across D3 is about 5V while the output voltage is at 15V. It means that V_{DD} is about 10V

because the input voltage is too low to insure a proper operation of the converter, which is about to shut down.

Figure 4: Buck non isolated - VIPer20 source voltage with V_{IN} = 47 V, I_{OUT}=5 mA. DZ1 conducting



2.2 VIPer20 In Inverter Topology

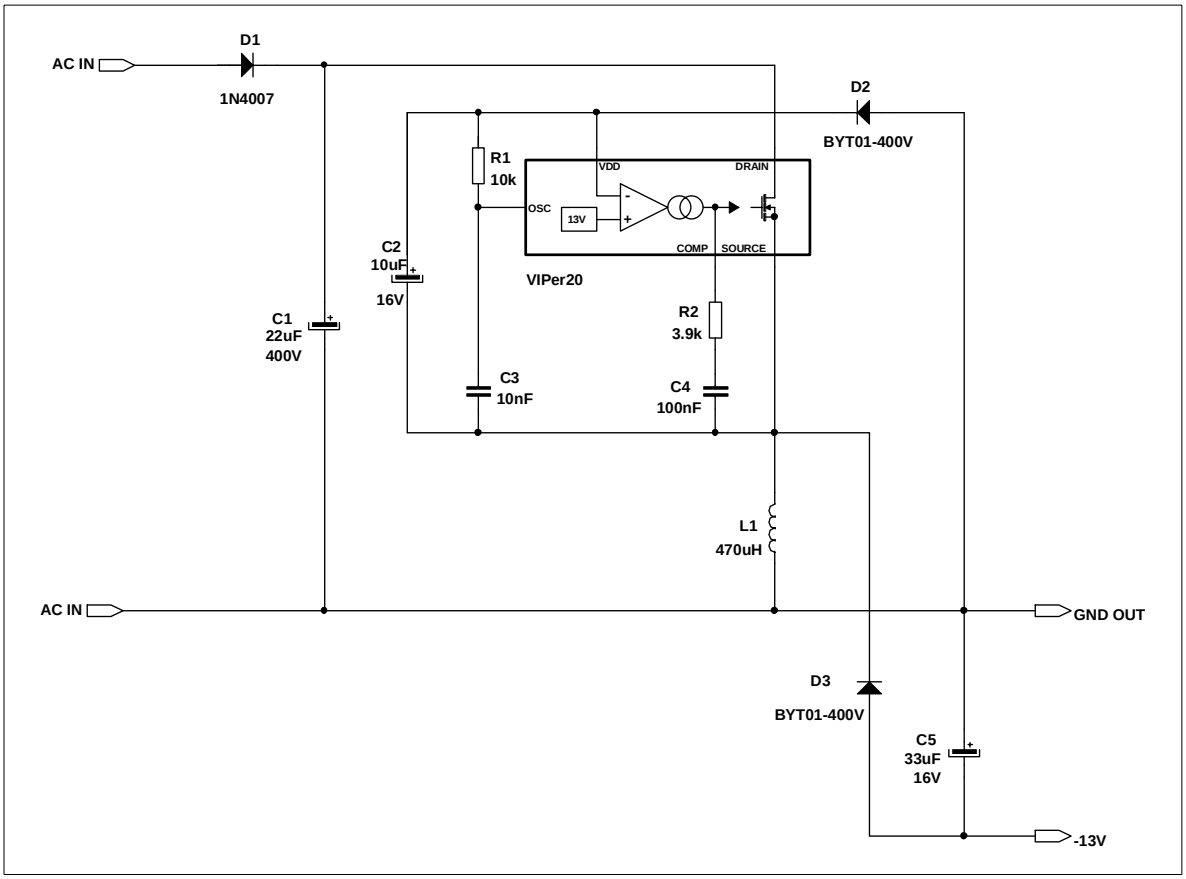
The inverter schematic is derived from the Buck one of fig. 1 by just swapping the inductor L1 and the free wheeling diode D3. The resulting schematic is given fig. 5. There is a major difference with the Buck from a functional point of view : when the on chip Power MOSFET is turned on, the inductor L1 does not charge anymore through the load but between the mains lines. The output load now gets all its energy during the MOSFET off state, through the inductor L1 and the free wheeling diode D3.

As a consequence, the zener diode DZ1 is no more necessary because of two reasons:

- The charge of the tank capacitor C2, now independent from the load, is always possible.
- Both VIPer20 supply (V_{DD} pin) and output load are receiving energy form the inductor L1 at the same period of time. So, there is no possible difference between the V_{DD} voltage and the output one, which is always under control.

Compared to the Buck, the current flowing through the load is in the opposite direction so that the output voltage becomes now negative. As a consequence, the output capacitor C5 polarity must be swapped and the anode of the diode D2, supplying the VIPer20, must now be connected to the ground lead GND OUT to insure a correct positive supply to the V_{DD} pin.

Figure 5: 2W typical single output not isolated power supply with Inverter topology



3. DESIGN METHODOLOGY

The schematic of either fig. 1 or fig. 5 can be separated into six blocks:

- The oscillator network composed by R1 and C3.
- The Buck or inverter structure, which is composed by the on chip MOSFET, the inductor L1, the free wheeling diode D3 and the output filtering capacitor C5.
- The VIPer20 supply circuit, composed by D2 and C2.
- The front rectifier and filter.
- The error amplifier compensation network composed by R2 and C4.

All these functions will be detailed in the next paragraphs.

3.1 Switching Frequency And Duty Cycle

Sections 1 and 2 showed that the input voltage transformation is entirely managed by the VIPer20 which controls the switching duty cycle. Whatever the topology is, the goal is to look for the widest load regulation range, trying to reach the VIPer20 minimum turn on time (T_{ONmin} = 500 ns typ.) for the lowest output load. For maximum load, although the VIPer20 is perfectly compatible from the continuous mode, it must be avoided because the power dissipation in the free wheeling diode D3 would be too high and the inductor size and price would increase. For all the above reasons, these topologies are operated at

low switching frequency and always in discontinuous mode.

As an example, to get a 13V output voltage with a 265 Vrms input voltage, the maximum duty cycle $d = \frac{V_{out}}{V_{in}}$ would be less than 5%. With a switching frequency of 100 kHz, the maximum conduction time would always be equal or lower than T_{ONmin}, leading to a permanent burst mode operation. In practice the switching frequency is chosen just above the audio ones, in the 20 kHz to 30 kHz range and the VIPer20 will work in discontinuous mode with a duty cycle of about 2% to 3% at high line and about 6% to 10% at low line.

From the VIPer20 datasheet, the switching frequency is given here below:

$$F_s = \frac{2.3}{R_1 \cdot C_3} \cdot \left(1 - \frac{550}{R_1 - 150}\right)$$

On the schematic of fig. 1 and fig. 5, R1=10kΩ and C3=10nF have been chosen to get a switching frequency near by 20 kHz (21.7 kHz typical).

3.2 Inductor

In normal operation, for both topologies, the switching cycle consists of two phases. First, the Power MOSFET is switched on during t_{on}, D3 is blocked, the inductor connected to the high voltage source stores the energy. Second, the Power MOSFET is switched off during t_{dis}, the inductor restores its energy to the load through D3, and to the V_{DD} pin through D2. As described in section 2, the load is supplied during t_{on} and t_{dis} with the Buck topology, and only during t_{dis} with the inverter one. A typical switching cycle is shown on fig. 6.

Knowing the output power, the switching frequency and the maximum VIPer20 peak current, L1 can be computed as follow:

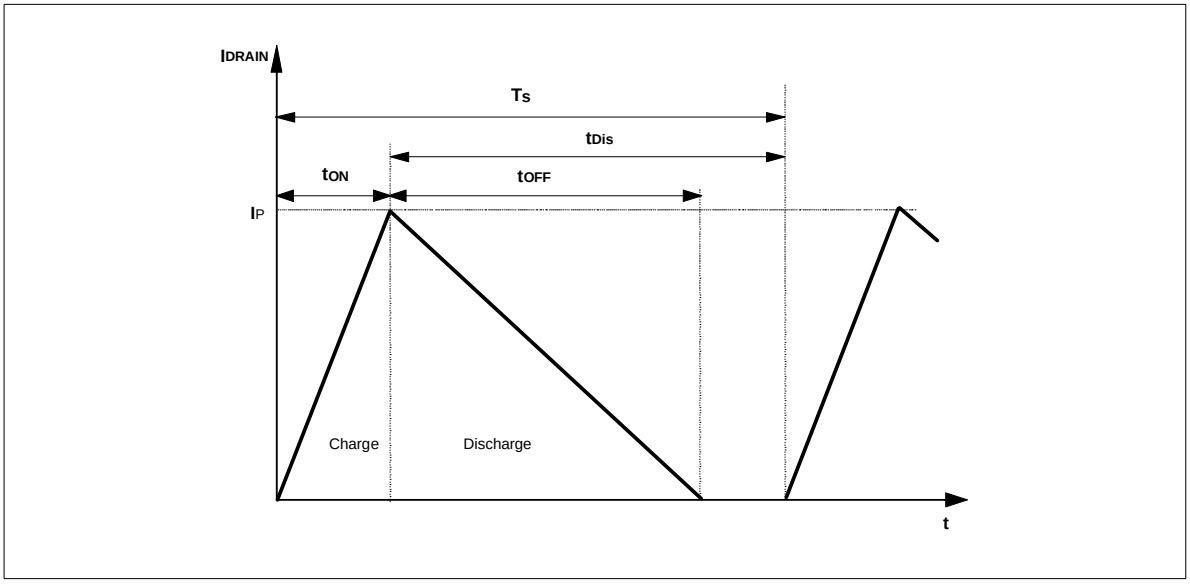
for the Buck:
$$P_{out} = \frac{1}{2} L_1 \cdot I_p^2 \cdot F_s + \frac{1}{2} I_p \cdot V_{out} \cdot d - I_{DD} \cdot V_{out}$$

with $d = t_{on} \cdot F_s$ and $t_{on}(V_{in} - V_{out}) = L_1 \cdot I_p$

$$P_{out} = \frac{1}{2} L_1 \cdot I_p^2 \cdot F_s \cdot \left(1 + \frac{V_{out}}{V_{in} - V_{out}}\right) - I_{DD} \cdot V_{out}$$

$$L_1 = 2 \cdot \frac{P_{out} + I_{DD} \cdot V_{out}}{I_p^2 \cdot F_s \cdot \left(1 + \frac{V_{out}}{V_{in} - V_{out}}\right)}$$

Figure 6: Switching diagram in normal operation (discontinuous mode)



for the Inverter: $P_{out} = \frac{1}{2} L_1 \cdot I^2_p \cdot F_s - I_{DD} \cdot V_{out}$

$$L_1 = 2 \cdot \frac{P_{out} + I_{DD} \cdot V_{out}}{I^2_p \cdot F_s}$$

In practice, with a less than 10% error, the VIPer20 consumption and also the power transferred to the load during the conduction time of the MOSFET for the Buck ($V_{in} \gg V_{out}$) can be neglected. In this case, the calculation becomes the same for both topologies:

$$L_1 \approx 2 \cdot \frac{P_{out}}{I^2_p \cdot F_s}$$

For a 2W maximum output power, with $I_p=I_{Dpeak}$=0.5A min, F_s=20kHz, it gives $L_1 \approx$ 800µH.

The power delivered by these topologies is limited by the minimum VIPer20 current capability and by the fact that continuous mode has to be avoided. The maximum output current is therefore about $\frac{I_{Dlim}}{2}$.

It gives also a maximum inductance value, for a given frequency:

$$L_{1max} \approx \frac{V_{out}}{I_{Dlim} \cdot F_s}$$

On fig. 9 and 11 of section 4, a 2 W typical output power can be obtained with an inductor value of 470 µH (I_{Dlim}=0.67A typical).

3.3 Output Capacitor

The output capacitor C5 is an element linked with the desired output ripple amplitude ΔV_{out}, which depends on the output voltage and on the application to supply.

The worst case occurs for the maximum load, when the VIPer20 delivers its maximum peak current during the longer conduction time. The charge of the capacitor C5 is:

$$Q_5 = \int i \cdot dt = (C_5 \cdot \Delta V_{out})$$

With the hypothesis that the VIPer20 is at the limit of the continuous mode, which is a worst case making easier the calculation of the current in the capacitor:

$$\int i \cdot dt = \frac{1}{2}\left(\frac{T_s}{2} \cdot \frac{I_p}{2}\right) = \frac{1}{8} T_s \cdot I_p$$

$$C_5 = \frac{\frac{1}{8} T_s \cdot I_p}{\Delta V_{out}}$$

Example with ΔV_{out}=100 mVpp, F_s=20 kHz, I_p=I_{Dpeak}=0.5 A min, $C_5 \approx$ 31 µF

The maximum peak current flowing through this capacitor is $\frac{I_p}{2}$ during the charge and $-\frac{I_p}{2}$ during the discharge. To avoid an excessive power dissipation in the capacitor and a high output ripple, the ESR of the output capacitor must be low. Table 1 gives a picture of the ESR impact, with I_p =0.7A typical.

Table 1: Output ripple versus capacitor technology

Capacitor Type	Capacitor Value	ESR at 100KHz	I_R at 100KHz	Output Ripple $V_R = I_p \cdot ESR$
Standard Electrolytic	33 µF / 16V	7 Ω	90 mA	4.9 V
Electrolytic Solid Al	33 µF / 16V	700 mΩ	1460 mA	490 mV
Electrolytic OS-CON	33 µF / 16V	50 mΩ	1580 mA	35 mV
Electrolytic Low Z	270 µF / 16V	120 mΩ	630 mA	84 mV

The above example illustrates that the computed capacitor value has to be tuned according to the application needs, the capacitor technology and its associated cost.

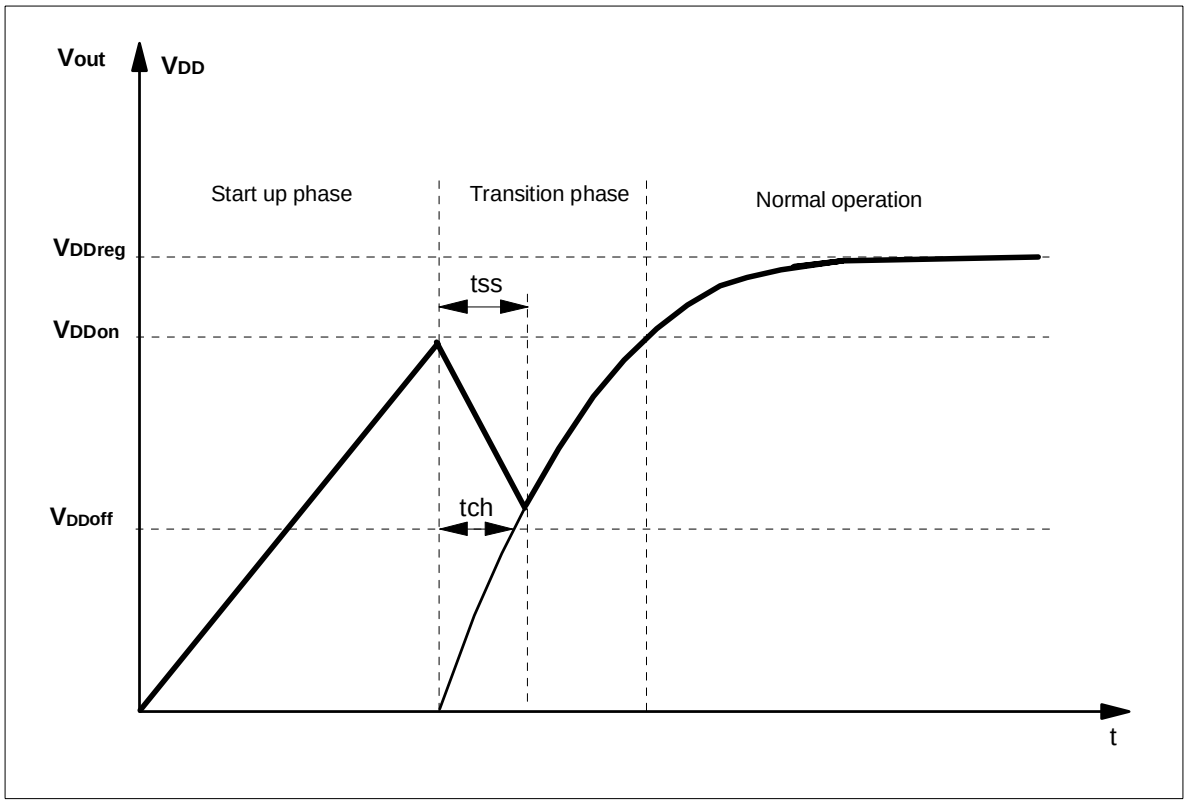
3.4 VIPer20 Supply Circuit

For both topologies, fig. 7 shows the three different mode:

- The start up phase: The on chip high voltage current source is turned on. It sources a current out of the V_{DD} pin in order to charge the tank capacitor C2 until the V_{DDon} threshold is reached. This capacitor then supplies the VIPer20 during the following phase.

- A transition phase: It takes place immediately after the previous one. The current source is turned off and the device starts switching. At the very beginning, the output voltage is lower than V_{DD} one, the diode D2 is blocked, the VIPer20 is still supplied by C2. When the output voltage, increasing cycles after cycles, reaches V_{DDon}, D2 conducts, supplying the VIPer20 from the output. Obviously, the value of C2 must be large enough to maintain the V_{DD} voltage above the V_{DDoff} threshold, before being supplied from the output. If it is not the case, the VIPer20 will loop into endless start up cycles.
- The normal operation: The V_{DD} pin is fully supplied by the low voltage output and regulated at 13 V.

Figure 7: VIPer20 supply phases in Buck or Inverter topologies



The calculation of the V_{DD} tank capacitor C2 can be done as follow:

The minimum start up time t_{ss} must be higher than the output capacitor C5 charging time t_{ch}, which is function of the nominal output voltage and the average output current:

$$t_{ss} > t_{ch} = \frac{C_5 \cdot V_{DDoff}}{I_{outavg}}$$

During the very first start up cycles, C5 is empty, the output voltage is more or less null and the VIPer20 delivers its maximum peak current I_{Dlim} during the Power MOSFET on state. Due to the low output voltage, the inductor L1 discharges very slowly ($t_{dis} \gg T_s$) so that the switching is done in continuous mode. At that time, the average output current is almost equal to I_{Dlim}.

While the output voltage grows up, the discontinuous mode is reached and the average output current becomes the half of the maximum peak current:

$t = 0 \Rightarrow I_{outavg} \approx I_{Dlim}$ and $t = t_{ss} \Rightarrow I_{outavg} \approx \frac{1}{2} I_{Dlim}$

The average output current for $0 \le t \le t_{ss}$ can be approximate as:

$$I_{outavg} \approx \frac{3}{4} I_{Dlim}$$

At the beginning of the start up phase, the capacitor C2 is charged at V_{DDon}, and it can supply the V_{DD} pin down to V_{DDoff}. So, t_{ss} can be expressed as:

$t_{ss} = \frac{I_{DDo} \cdot C_2}{V_{DDhyst}}$, with $V_{DDhyst} = V_{DDon} - V_{DDoff}$

So: $C_2 = \frac{I_{DD0} \cdot t_{ss}}{V_{DDhyst}} > I_{DD0} \frac{(C_5 \cdot V_{out}) / (\frac{3}{4} \cdot I_{Dlim})}{V_{DDhyst}}$

Finally:

$$C_2 > I_{DD0} \frac{4 \cdot C_5 \cdot V_{out}}{3 \cdot I_{Dlim} \cdot V_{DDhyst}}$$

With: V_{out}=13V, I_{DD0}=16mA, I_p=I_{Dlim}=0.5A min, V_{DDhyst}=2.4V, C_5=33µF, C_2>7.6 µF.

3.5 Front Rectifier And Filter

As single wave rectification is chosen because it allows to have the output ground connected to one of the mains lines, as it is required in most of the non isolated applications. As the involved power is low, the input filtering can be achieved without huge bulk capacitor. Any usual rectification diode having a reverse voltage of 800 V will fit the needs. On the schematic of fig. 1 and 5, we used the part number 1N4007.

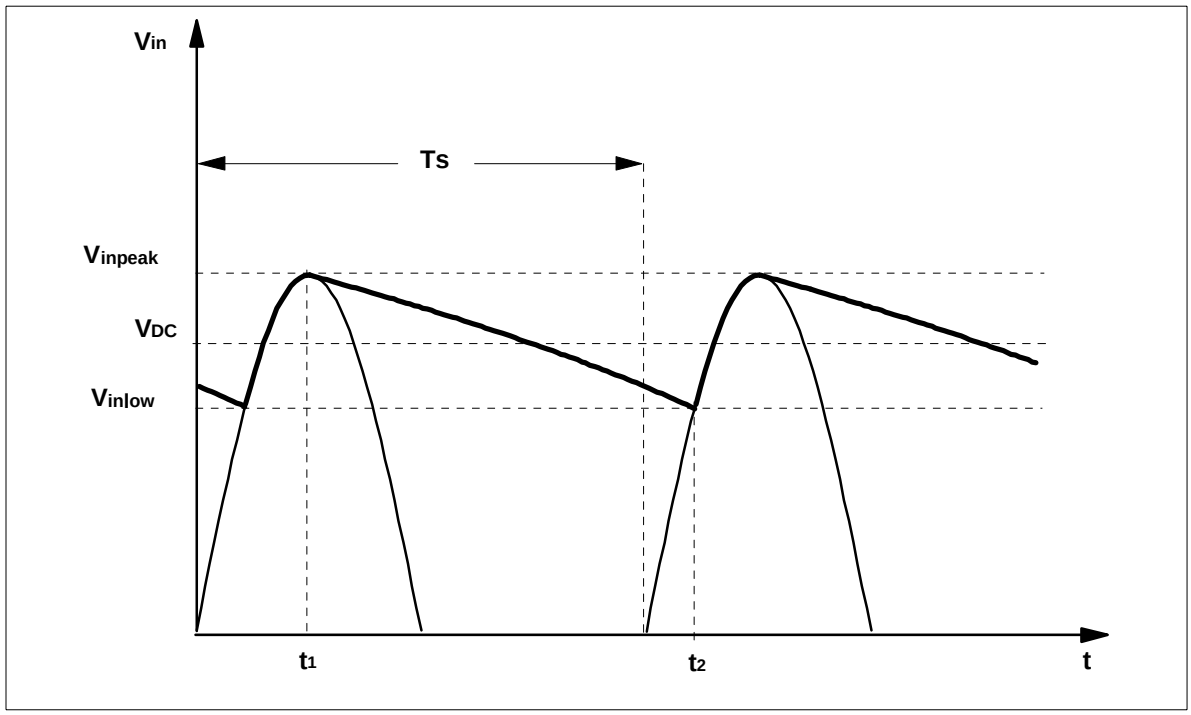
The energy stored in the bulk capacitor during the conduction time of the diode must be equal to the total power dissipated when the diode is blocked.

Referring to fig. 8 and with the efficiency of the converter $\eta = \frac{P_{out}}{P_{in}}$, it comes:

$$\frac{1}{2} C_1 (V^2_{inpeak} - V^2_{inlow}) = (t_2 - t_1) \cdot P_{out} \cdot \frac{1}{\eta}$$

The designer can easily choose V_{inlow} according to the input voltage range and the output ripple he can accept, knowing that a V_{inlow} reasonable value is 70% of V_{inpeak}.

Figure 8: Single wave filtering



t_2 and C_1 can now be extracted as follow:

$$V_{inlow} = V_{inpeak} \cdot \sin\left(2\pi\frac{t_2}{T_s}\right) \Rightarrow t_2 = \frac{T_s}{2\pi} \cdot \arcsin\frac{V_{inlow}}{V_{inpeak}} + T_s$$

$$C_1 = 2 \cdot \frac{(t_2 - t_1) \cdot P_{out} \cdot \frac{1}{\eta}}{(V^2_{inpeak} - V^2_{low})}, \text{ with } \quad t_1 = \frac{T_s}{4}$$

A wide range input voltage design, fitting both American and European standards, is considered: The minimum AC voltage is 85 Vrms, so V_{inpeak}=120V, 60 Hz. The designer needs a 2 W maximum output power and he chooses V_{inlow}=80% of V_{inpeak}. Knowing that the typical efficiency η for this type of converter is about 70%, he gets C_1=19.4µF. He will retain 22 µF which is the closest higher normalized value, with a voltage of 400 V to cover the whole range.

3.6 Compensation Network

The R2 and C4 network connected on the COMP pin of the VIPer20 insures a correct stability of the converter. Note that both Buck and inverter topologies are working in discontinuous, and have a very similar dynamic behavior. So, the values indicated on the schematics are convenient for both topologies and in all load conditions.

4. MEASUREMENT RESULTS

The following graphs show typical results using the schematics of fig. 1 and fig. 5. Unless specified, the measurements are done at ambient temperature.

4.1 Buck And Inverter Output Characteristics

Figure 9: Typical output characteristic of the Buck topology

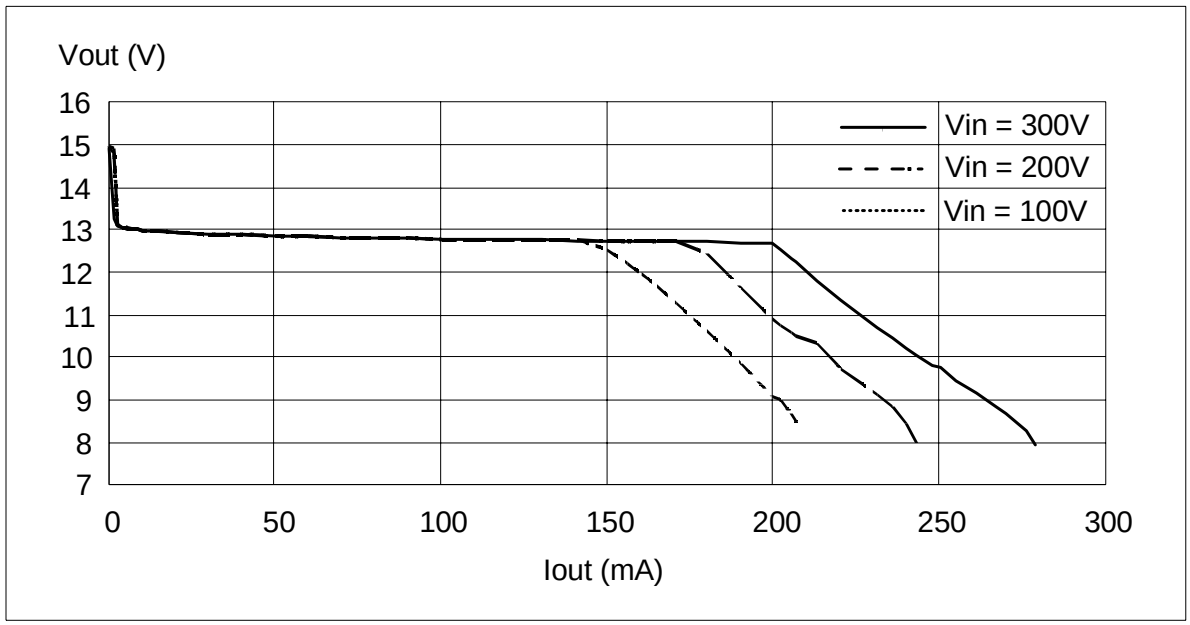


Figure 10: Buck non isolated - Output voltage at low load and low input voltage

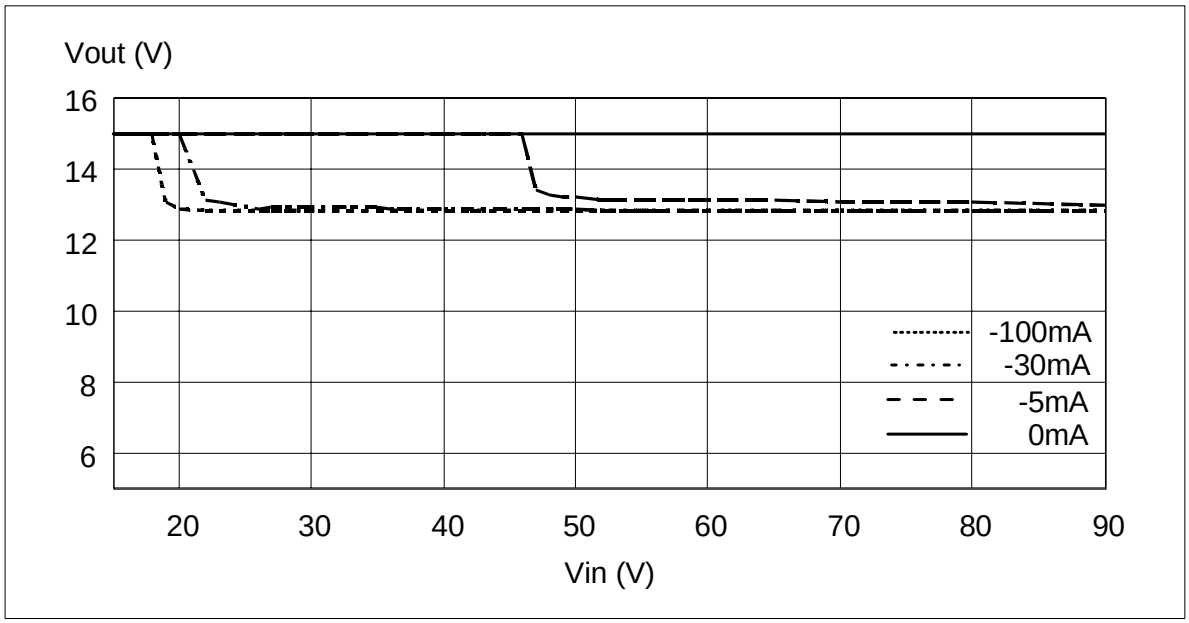


Fig. 10 illustrates the Buck behavior in low load and low input voltage conditions, as described in section 2.1. The output voltage is clamped to 15V by the zener diode.

At the opposite, as shown in fig. 11 and fig. 12, the output voltage regulation of the Inverter is much better whatever are the load and the input voltage.

Figure 11: Typical output characteristic of the fig. 5 Inverter schematic

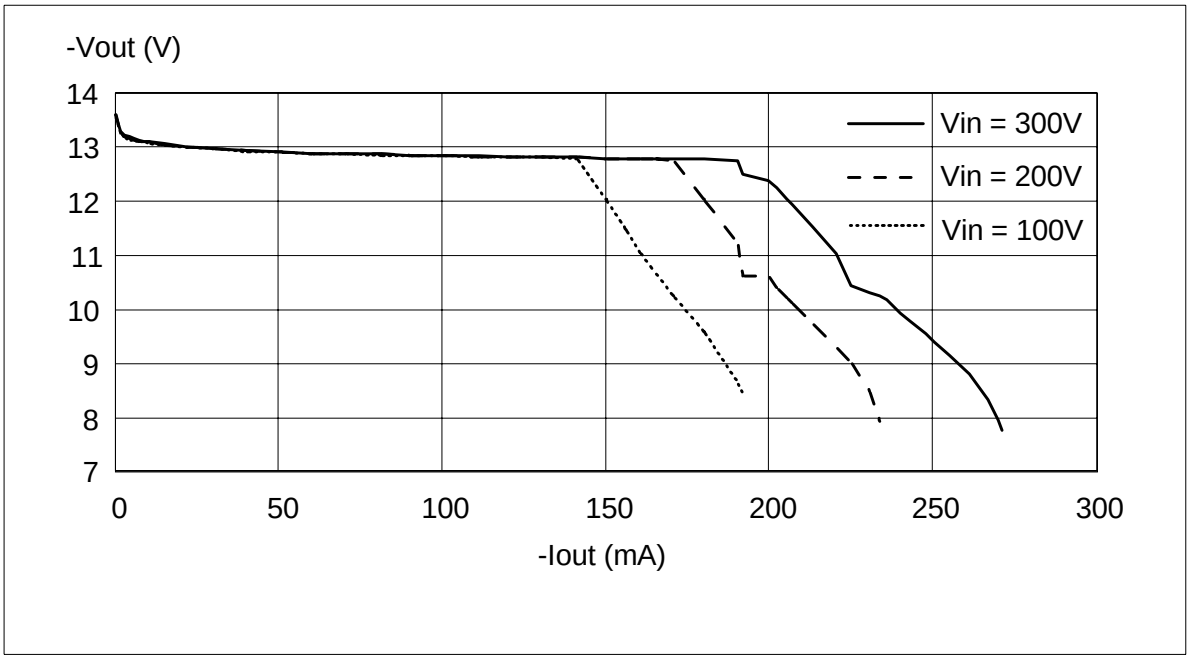
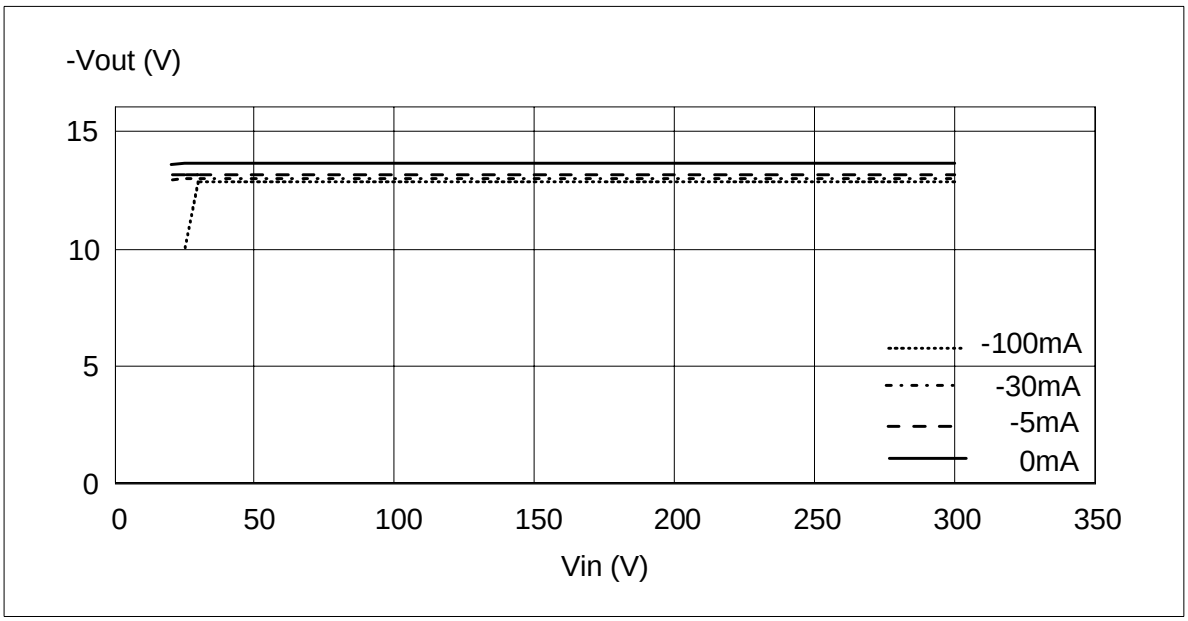


Figure 12: Inverter non isolated - Output voltage versus load and input voltage



4.2 Buck And Inverter Power Measurements

Figure 13: Buck non isolated - Input power versus output power

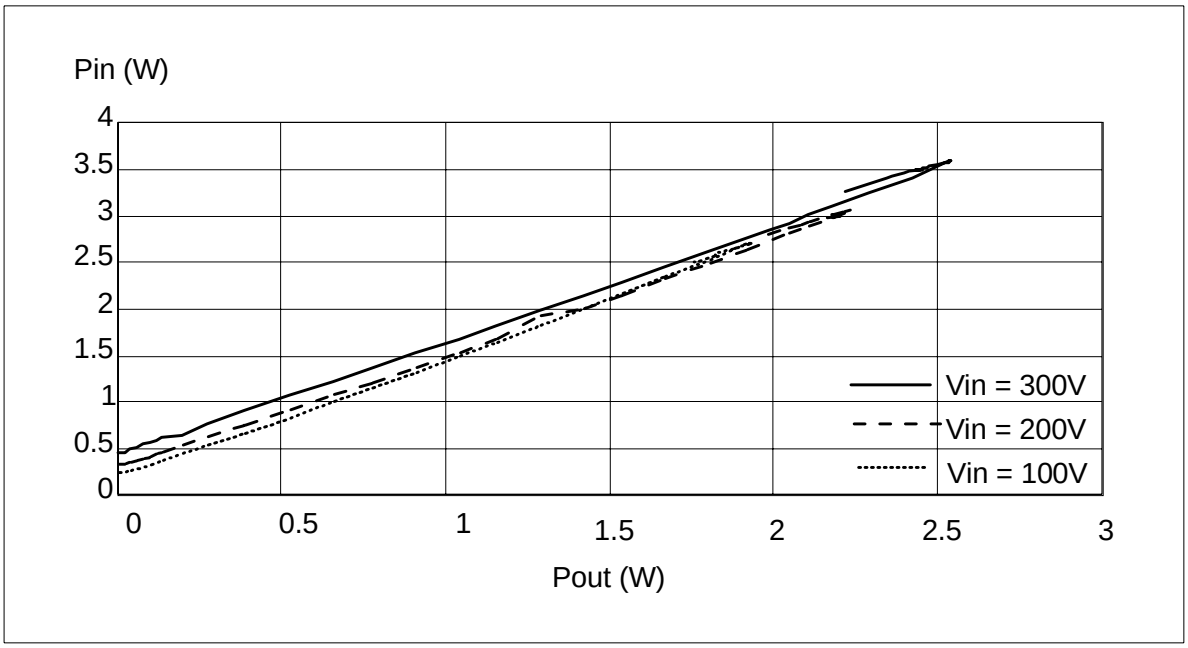


Figure 14: Inverter non isolated - Input power versus output power

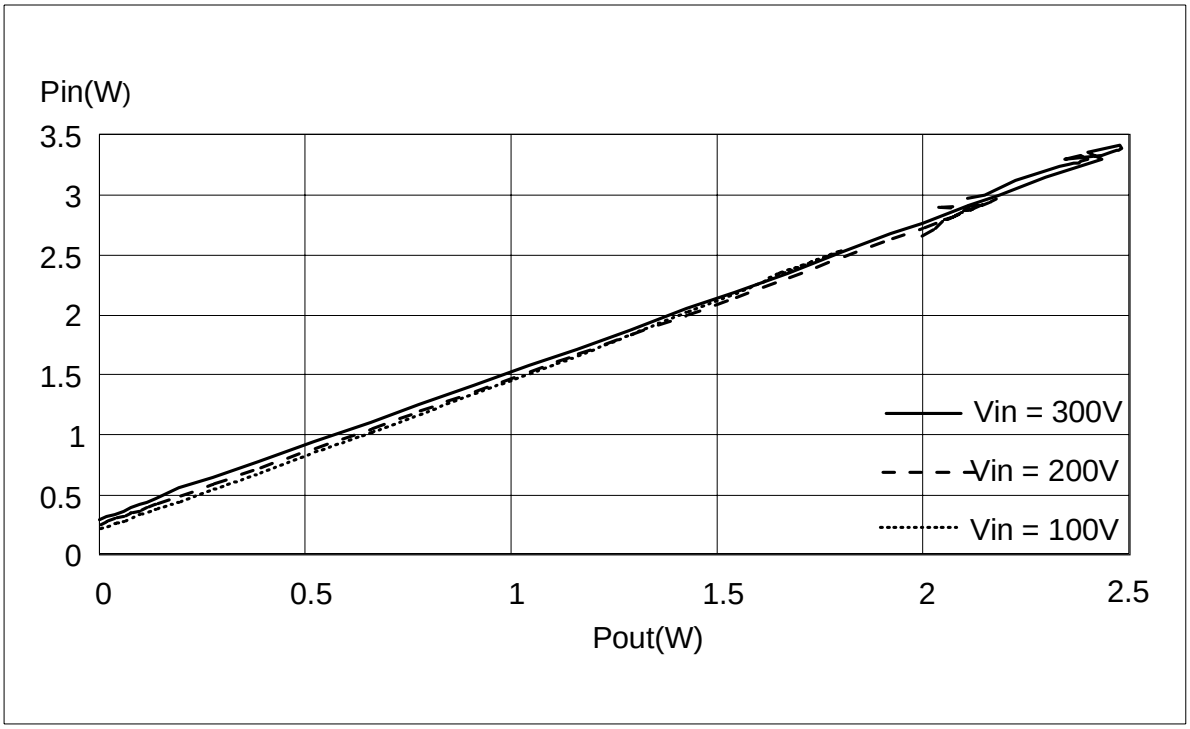


Figure 15: Typical efficiency of a Buck non isolated

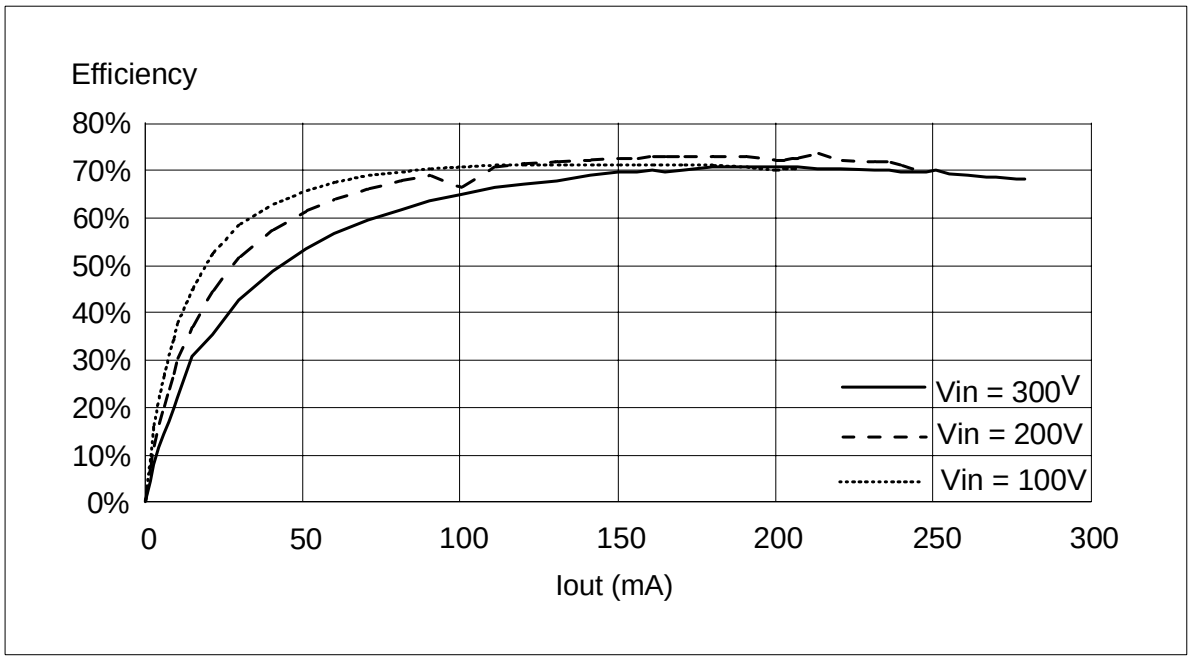
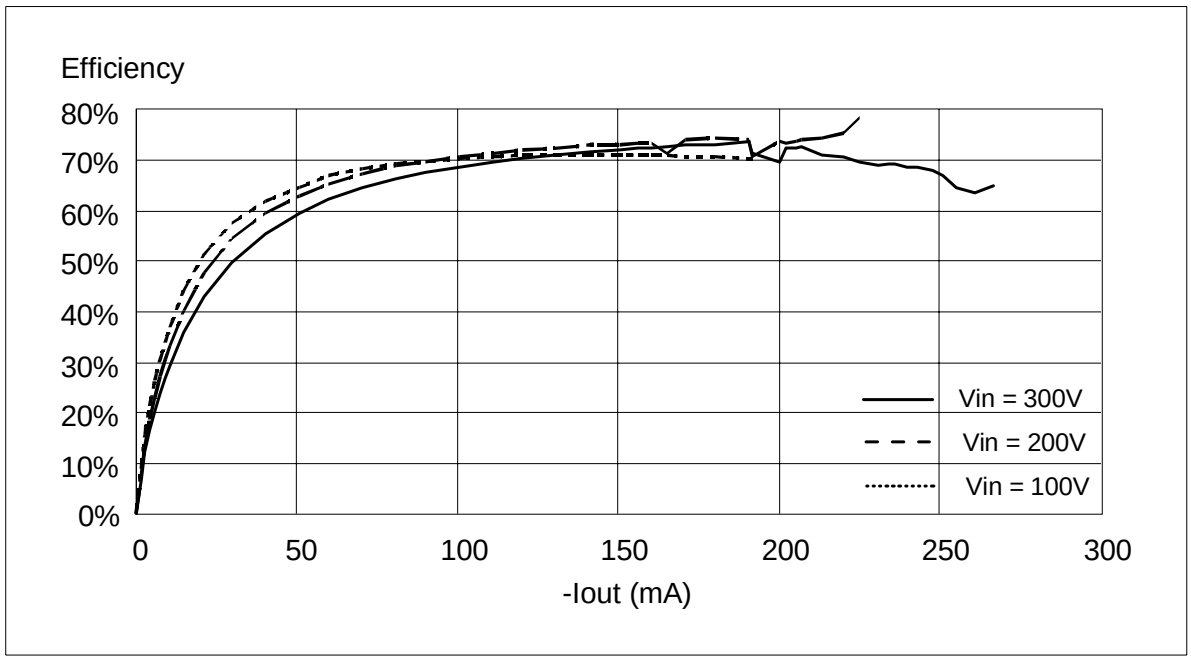


Figure 16: Typical efficiency of an non isolated inverter

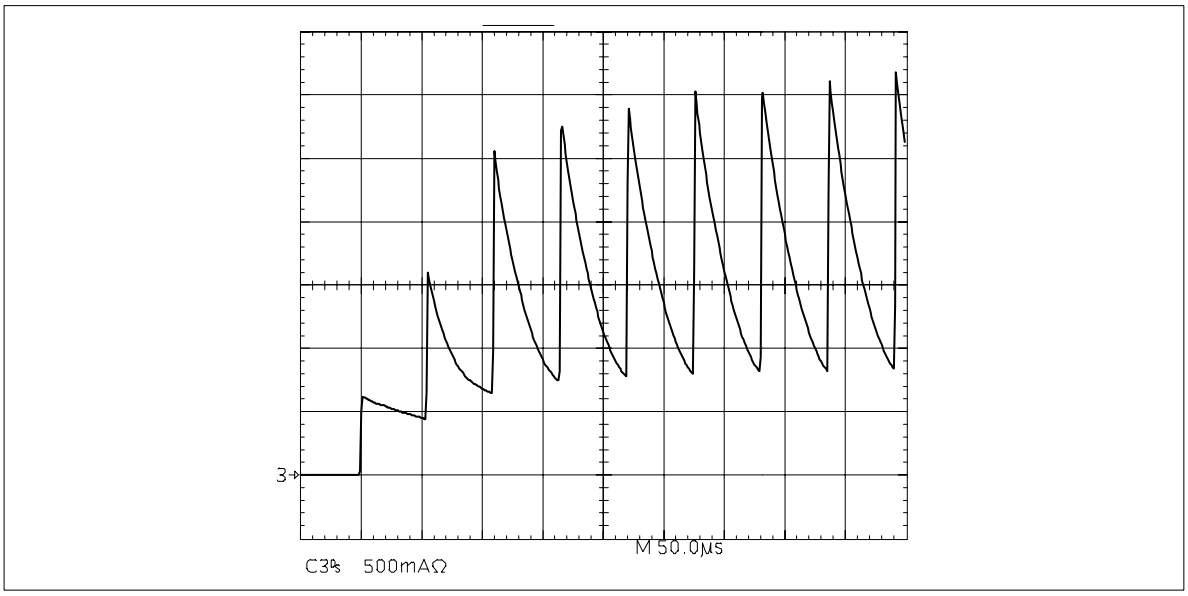


4.3 Short Circuit

Fig. 17 shows the inductor current when submitted to a short circuit on the output. It can be seen that this current exceeds the current limitation of the VIPer20 (It is about 3 A for a limitation of 0.67 A for the

device). This situation is due to the fact that the minimum turn on of the device is not sufficiently short to keep the drain current under control, especially because the inductor is saturated.

Figure 17: Buck non isolated - Inductor current in short circuit condition at V_{in} = 400 V



Nevertheless, the device is protected against such events and can be connected directly across the front bulk capacitor charged at 400 V without any problem. This corresponds to the worst case of a saturated transformer, which is never reached practically. Would it happen, the resulting power dissipation would be limited by the thermal shutdown of the device.

Figure 18: Buck non isolated - Short circuit output current at V_{in} = 400 V

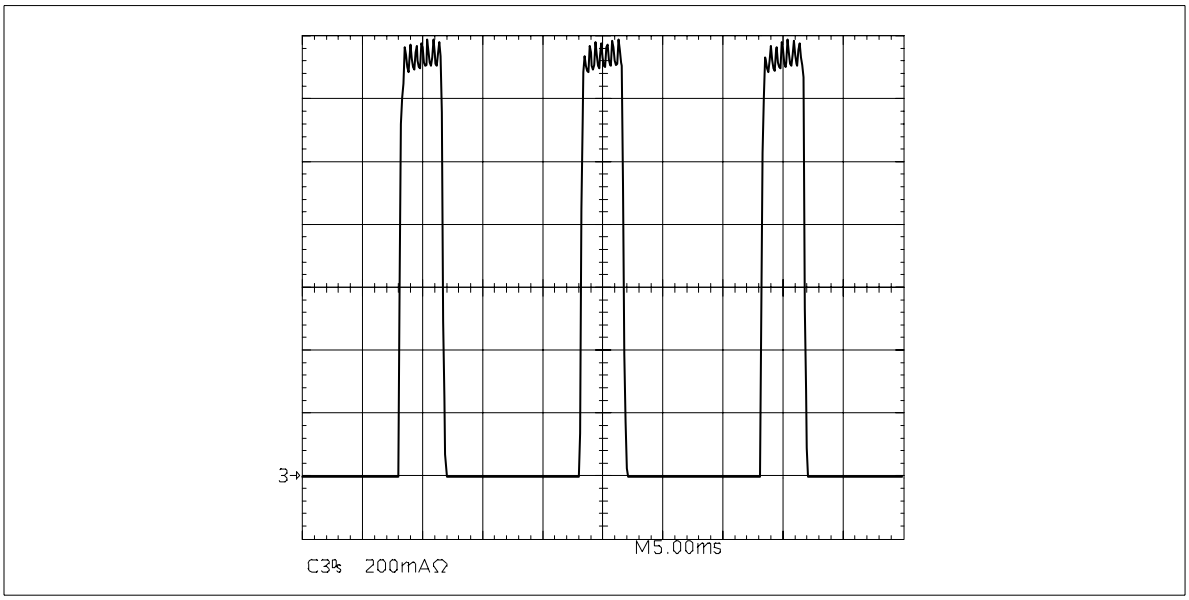


Fig. 18 represents the output short circuit current. Its duty cycle is about 27% for a peak value of 1.4 A. This results in an average current of 0.4 A which is perfectly compatible with the type of diodes generally used for rectifying the output. Actually, these types of converter can withstand the short circuit condition indefinitely. The temperature elevation of the components is quite moderate.

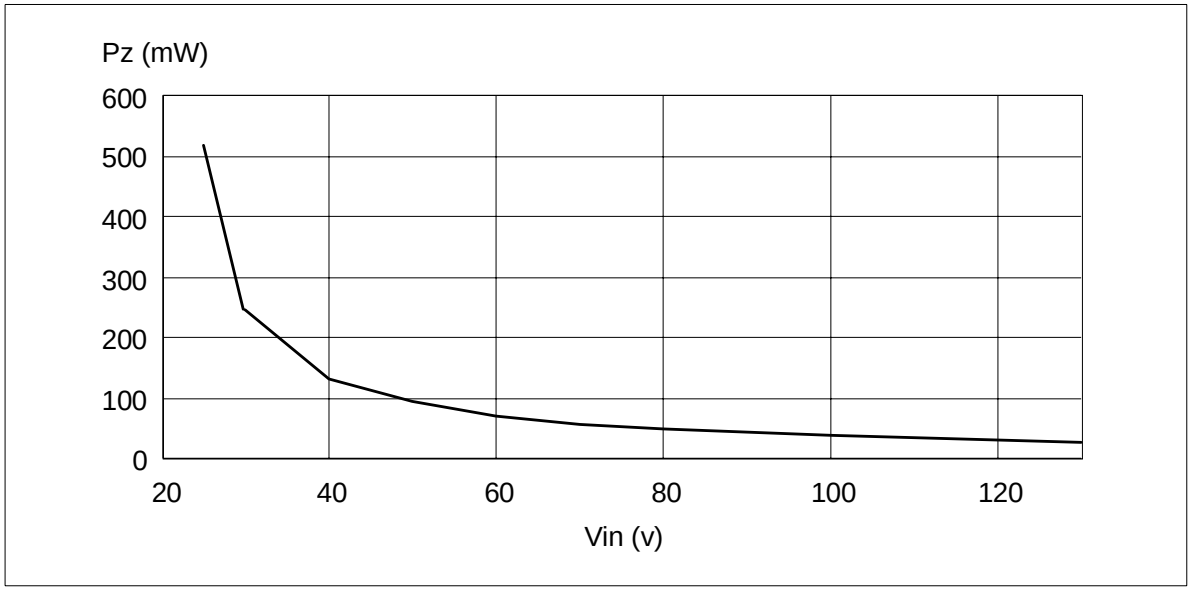
5. SCHEMATICS IMPROVEMENTS AND VARIANTS

5.1 Non Isolated Buck With Output Overvoltage Protection

The inherent inconvenient of the Buck, already described in paragraph 2.1 and 4.1, is the output voltage increase, in low load and low input voltage conditions.

On the initial schematic of fig. 1, the zener diode properly clamps the output voltage surges when a minimum load is guaranteed and if the input voltage rise and fall times between 20V to 50V typical, is short enough. Otherwise, the output voltage may rise such values that the power dissipation in DZ1 becomes very high, as shown on fig. 19.

Figure 19: Buck non isolated - DZ1 power dissipation in short circuit



The solution implemented on the schematic of fig. 20, allows to drastically improve the output voltage control, by reducing the nominal switching frequency if the input voltage decreases below a threshold.

This frequency shifter consists of a diode D4 connected on the OSC pin of the VIPer20, and receiving a fraction of the input voltage through R3 and R4. When the input voltage becomes low, a current is sunk through D4 from the middle point of the oscillator network R1-C3, thus increasing the charging time of C3 and decreasing the switching frequency. The resistances R3 and R4 are chosen in such a way that the frequency begins to decrease at 100 Vdc of input bulk voltage, and stops completely the oscillator at 30 Vdc. Fig. 21 and 22 illustrates this behavior for two input voltages, and the final results is shown on fig. 23: Overvoltages still occur at low input voltage or at low output load conditions, but with a reasonable amount of power dissipated in the clamping zener diode.

Figure 20: Buck non isolated with switching frequency shifter

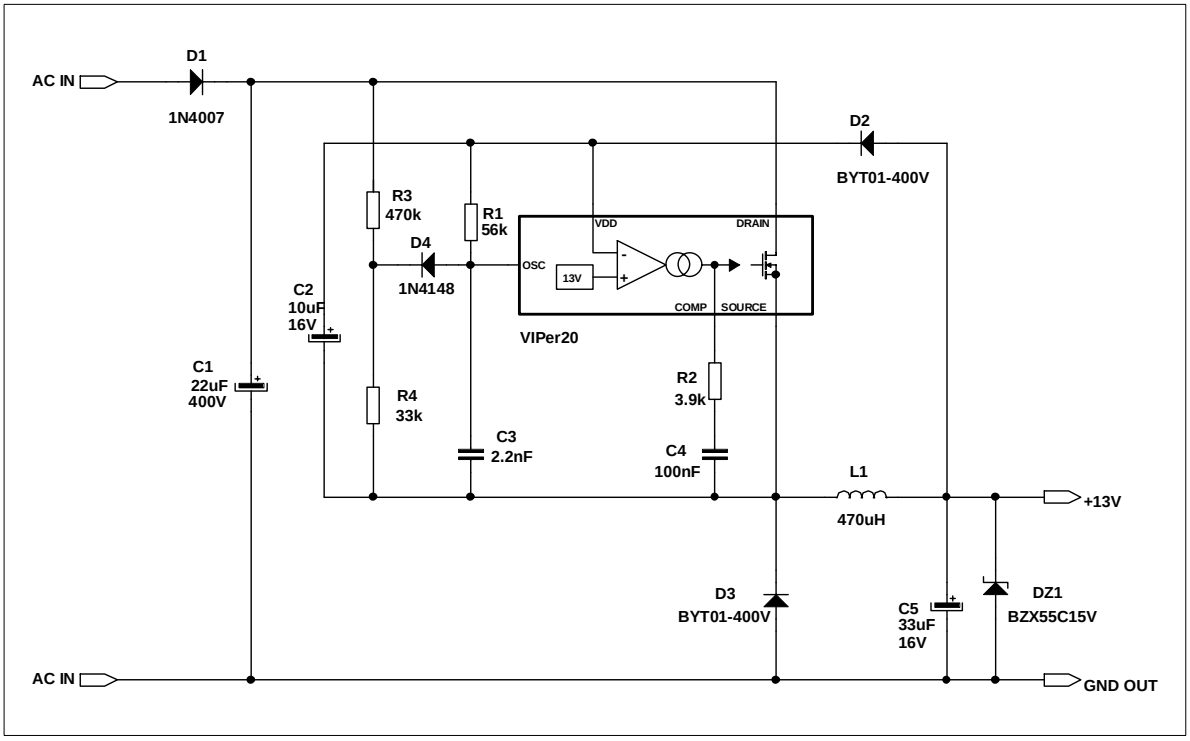


Figure 21: Nominal oscillator frequency at V_{in} = 140V

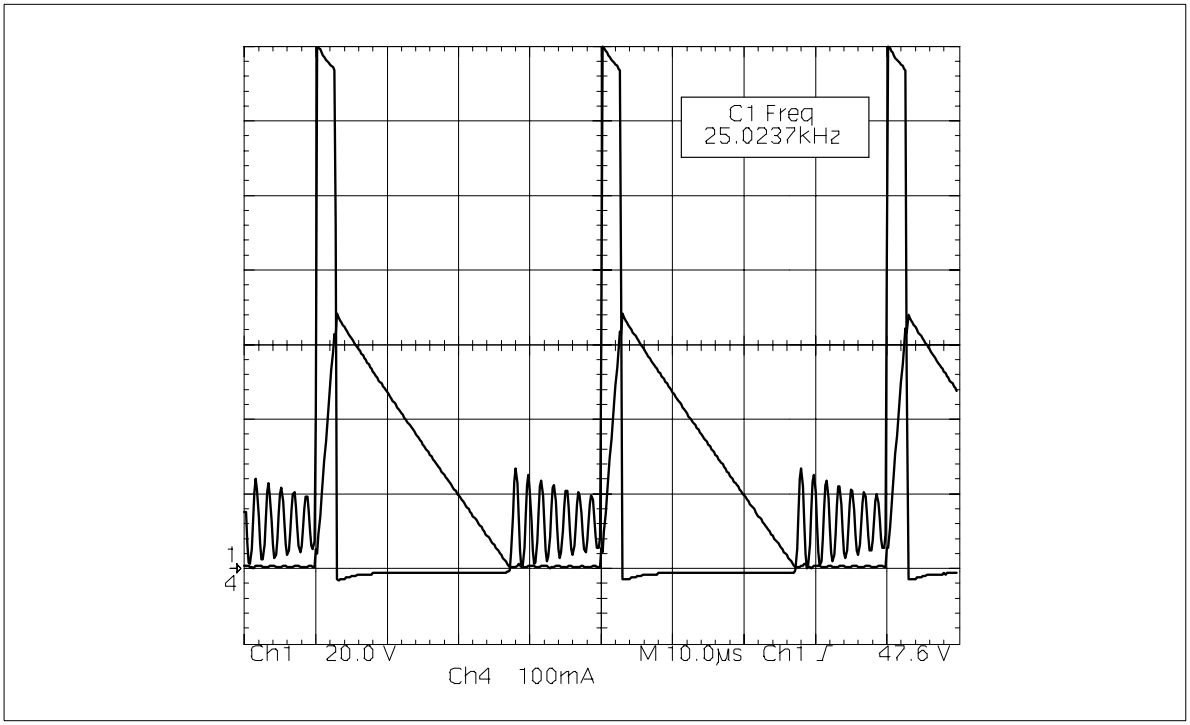


Figure 22: Shifted oscillator frequency at V_{in}=70V

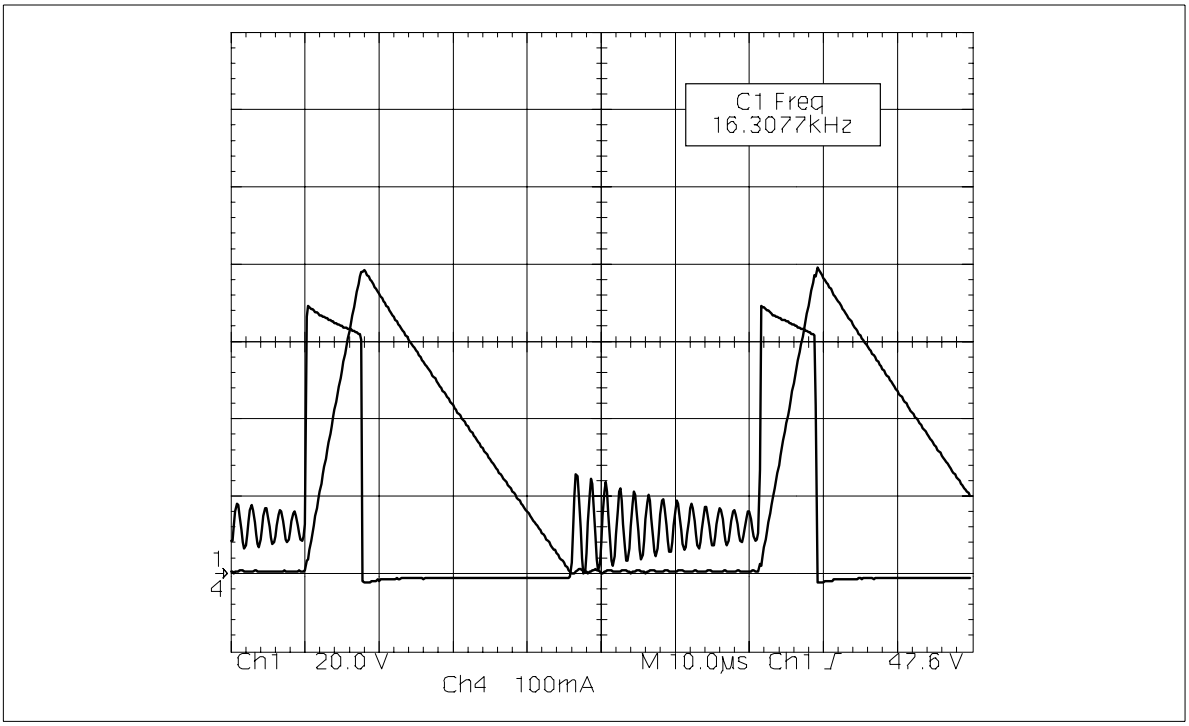
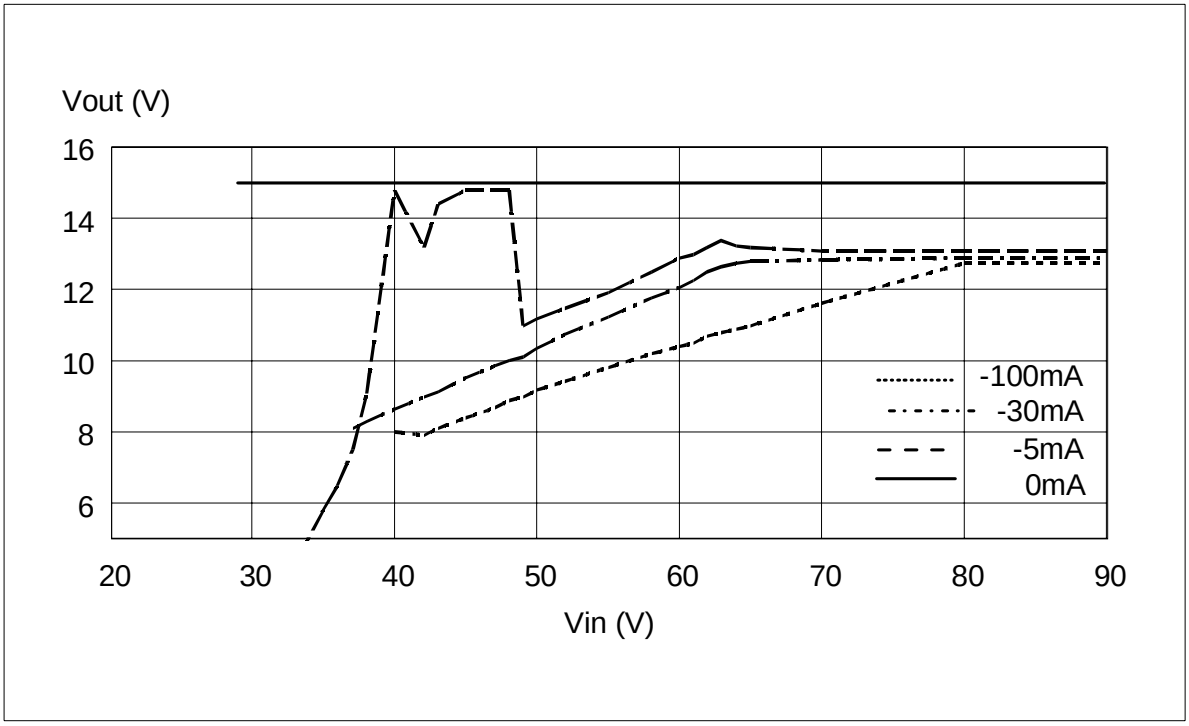


Figure 23: Buck non isolated - Output voltage response with frequency shifter



5.2 Adjustable Output Voltage Structures

On the schematics of fig. 1 and 5, the output voltage is fixed and equal to the reference voltage of the VIPer20, that is to say 13 V. When different voltages are needed, it is possible to modify these basic structures to get other values.

Fig. 24 presents a +23V output non isolated Buck converter with a zener diode DZ2 in series with the V_{DD} pin which imposes the output voltage to be 10 V higher than the reference of the VIPer20. As a results, the output voltage will be regulated at +23 V.

The resistor R1, optionally added here on the line input, is an example of an inrush limiter and filter.

When lower output voltages are specified, an another configuration can be used, as shown on fig. 25. An inductor with an intermediate tap is used in order to deliver a -5 V. This inductor can be of the same type than an inexpensive drum vertically mounted on a PCB, except that three pins are provided instead of two for a standard inductor.

Figure 24: Buck non isolated - Output voltage increased

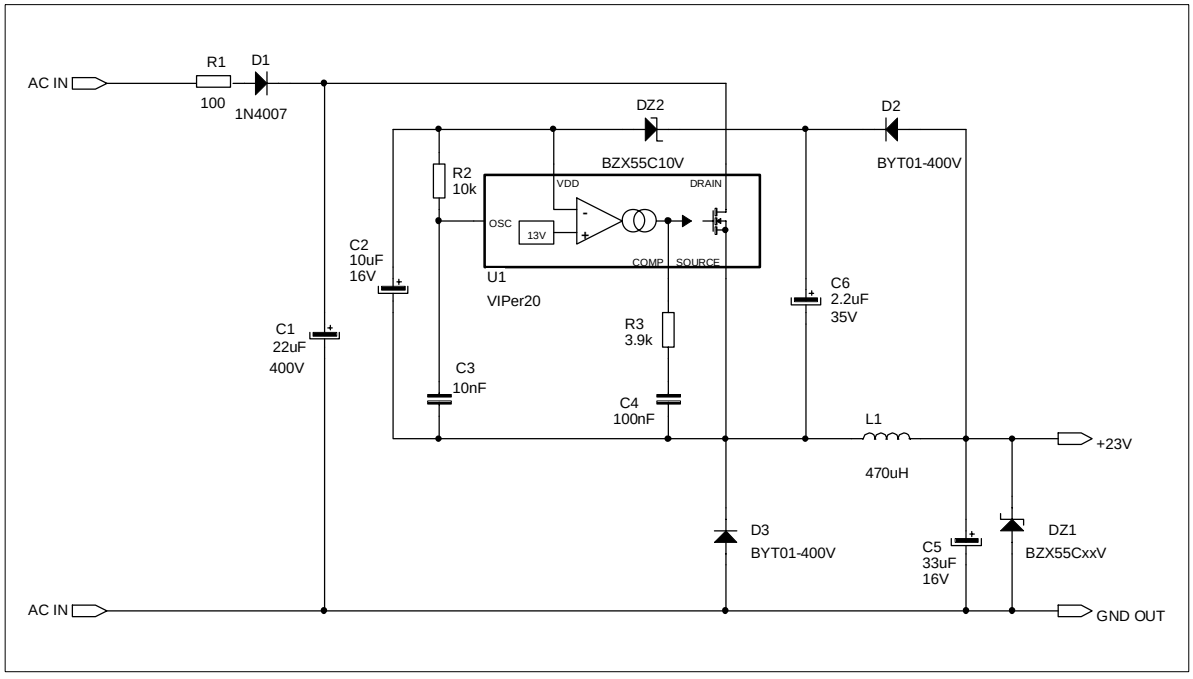
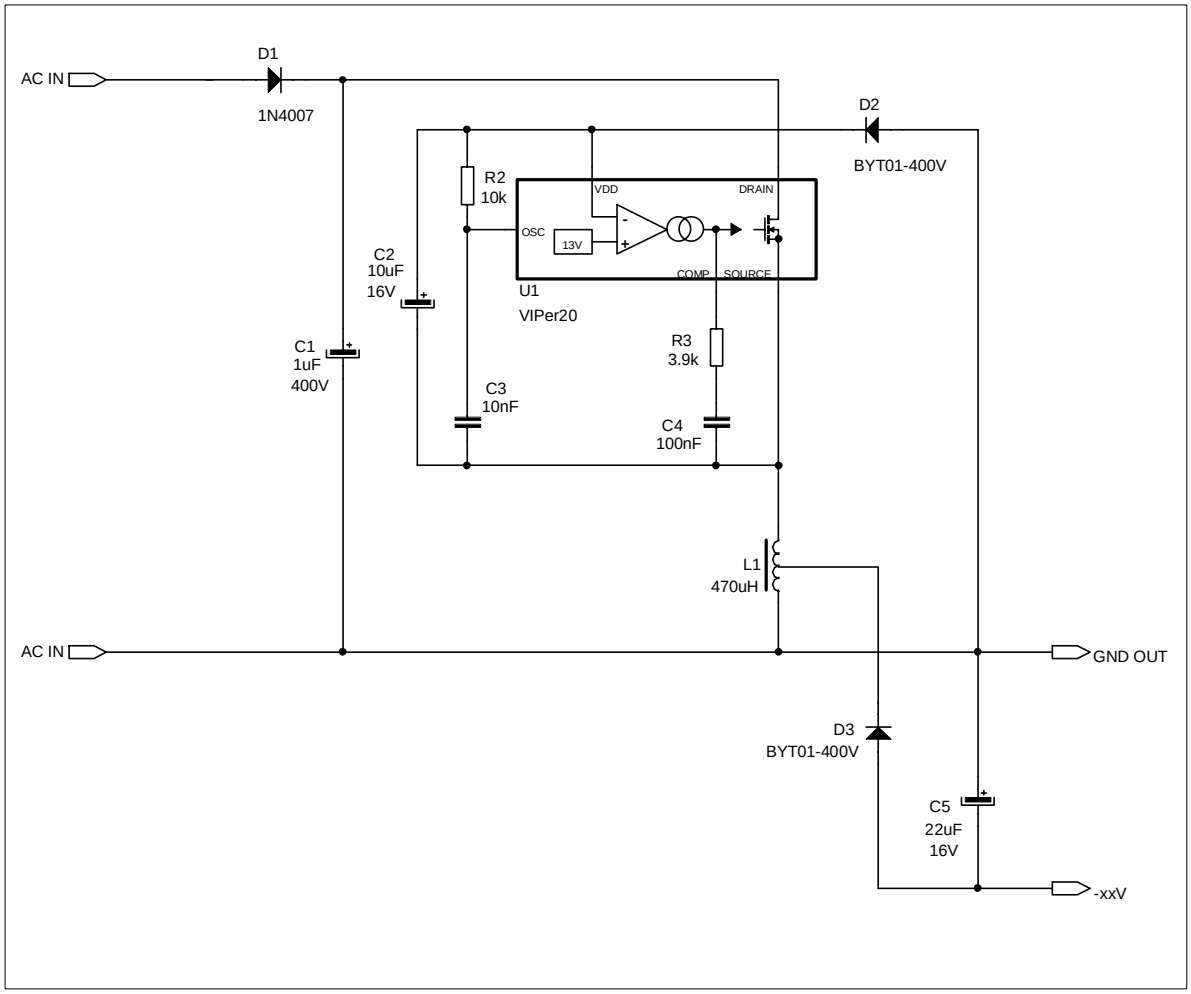


Figure 25: Non isolated inverter - Reduced output voltage.



6. CONCLUSION

It has been demonstrated that the simple topologies as the Buck or the inverter can be used directly on off line applications to build efficient non isolated power supplies in the range of a few watts. A VIPer20 device can minimize the total number of components by offering the error amplifier, the PWM and the Power MOSFET together inside a single piece of silicon.

A special care must be taken when designing the Buck topology, as it can provide serious output overvoltages in case of low input voltage, and/or low output load. A simple zener diode on the output, or a more efficient switching frequency shifter network can overcome this issue.

The benefits of such low power structures over more conventional 50 Hz transformers followed by rectifiers, filters and serial regulators can be listed as follow:

- Wide range of input voltages with good output regulation
- Higher efficiency and lower standby consumption
- Lighter weight, with direct implementation on a standard PCB

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may results from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.
The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in ITALY- All Rights Reserved.

STMicroelectronics GROUP OF COMPANIES
Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

http://www.st.com