M2004-02

Frequency Synthesizer

FEATURES

- Output Clock Frequency up to 700MHz
- Internal Low-jitter SAW-based Oscillator
- Intrinsic Jitter <1ps rms (12kHz - 20MHz)
- Differential Input Compatible with LVPECL, LVDS, HSTL, SSTL, etc.
- Dual Input MUX
- Parallel Programming
- Tunable Loop Filter Response
- Differential LVPECL Outputs
- 3.3V Operation
- Small 9mm x 9mm SMT Package

APPLICATIONS

- SONET / SDH / 10GbE System Synchronization
- Add / Drop Muxes, Access and Edge Switches
- Line Card System Clock Cleaner / Translator
- Optical Module Clock Cleaner / Translator

DESCRIPTION

The M2004-02 integrates a high performance Phase Locked Loop (PLL) with a Voltage Controlled SAW Oscillator (VCSO) to provide a low jitter Frequency Synthesizer in a 9mm x 9mm surface mount package.

The internal high “Q” SAW filter provides low jitter signal performance and determines the maximum output frequency of the VCSO.

A programmable output divider can divide the VCSO frequency to achieve an output as low as 38.88MHz.

The input to the Frequency Synthesizer is provided by selecting between a differential input clock or a single ended input clock.

The output frequency is an integer multiple of the input reference frequency. The multiplying factor is programmed via a 6 bit parallel address.

An external loop filter sets the PLL bandwidth which can be optimized to provide jitter attenuation of the input reference clock.

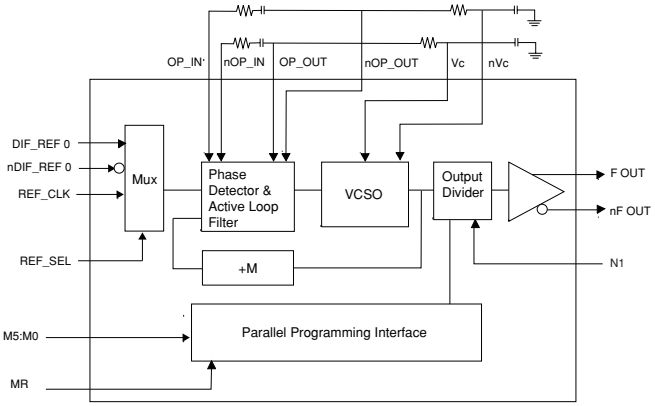
The bandwidth control, low phase noise, and HOLD features make the M2004-02 ideal for use as a clock jitter attenuator, frequency translator, and clock frequency generator in OC-3 through OC-192 applications.

ISO 9001 Registered

FUNCTIONAL BLOCK DIAGRAM

Functional Description:

The internal PLL will adjust the VCSO output frequency to be M (feedback divider) times the selected input reference clock frequency. Note that the product of M x the input reference frequency



must be such that it falls within the “lock” range of the VCSO. The N output divider can be programmed to divide the VCSO output frequency by 1, 2, 4, or 8 and provide a 50% output duty cycle.

The multiplying factor is programmed via a 6-bit parallel bus.

The relationship between the VCSO frequency, the M divider, and the Differential Input reference clock is defined as follows:

$$F\ VCSO = F\ REF\_CLK \times M$$

When the N output divider is included, the complete relationship for the output frequency is defined as:

$$FOUT = \frac{F\ VCSO}{N} = F\ REF\_CLK \times \frac{M}{N}$$

The N1 input can be hard wired to set the N divider to a specific state that will automatically occur during power-up.

FUNCTIONAL DESCRIPTION

LOOP FILTER

The M2004-02 requires the use of an external loop filter via the provided filter pins. Due to the differential design, the implementation requires two identical RC filters as shown in Figure 2.

FIGURE 2

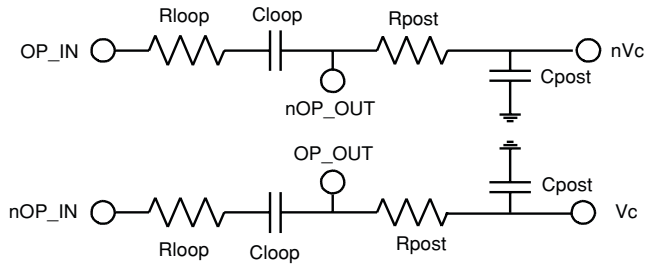


TABLE 1. RECOMMENDED LOOP FILTER VALUES

REF_CLK Frequency	VCSO Frequency	M	N	FOUT	Rloop	Cloop	Rpost	Cpost
19.44MHz	622.0800MHz	32	1	622.0800MHz	5kΩ	1MF	20kΩ	250pf

PIN DESCRIPTIONS

TABLE 2

Pin Number	Name	I/O	Configuration	Description
1, 2, 3	GND	GND		Power Supply Ground
4, 9	OP_IN, nOP_IN	Analog I/O		Used for external loop filter. See Figure 2.
5, 8	nOP_OUT, OP_OUT	Analog I/O		Used for external loop filter. See Figure 2
6, 7	nVC, VC	Input		VCSO Differential Control Voltage Input Pair
10, 14, 26	GND	GND		Power Supply Ground
11, 19, 33	V_{CC}	Power		Positive Supply Pins
12, 13	N0, N1	Input	Pull - down	Determines the output divider value as defined in Table 3C. LVCMOS / LVTTL interface levels.
15, 16	FOUT, nFOUT	Output	Unterminated	Differential output, 3.3V LVPECL levels.
17	MR	Input	Pull - down	Logic HIGH resets the reference frequency and N output dividers. Logic LOW enables the outputs. LVCMOS / LVTTL interface levels.
18, 20, 21	NC			No Connection
22	REF_SEL	Input	Pull - down	Selects between the different reference clock inputs as the PLL reference source. See table 3D. LVCMOS / LVTTL interface levels.
23	NDIF_REF	Input	Pull - down	Inverting differential clock input. Compatible logic levels include LVCMOS, LVDS, HSTL, etc.
24	DIF_REF	Input	Pull - down	Non-inverting differential clock input. Compatible logic levels include LVCMOS, LVDS, HSTL, etc.
25	REF_ CLK	Input	Pull - down	Input reference clock. LVCMOS / LVTTL interface levels.
27, 28, 29, 30, 31	M0, M1, M2, M3, M4	Input	Pull - down	M divider inputs. Data is always transparent. No latch signal is required.
32	M5	Input	Pull - down	
34, 35, 36	DNC			Do not connect. Internal test pins.

PIN CHARACTERISTICS

TABLE 4

Symbol	Parameter	Test Conditions	Min	Typical	Max	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

PARALLEL & SERIAL MODES FUNCTION

TABLE 5A

Inputs			
MR	M	N	Conditions
H	X	X	Reset, Forces outputs LOW.
L	Data	Data	Data on M and N inputs passed directly to the M divider and N output divider.

Note: L = Low; H = High; X = Don't care; ↑ = Rising Edge Transition; ↓ = Falling Edge Transition

PROGRAMMABLE VCSO FREQUENCY FUNCTION

TABLE 5B

VCSO Frequency (MHz)	M Divide	32 M5	16 M4	8 M3	4 M2	2 M1	1 M0
325	13	0	0	1	1	0	1
350	14	0	0	1	1	1	0
375	15	0	0	1	1	1	1
400	16	0	1	0	0	0	0
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
600	24	0	1	1	0	0	0
625	25	0	1	1	0	0	1
650	26	0	1	1	0	1	0

NOTE 1: These M divide values and the resulting frequencies correspond to a reference frequency of 25MHz.

PARALLEL MODE FUNCTION

TABLE 5C

Inputs N1	Inputs N0	N Divider Value	Output Frequency (MHz) Min	Output Frequency (MHz) Max
0	0	1	311	700
0	1	2	155.5	350
1	0	4	77.75	175
1	1	8	38.875	87.5

SERIAL MODE FUNCTION

TABLE 5D

Inputs REF SEL	Inputs Reference
0	DIFF_REF
1	REF_CLK

POWER SUPPLY DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			162		mA

V_{CC}= 3.3V ±5%, T_A= 0°C to 70°C

DIFFERENTIAL INPUT DC CHARACTERISTICS

Symbol		Parameter	Test Conditions	Min	Max	Units
I_{IH}	Input High Current	nDIF_REF			5	µA
		DIF_REF			150	µA
I_{IL}	Input Low Current	nDIF_REF		-150		µA
		DIF_REF		-5		µA
V_{P-P}	Peak to Peak Input Voltage			0.15		V
V_{CMR}	REF_SEL, REF_CLK			V_{CC} +0.3	V_{CC} -0.85	V

V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C

LVCMOS/LVTTL DC CHARACTERISTICS

Symbol		Parameter	Test Conditions	Min	Max	Units
V_{IH}	Input High Voltage	REF_SEL, REF_CLK, N0:N1, M0:M5, MR		2	VCC + 0.3	V
V_{IL}	Input Low Voltage	REF_SEL, N0:N1, M0:M5, MR				
		REF_CLK		-0.3	1.3	V
I_{IH}	Input High Current	M5	V_{DD} = V_{IN} = 3.465V		5	µA
		N0, N1, MR, M0:M4, S_CLOCK, REF_SEL, REF_CLK	V_{DD} = V_{IN} = 3.465V		150	µA
I_{IL}	Input Low Current	M5	V_{DD} = 3.465, V_{IN} = 0V	-150		µA
		N0, N1, MR, M0:M4, REF_SEL, REF_CLK	V_{DD} = 3.465, V_{IN} = 0V	-5		µA

LVPECL DC CHARACTERISTICS

Symbol	Parameter	Signal	Min	Max	Units
V_{OH}	Output High Voltage: Note 1	FOUT, nFOUT	V_{DD} – 1.4	Vcc – 1.0	V
V_{OL}	Output Low Voltage: Note 1	FOUT, nFOUT	V_{DD} – 2.0	Vcc – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	FOUT, nFOUT	0.6	0.85	V

Note 1: Output terminated with 50Ω to V_{DD}–2.V

INPUT FREQUENCY CHARACTERISTICS

Symbol	Parameter		Test Conditions	Min	Max	Units
F_{IN}	Input Frequency	DIF_REF		10	175	MHz
		nDIF_REF		10	175	MHz

V_{CC} = 3.3V±5%, T_A = 0°C to 70°C

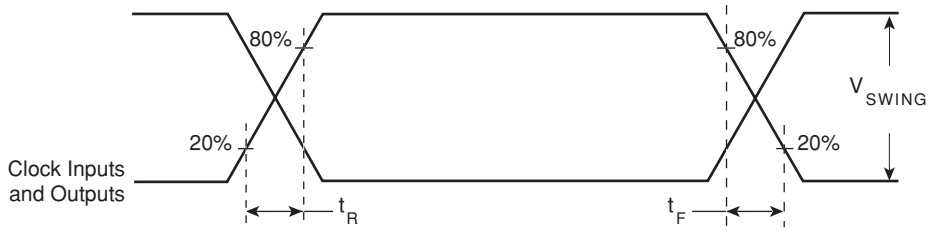
AC CHARACTERISTICS

Symbol	Parameter		Test Conditions	Min	Typ	Max	Units
F_{OUT}	Output Frequency			38.88		667	MHz
ØNOISE	Single Side Band		1kHz offset		-72		dBc/Hz
	Phase Noise		10kHz offset		-94		dBc/Hz
			100kHz offset		-123		dBc/Hz
J (t)	Jitter (RMS)		12kHz to 20 MHz		0.69		ps
odc	Output Duty Cycle				50		%
t_R	Output Rise Time	FOUT = 155MHz	20% to 80%, each	350	450	550	ps
(Note 1)	for output pairs	FOUT = 311MHz	output of pair measured	325	425	500	ps
	FOUT0, nFOUT0 &	FOUT= 622MHz	is terminated into 50Ω	200	275	350	ps
	FOUT1, nFOUT1		load biased at Vcc-2V				
t_F	Output Fall Time	FOUT = 155MHz	20% to 80%, each	350	450	550	ps
(Note 1)	for output pairs	FOUT = 311MHz	output of pair measured	325	425	500	ps
	FOUT0, nFOUT0 &	FOUT = 622MHz	is terminated into 50Ω	200	275	350	ps
	FOUT1, nFOUT1		load biased at Vcc-2V				
t_{LOCK}	PLL Lock Time					1	ms

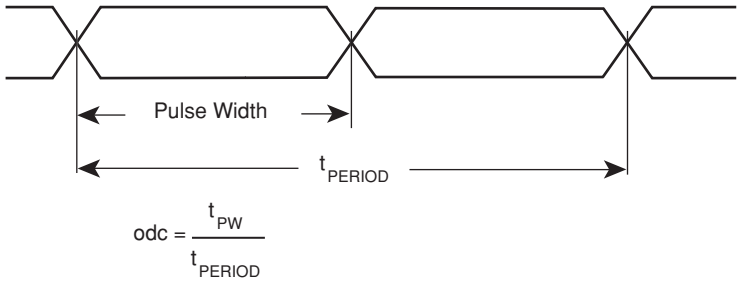
Note: The output frequencies of 155MHz, 311MHz and 622MHz were chosen for device characterization as these are common optical network clock frequencies.

PARAMETER MEASUREMENT INFORMATION

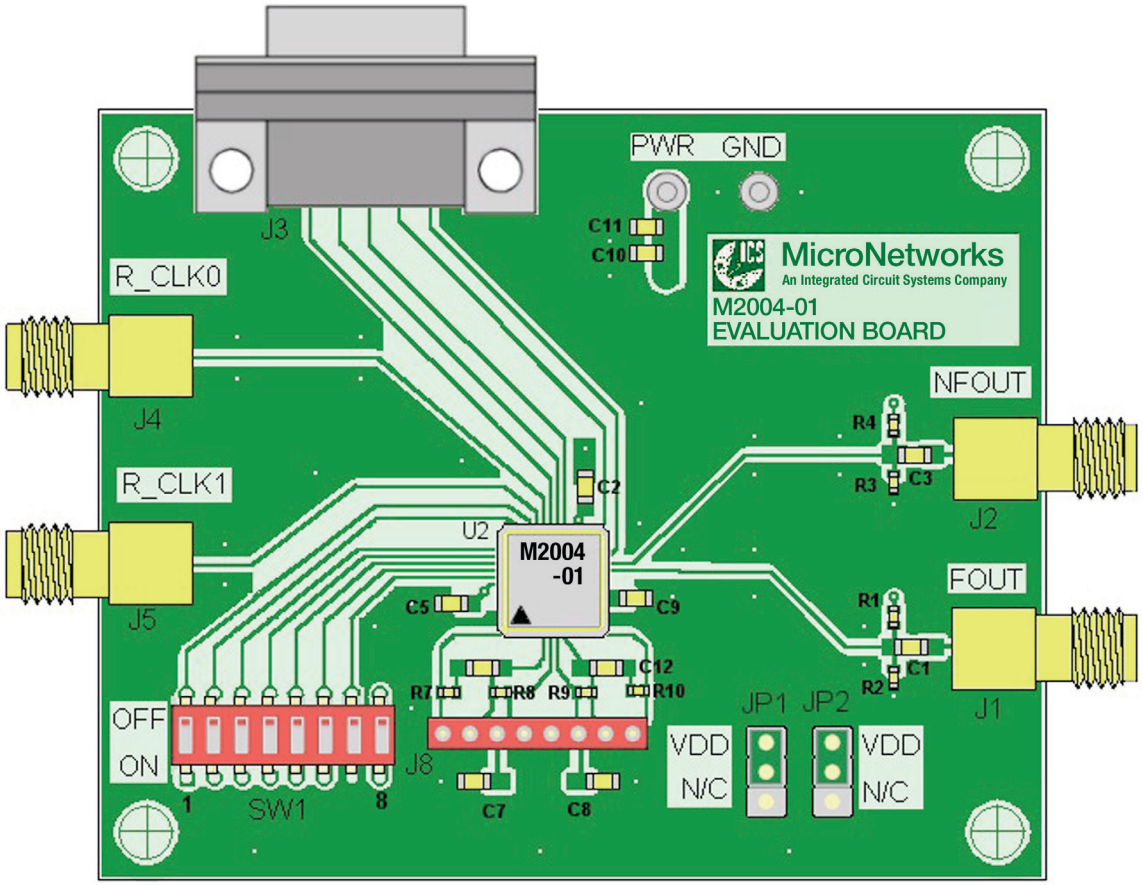
INPUT AND OUTPUT RISE AND FALL TIME



ODC & t_{PERIOD}



TEST EVALUATION BOARD



J3 9-PIN D CONNECTOR

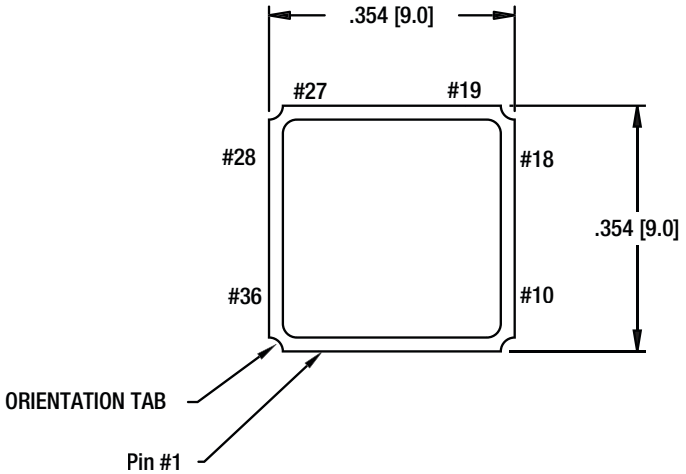
Pin	Signal
1	MR
3	S_CLOCK
5	S_DATA
7	S_LOAD
9	nP_LOAD

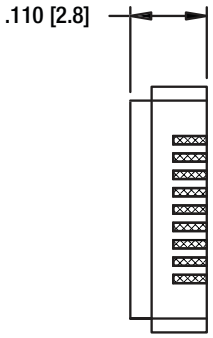
SW1

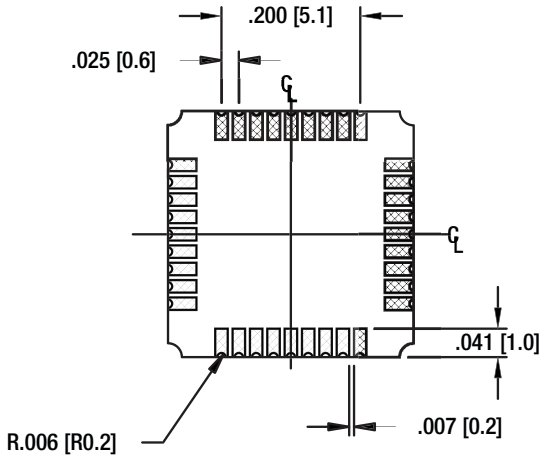
	1	2	3	4	5	6	7	8
Position	REF Select	M5	M4	M3	M2	M1	M0	N/C
Off	REF_CLK0	“1”	“0”	“0”	“0”	“0”	“0”	N/C
On	REF_CLK1	“0”	“1”	“1”	“1”	“1”	“1”	N/C

JP1: N0 Logic “1” when installed
JP2: N1 Logic “0” when installed

MECHANICAL DIMENSIONS & PIN CONFIGURATION







Pin#	Designation	Pin#	Designation
1	GND	18	N/C
2	GND	19	VCC
3	GND	20	N/C
4	OP_IN	21	N/C
5	nOP_OUT	22	REF_SEL
6	nVC	23	nDIF_REF
7	VC	24	DIF_REF
8	OP_OUT	25	REF_CLK
9	nOP_IN	26	GND
10	GND	27	M0
11	VCC	28	M1
12	NO	29	M2
13	N1	30	M3
14	GND	31	M4
15	FOUT	32	M5
16	nFOUT	33	VCC
17	MR	34, 35, 36	DNC

Dimensions are in inches, (dimensions) are in mm.

ORDERING INFORMATION

PART NUMBER **M2004-02-622.0800**

Series

Model

VCSO Center Frequency
(i.e. 622.0800MHz)

Available VCSO Frequencies

500.0000	
622.0800	669.1281
625.0000	669.3266
627.3296	672.1600
644.5313	690.5692
666.5143	693.4830

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