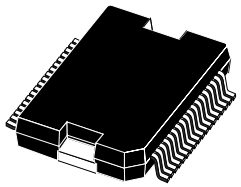
L6258E

PWM controlled high current DMOS universal motor driver

Not For New Design

Features

- Able to drive both windings of a bipolar stepper motor or two DC motors
- Output current up to 1.2A each winding
- Wide voltage range: 12V to 40V
- Four quadrant current control, ideal for microstepping and DC motor control
- Precision PWM control
- No need for recirculation diodes
- TTL/CMOS compatible inputs
- Cross conduction protection
- Thermal shutdow



PowerSO36

The power stage is a dual DMOS full bridge capable of sustaining up to 40V, and includes the diodes for current recirculation.The output current capability is 1.2A per winding in continuous mode, with peak start-up current up to 1.5A. A thermal protection circuitry disables the outputs if the chip temperature exceeds the safe limits.

Description

L6258E is a dual full bridge for motor control applications realized in BCD technology, with the capability of driving both windings of a bipolar stepper motor or bidirectionally control two DC motors.

L6258E and a few external components form a complete control and drive circuit. It has high efficiency phase shift chopping that allows a very low current ripple at the lowest current control levels, and makes this device ideal for steppers as well as for DC motors.

Table 1. Device summary

Order code	Package	Packing
L6258E (Replaced by **L6258EX**)	PowerSO36	Tube

This is information on a product still in production but not recommended for new designs. www.st.com

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1 Block diagram

Figure 1. Block diagram

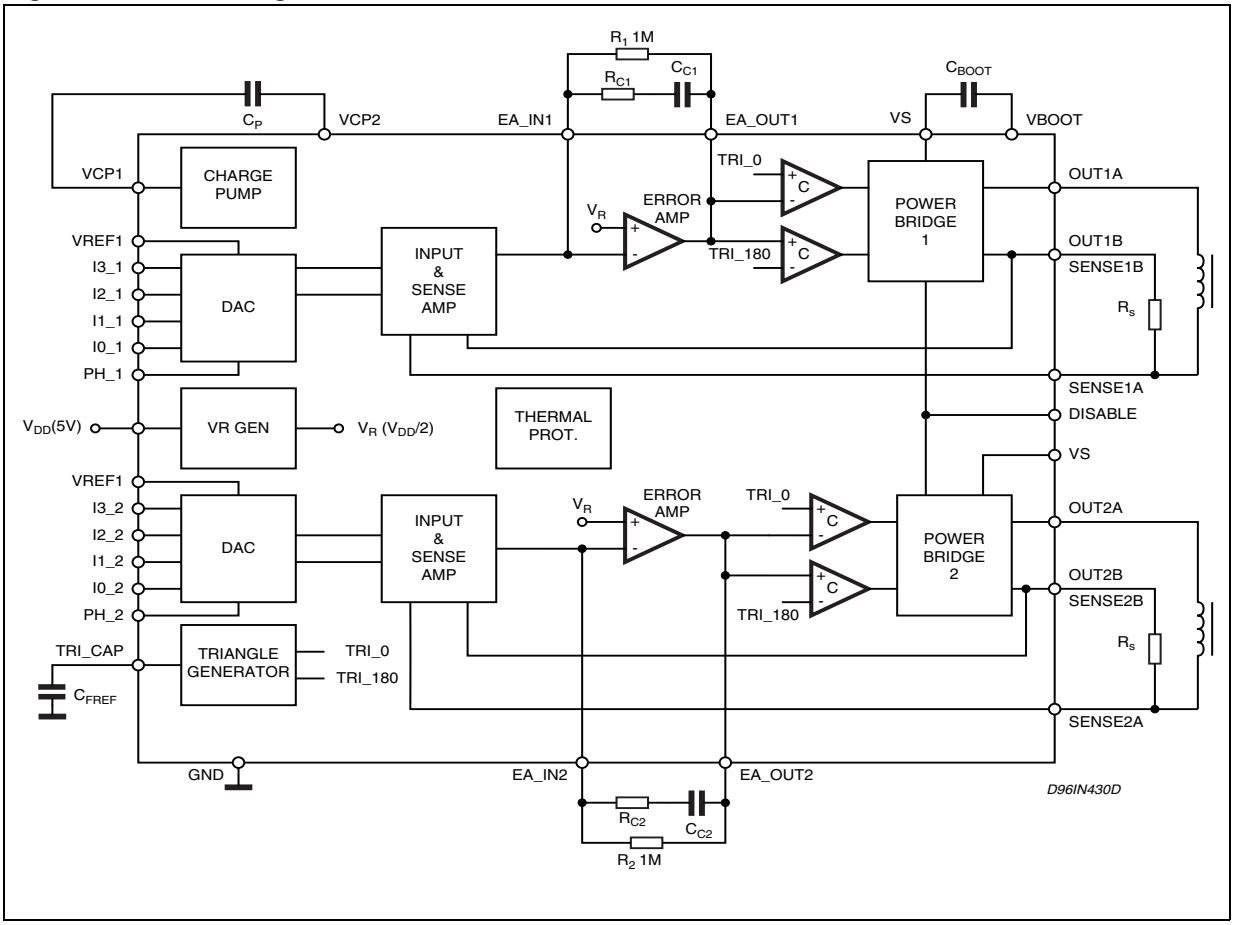


Table 2. Absolute maximum rating

Parameter	Description	Value	Unit
V_s	Supply voltage	45	V
V_{DD}	Logic supply voltage	7	V
V_{ref1}/V_{ref2}	Reference voltage	2.5	V
I_O	Output current (peak)	1.5	A
I_O	Output current (continuous)	1.2	A
V_{in}	Logic input voltage range	-0.3 to 7	V
V_{boot}	Bootstrap supply	60	V
V_{boot} - V_s	Maximum Vgate applicable	15	V
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Figure 2. Pin connection (top view)

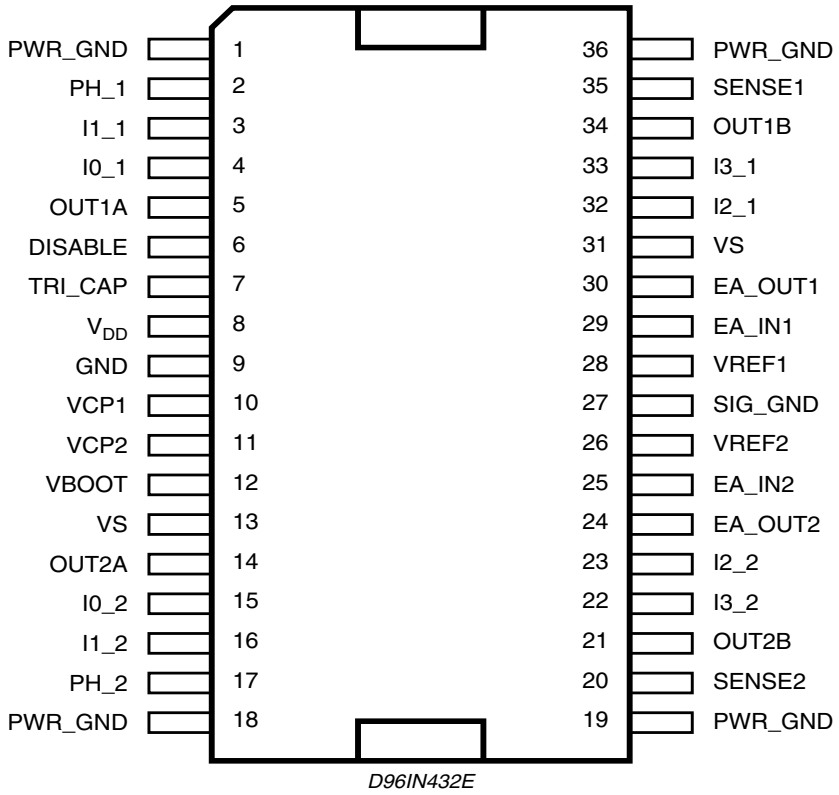


Table 3. Pin functions

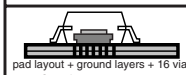
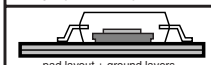
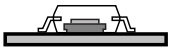
Pin #	Name	Description
1, 36	PWR_GND	Ground connection (1). They also conduct heat from die to printed circuit copper.
2, 17	PH_1, PH_2	These TTL compatible logic inputs set the direction of current flow through the load. A high level causes current to flow from OUTPUT A to OUTPUT B.
3	I_{1_1}	Logic input of the internal DAC (1). The output voltage of the DAC is a percentage of the Vref voltage applied according to the thruth *Table 5 on page 12*.
4	I_{0_1}	See pin 3
5	OUT1A	Bridge output connection (1)
6	DISABLE	Disables the bridges for additional safety during switching. When not connected the bridges are enabled
7	TRI_cap	Triangular wave generation circuit capacitor. The value of this capacitor defines the output switching frequency

Table 3. Pin functions (continued)

Pin #	Name	Description
8	V_{DD} (5V)	Supply voltage input for logic circuitry
9	GND	Power ground connection of the internal charge pump circuit
10	V_{CP1}	Charge pump oscillator output
11	V_{CP2}	Input for external charge pump capacitor
12	V_{BOOT}	Overvoltage input for driving of the upper DMOS
13, 31	V_S	Supply voltage input for output stage. They are shorted internally
14	OUT2A	Bridge output connection (2)
15	I_{0_2}	Logic input of the internal DAC (2). The output voltage of the DAC is a percentage of the VRef voltage applied according to the truth *Table 5 on page 12*.
16	I_{1_2}	See pin 15
18, 19	PWR_GND	Ground connection. They also conduct heat from die to printed circuit copper
20, 35	SENSE2, SENSE1	Negative input of the transconductance input amplifier (2, 1)
21	OUT2B	Bridge output connection and positive input of the tranconductance (2)
22	I_{3_2}	See pin 15
23	I_{2_2}	See pin 15
24	EA_OUT_2	Error amplifier output (2)
25	EA_IN_2	Negative input of error amplifier (2)
26, 28	V_{REF2}, V_{REF1}	Reference voltages for the internal DACs, determining the output current value. Output current also depends on the logic inputs of the DAC and on the sensing resistor value
27	SIG_GND	Signal ground connection
29	EA_IN_1	Negative input of error amplifier (1)
30	EA_OUT_1	Error amplifier output (1)
32	I_{2_1}	See pin 3
33	I_{3_1}	See pin 3
34	OUT1B	Bridge output connection and positive input of the tranconductance (1)

Note: The number in parenthesis shows the relevant Power Bridge of the circuit. Pins 18, 19, 1 and 36 are connected together.

Figure 3. Thermal characteristics

Conditions	Power Dissipated (W)	T Ambient (˚C)	Thermal J-A resistance (˚C/W)
 pad layout + ground layers + 16 via hol PCB ref.: 4 LAYER cm 12 x 12	5.3	70	15
 pad layout + ground layers PCB ref.: 4 LAYER cm 12 x 12	4.0	70	20
 pad layout + 6cm2 on board heat sink PCB ref.: 2 LAYER cm 12 x 12	2.3	70	35

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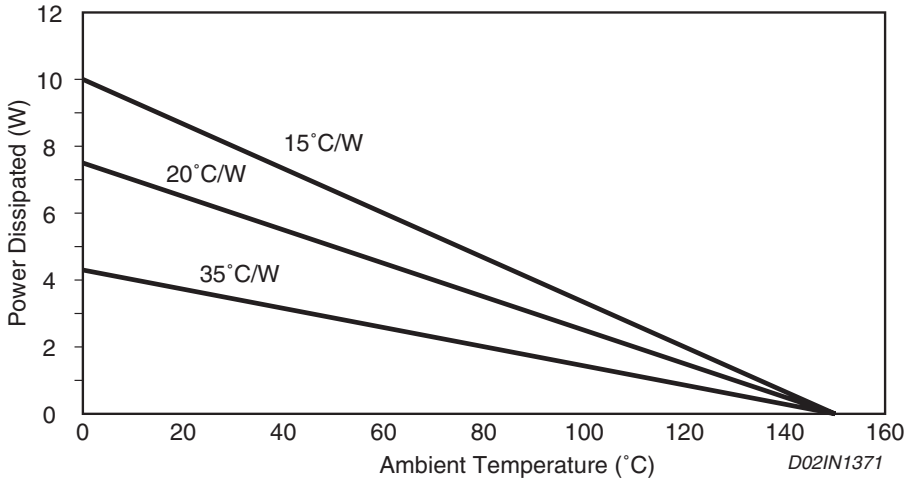


Table 4. Electrical characteristics

(V_S = 40V; V_{DD} = 5V; T_j = 25°; unless otherwise specified.)

Parameter	Description	Test condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage		12		40	V
V_{DD}	Logic supply voltage		4.75		5.25	V
V_{BOOT}	Storage voltage	V_S = 12 to 40V	V_S+6		V_S+12	V
V_{Sense}	Max drop across sense resistor				1.25	V
$V_{S(off)}$	Power off reset	Off threshold	6		7.2	V
$V_{DD(off)}$	Power off reset	Off threshold	3.3		4.1	V
$I_{S(on)}$	V_S quiescent current	Both bridges ON, no load			15	mA
$I_{S(off)}$	V_S quiescent current	Both bridges OFF			7	mA
I_{DD}	V_{DD} operative current				15	mA

Table 4. Electrical characteristics (continued)
(V_S = 40V; V_{DD} = 5V; T_j = 25°; unless otherwise specified.)

Parameter	Description	Test condition	Min.	Typ.	Max.	Unit
ΔT_{SD-H}	Shut down hysteresis			25		°C
T_{SD}	Thermal shutdown			150		°C
f_{osc}	Triangular oscillator frequency(1)	C_{FREF} = 1nF	12.5	15	18.5	KHz
TRANSISTORS						
I_{DSS}	Leakage current	OFF State			500	µA
$R_{ds(on)}$	On resistance	ON state		0.6	0.75	W
V_f	Flywheel diode voltage	If =1.0A		1	1.4	V
CONTROL LOGIC						
$V_{in(H)}$	Input voltage	All Inputs	2		V_{DD}	V
$V_{in(L)}$	Input voltage	All inputs	0		0.8	V
I_{in}	Input current (2)	0 < V_{in} < 5V	-150		+10	µA
I_{dis}	Disable pin input current		-10		+150	µA
$V_{ref1}/_{ref2}$	Reference voltage	Operating	0		2.5	V
I_{ref}	V_{ref} terminal input current	V_{ref} = 1.25	-2		5	µA
FI = V_{ref}/V_{sense}	PWM loop transfer ratio			2		
V_{FS}	DAC full scale precision	V_{ref} = 2.5V $I_0/I_1/I_2/I_3$ = L	1.23		1.34	V
V_{offset}	Current loop offset	V_{ref} = 2.5V $I_0/I_1/I_2/I_3$ = H	-30		+30	mV
	DAC factor ratio	Normalized @ full scale value	-2		+2	%
SENSE AMPLIFIER						
V_{cm}	Input common mode voltage range		-0.7		V_S+0.7	V
I_{inp}	Input bias	sense1/sense2	-200		0	µA
ERROR AMPLIFIER						
G_V	Open loop voltage gain			70		dB
SR	Output slew rate	Open loop		0.2		V/µs
GBW	Gain bandwidth product			400		kHz

1. Chopping frequency is twice fosc value.
2. This is true for all the logic inputs except the disable input.

2 Functional description

The circuit is intended to drive both windings of a bipolar stepper motor or two DC motors.

The current control is generated through a switch mode regulation.

With this system the direction and the amplitude of the load current are depending on the relation of phase and duty cycle between the two outputs of the current control loop.

The L6258E power stage is composed by power DMOS in bridge configuration as it is shown in *Figure 4*, where the bridge outputs OUT_A and OUT_B are driven to V_s with an high level at the inputs IN_A and IN_B while are driven to ground with a low level at the same inputs.

The zero current condition is obtained by driving the two half bridge using signals IN_A and IN_B with the same phase and 50% of duty cycle.

In this case the outputs of the two half bridges are continuously switched between power supply (V_s) and ground, but keeping the differential voltage across the load equal to zero.

In *Figure 4* is shown the timing diagram of the two outputs and the load current for this working condition.

Following we consider positive the current flowing into the load with a direction from OUT_A to OUT_B, while we consider negative the current flowing into load with a direction from OUT_B to OUT_A.

Now just increasing the duty cycle of the IN_A signal and decreasing the duty cycle of IN_B signal we drive positive current into the load.

In this way the two outputs are not in phase, and the current can flow into the load trough the diagonal bridge formed by T1 and T4 when the output OUT_A is driven to V_s and the output OUT_B is driven to ground, while there will be a current recirculation into the higher side of the bridge, through T1 and T2, when both the outputs are at Vs and a current recirculation into the lower side of the bridge, through T3 and T4, when both the outputs are connected to ground.

Since the voltage applied to the load for recirculation is low, the resulting current discharge time constant is higher than the current charging time constant during the period in which the current flows into the load through the diagonal bridge formed by T1 and T4. In this way the load current will be positive with an average amplitude depending on the difference in duty cycle of the two driving signals.

In *Figure 4* is shown the timing diagram in the case of positive load current

On the contrary, if we want to drive negative current into the load is necessary to decrease the duty cycle of the IN_A signal and increase the duty cycle of the IN_B signal. In this way we obtain a phase shift between the two outputs such to have current flowing into the diagonal bridge formed by T2 and T3 when the output OUT_A is driven to ground and output OUT_B is driven to Vs, while we will have the same current recirculation conditions of the previous case when both the outputs are driven to Vs or to ground.

So, in this case the load current will be negative with an average amplitude always depending by the difference in duty cycle of the two driving signals.

In *Figure 4* is shown the timing diagram in the case of negative load current.

Figure 5 shows the device block diagram of the complete current control loop.

2.1 Reference voltage

The voltage applied to VREF pin is the reference for the internal DAC and, together with the sense resistor value, defines the maximum current into the motor winding according to the following relation:

$$I_{MAX} = \frac{0.5 \cdot V_{REF}}{R_S} = \frac{1}{FI} \cdot \frac{V_{REF}}{R_S}$$

where R_s = sense resistor value

Figure 4. Power bridge configuration

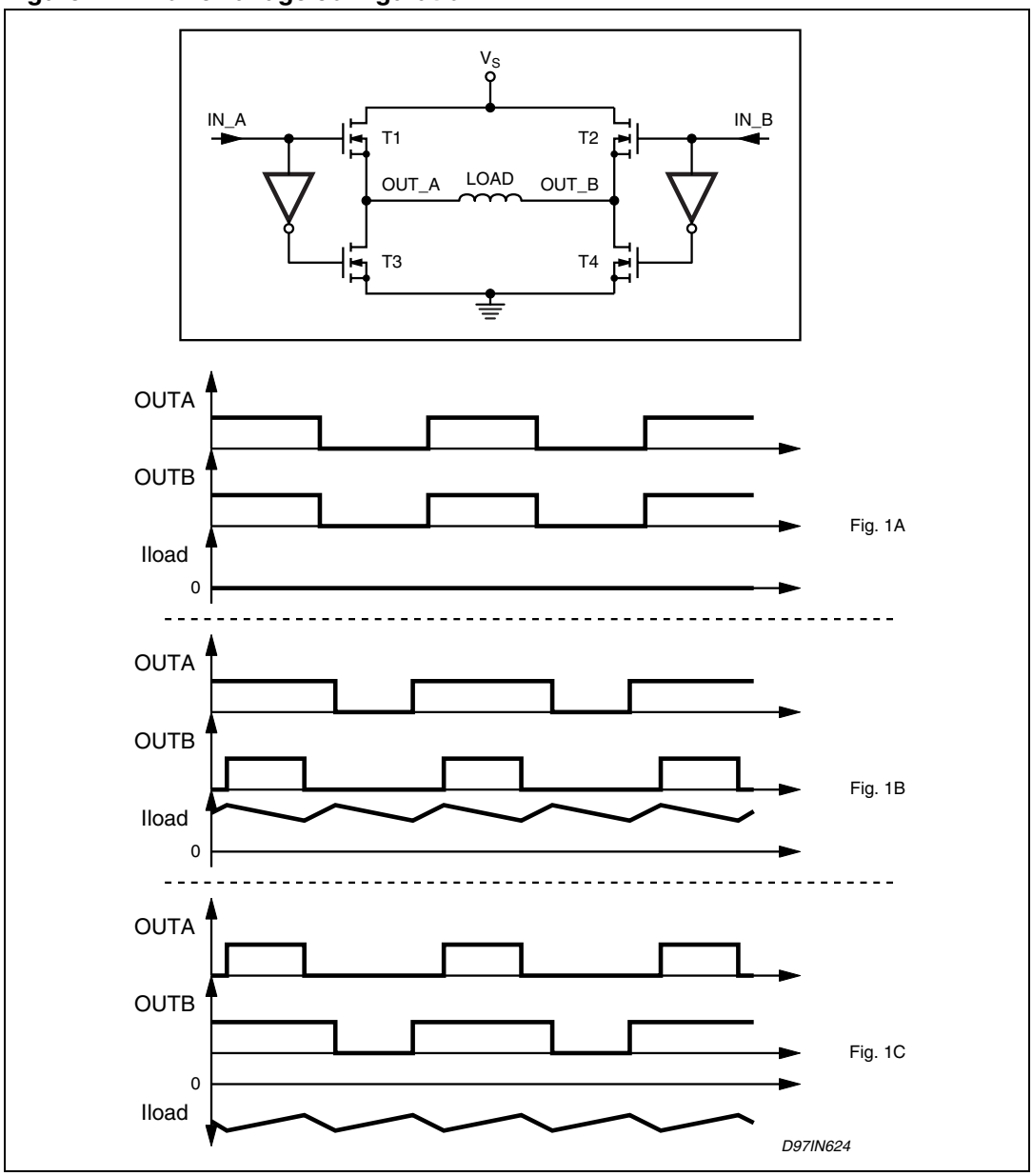
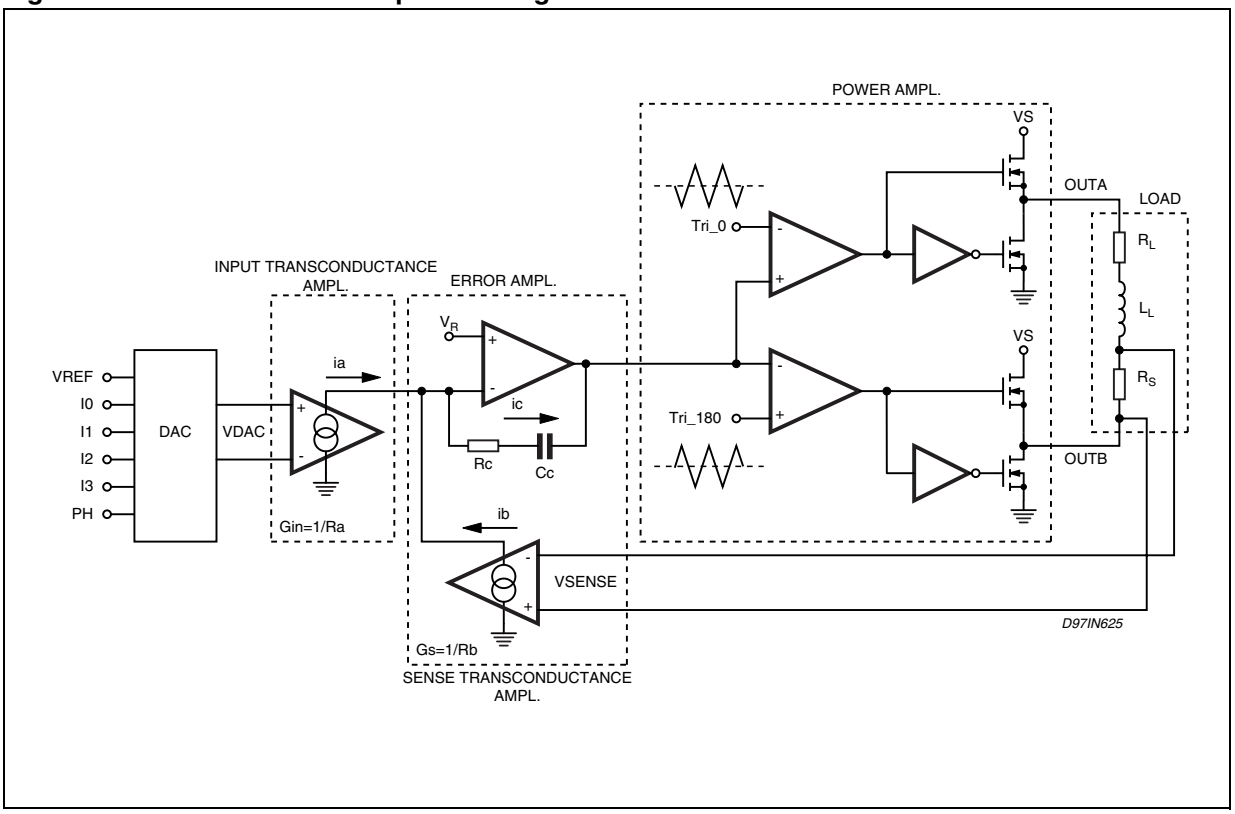


Figure 5. Current control loop block diagram



2.2 Input logic (I_0 - I_1 - I_2 - I_3)

The current level in the motor winding is selected according to this table:

Table 5. Current levels

I3	I2	I1	I0	Current level % of IMAX
H	H	H	H	No Current
H	H	H	L	9.5
H	H	L	H	19.1
H	H	L	L	28.6
H	L	H	H	38.1
H	L	H	L	47.6
H	L	L	H	55.6
H	L	L	L	63.5
L	H	H	H	71.4
L	H	H	L	77.8
L	H	L	H	82.5

Table 5. Current levels (continued)

I3	I2	I1	I0	Current level % of IMAX
L	H	L	L	88.9
L	L	H	H	92.1
L	L	H	L	95.2
L	L	L	H	98.4
L	L	L	L	100

2.3 Phase input (PH)

The logic level applied to this input determines the direction of the current flowing in the winding of the motor.

High level on the phase input causes the motor current flowing from OUT_A to OUT_B through the load.

2.4 Triangular generator

This circuit generates the two triangular waves TRI_0 and TRI_180 internally used to generate the duty cycle variation of the signals driving the output stage in bridge configuration.

The frequency of the triangular wave defines the switching frequency of the output, and can be adjusted by changing the capacitor connected at TR1_CAP pin:

$$F_{ref} = \frac{K}{C}$$

where: $K = 1.5 \times 10^{-5}$

2.5 Charge pump circuit

To ensure the correct driving of the high side drivers a voltage higher than Vs is supplied on the Vboot pin. This boostrap voltage is not needed for the low side power DMOS transistors because their sources terminals are grounded. To produce this voltage a charge pump method is used. It is made by using two external capacitors; one connected to the internal oscillator (CP) and the other (Cboot) to storage the overvoltage needed for the driving the gates of the high side DMOS. The value suggested for the capacitors are:

Table 6. Charge pump capacitor's values

Component name	Component's function	Value	Unit
C_{boot}	Storage capacitor	100	nF
C_P	Pump capacitor	10	nF

2.6 Current control loop

The current control loop is a transconductance amplifier working in PWM mode.

The motor current is a function of the programmed DAC voltage.

To keep under control the output current, the current control modulates the duty cycle of the two outputs OUT_A and OUT_B, and a sensing resistor Rs is connected in series with the motor winding in order to produce a voltage feedback compared with the programmed voltage of the DAC.

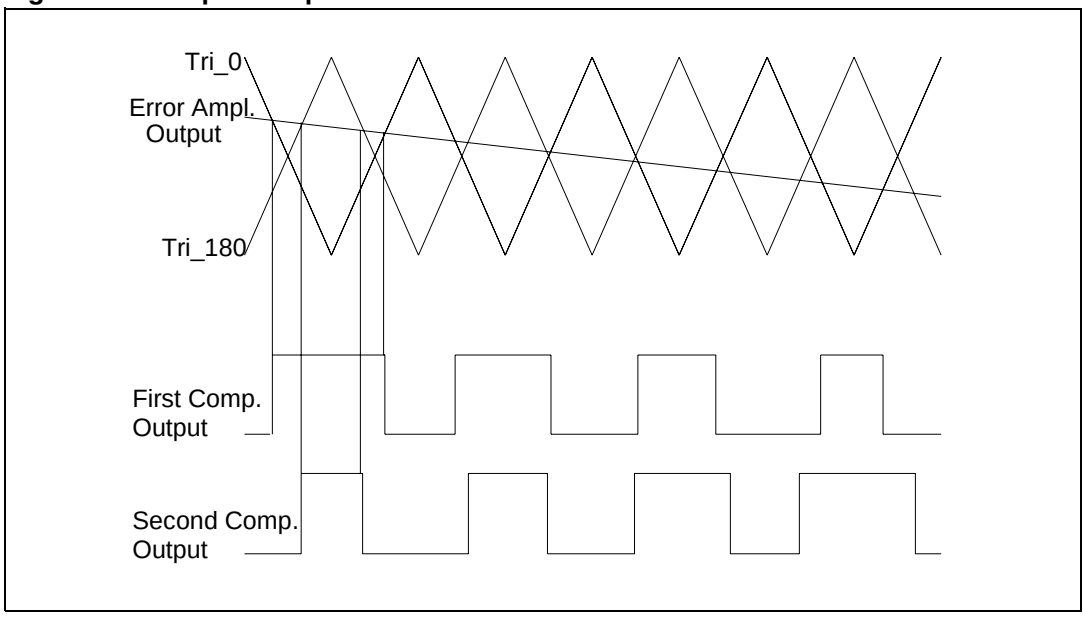
The duty cycle modulation of the two outputs is generated comparing the voltage at the outputs of the error amplifier, with the two triangular wave references.

In order to drive the output bridge with the duty cycle modulation explained before, the signals driving each output (OUTA & OUTB) are generated by the use of the two comparators having as reference two triangular wave signals Tri_0 and Tri_180 of the same amplitude, the same average value (in our case Vr), but with a 180° of phase shift each other.

The two triangular wave references are respectively applied to the inverting input of the first comparator and to the non inverting input of the second comparator.

The other two inputs of the comparators are connected together to the error amplifier output voltage resulting by the difference between the programmed DAC. The reset of the comparison between the mentioned signals is shown in *Figure 6*.

Figure 6. Output comparator waveforms



In the case of V_{DAC} equal to zero, the transconductance loop is balanced at the value of Vr, so the outputs of the two comparators are signals having the same phase and 50% of duty cycle.

As we have already mentioned, in this situation, the two outputs OUT_A and OUT_B are simultaneously driven from V_s to ground; and the differential voltage across the load in this case is zero and no current flows in the motor winding.

With a positive differential voltage on V_{DAC} (see *Figure 5*, the transconductance loop will be positively unbalanced respected Vr.

In this case being the error amplifier output voltage greater than Vr, the output of the first comparator is a square wave with a duty cycle higher than 50%, while the output of the second comparator is a square wave with a duty cycle lower than 50%.

The variation in duty cycle obtained at the outputs of the two comparators is the same, but one is positive and the other is negative with respect to the 50% level.

The two driving signals, generated in this case, drive the two outputs in such a way to have switched current flowing from OUT_A through the motor winding to OUT_B.

With a negative differential voltage V_{DAC}, the transconductance loop will be negatively unbalanced respected Vr.

In this case the output of the first comparator is a square wave with a duty cycle lower than 50%, while the output of the second comparator is a square wave with a duty cycle higher than 50%.

The variation in the duty cycle obtained at the outputs of the two comparators is always of the same.

The two driving signals, generated in this case, drive the the two outputs in order to have the switched current flowing from OUT_B through the motor winding to OUT_A.

2.7 Current control loop compensation

In order to have a flexible system able to drive motors with different electrical characteristics, the non inverting input and the output of the error amplifier (EA_OUT) are available.

Connecting at these pins an external RC compensation network it is possible to adjust the gain and the bandwidth of the current control loop.

3 PWM current control loop

3.1 Open loop transfer function analysis

Block diagram: refer to *Figure 5.*

Input parameters:

- V_S = 24V
- L_L = 12mH
- R_L = 12Ω
- R_S = 0.33Ω
- R_C = to be calculated
- C_C = to be calculated
- Gs transconductance gain = 1/Rb
- Gin transconductance gain = 1/Ra
- Ampl. of the Tria_0_180 ref. = 1.6V (peak to peak)
- R_a = 40KΩ
- R_b = 20KΩ
- V_r = Internal reference equal to $V_{DD}/2$ (Typ. 2.5V)

these data refer to a typical application, and will be used as an example during the analysis of the stability of the current control loop.

The block diagram shows the schematics of the L6258E internal current control loop working in PWM mode; the current into the load is a function of the input control voltage V_{DAC} , and the relation between the two variables is given by the following formula:

$$I_{LOAD} \cdot R_S \cdot G_S = V_{DAC} \cdot G_{in}$$

$$I_{LOAD} \cdot R_S \cdot \frac{1}{R_b} = V_{DAC} \cdot \frac{1}{R_a}$$

$$I_{LOAD} = V_{DAC} \cdot \frac{R_b}{R_a \cdot R_s} = 0.5 \cdot \frac{V_{DAC}}{R_S}(A)$$

where:

V_{DAC} is the control voltage defining the load current value

G_{in} is the gain of the input transconductance amplifier (1/Ra)

G_s is the gain of the sense transconductance amplifier (1/Rb)

R_s is the resistor connected in series to the output to sense the load current

In this configuration the input voltage is compared with the feedback voltage coming from the sense resistor, then the difference between this two signals is amplified by the error amplifier in order to have an error signal controlling the duty cycle of the output stage keeping the load current under control.

It is clear that to have a good performance of the current control loop, the error amplifier must have an high DC gain and a large bandwidth.

Gain and bandwidth must be chosen depending on many parameters of the application, like the characteristics of the load, power supply etc..., and most important is the stability of the system that must always be guaranteed.

To have a very flexible system and to have the possibility to adapt the system to any application, the error amplifier must be compensated using an RC network connected between the output and the negative input of the same.

For the evaluation of the stability of the system, we have to consider the open loop gain of the current control loop:

$$Aloop = ACerr \cdot ACpw \cdot ACload \cdot ACsense$$

where AC... is the gain of the blocks that refers to the error, power and sense amplifier plus the attenuation of the load block.

The same formula in dB can be written in this way:

$$Aloop_{dB} = ACerr_{dB} + ACpw_{dB} + ACload_{dB} + ACsense_{dB}$$

So now we can start to analyse the dynamic characteristics of each single block, with particular attention to the error amplifier.

3.2 Power amplifier

The power amplifier is not a linear amplifier, but is a circuit driving in PWM mode the output stage in full bridge configuration.

The output duty cycle variation is given by the comparison between the voltage of the error amplifier and two triangular wave references Tri_0 and Tri_180. Because all the current control loop is referred to the Vr reference, the result is that when the output voltage of the error amplifier is equal to the Vr voltage the two output Out_A and Out_B have the same phase and duty cycle at 50%; increasing the output voltage of the error amplifier above the Vr voltage, the duty cycle of the Out_A increases and the duty cycle of the Out_B decreases of the same percentage; on the contrary decreasing the voltage of the error amplifier below the Vr voltage, the duty cycle of the Out_A decreases and the duty cycle of the Out_B increases of the same percentage.

The gain of this block is defined by the amplitude of the two triangular wave references; more precisely the gain of the power amplifier block is a reversed proportion of the amplitude of the two references.

In fact a variation of the error amplifier output voltage produces a larger variation in duty cycle of the two outputs Out_A and Out_B in case of low amplitude of the two triangular wave references.

The duty cycle has the max value of 100% when the input voltage is equal to the amplitude of the two triangular references.

The transfer function of this block consist in the relation between the output duty cycle and the amplitude of the triangular references.

$$Vout = 2 \cdot V_S \cdot (0.5 - DutyCycle)$$

$$ACpw_{dB} = 20 \cdot \log \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{2 \cdot V_S}{\text{Triangular Amplitude}}$$

$$ACpw|_{dB} = 20 \cdot \log\frac{2 \cdot 24}{1.6} = 29.5dB$$

Moreover, having the two references Tri_0 and Tri_180 a triangular shape it is clear that the transfer function of this block is a linear constant gain without poles and zeros.

3.3 Load attenuation

The load block is composed by the equivalent circuit of the motor winding (resistance and inductance) plus the sense resistor.

We will considered the effect of the Bemf voltage of the motor in the next chapter.

The input of this block is the PWM voltage of the power amplifier and as output we have the voltage across the sense resistor produced by the current flowing into the motor winding. The relation between the two variable is:

$$V_{sense} = \frac{V_{out}}{R_L + R_S} \cdot R_S$$

so the gain of this block is:

$$ACload = \frac{V_{sense}}{v_{out}} = \frac{R_S}{R_L + R_S}$$

$$ACload_{dB} = 20 \cdot \log\frac{R_S}{R_L + R_S}$$

$$Aload_{dB} = 20 \cdot \log\frac{0.33}{12 + 0.33} = -31.4dB$$

where:

R_L = equivalent resistance of the motor winding
R_S = sense resistor

Because of the inductance of the motor L_L, the load has a pole at the frequency:

$$Fpole = \frac{1}{2\pi \cdot \frac{L_L}{R_L + R_S}}$$

$$Fpole = \frac{1}{6.28 \cdot \frac{12 \cdot 10^{-3}}{12 + 0.33}} = 163Hz$$

Before analysing the error amplifier block and the sense transconductance block, we have to do this consideration:

$Aloop_{dB} = Ax_{dB} + Bx_{dB}$

$Ax|_{dB} = ACpw|_{dB} + ACload|_{dB}$

and

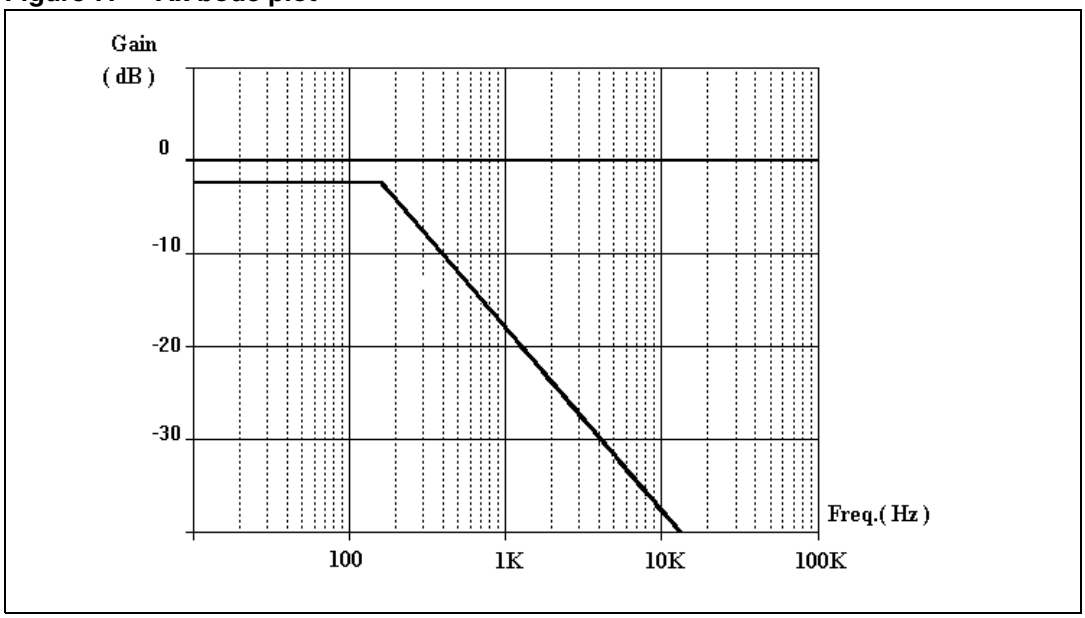
$Bx|_{dB} = ACerr|_{dB} + ACsense|_{dB}$

this means that Ax|dB is the sum of the power amplifier and load blocks;

$Ax|_{dB} = (29,5) + (-31.4) = -1.9dB$

The BODE analysis of the transfer function of Ax is:

Figure 7. Ax bode plot



The Bode plot of the Ax|dB function shows a DC gain of -1.9dB and a pole at 163Hz.

It is clear now that (because of the negative gain of the Ax function), Bx function must have an high DC gain in order to increment the total open loop gain increasing the bandwidth too.

3.4 Error amplifier and sense amplifier

As explained before the gain of these two blocks is:

$Bx_{dB} = ACerr_{dB} + ACsense_{dB}$

Being the voltage across the sense resistor the input of the Bx block and the error amplifier voltage the output of the same, the voltage gain is given by:

$$ib = Vsense \cdot Gs = Vsense \cdot \frac{1}{Rb}$$

$$Verr_out = -(ic \cdot Zc) \text{ so } ic = -(Verr_out \cdot \frac{1}{Zc})$$

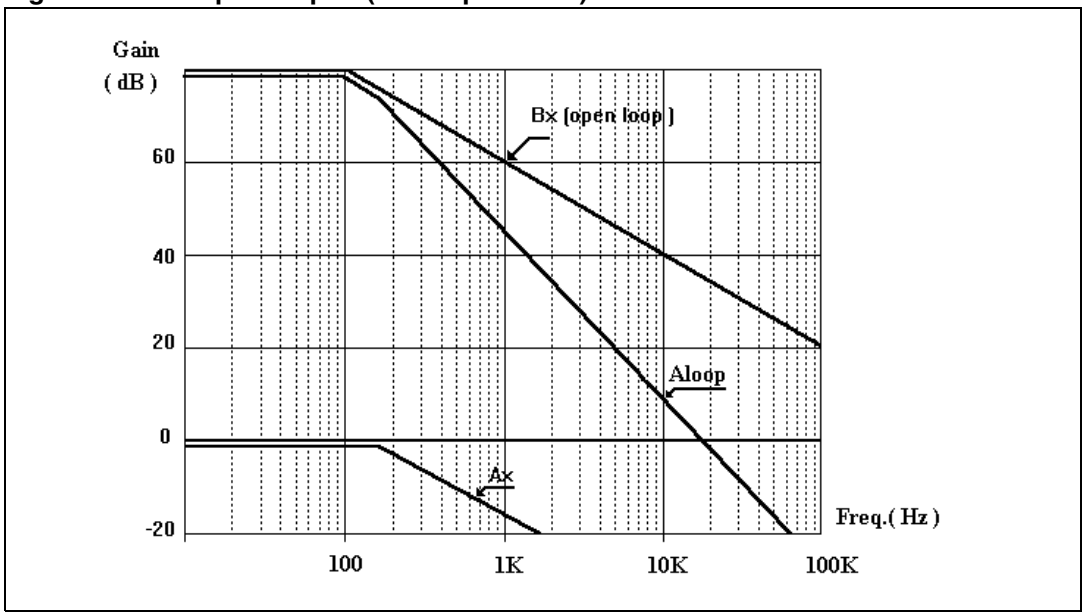
because ib = icwe have:

$$Vsense \cdot \frac{1}{Rb} = -(Verr_out \cdot \frac{1}{Zc})$$

$$Bx = -\frac{Verr_out}{Vsense} = -\frac{Zc}{Rb}$$

In the case of no external RC network is used to compensate the error amplifier, the typical open loop transfer function of the error plus the sense amplifier is something with a gain around 80dB and a unity gain bandwidth at 400kHz. In this case the situation of the total transfer function Aloop, given by the sum of the Ax_{dB} and Bx_{dB} is:

Figure 8. Aloop bode plot (uncompensated)



The BODE diagram shows together the error amplifier open loop transfer function, the Ax function and the resultant total Aloop given by the following equation:

$$Aloop_{dB} = AxdB + Bx_{dB}$$

The total Aloop has an high DC gain of 78.1dB with a bandwidth of 15KHz, but the problem in this case is the stability of the system; in fact the total Aloop cross the zero dB axis with a slope of -40dB/decade.

Now it is necessary to compensate the error amplifier in order to obtain a total Aloop with an high DC gain and a large bandwidth. Aloop must have enough phase margin to guarantee the stability of the system.

A method to reach the stability of the system, using the RC network showed in the block diagram, is to cancel the load pole with the zero given by the compensation of the error amplifier.

The transfer function of the Bx block with the compensation on the error amplifier is:

$$Bx = -\frac{Zc}{Rb} = -\frac{Rc - j\frac{1}{2\pi \cdot f \cdot Cc}}{Rb}$$

In this case the Bx block has a DC gain equal to the open loop and equal to zero at a frequency given by the following formula:

$$Fzero = \frac{1}{2\pi \cdot Rc \cdot Cc}$$

In order to cancel the pole of the load, the zero of the Bx block must be located at the same frequency of 163Hz; so now we have to find a compromise between the resistor and the capacitor of the compensation network.

Considering that the resistor value defines the gain of the Bx block at the zero frequency, it is clear that this parameter will influence the total bandwidth of the system because, annulling the load pole with the error amplifier zero, the slope of the total transfer function is -20dB/decade.

So the resistor value must be chosen in order to have an error amplifier gain enough to guarantee a desired total bandwidth.

In our example we fix at 35dB the gain of the Bx block at zero frequency, so from the formula:

$$Bx_gain_{@\ zero\ freq.} = 20 \cdot \log\frac{Rc}{Rb}$$

where: Rb = 20kΩ

we have: Rc = 1.1MΩ

Therefore we have the zero with a 163Hz the capacitor value:

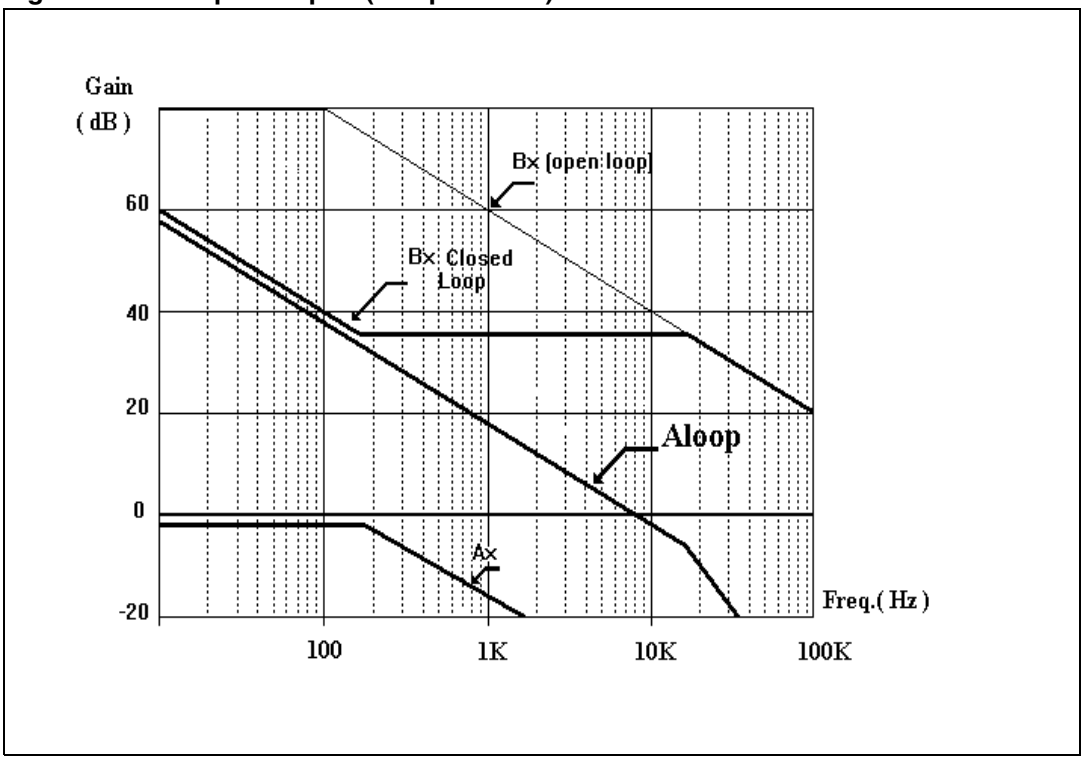
$$Cc = \frac{1}{2\pi \cdot Fzero \cdot Rc} = \frac{1}{6.28 \cdot 163 \cdot 1.1 \cdot 10^{-6}} = 880pF$$

Now we have to analyse how the new Aloop transfer function with a compensation network on the error amplifier is.

The following bode diagram shows:

- the Ax function showing the position of the load pole
- the open loop transfer function of the Bx block
- the transfer function of the Bx with the RC compensation network on the error amplifier
- the total Aloop transfer function that is the sum of the Ax function plus the transfer function of the compensated Bx block.

Figure 9. Aloop bode plot (compensated)



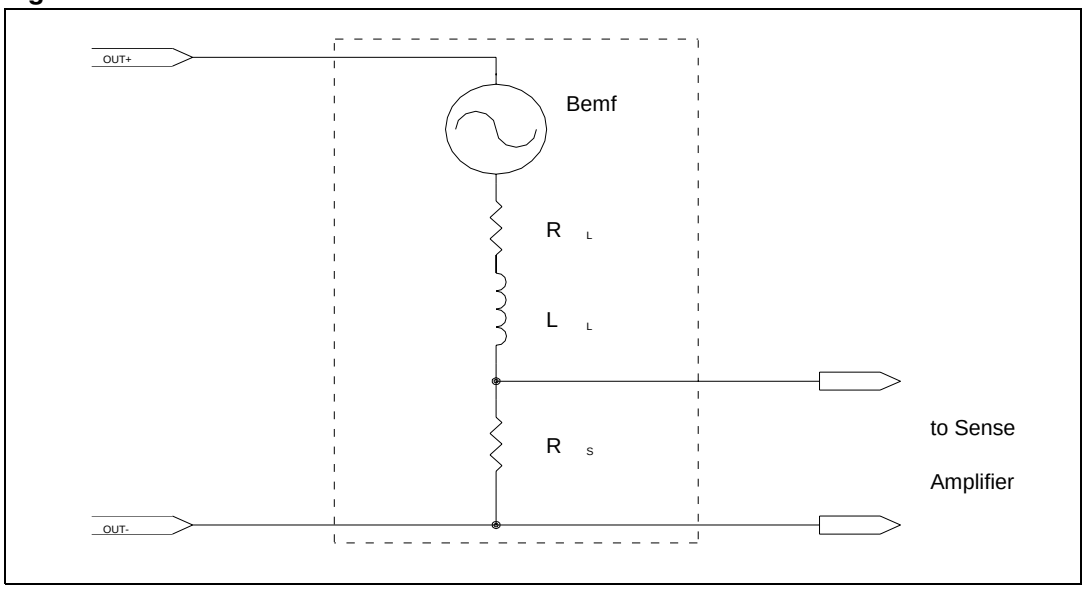
We can see that the effect of the load pole is cancelled by the zero of the Bx block ; the total Aloop cross a the 0dB axis with a slope of -20dB/decade, having in this way a stable system with an high gain at low frequency and a bandwidth of around 8KHz.

To increase the bandwidth of the system, we should increase the gain of the Bx block, keeping the zero in the same position. In this way the result is a shift of the total Aloop transfer function up to a greater value.

3.5 Effect of the Bemf on the current control loop stability

In order to evaluate what is the effect of the Bemf voltage of the stepper motor we have to look at the load block:

Figure 10. Electrical model of the load



The schematic now shows the equivalent circuit of the stepper motor including a sine wave voltage generator of the Bemf. The Bemf voltage of the motor is not constant, its value changes depending on the speed of the motor.

Increasing the motor speed the Bemf voltage increases:

$Bemf = Kt \cdot \omega$

where:

Kt is the motor constant

ω is the motor speed in radiant per second

The formula defining the gain of the load considering the Bemf of the stepper motor becomes:

$$ACload = \frac{Vsense}{Vout} = \frac{(V_S - Bemf) \cdot \frac{R_S}{R_L + R_S}}{V_S}$$

$$Acload = \frac{V_S - Bemf}{V_S} \cdot \frac{R_S}{R_L + R_S}$$

$$ACload_{dB} = 20 \cdot \log\left(\frac{V_S - Bemf}{V_S} \cdot \frac{R_S}{R_L + R_S}\right)$$

we can see that the Bemf influences only the gain of the load block and does not introduce any other additional pole or zero, so from the stability point of view the effect of the Bemf of the motor is not critical because the phase margin remains the same.
Practically the only effect of the Bemf is to limit the gain of the total Aloop with a consequent variation of the bandwidth of the system.

4 Application information

A typical application circuit is shown in *Figure 11*.

Note: For avoid current spikes on falling edge of DISABLE a "DC feedback" would be added to the ERROR Amplifier. (R1-R2 on Figure 11).

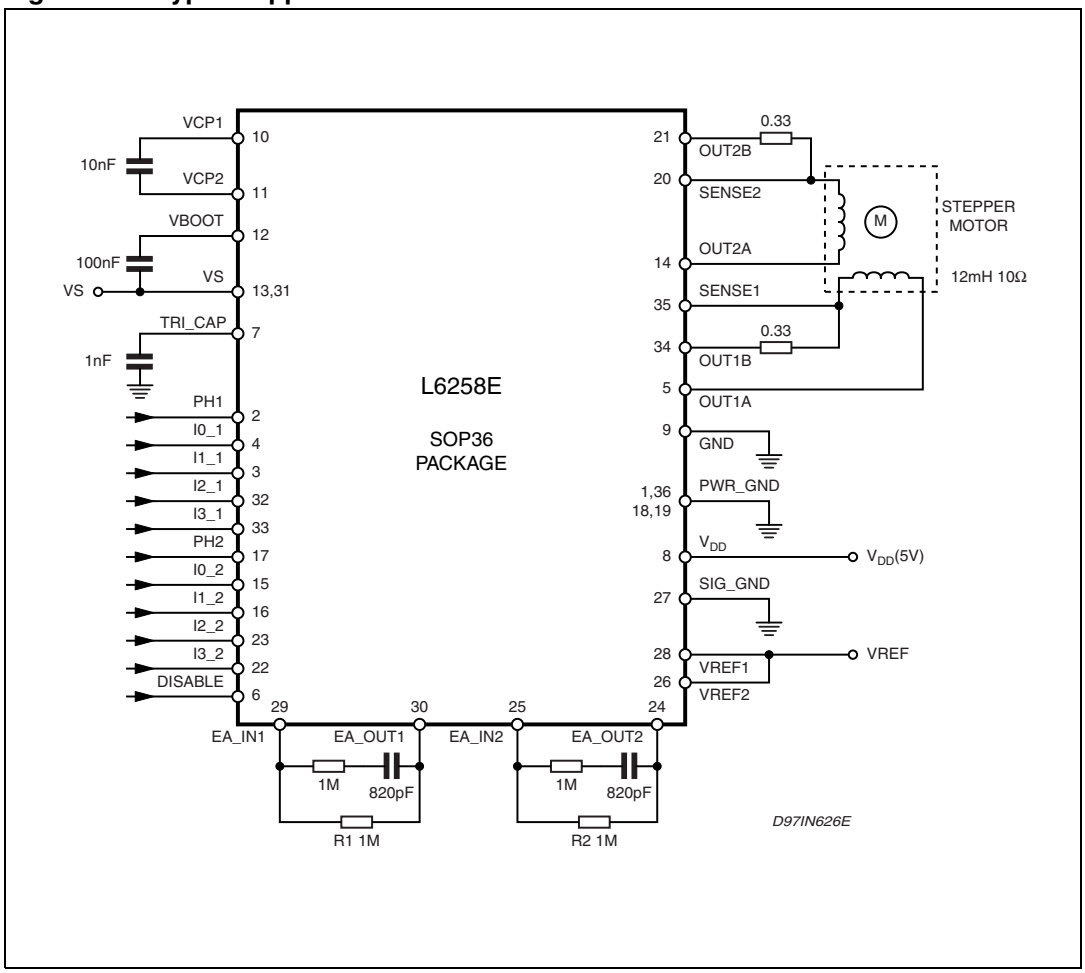
4.1 Interference

Due to the fact that the circuit operates with switch mode current regulation, to reduce the effect of the wiring inductance a good capacitor (100nF) can be placed on the board near the package, between the power supply line (pin 13,31) and the power ground (pin 1,36,18,19) to absorb the small amount of inductive energy.
It should be noted that this capacitor is usually required in addition to an electrolytic capacitor, that has poor performance at the high frequencies, always located near the package, between power supply voltage (pin 13,31) and power ground (pin 1,36,18,19), just to have a current recirculation path during the fast current decay or during the phase change.
The range value of this capacitor is between few µF and 100µF, and it must be chosen depending on application parameters like the motor inductance and load current amplitude.
A decoupling capacitor of 100nF is suggested also between the logic supply and ground.

The EA_IN1 and EA_IN2 pins carry out high impedance lines and care must be taken to avoid coupled noise on this signals. The suggestion is to put the components connected to this pins close to the L6258E, to surround them with ground tracks and to keep as far as possible fast switching outputs of the device. Remember also an 1 Mohm resistor between EA_INx and EA_OUTx to avoid output current spike during supply startup/shutdown.
A non inductive resistor is the best way to implement the sensing. Whether this is not possible, some metal film resistor of the same value can be paralleled.
The two inputs for the sensing of the winding motor current (SENSE_A & SENSE_B) should be connected directly on the sensing resistor Rs terminals, and the path lead between the Rs and the two sensing inputs should be as short as possible.

Note: Connect the DISABLE pin to a low impedance (< 300 Ω) voltage source to reduce at minimum the interference on the output current due to capacitive coupling of OUT1A (pin5) and DISABLE (pin 6).

Figure 11. Typical application circuit



4.2 Motor selection

Some stepper motor have such high core losses that they are not suitable for switch mode current regulation. Furthermore, some stepper motors are not designed for continuous operating at maximum current. Since the circuit can drive a constant current through the motor, its temperature might exceed, both at low and high speed operation.

4.3 Unused inputs

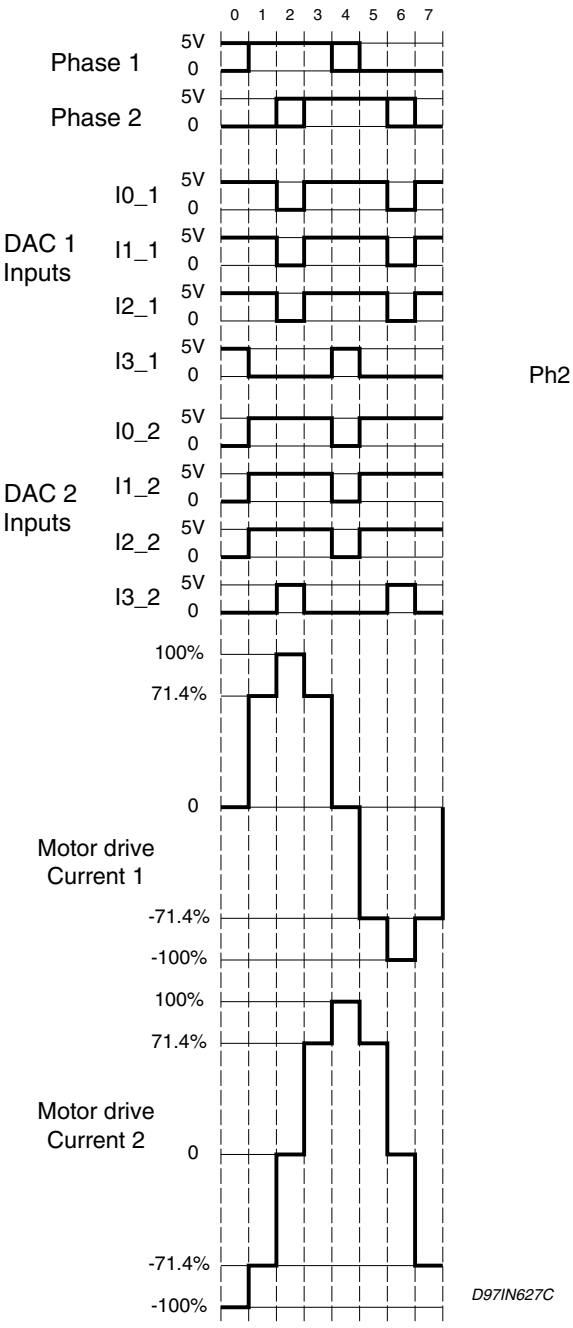
Unused inputs should be connected to the proper voltage levels in order to get the highest noise immunity.

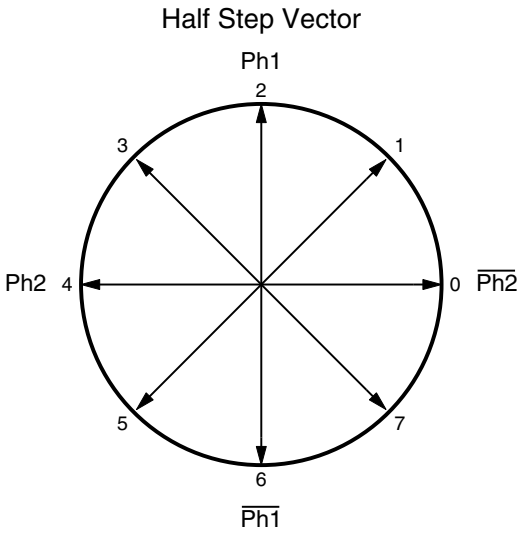
4.4 Notes on PCB design

We recommend to observe the following layout rules to avoid application problems with ground and anomalous recirculation current.
The by-pass capacitors for the power and logic supply must be kept as near as possible to the IC.
It's important to separate on the PCB board the logic and power grounds and the internal charge pump circuit ground avoiding that ground traces of the logic signals cross the ground traces of the power signals.
Because the IC uses the board as a heat sink, the dissipating copper area must be sized in accordance with the required value of $R_{thj\text{-}amb}$.

5 Operation mode time diagrams

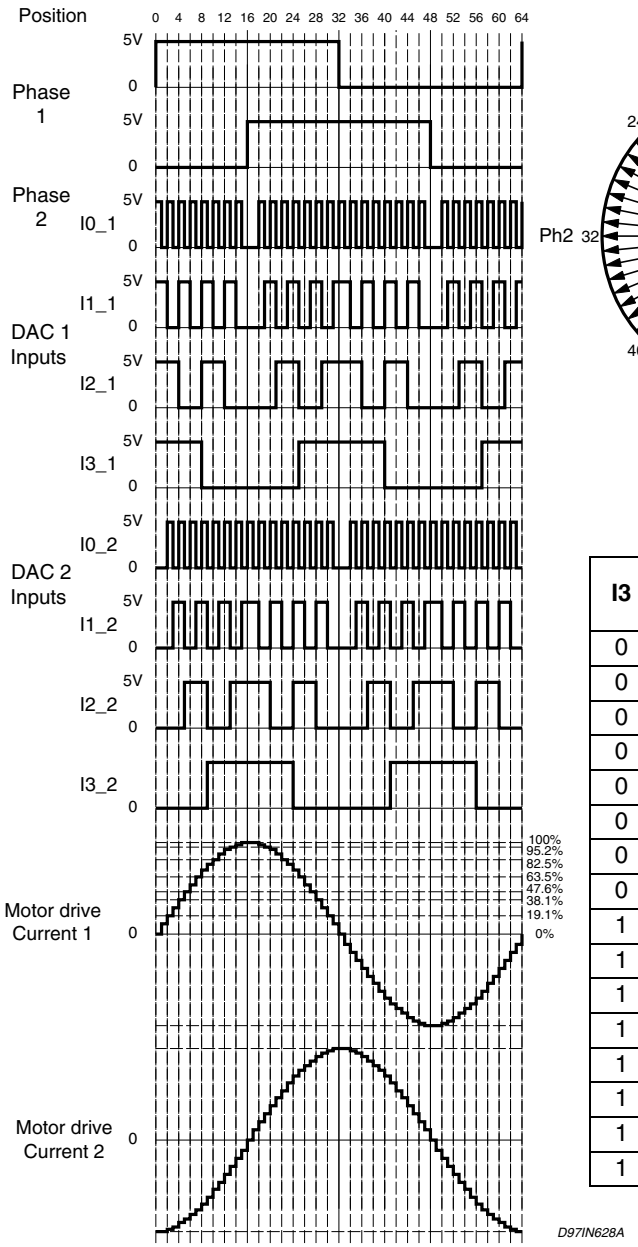
Figure 12. Half step operation mode timing diagram
(Phase - DAC input and motor current)

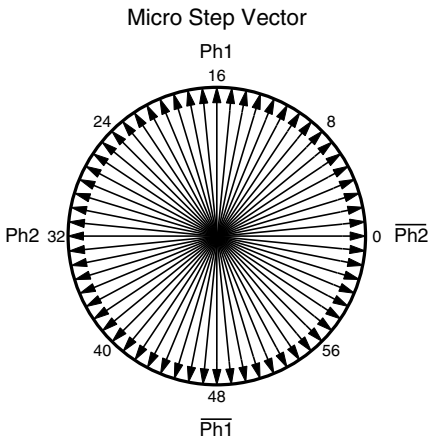




I3	I2	I1	I0	Current level% of I_{MAX}
0	0	0	0	100
0	0	0	1	98.4
0	0	1	0	95.2
0	0	1	1	92.1
0	1	0	0	88.9
0	1	0	1	82.5
0	1	1	0	77.8
0	1	1	1	71.4
1	0	0	0	63.5
1	0	0	1	55.6
1	0	1	0	47.6
1	0	1	1	38.1
1	1	0	0	28.6
1	1	0	1	19.1
1	1	1	0	9.5
1	1	1	1	No Current

Figure 13. 4 bit microstep operation mode timing diagram
(Phase - DAC input and motor current)





I3	I2	I1	I0	Current level% of I_{MAX}
0	0	0	0	100
0	0	0	1	98.4
0	0	1	0	95.2
0	0	1	1	92.1
0	1	0	0	88.9
0	1	0	1	82.5
0	1	1	0	77.8
0	1	1	1	71.4
1	0	0	0	63.5
1	0	0	1	55.6
1	0	1	0	47.6
1	0	1	1	38.1
1	1	0	0	28.6
1	1	0	1	19.1
1	1	1	0	9.5
1	1	1	1	No Current

6 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

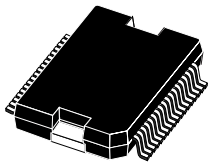
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 14. PowerSO36 mechanical data & package dimensions

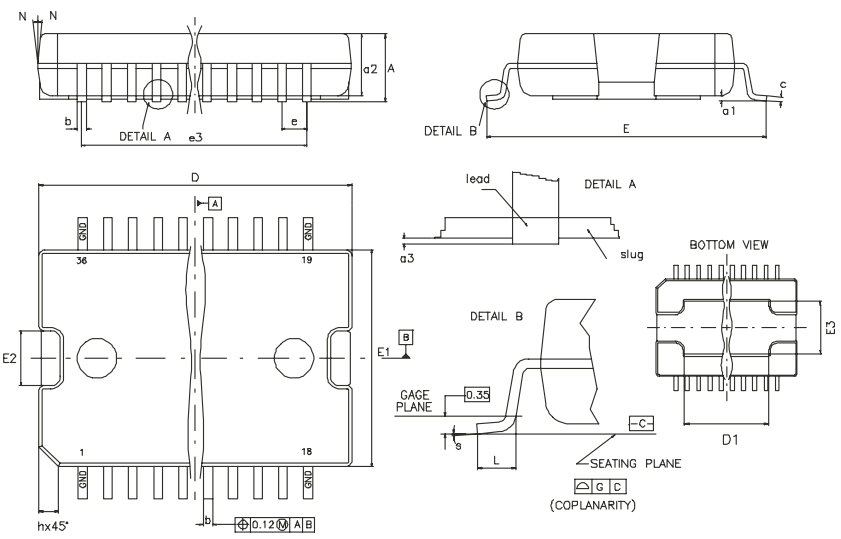
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10			0.0039
b	0.22		0.38	0.0087		0.0150
c	0.23		0.32	0.0091		0.0126
D	15.80		16.00	0.6220		0.6299
D1	9.40		9.80	0.3701		0.3858
E	13.90		14.5	0.5472		0.5709
E1	10.90		11.10	0.4291		0.4370
E2			2.90			0.1142
E3	5.80		6.20	0.2283		0.2441
e		0.65			0.0256	
e3		11.05			0.4350	
G	0		0.10			0.0039
H	15.50		15.90	0.6102		0.6260
h			1.10			0.0433
L	0.8		1.10	0.0315		0.0433
N	10° (max)					
s	8° (max)					

Note: "D and E1" do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006")
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA



PowerSO-36



7 Revision history

Table 7. Document revision history

Date	Revision	Changes
28-Jan-2004	5	First Issue in EDOCS DMS
11-May-2004	6	Restyling of the graphic form, changed all V_{CC} with V_{DD}; delete TSD parameter in the Electrical characteristic on *Table 4*. NOT FOR NEW DESIGN, it has been replaced by equivalent L6258EX.
24-Sep-2004	7	Changed on the page 5 the f_{osc} parameter max. value from 17.5 to 18.5kHz
03-Dec-2007	8	Document reformatted. Modified the ACpw formula in *Section 3.2 on page 17*. Added the disable note in *Section 4.1 on page 24*

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