2.7V to 5.5V Input, 6A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9A600MUV

General Description

BD9A600MUV is a synchronous buck switching regulator with built-in low on-resistance power MOSFETs. It is capable of providing current up to 6A.The SLLM™ control provides excellent efficiency characteristics in light-load conditions which make the product ideal for equipment and devices that demand minimal standby power consumption. The oscillating frequency is high at 1MHz using a small value of inductance. It is a current mode control DC/DC converter and features high-speed transient response. Phase compensation can also be set easily.

Key Specifications

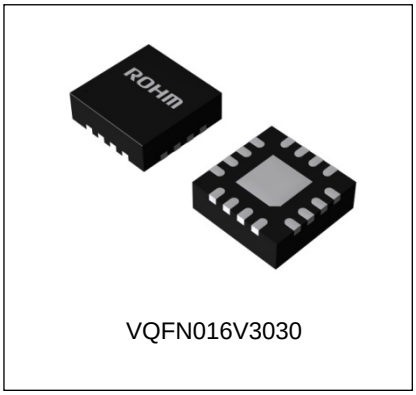
- Input Voltage Range : 2.7V to 5.5V
- Output Voltage Range : 0.8V to V_{PVIN} x 0.7V
- Average Output Current : 6A(Max)
- Switching Frequency : 1MHz(Typ)
- High-Side MOSFET On-Resistance : 25mΩ(Typ)
- Low-Side MOSFET On-Resistance : 25mΩ(Typ)
- Standby Current : 0μA(Typ)

Package

	W(Typ) x D(Typ) x H(Max)
VQFN016V3030	3.00mm x 3.00mm x 1.00mm

Features

- Synchronous Single DC/DC Converter.
- SLLM™ (Simple Light Load Mode)Control.
- Over Current Protection.
- Short Circuit Protection.
- Thermal Shutdown Protection.
- Under Voltage Lockout Protection.
- Adjustable Soft start Function.
- Power Good Output.
- VQFN016V3030 Package(Backside Heat Dissipation)



VQFN016V3030

Applications

- Step-down Power Supply for DSPs, FPGAs, Microprocessors, etc.
- Laptop PCs/ Tablet PCs/ Servers.
- LCD TVs.
- Storage Devices (HDDs/SSDs).
- Printers, OA Equipment.
- Entertainment Devices.
- Distributed Power Supply, Secondary Power Supply.

Typical Application Circuit

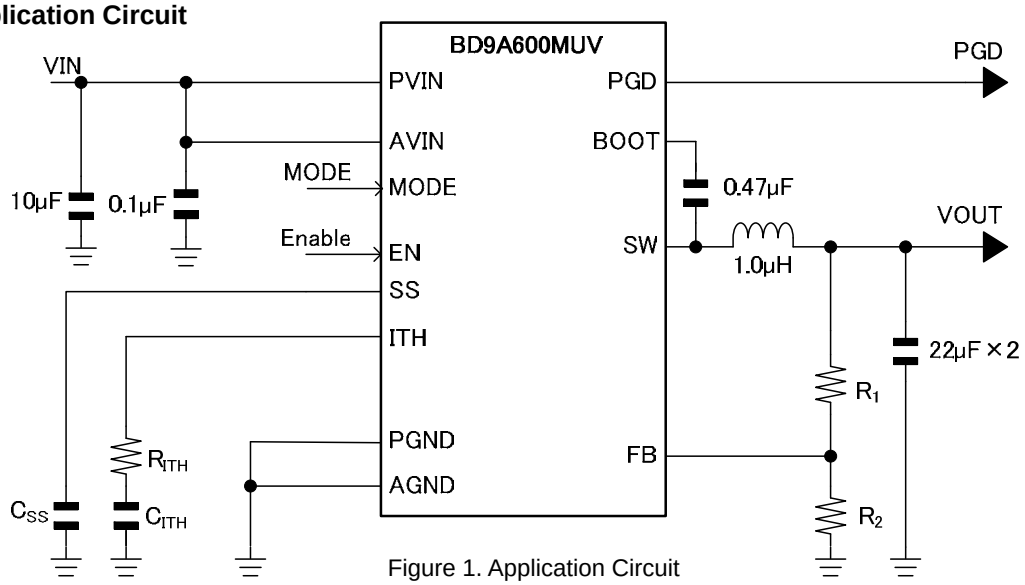


Figure 1. Application Circuit

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Pin Configuration

(TOP VIEW)

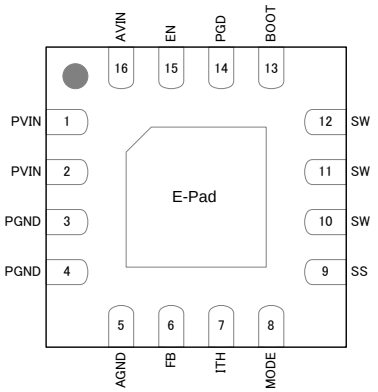


Figure 2. Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Function
1, 2	PVIN	Power supply terminals for the switching regulator. These terminals supply power to the output stage of the switching regulator. Connecting a 10µF ceramic capacitor is recommended.
3, 4	PGND	Ground terminals for the output stage of the switching regulator.
5	AGND	Ground terminal for the control circuit.
6	FB	An inverting input node for the gm error amplifier. See page 23 for how to calculate the resistance of the output voltage setting.
7	ITH	An input terminal for the gm error amplifier output and the output switch current comparator. Connect a frequency phase compensation component to this terminal. See page 24 for how to calculate the resistance and capacitance for phase compensation.
8	MODE	Turning this terminal signal Low (0.2V or lower) forces the device to operate in the fixed frequency PWM mode. Turning this terminal signal High (0.8V or higher) enables the SLLM control and the mode is automatically switched between the SLLM control and fixed frequency PWM mode.
9	SS	Terminal for setting the soft start time. The rise time of the output voltage can be specified by connecting a capacitor to this terminal. See page 23 for how to calculate the capacitance.
10, 11, 12	SW	Switch nodes. These terminals are connected to the source of the high-side MOSFET and drain of the low-side MOSFET. Connect a bootstrap capacitor of 0.47µF between these terminals and BOOT terminals. In addition, connect an inductor of considering the direct current superimposition characteristic.
13	BOOT	Connect a bootstrap capacitor of 0.47µF between this terminal and SW terminals. The voltage of this capacitor is the gate drive voltage of the high-side MOSFET.
14	PGD	A “Power Good” terminal, an open drain output. Use of pull up resistor is needed. See page 18 for how to specify the resistance. When the FB terminal voltage reaches within ±7% of 0.8V (Typ), the internal Nch MOSFET turns off and the output turns High.
15	EN	Turning this terminal signal low (0.8V or lower) forces the device to enter the shutdown mode. Turning this terminal signal high (2.0V or higher) enables the device. This terminal must be terminated.
16	AVIN	Supplies power to the control circuit of the switching regulator. Connecting a 0.1µF ceramic capacitor is recommended.
-	E-Pad	A backside heat dissipation pad. Connecting to the internal PCB ground plane by using multiple vias provides excellent heat dissipation characteristics.

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Block Diagram

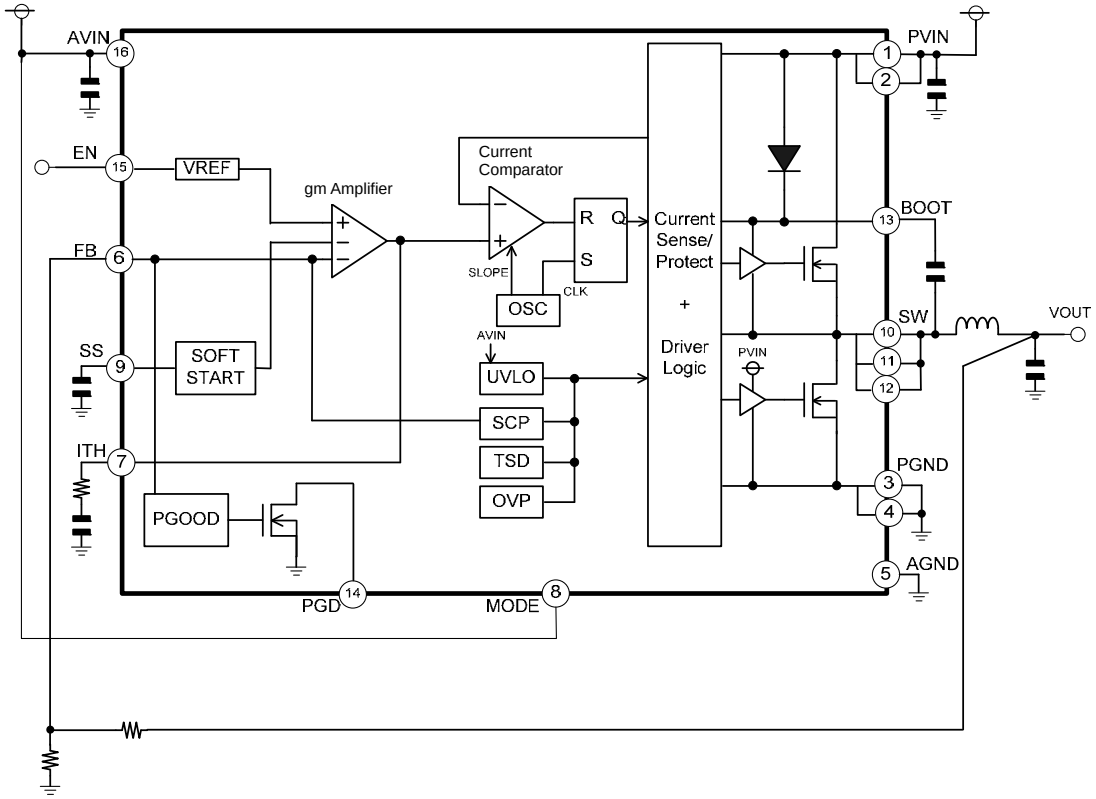


Figure 3. Block Diagram

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Description of Blocks

1. VREF
   The VREF block generates the internal reference voltage.

2. UVLO
   The UVLO block is for under voltage lockout protection. It will shut down the IC when the VIN falls to 2.45V (Typ) or lower. The threshold voltage has a hysteresis of 100mV (Typ).

3. SCP
   After the soft start is completed and when the feedback voltage of the output voltage has fallen below 0.4V (Typ) for 1msec (Typ), the SCP stops the operation for 16msec (Typ) and subsequently initiates restart.

4. OVP
   Over voltage protection function (OVP) compares FB terminal voltage with the internal standard voltage VREF. When the FB terminal voltage exceeds 0.88V (Typ) it turns MOSFET of output part MOSFET off. After output voltage drop it returns with hysteresis.

5. TSD
   The TSD block is for thermal protection. The thermal protection circuit shuts down the device when the internal temperature of IC rises to 175°C (Typ) or higher. Thermal protection circuit resets when the temperature falls. The circuit has a hysteresis of 25°C (Typ).

6. SOFT START
   The Soft Start circuit slows down the rise of output voltage during start-up and controls the current, which allows the prevention of output voltage overshoot and inrush current. A built-in soft start function is provided and a soft start is initiated in 1msec (Typ) when the SS terminal is open.

7. gm Amplifier
   The gm Amplifier block compares the reference voltage with the feedback voltage of the output voltage. The error and the ITH terminal voltage determine the switching duty. A soft start is applied at startup. The ITH terminal voltage is limited by the internal slope voltage.

8. Current Comparator
   The Current Comparator block compares the output ITH terminal voltage of the error amplifier and the slope block signal to determine the switching duty. In the event of over current, the current that flows through the high-side MOSFET is limited at each cycle of the switching frequency.

9. OSC
   This block generates the oscillating frequency.

10. DRIVER LOGIC
    This block is a DC/DC driver. A signal from current comparator is applied to drive the MOSFETs.

11. PGOOD
    When the FB terminal voltage reaches 0.8V (Typ) within ±7%, the Nch MOSFET of the built-in open drain output turns off and the output turns high.

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Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{PVIN}, V_{AVIN}	-0.3 to +7	V
EN Voltage	V_{EN}	-0.3 to +7	V
MODE Voltage	V_{MODE}	-0.3 to +7	V
PGD Voltage	V_{PGD}	-0.3 to +7	V
Voltage from GND to BOOT	V_{BOOT}	-0.3 to +14	V
Voltage from SW to BOOT	ΔV_{BOOT}	-0.3 to +7	V
FB Voltage	V_{FB}	-0.3 to +7	V
ITH Voltage	V_{ITH}	-0.3 to +7	V
SW Voltage	V_{SW}	-0.3 to V_{PVIN} + 0.3	V
Allowable Power Dissipation(Note 1)	Pd	2.66	W
Operating Temperature Range	Topr	-40 to 85	°C
Storage Temperature Range	Tstg	-55 to 150	°C

(Note 1) When mounted on a 70mm x 70mm x 1.6mm 4-layer glass epoxy board (copper foil area: 70 mm x 70 mm)
Derate by 21.3mW when operating above 25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= -40°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{PVIN}, V_{AVIN}	2.7	-	5.5	V
Output Current(Note 2)	I_{OUT}	-	-	6	A
Output Voltage Range	V_{RANGE}	0.8	-	V_{PVIN} × 0.7	V

(Note 2) Pd,ASO should not be exceeded.

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Electrical Characteristics (Unless otherwise specified Ta = 25°C, VAVIN = VPVIN = 5V, VEN = 5V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
AVIN PIN						
Standby Supply Current	I_{STB}	-	0	10	µA	EN= GND
Operating Supply Current	I_{CC}	-	400	600	µA	I_{OUT}= 0mA Non-switching
UVLO Detection Voltage	V_{UVLO1}	2.35	2.45	2.55	V	V_{IN} Falling
UVLO Release Voltage	V_{UVLO2}	2.425	2.55	2.7	V	V_{IN} Rising
ENABLE						
EN Input High Level Voltage	V_{ENH}	2.0	-	-	V	
EN Input Low Hysteresis Voltage	V_{ENL}	-	-	0.8	V	
EN Input Current	I_{EN}	-	5	10	µA	EN= 5V
MODE						
MODE Input High Level Voltage	V_{MODEH}	0.2	0.4	0.8	V	
MODE Input Current	I_{MODE}	-	10	20	µA	MODE= 5V
Reference Voltage, Error Amplifier						
FB Terminal Voltage	V_{FB}	0.792	0.8	0.808	V	
FB Input Current	I_{FB}	-	0	1	µA	FB= 0.8V
ITH Sink Current	I_{THSI}	10	20	40	µA	FB= 0.9V
ITH Source Current	I_{THSO}	10	20	40	µA	FB= 0.7V
Soft Start Time	T_{SS}	0.5	1.0	2.0	ms	With internal constant
Soft Start Current	I_{SS}	0.9	1.8	3.6	µA	
SWITCHING FREQUENCY						
Switching Frequency	F_{OSC}	800	1000	1200	kHz	
POWER GOOD						
Falling (Fault) Voltage	V_{PGDFF}	87	90	93	%	OUTPUT voltage falling
Rising (Good) Voltage	V_{PGDRG}	90	93	96	%	OUTPUT voltage rising
Rising (Fault) Voltage	V_{PGDRF}	107	110	113	%	OUTPUT voltage rising
Falling (Good) Voltage	V_{PGDFG}	104	107	110	%	OUTPUT voltage falling
PGD Output Leakage Current	I_{LKPGD}	-	0	5	µA	PGD= 5V
Power Good ON Resistance	R_{PGD}	-	50	100	Ω	
Power Good Low Level Voltage	P_{GDVL}	-	0.05	0.1	V	I_{PGD}= 1mA
SWITCH MOSFET						
High Side FET ON Resistance	R_{ONH}	-	25	50	mΩ	BOOT – SW= 5V
Low Side FET ON Resistance	R_{ONL}	-	25	50	mΩ	
High Side Output Leakage Current	R_{ILH}	-	0	10	µA	Non-switching
Low Side Output Leakage Current	R_{ILL}	-	0	10	µA	Non-switching
SCP						
Short Circuit Protection Detection Voltage	V_{SCP}	0.28	0.4	0.52	V	

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Typical Performance Curves

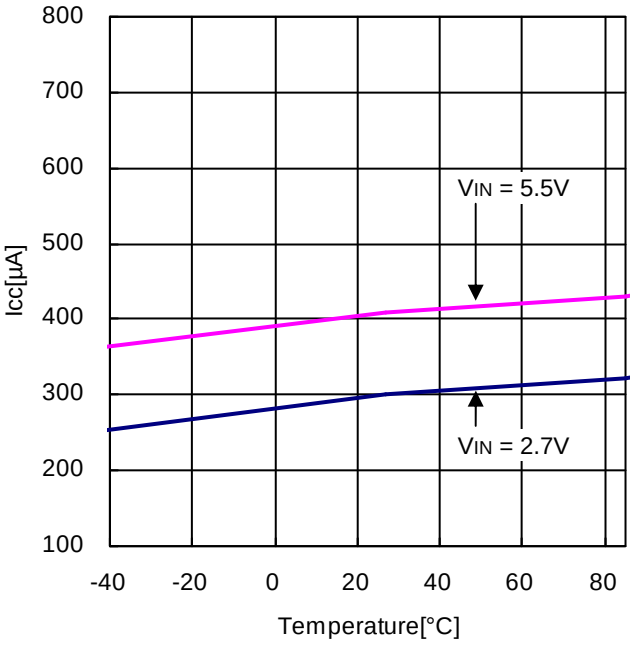


Figure 4. Operating Current vs Temperature

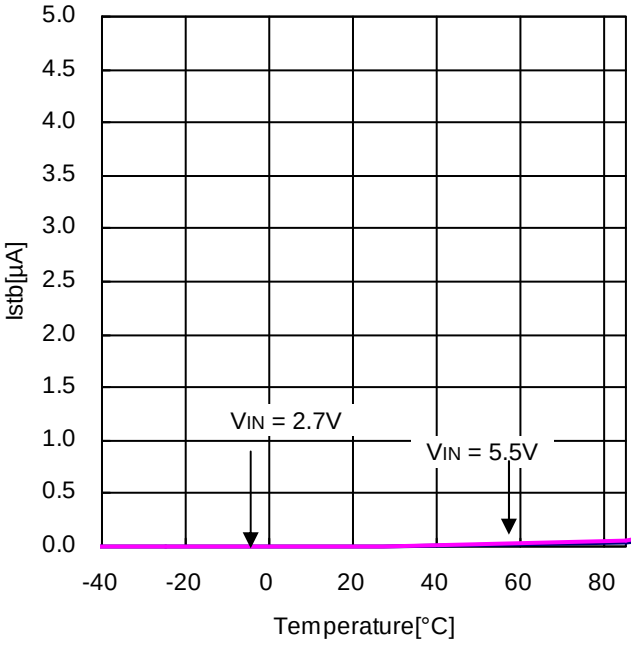


Figure 5. Stand-by Current vs Temperature

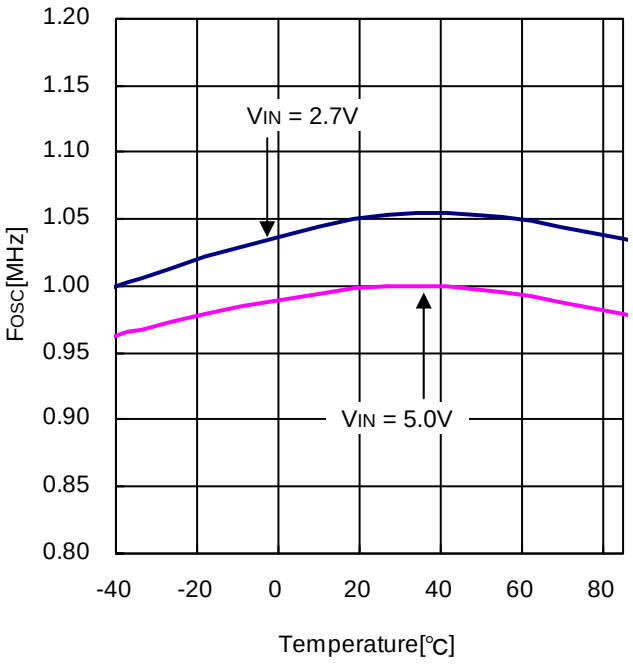


Figure 6. Switching Frequency vs Temperature

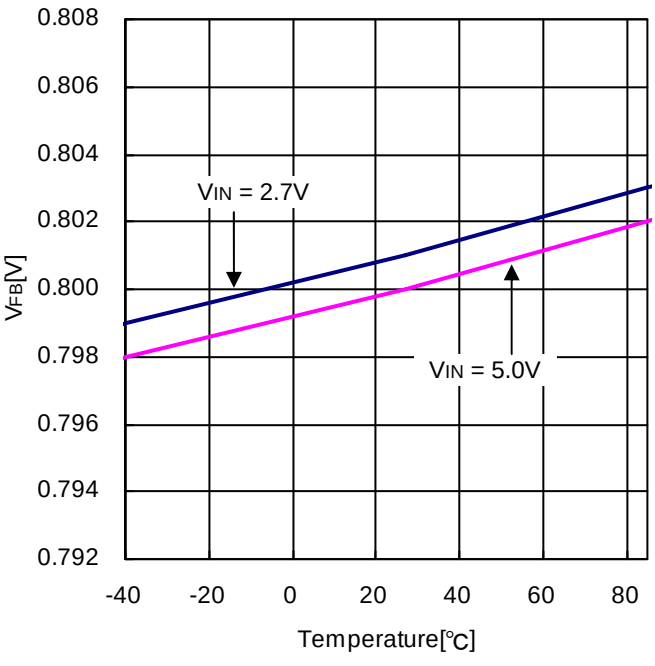


Figure 7. FB Voltage Reference vs Temperature

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Typical Performance Curves - continued

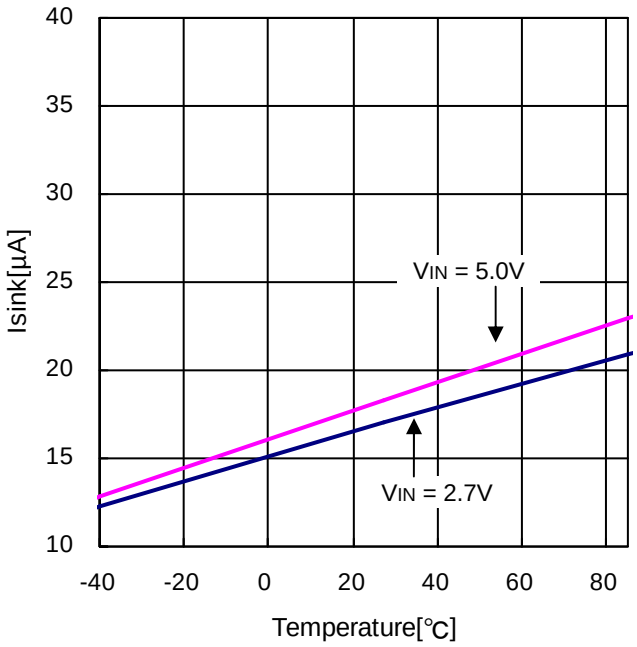


Figure 8. ITH Sink Current vs Temperature

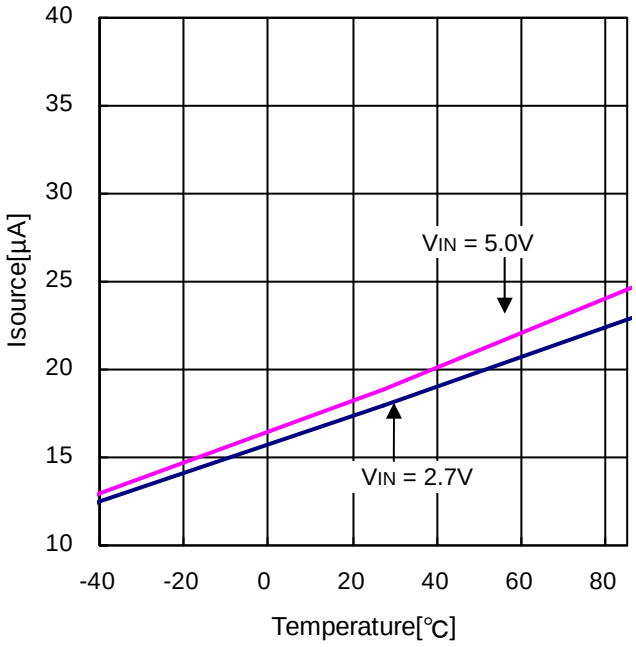


Figure 9. ITH Source Current vs Temperature

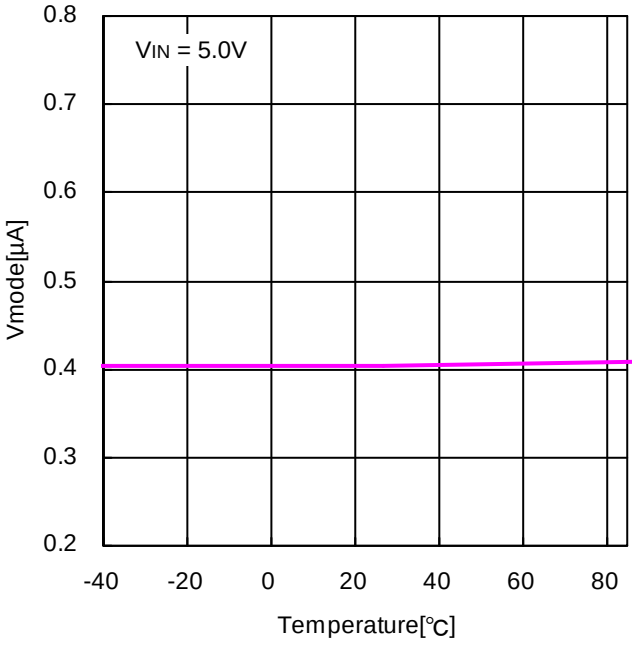


Figure 10. Mode Threshold vs Temperature

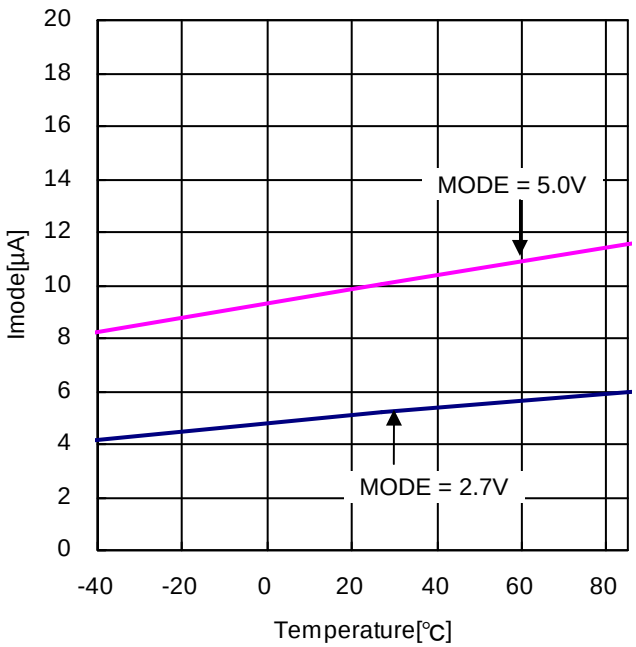


Figure 11. Mode Input Current vs Temperature

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Typical Performance Curves - continued

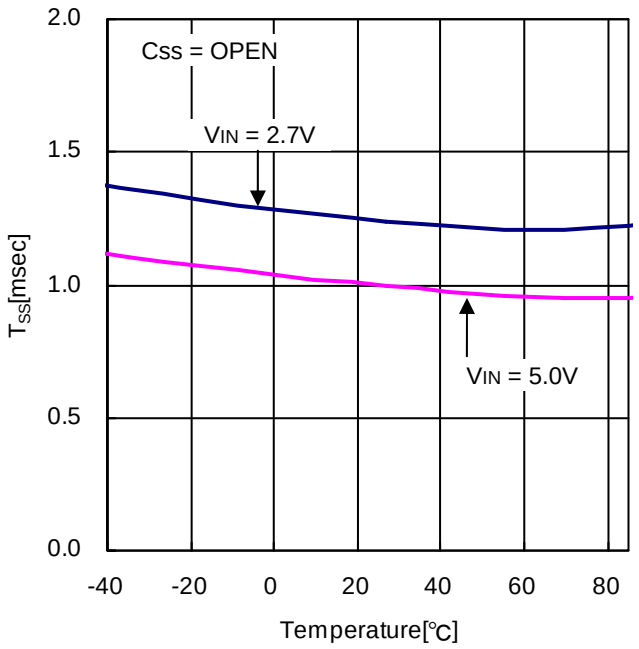


Figure 12. Soft Start Time vs Temperature

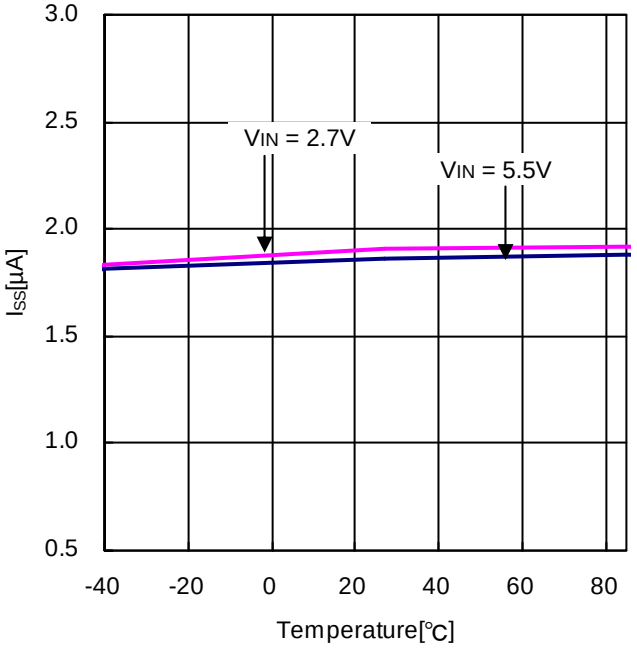


Figure 13. Soft Start Terminal Current vs Temperature

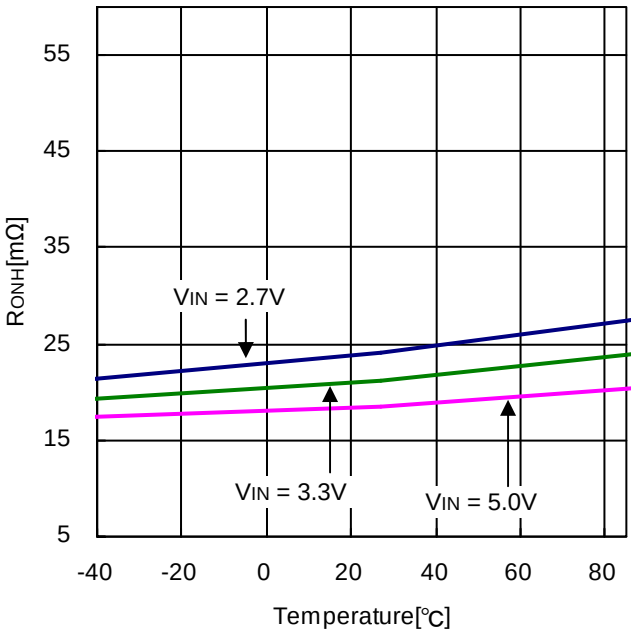


Figure 14. High-side FET ON-Resistance vs Temperature

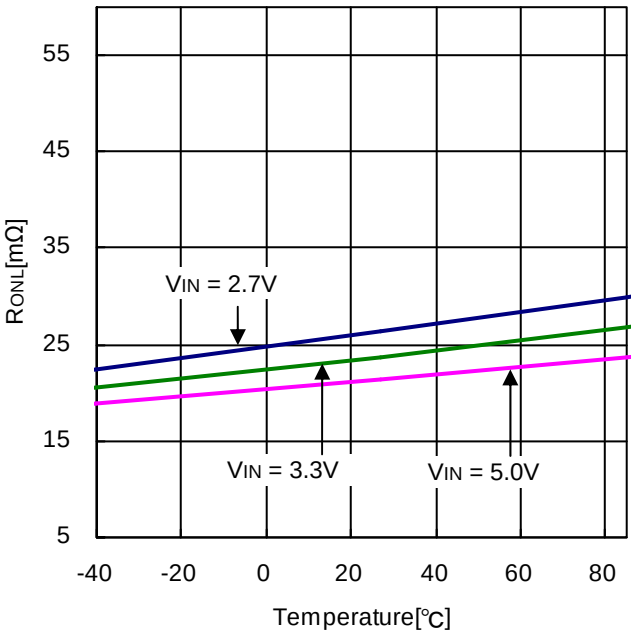


Figure 15. Low-side FET ON-Resistance vs Temperature

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Typical Performance Curves - continued

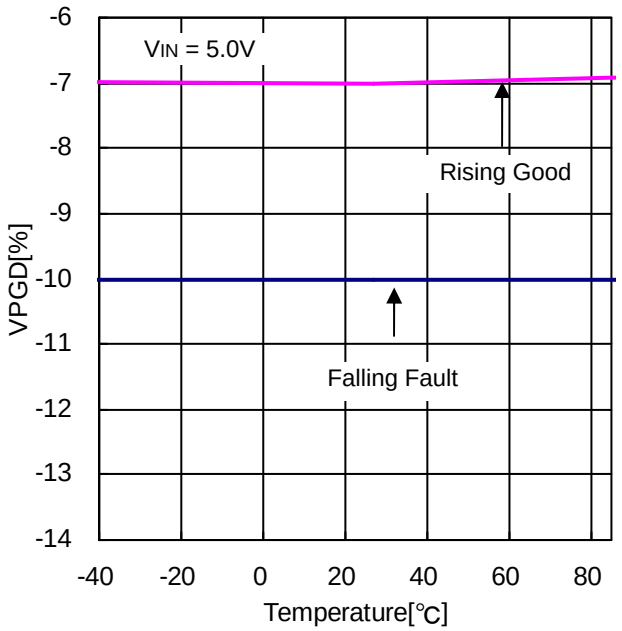


Figure 16. PGD Falling Voltage vs Temperature

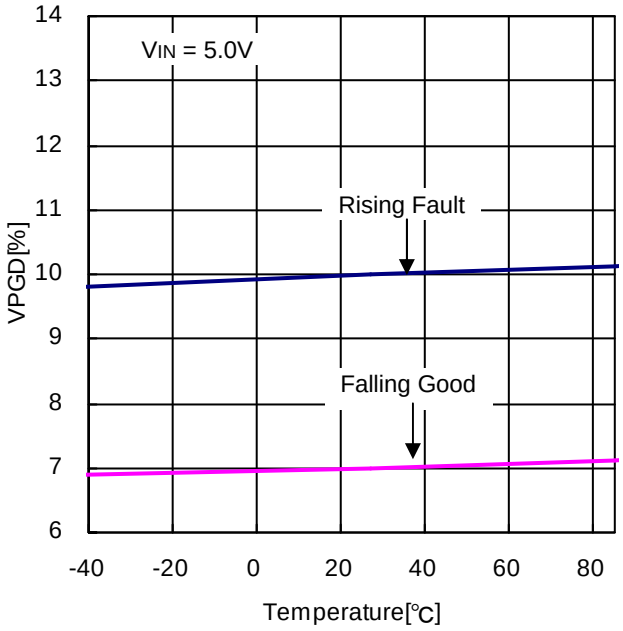


Figure 17. PGD Rising Voltage vs Temperature

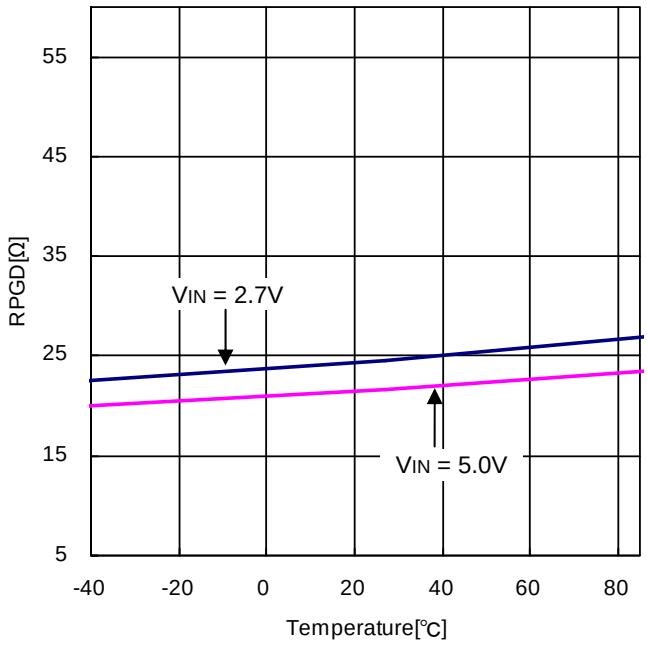


Figure 18. PGD ON-Resistance vs Temperature

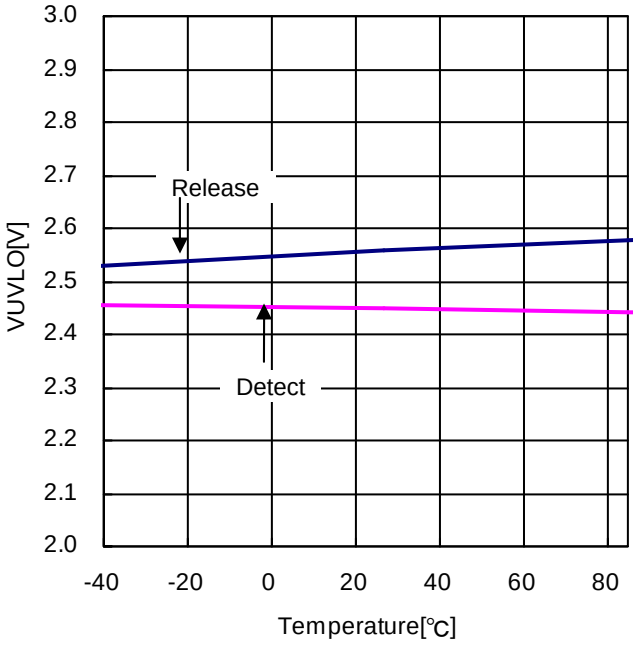


Figure 19. UVLO Threshold vs Temperature

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Typical Performance Curves - continued

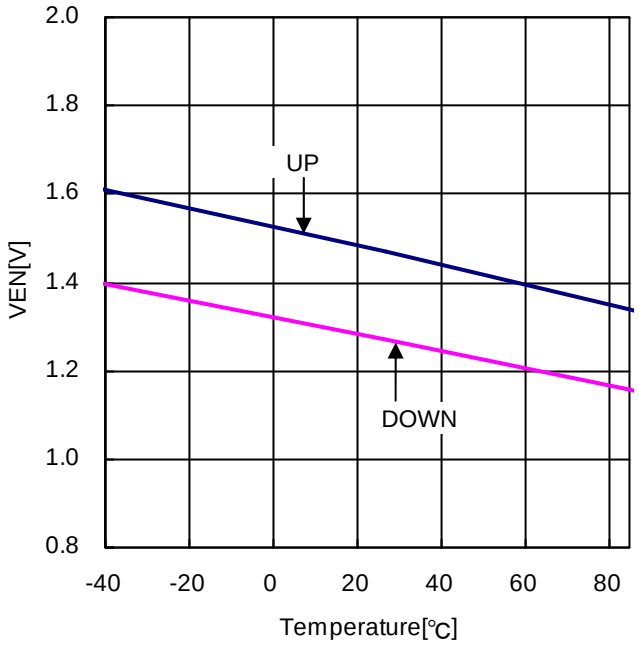


Figure 20. EN Threshold vs Temperature

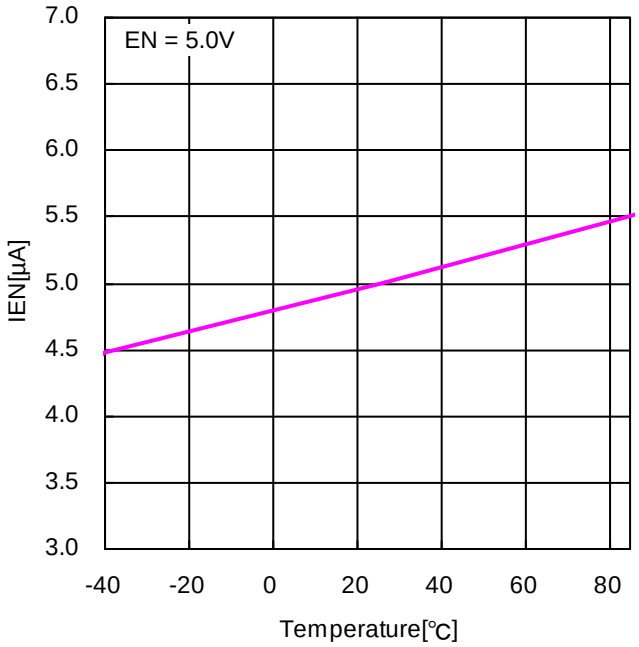


Figure 21. EN Input Current vs Temperature

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Typical Performance Curves (Application)

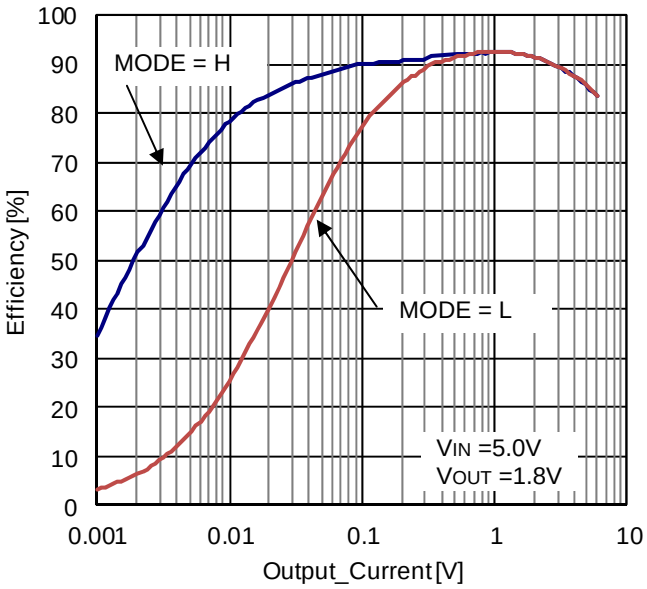


Figure 22. Efficiency vs Load Current
(VIN= 5V, VOUT= 1.8V, L= 1.5μH)

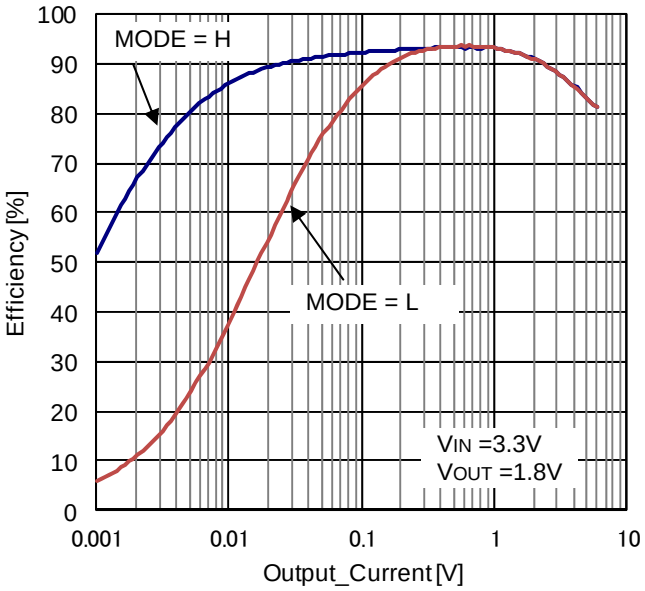


Figure 23. Efficiency vs Load Current
(VIN= 3.3V, VOUT= 1.8V, L= 1.0μH)

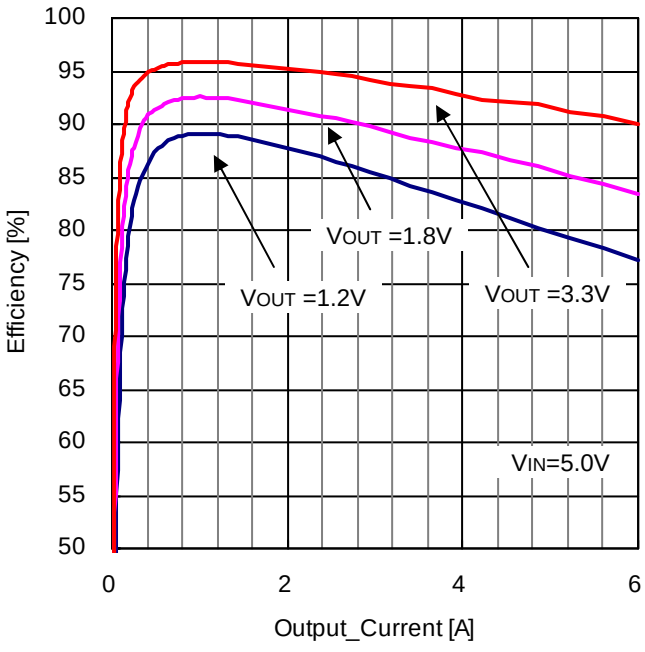


Figure 24. Efficiency vs Load Current
(VIN= 5.0V, MODE= 5.0V)

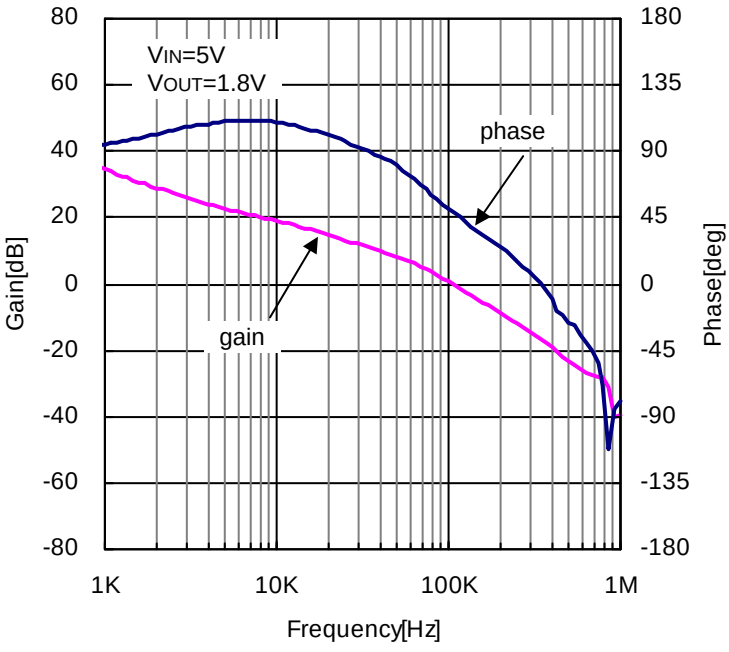


Figure 25. Closed Loop Response
(VIN=5V, VOUT=1.8V, IOUT=6A, L=1.5μH,
R3=6.8kΩ, C6=5600pF, C14=100pF)

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Typical Performance Curves (Application) - continued

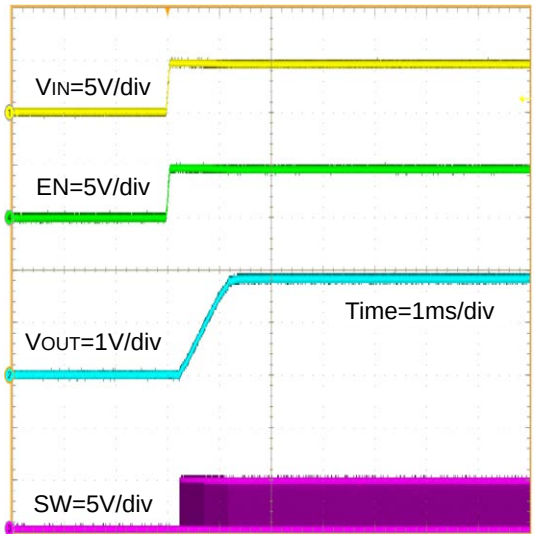


Figure 26. Power Up (VIN= EN)

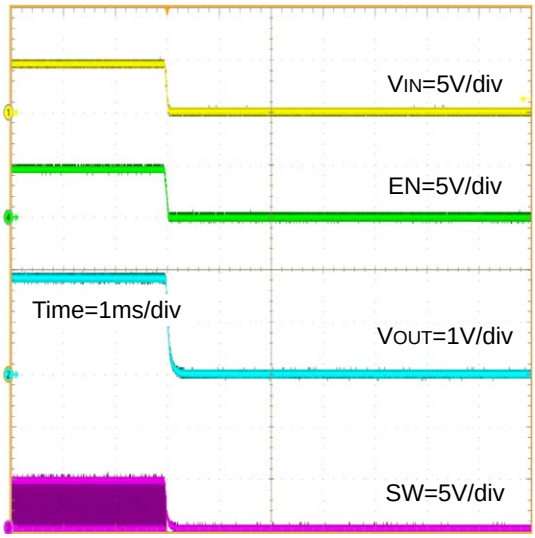


Figure 27. Power Down (VIN= EN)

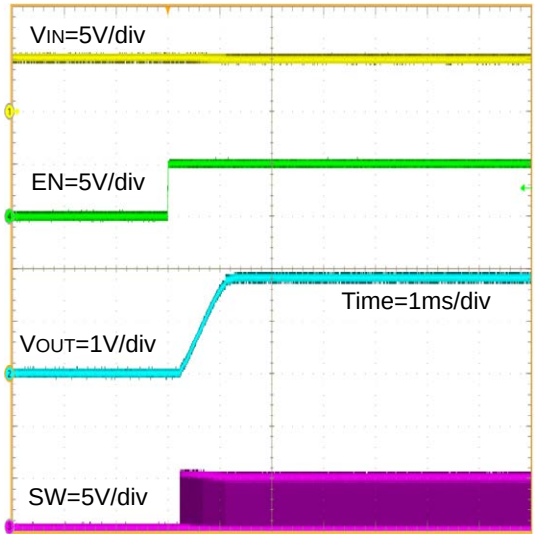


Figure 28. Power Up (EN= 0V→5V)

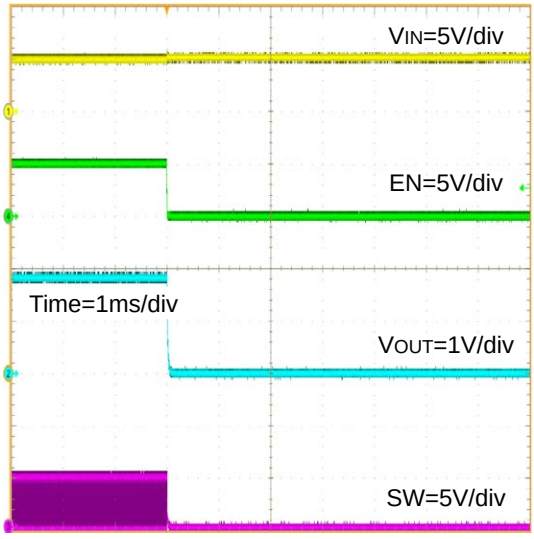


Figure 29. Power Down (EN= 5V→0V)

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Typical Performance Curves (Application) - continued

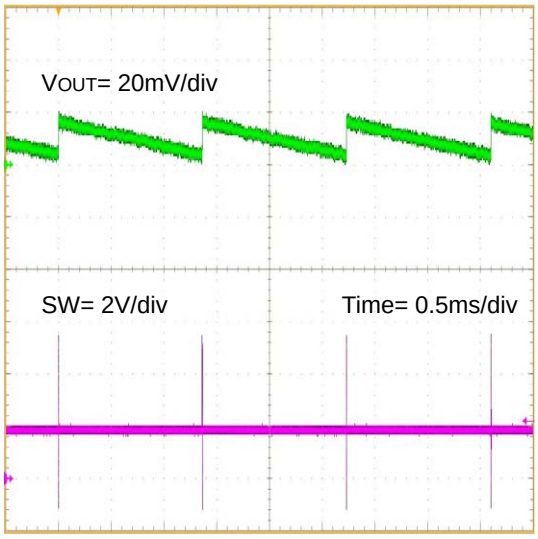


Figure 30. Output Ripple
(V_{IN}= 5V, VOUT= 1.8V, IOUT= 0A)

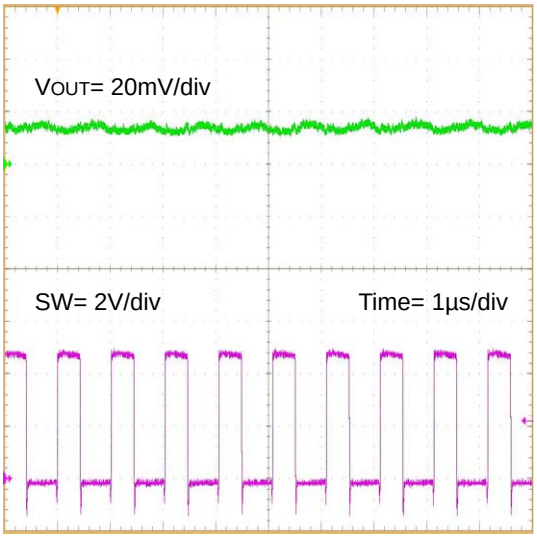


Figure 31. Output Ripple
(V_{IN}= 5V, VOUT= 1.8V, IOUT= 6A)

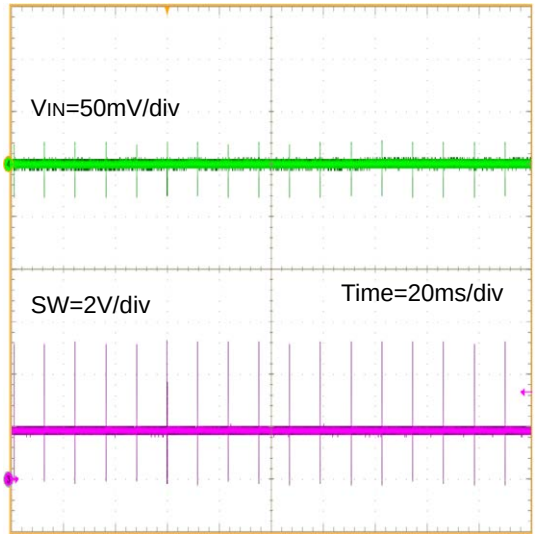


Figure 32. Input Ripple
(V_{IN}= 5V, VOUT= 1.8V, IOUT= 0A)

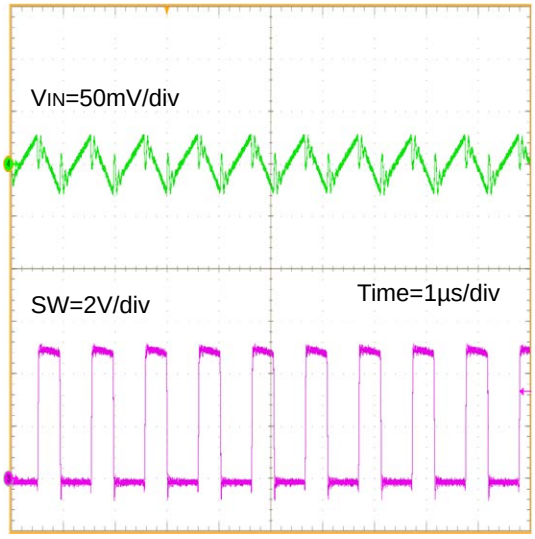


Figure 33. Input Ripple
(V_{IN}= 5V, VOUT= 1.8V, IOUT= 6A)

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Typical Performance Curves (Application) - continued

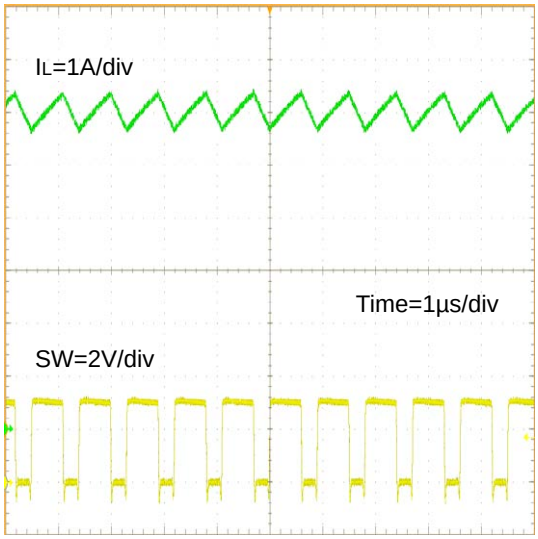


Figure 34. Switching Waveform
(V_{IN}= 3.3V, V_{OUT}= 1.8V, I_{OUT}= 6A, L= 1.0µH)

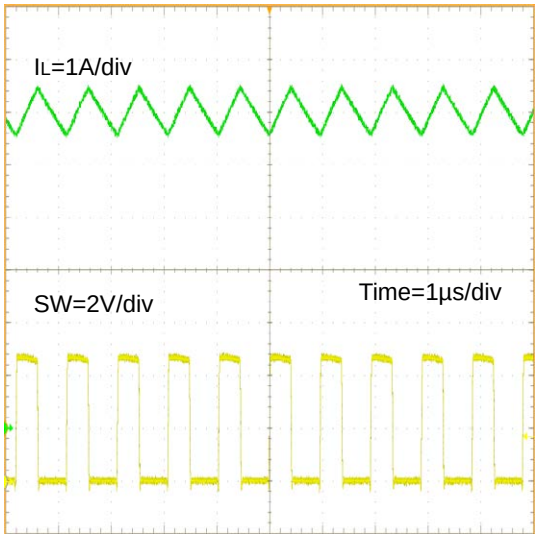


Figure 35. Switching Waveform
(V_{IN}= 5.0V, V_{OUT}= 1.8V, I_{OUT}= 6A, L= 1.5µH)

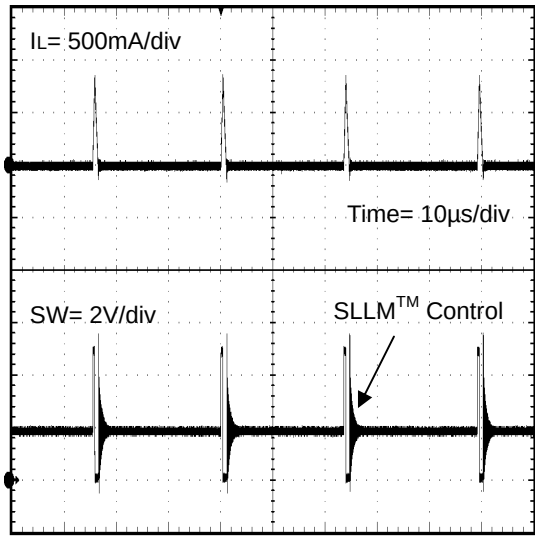


Figure 36. Switching Waveform with SLLM™
(V_{IN}= 5V, V_{OUT}= 1.8V, I_{OUT}= 30mA, L=1.5µH)

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Typical Performance Curves (Application) - continued

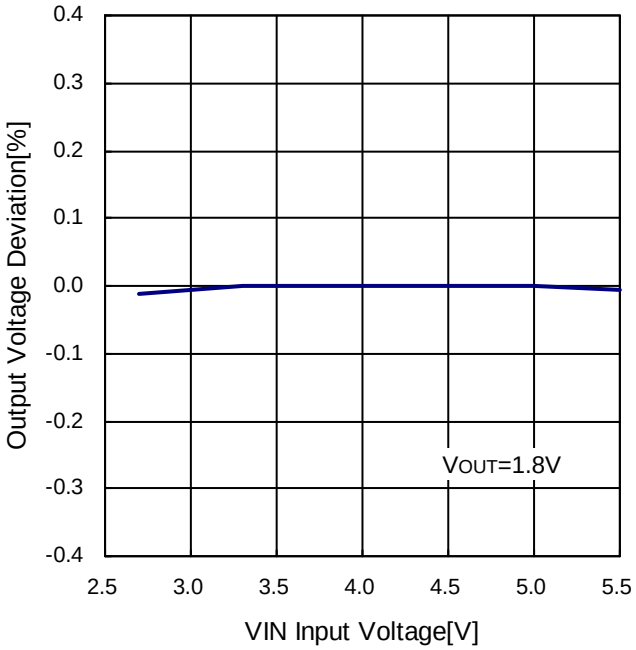


Figure 37. Line Regulation vs Input Voltage

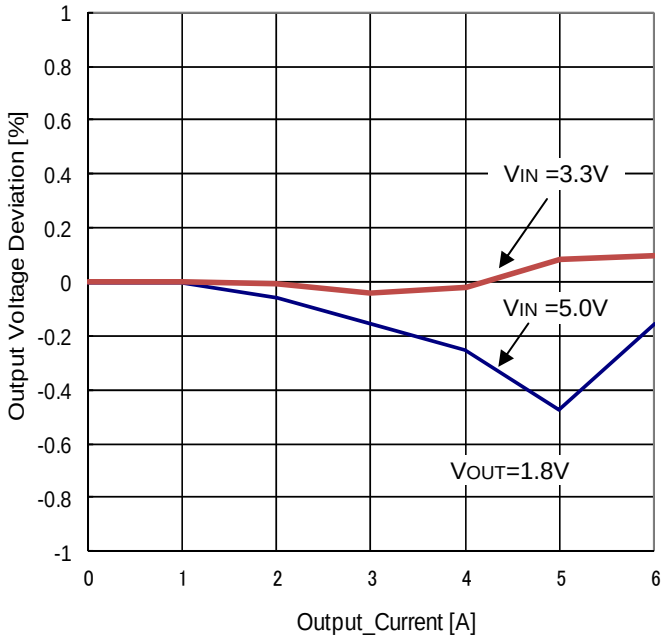


Figure 38. Load Regulation vs Load Current

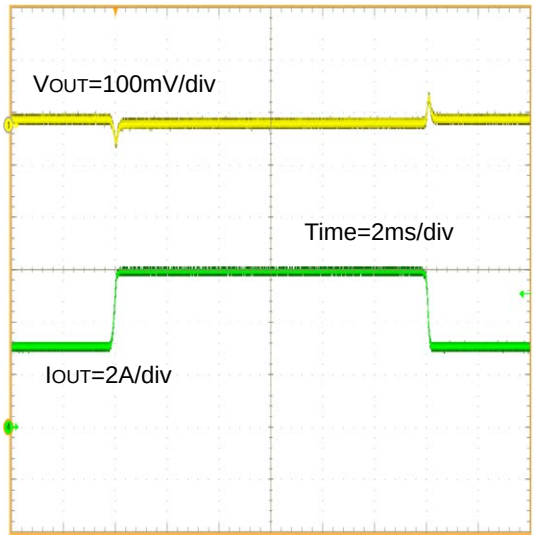


Figure 39. Load Transient Response
IOUT= 3A to 6A load step
(VIN=5V, VOUT=1.8V, L=1.5µH,
R3=6.8kΩ, C6=5600pF, C14=100pF)

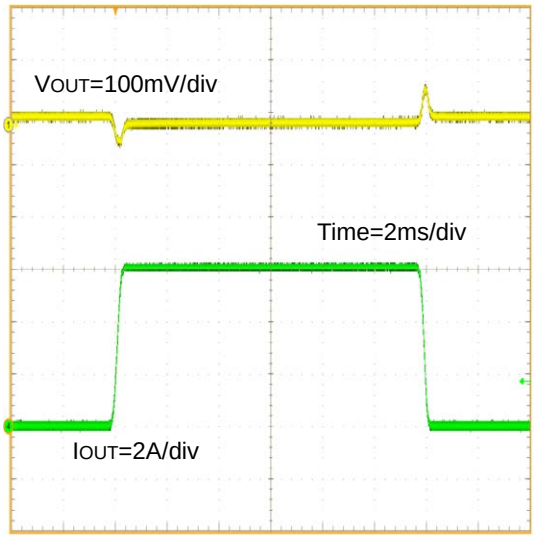


Figure 40. Load Transient Response
IOUT=0A to 6A load step
(VIN=5V, VOUT=1.8V, L=1.5µH,
R3=6.8kΩ, C6=5600pF, C14=100pF)

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1. Function Explanations
   (1) DC/DC converter operation

BD9A600MUV is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. It utilizes switching operation in PWM (Pulse Width Modulation) mode for heavier load, while it utilizes SLLM(Simple Light Load Mode) control for lighter load to improve efficiency.

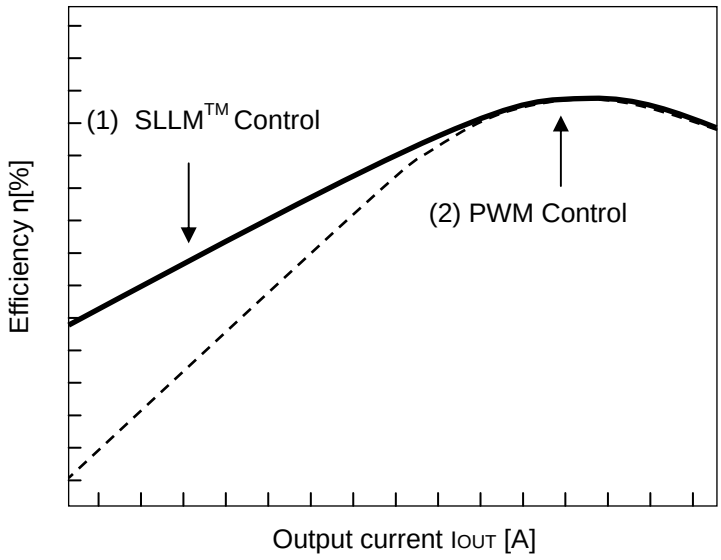


Figure 41. Efficiency (SLLM™ Control and PWM Control)

①SLLM™ Control

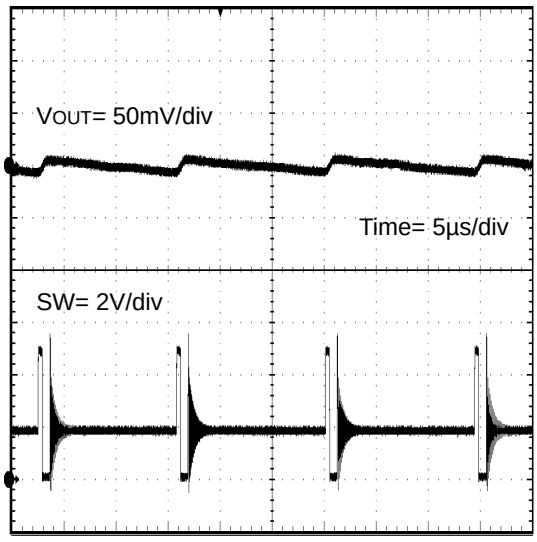


Figure 42. SW Waveform(SLLM™ Control)
(V_{IN}= 5.0V, VOUT= 1.8V, IOUT= 50mA)

②PWM Control

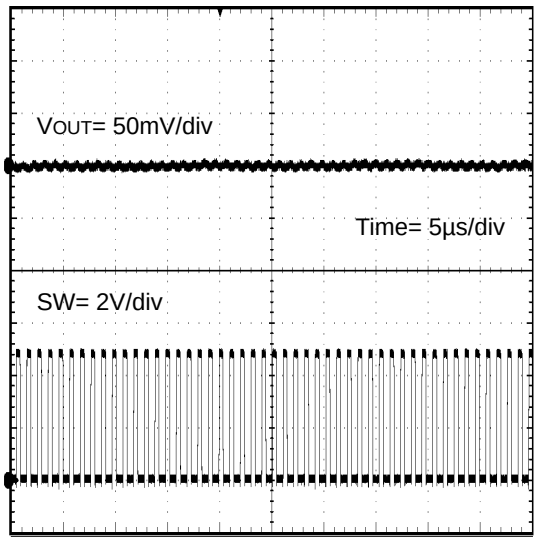


Figure 43. SW Waveform (PWM Control)
(V_{IN}= 5.0V, VOUT= 1.8V, IOUT= 1A)

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(2) Enable Control

The IC shutdown can be controlled by the voltage applied to the EN terminal. When VEN reaches 2.0V (Typ), the internal circuit is activated and the IC starts up. To enable shutdown control with the EN terminal, the shutdown interval (Low level interval of EN) must be set to 100µs or longer.

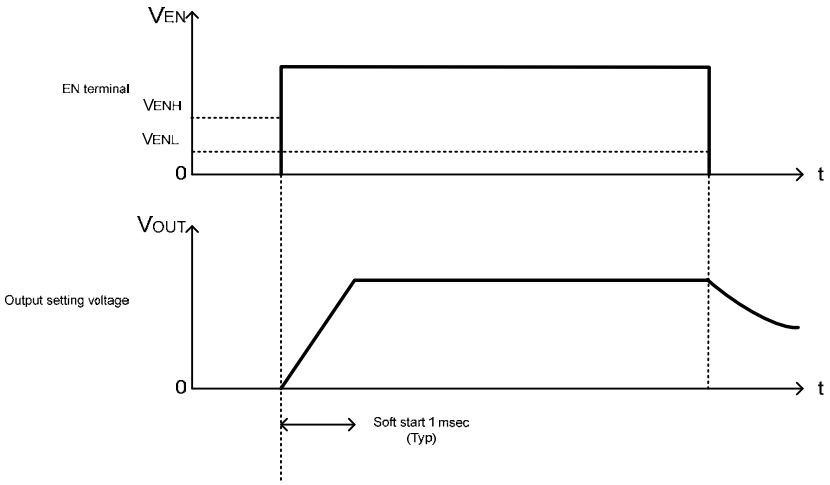


Figure 44. Start Up and Down with Enable

(3) Power Good

When the output voltage reaches outside ±10% of the voltage setting, the open drain N-ch MOSFET internally connected to the PGD terminal turns on and the PGD terminal is pulled down with an impedance of 50Ω(Typ). A hysteresis of 3% applies to resetting. Connecting a pull up resistor (10kΩ to 100kΩ) is recommended.

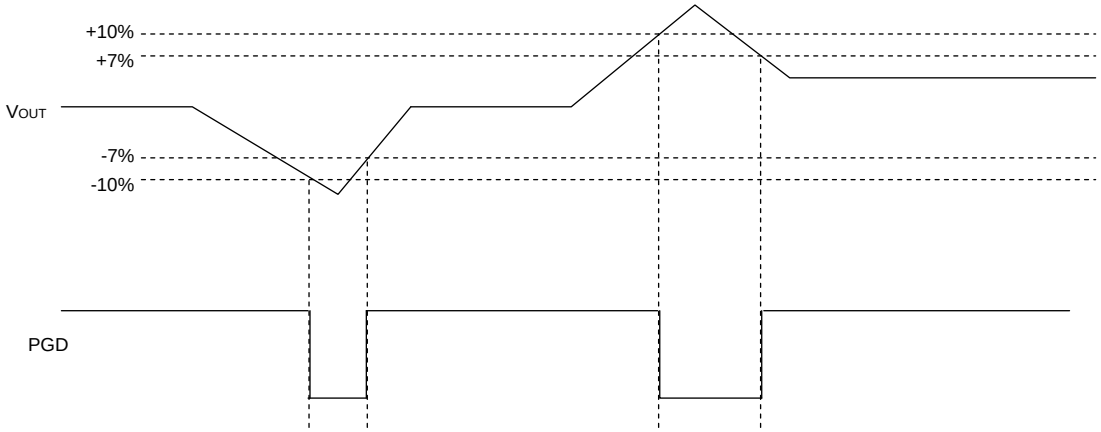


Figure 45. PGD Timing Chart

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2. Protection

The protective circuits are intended for prevention of damage caused by unexpected accidents. Do not use them for continuous protective operation.

(1) Short Circuit Protection (SCP)

The short circuit protection block compares the FB terminal voltage with the internal reference voltage VREF. When the FB terminal voltage has fallen below 0.4V(Typ) and remained there for 1msec(Typ), SCP stops the operation for 16msec(Typ) and subsequently initiates a restart.

EN Terminal	FB Terminal	Short Circuit Protection	Short Circuit Protection Operation
2.0V or Higher	< 0.4V(Typ)	Enabled	ON
	> 0.4V(Typ)		OFF
0.8V or Lower	-	Disabled	OFF

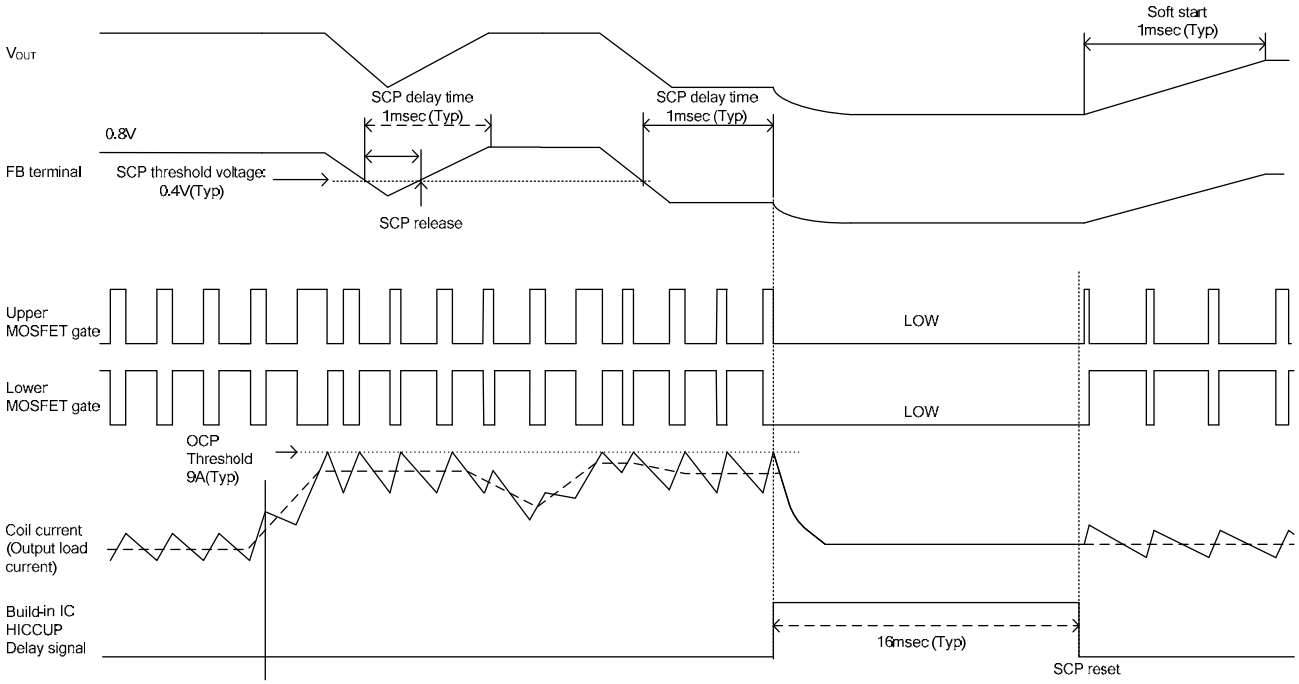


Figure 46. Short Circuit Protection (SCP) Timing Chart

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(2) Under Voltage Lockout Protection (UVLO)

The Under Voltage Lockout Protection circuit monitors the AVIN terminal voltage.
The operation enters standby when the AVIN terminal voltage is 2.45V(Typ) or lower.
The operation starts when the AVIN terminal voltage is 2.55V(Typ) or higher.

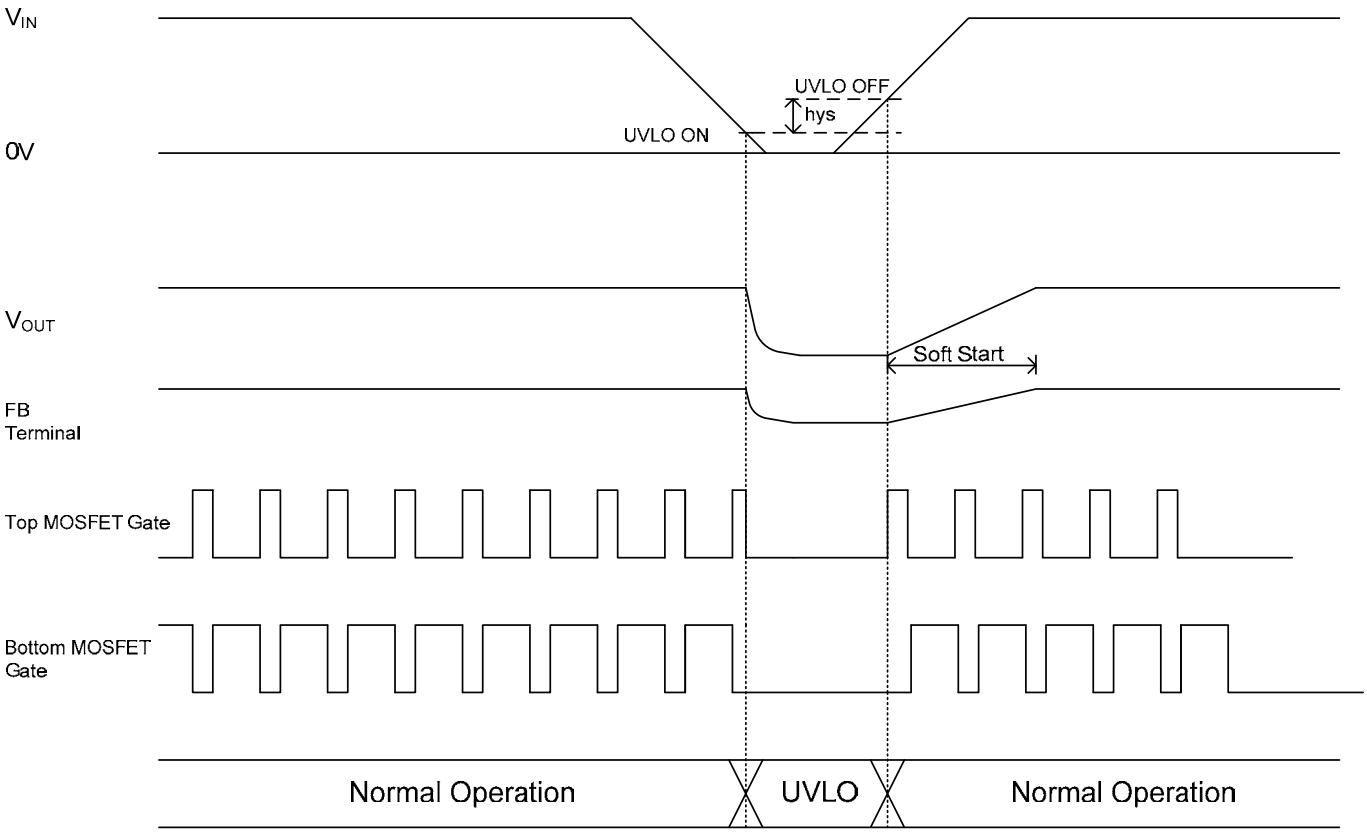


Figure 47. UVLO Timing Chart

(3) Thermal Shutdown

When the chip temperature exceeds Tj= 175°C(Typ), the DC/DC converter output is stopped. The thermal shutdown circuit is intended for shutting down the IC from thermal runaway in an abnormal state with the temperature exceeding Tjmax =150°C. It is not meant to protect or guarantee the soundness of the application. Do not use the function of this circuit for application protection design.

(4) Over Current Protection

The Over Current Protection function operates by using the current mode control to limit the current that flows through the High-side MOSFET at each cycle of the switching frequency. The designed over current limit value is 9A(Typ).

(5) Over Voltage Protection (OVP)

Over voltage protection function(OVP) compares FB terminal voltage with internal standard voltage VREF and when FB terminal voltage exceeds 0.88V(Typ) it turns MOSFET of output part MOSFET off. After output voltage drop it returns with hysteresis.

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Application Example

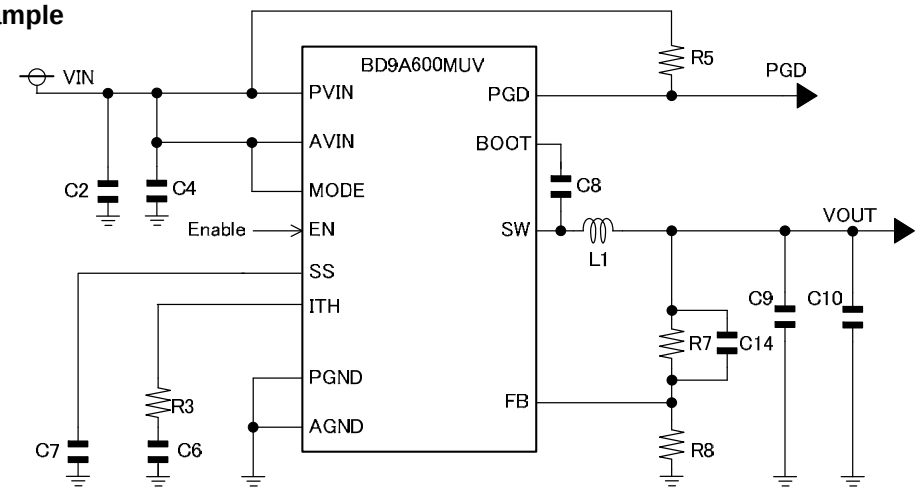


Figure 48. Application Circuit

Table 1. Recommended Component Values (V_{IN} = 5V)

Reference Designator	Output Voltage						Description
	1.0V	1.1V	1.2V	1.5V	1.8V	3.3V	
R3	4.3kΩ	4.7kΩ	5.1kΩ	6.2kΩ	6.8kΩ	13kΩ	-
R5	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	-
R7	7.5kΩ	10kΩ	10kΩ	16kΩ	30kΩ	75kΩ	-
R8	30kΩ	27kΩ	20kΩ	18kΩ	24kΩ	24kΩ	-
C2	10μF	10μF	10μF	10μF	10μF	10μF	10V, X5R, 3216
C4	0.1μF	0.1μF	0.1μF	0.1μF	0.1μF	0.1μF	16V, X5R, 1608
C6	5600pF	5600pF	5600pF	5600pF	5600pF	5600pF	-
C7	-	-	-	-	-	-	-
C8	0.47μF	0.47μF	0.47μF	0.47μF	0.47μF	0.47μF	16V, X5R, 1608
C9	22μF	22μF	22μF	22μF	22μF	22μF	10V, X5R, 2012
C10	22μF	22μF	22μF	22μF	22μF	22μF	10V, X5R, 2012
C14	430pF	330pF	330pF	200pF	100pF	33pF	
L1	1.0μH	1.0μH	1.0μH	1.5μH	1.5μH	1.5μH	TOKO, FDSD0630

Table 2. Recommended Component Values (V_{IN} = 3.3V)

Reference Designator	Output Voltage					Description
	1.0V	1.1V	1.2V	1.5V	1.8V	
R3	5.1kΩ	5.6kΩ	6.2kΩ	7.5kΩ	9.1kΩ	-
R5	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	-
R7	7.5kΩ	10kΩ	10kΩ	16kΩ	30kΩ	-
R8	30kΩ	27kΩ	20kΩ	18kΩ	24kΩ	-
C2	10μF	10μF	10μF	10μF	10μF	10V, X5R, 3216
C4	0.1μF	0.1μF	0.1μF	0.1μF	0.1μF	16V, X5R, 1608
C6	5600pF	5600pF	5600pF	5600pF	5600pF	-
C7	-	-	-	-	-	-
C8	0.47μF	0.47μF	0.47μF	0.47μF	0.47μF	16V, X5R, 1608
C9	22μF	22μF	22μF	22μF	22μF	10V, X5R, 2012
C10	22μF	22μF	22μF	22μF	22μF	10V, X5R, 2012
C14	430pF	330pF	330pF	200pF	100pF	
L1	1.0μH	1.0μH	1.0μH	1.0μH	1.0μH	TOKO, FDSD0630

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Selection of Components Externally Connected

1. Output LC Filter Constant

The DC/DC converter requires an LC filter for smoothing the output voltage in order to supply a continuous current to the load. BD9A600MUV is returned to the IC and IL ripple current flowing through the inductor for SLLM™ control.

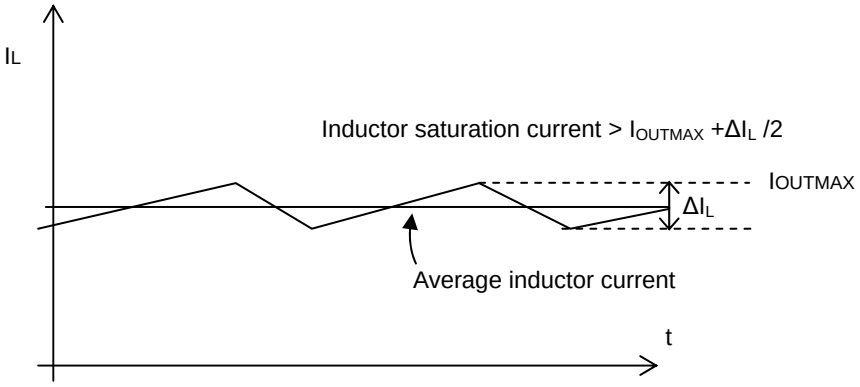


Figure 49. Waveform of Current Through Inductor

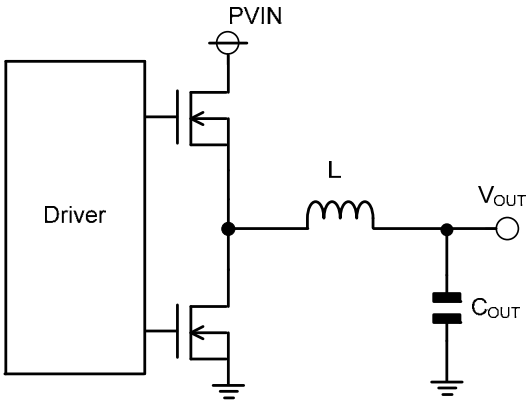


Figure 50. Output LC Filter Circuit

BD9A600MUV set up ΔI_L to be 0.8A for stable operation of the DC/DC converter.
Computation with V_{IN} = 5V, V_{OUT}= 1.8V, and the switching frequency F_{OSC}= 1MHz, the method is as below.

$$L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times F_{OSC} \times \Delta I_L} = 1.440 \fallingdotseq 1.5 [\mu H]$$

The saturation current of the inductor must be larger than the sum of the maximum output current and 1/2 of the inductor ripple current ΔIL.

The output capacitor C_{OUT} affects the output ripple voltage characteristics. The output capacitor C_{OUT} must satisfy the required ripple voltage characteristics.

The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{OSC}}) [V]$$

R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor.
With C_{OUT}= 44µF, R_{ESR} = 10mΩ the output ripple voltage is calculated as

$$\Delta V_{RPL} = 0.8 \times (10m + \frac{1}{(8 \times 44\mu \times 1MHz)}) = 10.3 [mV]$$

*Be careful of total capacitance value, when additional capacitor C_{LOAD} is connected in addition to output capacitor C_{OUT}. Use maximum additional capacitor C_{LOAD} (Max) condition which satisfies the following method.

$$Maximum\ starting\ inductor\ ripple\ current\ IL_{START} < Over\ Current\ limit\ 7.5A(min)$$

Maximum starting inductor ripple current I_{LSTART} can be expressed in the following method.

$$IL_{START} = Maximum\ starting\ output\ current(I_{OMAX}) + Charge\ current\ to\ output\ capacitor(I_{CAP}) + \frac{\Delta I_L}{2}$$

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Charge current to output capacitor I_{CAP} can be expressed in the following method.

$$I_{CAP} = \frac{(C_{OUT} + C_{LOAD}) \times V_{OUT}}{T_{SS}} [A]$$

Computation with V_{IN}= 5V, V_{OUT}= 3.3V, ΔI_L(Max)=0.935A, switching (frequency F_{OSC}= 800kHz(Min), L=1.5µH), Output capacitor C_{OUT}= 44µF, Soft Start time T_{SS}= 0.5ms(Min), load current during soft start I_{OSS}= 6A the method is as below.

$$C_{LOAD}(max) < \frac{(7.5 - I_{OSS} - \Delta I_L/2) \times T_{SS}}{V_{OUT}} - C_{OUT} = 112 [\mu F]$$

If the value of C_{LOAD} is large, and cannot meet the above equation,

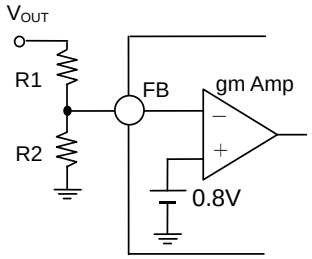
$$C_{LOAD}(max) < \frac{(7.5 - I_{OSS} - \Delta I_L/2) \times V_{FB}}{V_{OUT} \times I_{SS}} \times C_{SS} - C_{OUT}$$

Adjust the value of the capacitor C_{SS} to meet the above formula.
(Refer to the following items (3) Soft Start Setting equation of time T_{SS} and soft-start value of the capacitor to be connected to the C_{SS}.)

Computation with V_{IN} = 5V, V_{OUT} = 3.3V, I_{OSS}= 6A, ΔI_L(Max)=0.935A,, switching frequency (F_{OSC}= 800kHz (Min), L= 1.5µH) Output capacitor C_{OUT} = 44µF, V_{FB} = 0.792V(Min), I_{SS} = 3.6µA(Max), A capacitor connected to the C_{SS} if you want to connect the C_{LOAD} = 330uF is the following equation.

$$C_{SS} > \frac{V_{OUT} \times I_{SS}}{(7.5 - I_{OSS} - \Delta I_L/2) \times V_{FB}} \times (C_{LOAD} + C_{OUT}) = 5.43 [nF]$$

2. Output Voltage Setting
The output voltage value can be set by the feedback resistance ratio.



$$V_{OUT} = \frac{R1 + R2}{R2} \times 0.8 [V]$$

Figure 51. Feedback Resistor Circuit

3. Soft Start Setting
Turning the EN terminal signal high activates the soft start function. This causes the output voltage to rise gradually while the current at startup is placed under control. This allows the prevention of output voltage overshoot and inrush current. The rise time depends on the value of the capacitor connected to the SS terminal.

$T_{SS} = (C_{SS} \times V_{FB})/I_{SS}$

T_{SS} : Soft Start Time

C_{SS} : Capacitor connected to Soft Start Time Terminal

V_{FB} : FB Terminal Voltage (0.8V (Typ))

I_{SS} : Soft Start Terminal Source Current (1.8µA(Typ))

with $C_{SS} = 0.01$µF,

$$T_{SS} = (0.010[\mu F] \times 0.8[V])/1.8[\mu A]$$
$$= 4.44[msec]$$

Turning the EN terminal signal high with the SS terminal open (no capacitor connected) or with the terminal signal high causes the output voltage to rise in 1 msec (Typ).

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4. Phase Compensation Component

A current mode control buck DC/DC converter is a two-pole, one-zero system. Two poles are formed by an error amplifier and load and the one zero point is added by phase compensation. The phase compensation resistor R_{ITH} determines the crossover frequency FCRS where the total loop gain of the DC/DC converter is 0dB. A high value crossover frequency $_{FCRS}$ provides a good load transient response characteristic but inferior stability. Conversely, a low value crossover frequency F_{CRS} greatly stabilizes the characteristics but the load transient response characteristic is impaired. Please confirm recommended parts list for phase compensation.

(1) Selection of Phase Compensation Resistor R_{ITH}

The Phase Compensation Resistance R_{ITH} can be determined by using the following equation.

$$R_{ITH} = \frac{2\pi \times V_{OUT} \times F_{CRS} \times C_{OUT}}{V_{FB} \times G_{MP} \times G_{MA}} [\Omega]$$

V_{OUT} : Output Voltage [V]

F_{CRS}: Crossover Frequency [Hz]

C_{OUT} : Output Capacitance [F]

V_{FB} : Feedback Reference Voltage (0.8V (Typ))

G_{MP} (VIN = 5V) : Current Sense Gain (21.4A/V (Typ))

G_{MP} (VIN = 3.3V) : Current Sense Gain (17.6A/V (Typ))

G_{MA} : Error Amplifier Trans conductance (260μA/V(Typ))

(2) Selection of Phase Compensation Capacitance C_{ITH}

For stable operation of the DC/DC converter, zero for compensation cancels the phase delay due to the pole formed by the load.

The phase compensation capacitance C_{ITH} can be determined by using the following equation.

$$C_{ITH} = \frac{C_{OUT} \times V_{OUT}}{R_{ITH} \times I_{OUT}} [F]$$

(3) Selection of Phase Compensation Capacitance C_{14}

Adding zero system at 50kHz is recommended to get a better transient load response characteristic for DC/DC converter.

It can be obtained by using the following equation.

$$C_{14} = \frac{1}{2\pi R_{UP} \times 50kHz} [F]$$

(4) Loop stability

To ensure the stability of the DC/DC converter, make sure that a sufficient phase margin is provided. A phase margin of at least 45º in the worst conditions is recommended.

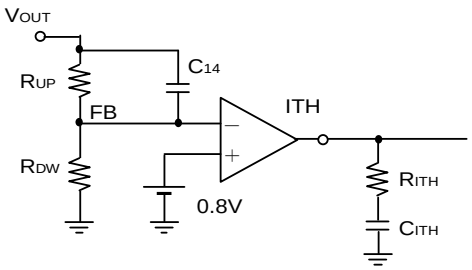


Figure 52. Phase Compensation Circuit

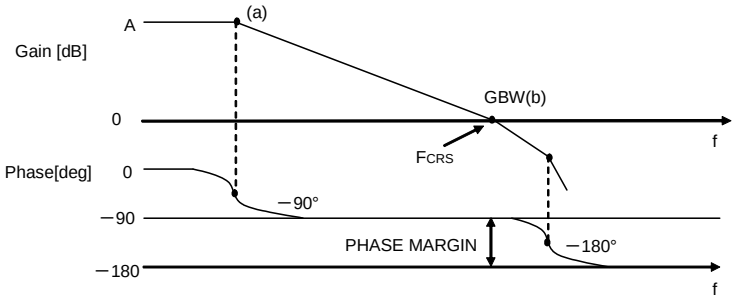


Figure 53. Bode Plot

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PCB Layout Design

In the buck DC/DC converter a large pulse current flows into two loops. The first loop is the one into which the current flows when the high-side FET is turned on. The flow starts from the input capacitor C_{IN}, runs through the FET, inductor L and output capacitor C_{OUT} and back to GND of C_{IN} via GND of C_{OUT}. The second loop is the one into which the current flows when the low-side FET is turned on. The flow starts from the low-side FET, runs through the inductor L and output capacitor C_{OUT} and back to GND of the low-side FET via GND of C_{OUT}. Route these two loops as thick and as short as possible to allow noise to be reduced for improved efficiency. It is recommended to connect the input and output capacitors directly to the GND plane. The PCB layout has a great influence on the DC/DC converter in terms of all of the heat generation, noise and efficiency characteristics.

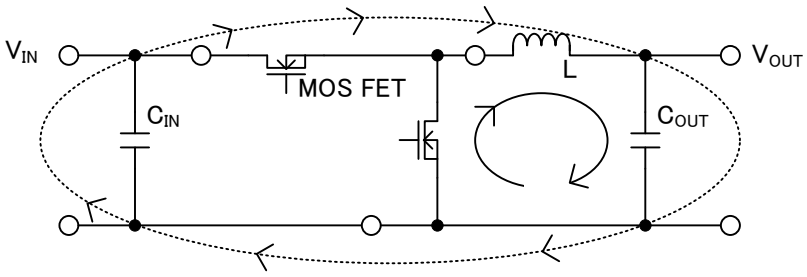
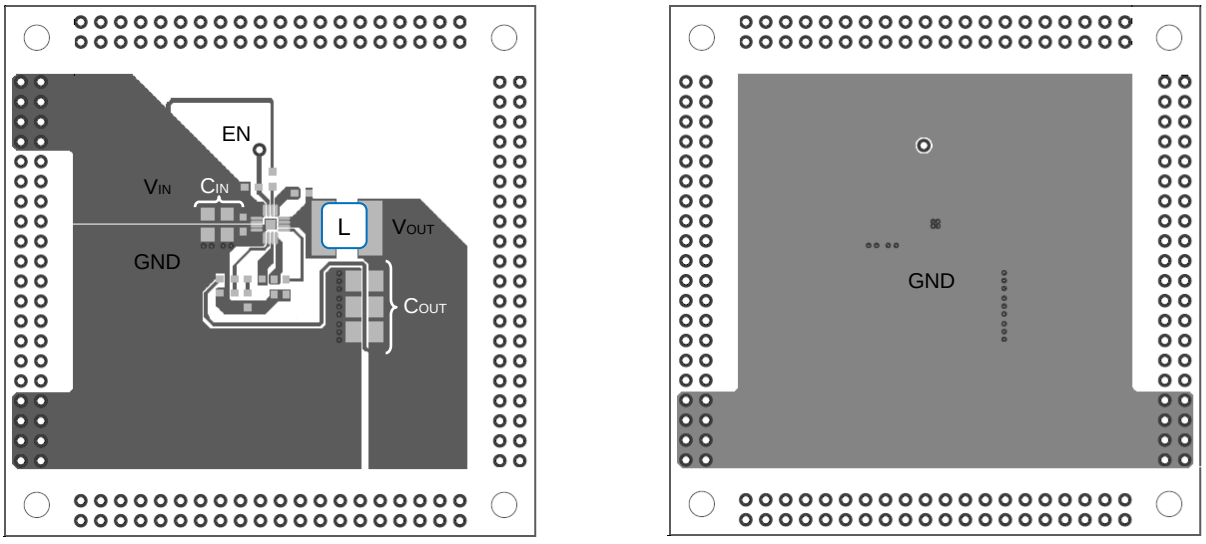


Figure 54. Current Loop of Buck DC/DC Converter

Accordingly, design the PCB layout considering the following points.

- Connect an input capacitor as close as possible to the IC PVIN terminal on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the GND node to assist heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the coil pattern as thick and as short as possible.
- Provide lines connected to FB and ITH far from the SW nodes.
- Place the output capacitor away from the input capacitor in order to avoid the effect of harmonic noise from the input.
- Large electric current raises the power supply voltage by the inverse current when protected circuit operates. Reduce the impedance of power supply line to avoid it.



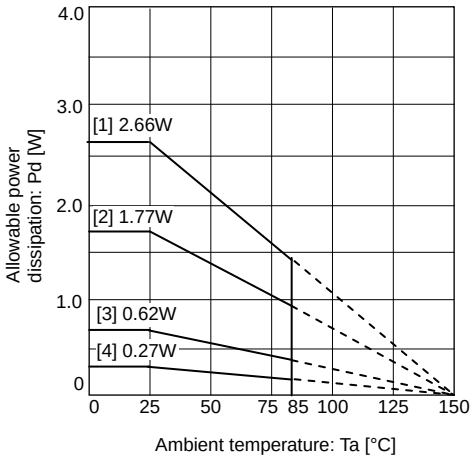
Top Layer Bottom Layer

Figure 55. Example of evaluation board layout

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Power Dissipation

When designing the PCB layout and peripheral circuitry, sufficient consideration must be given to ensure that the power dissipation is within the allowable dissipation curve.
This package incorporates an exposed thermal pad. Solder directly to the PCB ground plane. After soldering, the PCB can be used as a heatsink.
The exposed thermal pad dimensions for this package are shown in page 31.

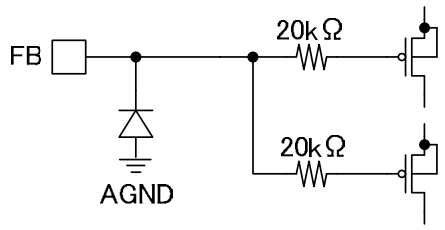
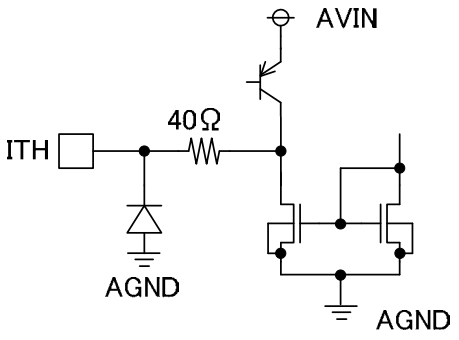
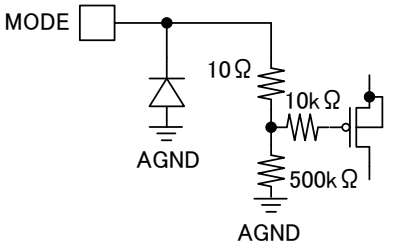
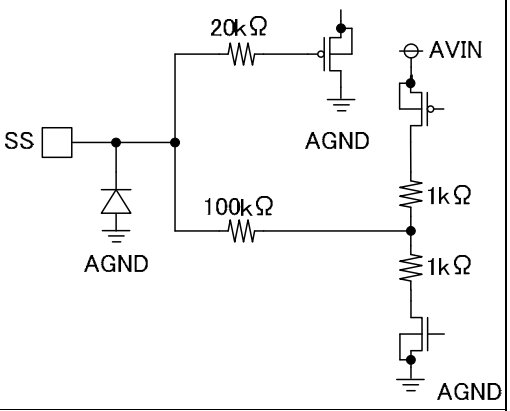
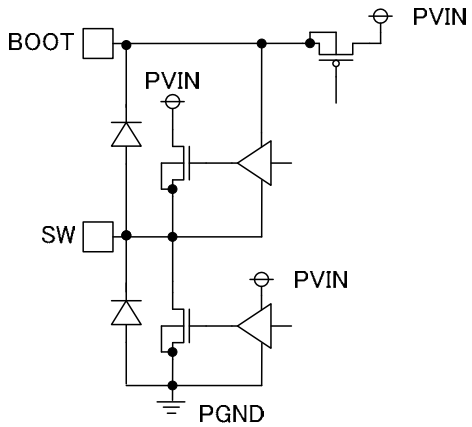
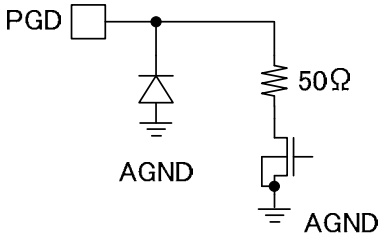
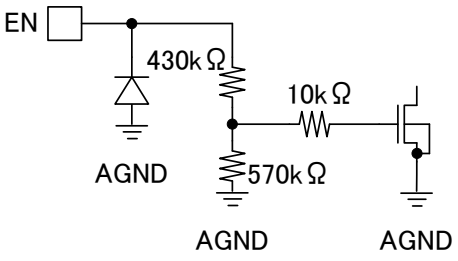


(1) 4-layer board (surface heat dissipation copper foil 5505mm^2)
(copper foil laminated on each layer)
θ_{JA}=47.0°C/W
(2) 4-layer board (surface heat dissipation copper foil 6.28mm^2)
(copper foil laminated on each layer)
θ_{JA}=70.62°C/W
(3) 1-layer board (surface heat dissipation copper foil 6.28mm^2)
θ_{JA}=201.6°C/W
(4) IC only
θ_{JA}=462.9°C/W

Figure 56. Thermal Derating Characteristics
(VQFN016V3030)

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I/O equivalence circuits

6. FB	7. ITH
	
8. MODE	**9. SS**
	
10.11.12. SW13. BOOT	**14. PGD**
	
15. EN	
	

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
   OR

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm 4-layer glass epoxy board. In case of exceeding this absolute maximum rating increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So, unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

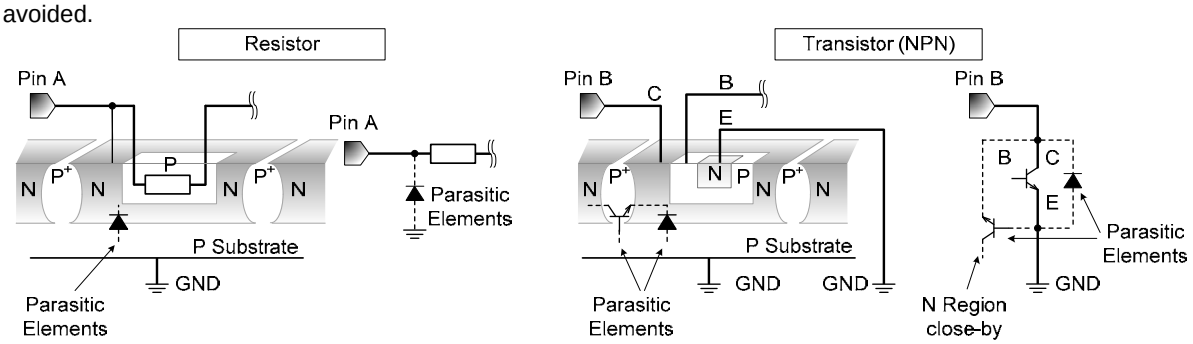


Figure 57. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

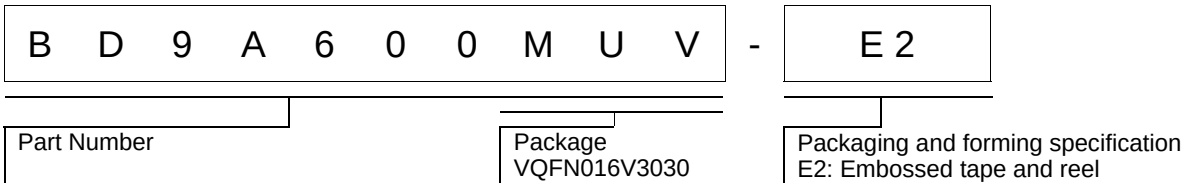
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

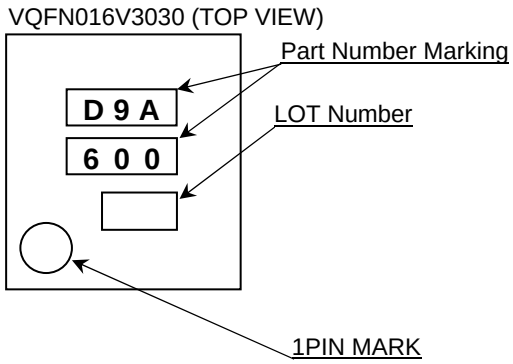
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information



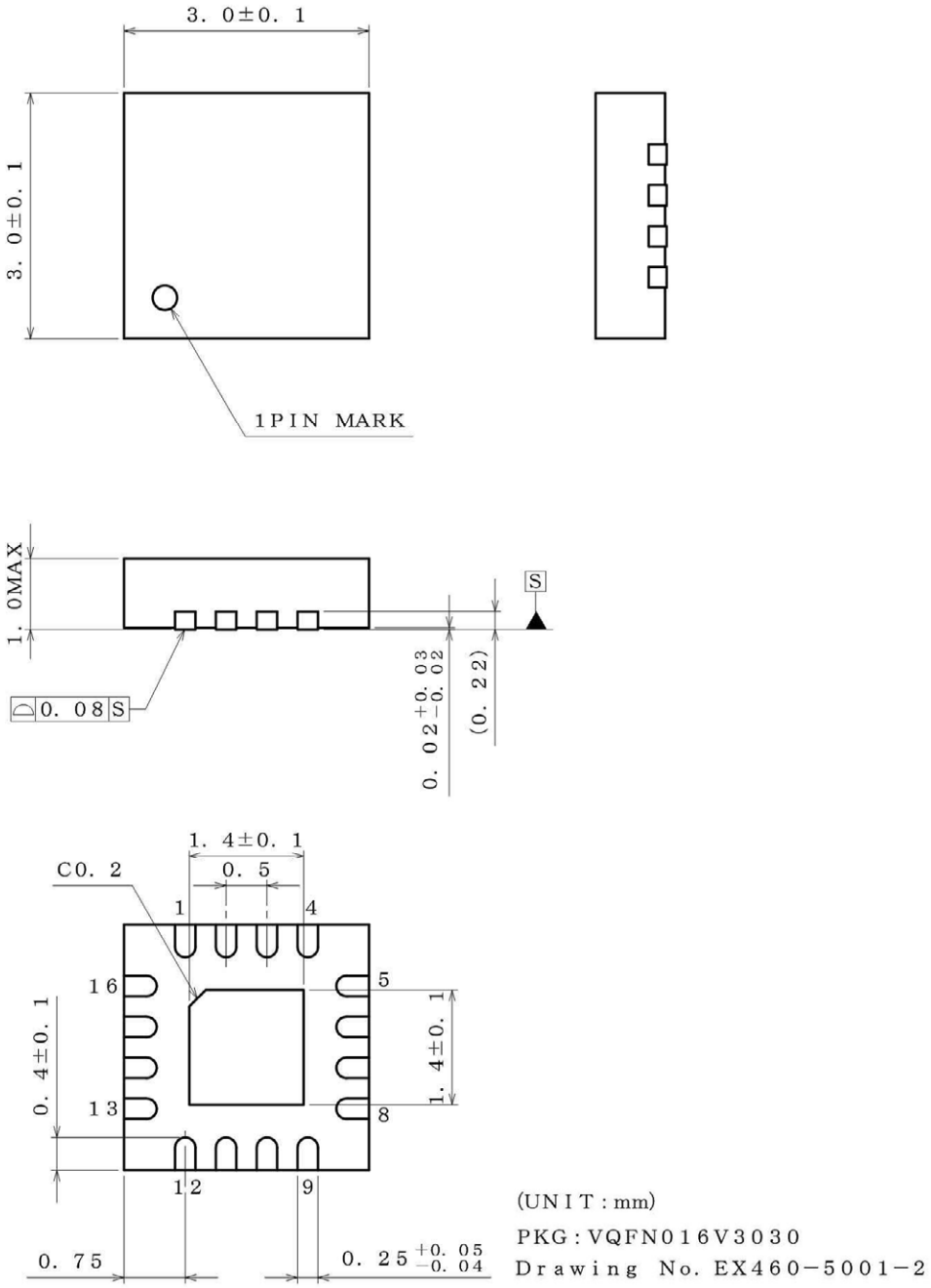
Marking Diagrams



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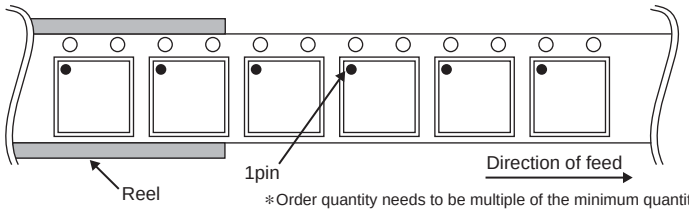
Physical Dimension, Tape and Reel Information

Package Name	VQFN016V3030



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Draft	Changes
10.Jul.2014	001	New

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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