Data Sheet | October 5, 2006 | FN6279.0

Monolithic 1A Step-Down Regulator with Low Quiescent Current

The ISL97536 is a synchronous, integrated FET 1A step-down regulator with internal compensation. It operates with an input voltage range from 2.5V to 6V, which accommodates supplies of 3.3V, 5V, or a Li-Ion battery source. The output can be externally set from 0.8V to V_{IN} with a resistive divider.

The ISL97536 features PWM control with a 1.4MHz typical switching frequency. The typical no load quiescent current is only 500µA. Additional features include a 100ms Power-On-Reset output, <1µA shutdown current, short-circuit protection, and over-temperature protection.

The ISL97536 is available in the 10 Ld MSOP package, making the entire converter occupy less than 0.15in^2 of PCB area with components on one side only. The 10 Ld MSOP package is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL97536IUZ (Note)	7536Z	-	10 Ld MSOP (Pb-free)	MDP0043
ISL97536IUZ-TK (Note)	7536Z	13" (1k pcs)	10 Ld MSOP (Pb-free)	MDP0043
ISL97536IUZ-T (Note)	7536Z	13" (2.5k pcs)	10 Ld MSOP (Pb-free)	MDP0043

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

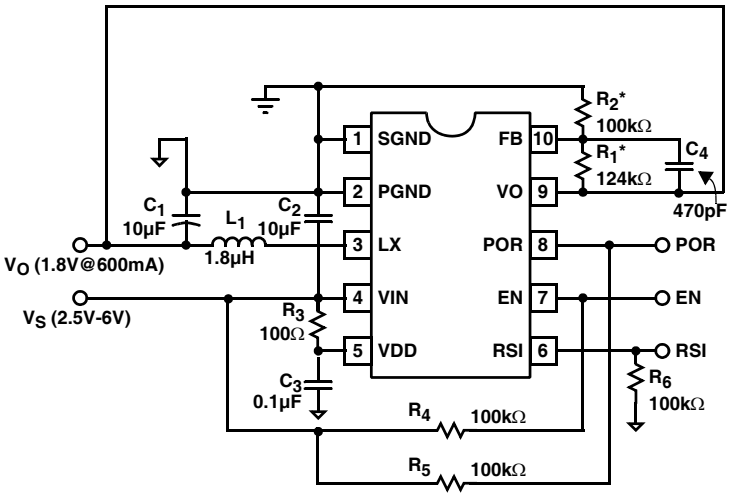
- Less than 0.15in^2 footprint for the complete 1A converter
- Components on one side of PCB
- Max height 1.1mm MSOP10
- 100ms Power-On-Reset output (POR)
- Internally-compensated voltage mode controller
- Up to 95% efficiency
- <1µA shutdown current
- 500µA quiescent current
- Hiccup mode overcurrent and over-temperature protection
- Pb-free plus anneal available (RoHS compliant)

Applications

- PDA and pocket PC computers
- Bar code readers
- Cellular phones
- Portable test equipment
- Li-Ion battery powered devices
- Small form factor (SFP) modules

Pinout and Typical Application Diagram

ISL97536
(10 LD MSOP)
TOP VIEW



* $V_O = 0.8V * (1 + R_1/R_2)$

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings (T_A = +25°C)

V_{IN}, V_{DD}, PG to SGND . . . . . -0.3V to +6.5V
LX to PGND . . . . . -0.3V to (V_{IN} + +0.3V)
SYNC, EN, V_O, FB to SGND . . . . . -0.3V to (V_{IN} + +0.3V)
PGND to SGND . . . . . -0.3V to +0.3V
Continuous Output Current 1A

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
MSOP10 Package 130
Operating Ambient Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

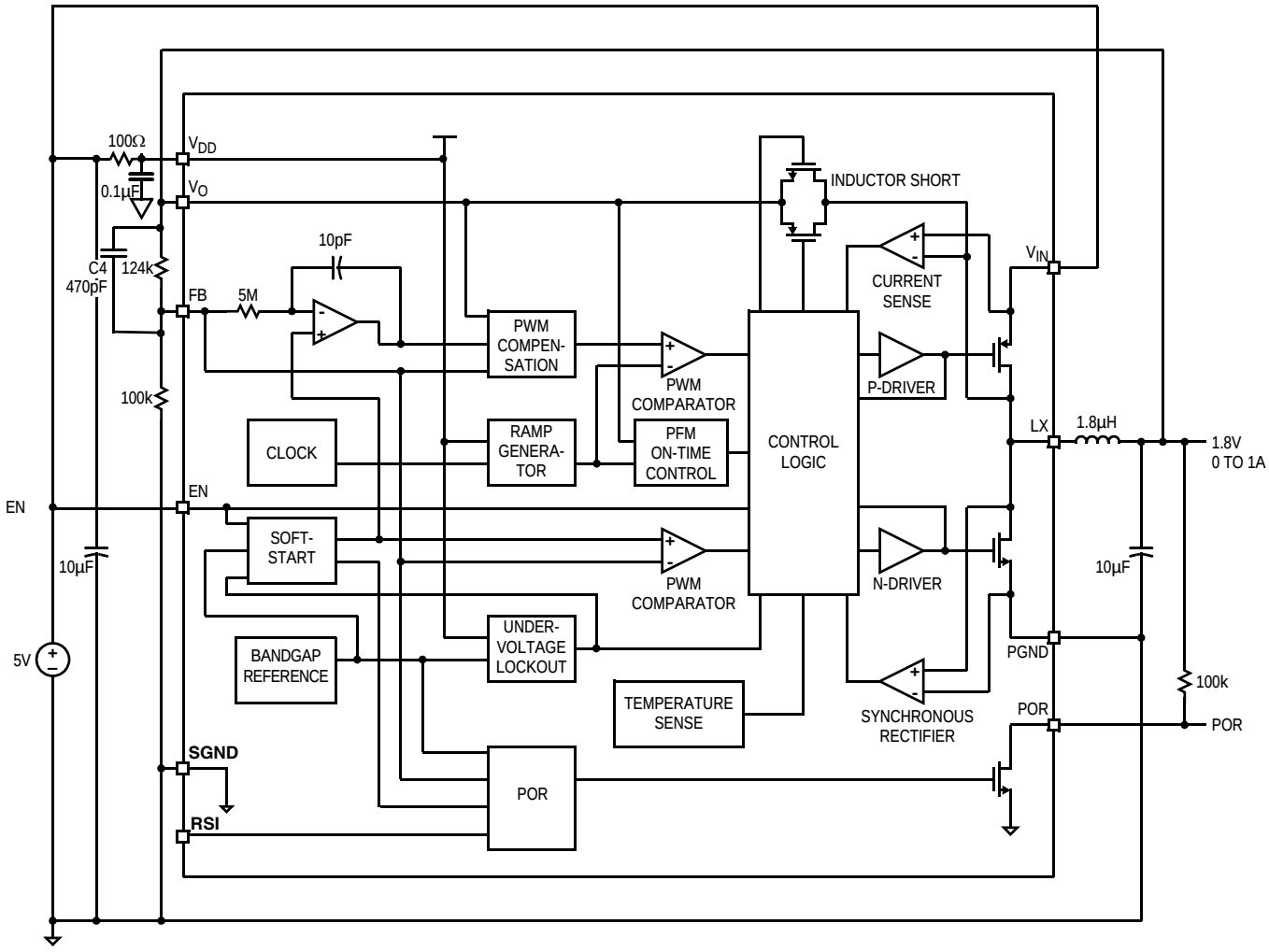
$V_{DD} = V_{IN} = V_{EN}$ = 3.3V, C1 = C2 = 10µF, L = 1.8µH, V_O = 1.8V (as shown in Typical Application Diagram), T_A = -40°C to +85°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
V_{FB}	Feedback Input Voltage		790	800	810	mV
I_{FB}	Feedback Input Current				250	nA
V_{IN}, V_{DD}	Input Voltage		2.5		6	V
$V_{IN,OFF}$	Minimum Voltage for Shutdown	V_{IN} falling, T_A = +25°C only	2		2.2	V
$V_{IN,ON}$	Maximum Voltage for Start-up	V_{IN} rising, T_A = +25°C only	2.2		2.4	V
I_{DD}	Supply Current	$V_{IN} = V_{DD}$ = 5V		400	500	µA
		EN = 0, $V_{IN} = V_{DD}$ = 5V		0.1	3	µA
$R_{DS(ON)-PMOS}$	PMOS FET Resistance	V_{DD} = 5V, T_A = +25°C		70		mΩ
$R_{DS(ON)-NMOS}$	NMOS FET Resistance	V_{DD} = 5V, T_A = +25°C		45		mΩ
I_{LMAX}	Current Limit			1.5		A
$T_{OT,OFF}$	Over-temperature Threshold	T rising		145		°C
$T_{OT,ON}$	Over-temperature Hysteresis	T falling		130		°C
I_{EN}, I_{RSI}	EN, RSI Current	V_{EN}, V_{RSI} = 0V and 3.3V	-1		1	µA
V_{EN1}, V_{RSI1}	EN, RSI Rising Threshold	V_{DD} = 3.3V			2.4	V
V_{EN2}, V_{RSI2}	EN, RSI Falling Threshold	V_{DD} = 3.3V	0.8			V
V_{POR}	Minimum V_{FB} for POR, WRT Targeted V_{FB} Value	V_{FB} rising			95	%
		V_{FB} falling	86			%
V_{OLPOR}	POR Voltage Drop	I_{SINK} = 3.3mA		35	70	mV
AC CHARACTERISTICS						
F_{PWM}	PWM Switching Frequency		1.25	1.4	1.6	MHz
t_{RSI}	Minimum RSI Pulse Width	Guaranteed by design		25	50	ns
t_{SS}	Soft-Start Time			650		µs
t_{POR}	Power On Reset Delay Time		80	100	120	ms

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	SGND	Negative supply for the controller stage
2	PGND	Negative supply for the power stage
3	LX	Inductor drive pin; high current digital output with average voltage equal to the regulator output voltage
4	VIN	Positive supply for the power stage
5	VDD	Power supply for the controller stage
6	RSI	Resets POR timer
7	EN	Enable
8	POR	Power on reset open drain output
9	VO	Output voltage sense
10	FB	Voltage feedback input; connected to an external resistor divider between V_O and SGND for variable output

Block Diagram



Performance Curves and Waveforms

All waveforms are taken at V_{IN} = 3.3V, V_O = 1.8V, I_O = 600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted.

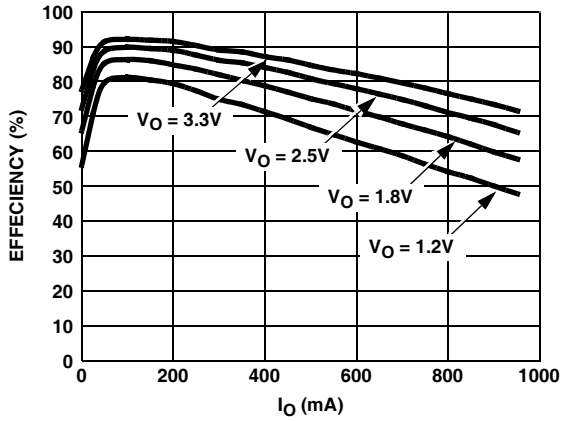


FIGURE 1. EFFICIENCY vs I_O AT 5V V_{IN}

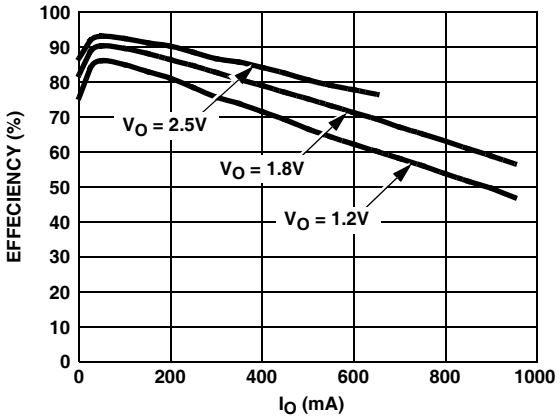


FIGURE 2. EFFICIENCY vs I_O AT 3.3V

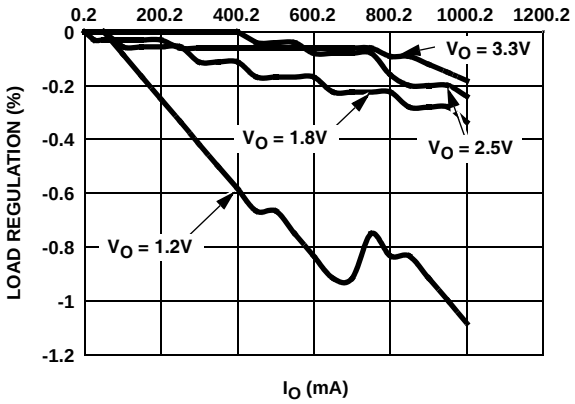


FIGURE 3. LOAD REGULATION vs I_O AT 5V V_{IN}

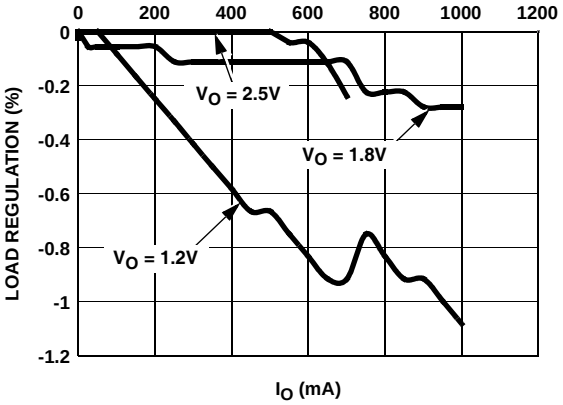


FIGURE 4. LOAD REGULATION vs I_O AT 3.3V V_{IN}

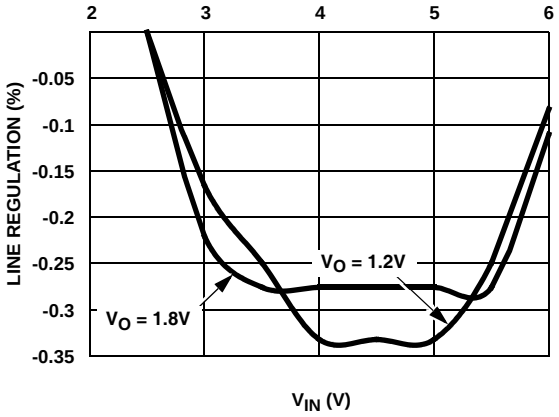


FIGURE 5. LINE REGULATION vs V_{IN}

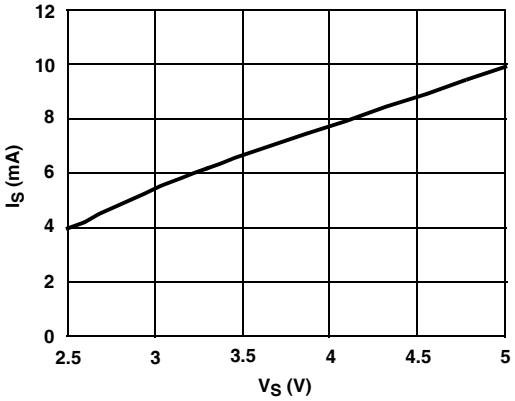


FIGURE 6. NO LOAD QUIESCENT CURRENT

Performance Curves and Waveforms (Continued)

All waveforms are taken at V_{IN} = 3.3V, V_O = 1.8V, I_O = 600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted.

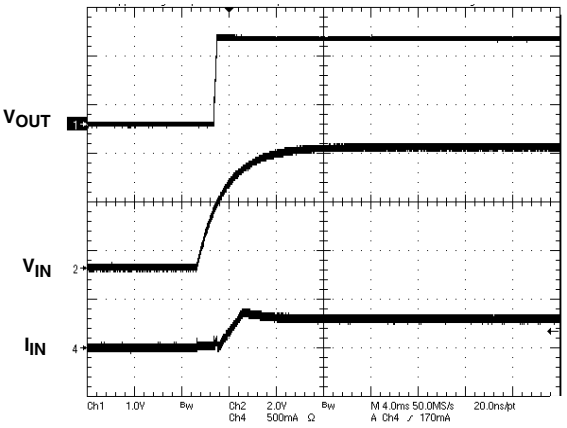


FIGURE 7. START-UP AT I_O = 600mA

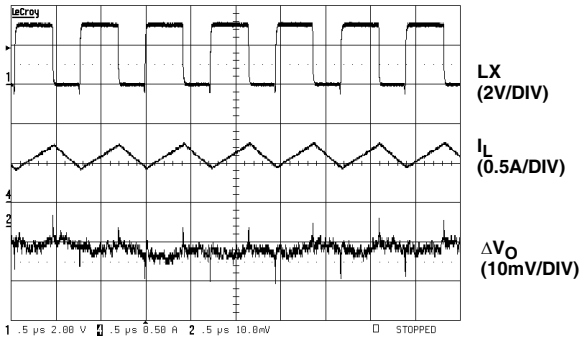


FIGURE 8. PWM STEADY-STATE OPERATION (I_O = 600mA)

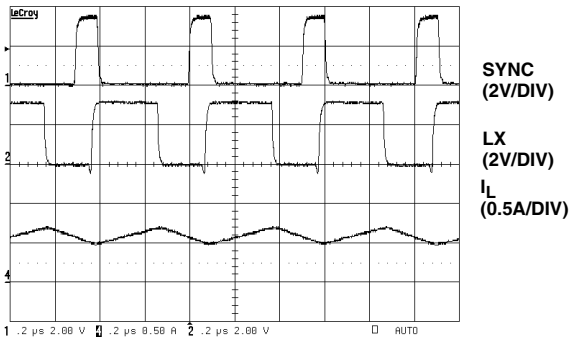


FIGURE 9. EXTERNAL SYNCHRONIZATION TO 2MHz

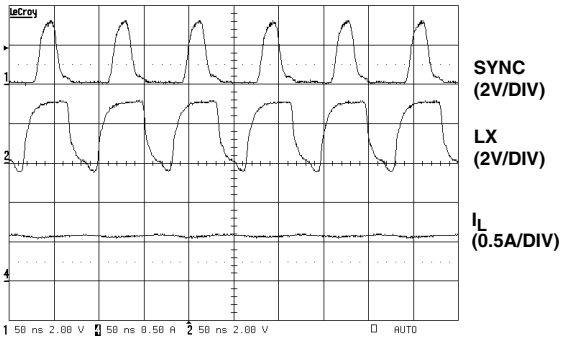


FIGURE 10. EXTERNAL SYNCHRONIZATION TO 12MHz

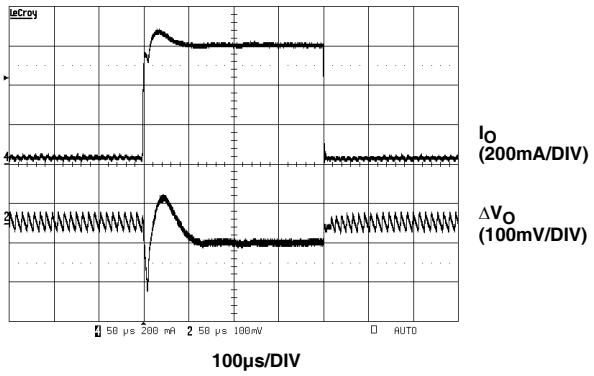


FIGURE 11. LOAD TRANSIENT RESPONSE (22mA TO 600mA)

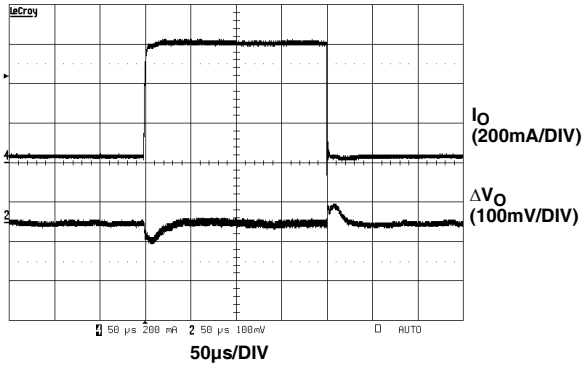


FIGURE 12. LOAD TRANSIENT RESPONSE (30mA TO 600mA)

Performance Curves and Waveforms (Continued)

All waveforms are taken at V_{IN} = 3.3V, V_O = 1.8V, I_O = 600mA with component values shown on page 1 at room ambient temperature, unless otherwise noted.

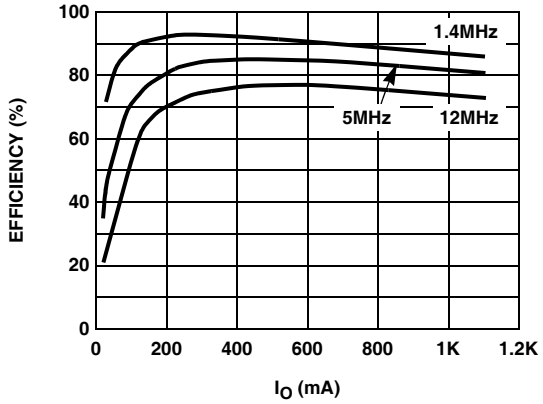


FIGURE 13. EFFICIENCY vs I_O

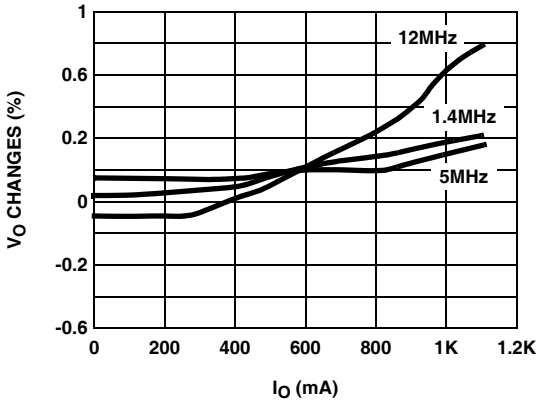


FIGURE 14. LOAD REGULATION

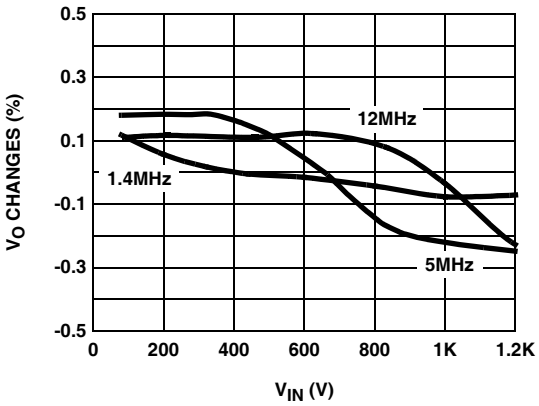


FIGURE 15. LINE REGULATION @ 500mA

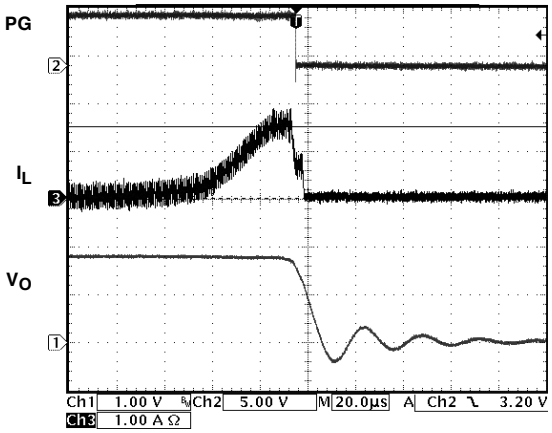


FIGURE 16. OVERCURRENT SHUTDOWN

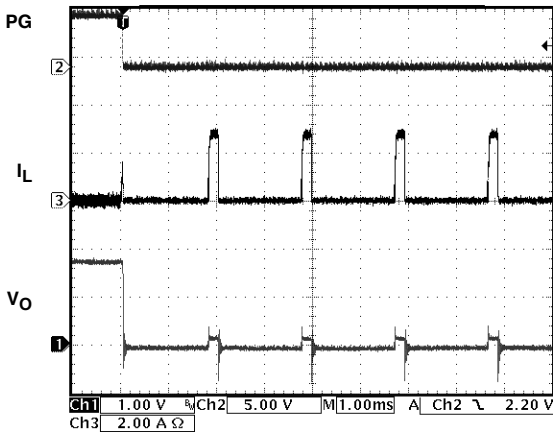


FIGURE 17. OVERCURRENT HICCUP MODE

Applications Information

Product Description

The ISL97536 is a synchronous, integrated FET 1A step-down regulator which operates from an input of 2.5V to 6V. The output voltage is user-adjustable with a pair of external resistors.

The internally-compensated controller makes it possible to use only two ceramic capacitors and one inductor to form a complete, very small footprint 1A DC:DC converter.

PWM Operation

In PWM switching mode, the P-channel MOSFET and N-channel MOSFET always operate complementary. When the P-channel MOSFET is on and the N-channel MOSFET off, the inductor current increases linearly. The input energy is transferred to the output and also stored in the inductor. When the P-channel MOSFET is off and the N-channel MOSFET on, the inductor current decreases linearly, and energy is transferred from the inductor to the output. Hence, the average current through the inductor is the output current. Since the inductor and the output capacitor act as a low pass filter, the duty cycle ratio is approximately equal to V_O divided by V_{IN}.

The output LC filter has a second order effect. To maintain the stability of the converter, the overall controller must be compensated. This is done with the fixed internally compensated error amplifier and the PWM compensator. Because the compensations are fixed, the values of input and output capacitors are 10µF to 40µF ceramic and inductor is 1.5µH to 2.2µH.

Start-Up and Shutdown

When the EN pin is tied to V_{IN}, and V_{IN} reaches approximately 2.4V, the regulator begins to switch. The inductor current limit is gradually increased to ensure proper soft-start operation.

When the EN pin is connected to a logic low, the ISL97536 is in the shutdown mode. All the control circuitry and both MOSFETs are off, and V_{OUT} falls to zero. In this mode, the total input current is less than 1µA.

When the EN reaches logic HI, the regulator repeats the start-up procedure, including the soft-start function.

Current Limit and Short-Circuit Protection

The current limit is set at about 1.5A for the PMOS. When a short-circuit occurs in the load, the preset current limit restricts the amount of current available to the output, which causes the output voltage to drop as load demand increases. When the output voltage drops 30mV below the reference voltage, the converter will shutdown for a period of time, approximated by Equation 1, and then restart. If the overcurrent condition still exists, it will repeat the shutdown-wait-restart event. This is called a “hiccup” event. The average power dissipation is reduced, thereby reducing the likelihood of damage current and thermal conditions in the IC.

$$tHICCUP \approx \left(\frac{700\mu \cdot V_{IN}}{3} + 216\mu\right) \quad \text{(EQ. 1)}$$

Thermal Shutdown

Once the junction reaches about 145°C, the regulator shuts down. Both the P-channel and the N-channel MOSFETs turn off. The output voltage will drop to zero. With the output MOSFETs turned off, the regulator will cool down. Once the junction temperature drops to about 130°C, the regulator will perform a normal restart.

Thermal Performance

The ISL97536 is available in a fused-lead MSOP10. Compared with regular MSOP10 package, the fused-lead package provides lower thermal resistance. The θ_{JA} is +100°C/W on a 4-layer board and +125°C/W on 2-layer board. Maximizing the copper area around the pins will further improve the thermal performance.

RSI/POR Function

When powering up, the open-collector Power-On-Reset output holds low for about 100ms after V_O reaches the preset voltage. When the active-HI reset signal RSI is issued, POR goes to low immediately and holds for the same period of time after RSI comes back to LOW. The output voltage is unaffected. (Please refer to the timing diagram). When the function is not used, connect RSI to ground and leave open the pull-up resister R_4 at POR pin.

The POR output also serves as a 100ms delayed Power Good signal when the pull-up resister R_4 is installed. The RSI pin needs to be directly (or indirectly through a resister R_6) connected to Ground for this to function properly.

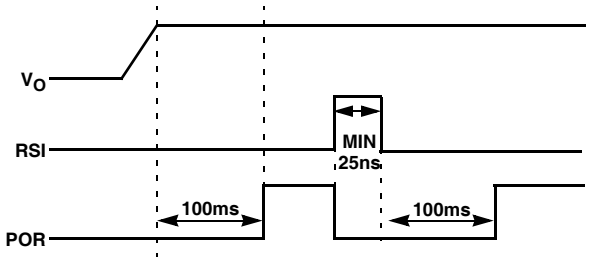


FIGURE 18. RSI AND POR TIMING DIAGRAM

Output Voltage Selection

Users can set the output voltage of the variable version with a resister divider, which can be chosen based on the following formula:

$$V_O = 0.8 \times \left(1 + \frac{R_2}{R_1}\right) \quad \text{(EQ. 2)}$$

Component Selection

Because of the fixed internal compensation, the component choice is relatively narrow. For a regulator with fixed output voltage, only two capacitors and one inductor are required. Capacitors must be chosen in the range of 10µF to 40µF, multilayer ceramic capacitors with X5R or X7R rating for both the input and output capacitors, and inductors in the range of 1.5µH to 2.2µH.

The RMS current present at the input capacitor is decided by the following formula:

$$I_{INRMS} = \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}} \times I_O \quad \text{(EQ. 3)}$$

This is about half of the output current I_O for all the V_O. This input capacitor must be able to handle this current.

The inductor peak-to-peak ripple current is given as:

$$\Delta I_{IL} = \frac{(V_{IN} - V_O) \times V_O}{L \times V_{IN} \times f_S} \quad \text{(EQ. 4)}$$

L is the inductance

f_S the switching frequency (nominally 1.4MHz)

The inductor must be able to handle I_O for the RMS load current, and to assure that the inductor is reliable, it must handle the 2A surge current that can occur during a current limit condition.

In addition to decoupling capacitors and inductor value, it is important to properly size the phase-lead capacitor C_4 (Refer to the Typical Application Diagram). The phase-lead capacitor creates additional phase margin in the control loop by generating a zero and a pole in the transfer function. As a general rule of thumb, C_4 should be sized to start the phase-lead at a frequency of ~2.5kHz. The zero will always appear at lower frequency than the pole and follow the equation below:

$$f_Z = \frac{1}{2\pi R_2 C_4} \quad \text{(EQ. 5)}$$

Over a normal range of R_2 (~10-100k), C_4 will range from ~470-4700pF. The pole frequency cannot be set once the zero frequency is chosen as it is dictated by the ratio of R_1 and R_2, which is solely determined by the desired output set point. The equation below shows the pole frequency relationship:

$$f_P = \frac{1}{2\pi (R_1 || R_2) C_4} \quad \text{(EQ. 6)}$$

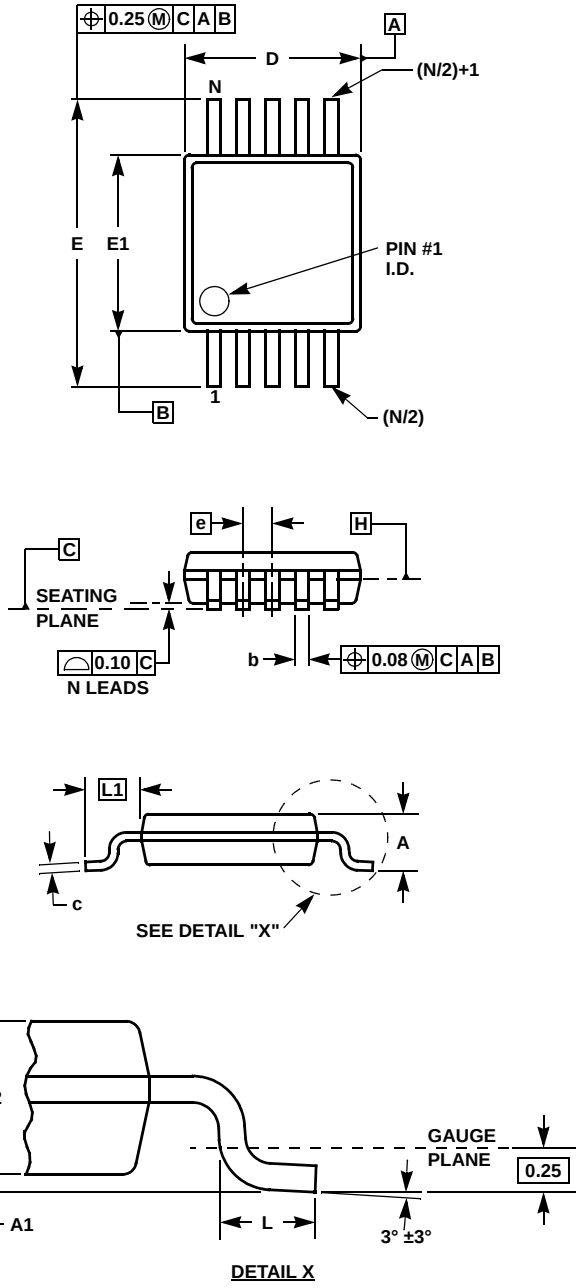
Layout Considerations

The layout is very important for the converter to function properly. The following PC layout guidelines should be followed:

1. Separate the Power Ground (⏚) and Signal Ground (⏚); connect them only at one point right at the pins
2. Place the input capacitor as close to V_{IN} and PGND pins as possible
3. Make the following PC traces as small as possible:
   - from LX pin to L
   - from C_O to PGND
4. If used, connect the trace from the FB pin to R_1 and R_2 as close as possible
5. Maximize the copper area around the PGND pin
6. Place several via holes under the chip to additional ground plane to improve heat dissipation

The demo board is a good example of layout based on this outline. Please refer to the ISL97536 Application Brief.

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MSOP8	MSOP10	TOLERANCE	NOTES
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. C 6/99

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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