LXP710

HDSL Framer/Mapper for 1168 kbps Applications

General Description

The LXP710 is a complete HDSL framer/mapper that multiplexes and demultiplexes a framed or unframed 2.048 Mbps E1 data stream onto two 1168 kbps HDSL lines. The LXP710 also supports point-to-point and point-to-multipoint fractional E1 applications with 1, 2 or 3 HDSL lines.

The LXP710 interfaces directly with the Level One SK70704/SK70707 1168 kbps HDSL data pump and industry standard E1 Framers or Line Interface ICs. The framer/mapper is controlled and monitored by an external processor using an 8-bit Intel or Motorola compatible parallel interface. The framer/mapper provides both programmable and 6ms interrupts synchronized to the HDSL frame rate.

The LXP710 provides fully programmable mapping between the E1 and HDSL interfaces on one or more loops. The LXP710 provides support for system performance monitoring with internal CRC, FEBE and BPV error counters and the capability to inject these errors.

The framer/mapper automatically controls the synchronization between the HDSL loop timing and the E1 payload timing using a digital PLL for E1 timing recovery and a transmitter stuffing control circuit.

Features

- Compliant with ETSI ETR-152 requirements
- Interfaces with 1, 2 or 3 Level One HDSL Data Pumps and industry standard E1 Framers or Line Interface ICs
- 8-bit, Intel or Motorola compatible parallel processor interface with programmable and 6ms interrupts
- E1 to HDSL Loop Multiplexing/Demultiplexing
  - Programmable timeslot mapping
  - Accepts framed or unframed E1 data
  - IDLE Code Insertion provides channel blocking in mux and demux directions
  - DS0 Channel Grouping
  - Loopbacks toward E1 and HDSL interfaces
- Diagnostics/Performance Monitoring
  - QRSS Pattern Generation and Detection
  - CRC, BPV and FEBE counters and error generators
- User definable 10 kbps overhead channel
- HDSL Overhead Management
- DPLL for E1 Timing Recovery
- HDSL Transmit Stuffing Control

LXP710 Block Diagram

