NJU6470

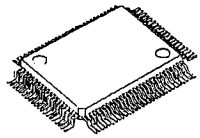
PRELIMINARY

16-CHARACTER 1-LINE DOT MATRIX LCD CONTROLLER DRIVER WITH KEYSCAN

■GENERAL DESCRIPTION

The NJU6470 is a Dot Matrix LCD controller driver for 16-character 1-line with keyscan in single chip.
It contains keyscan circuit and input/output ports, bleeder resistance, oscillation circuit, microprocessor interface circuits,instruction decoder controller, character generator ROM/RAM,high voltage operation common and segment drivers.
The microprocessor serial interface circuit which operates by 1MHz is incorporated.
The character generator ROM consists of 7,680 bits stores 192 kinds of 5 x 8 dots character Font. Each 160 bits CG RAM and Icon display RAM stores 4 kinds of special character displayed on the dot matrix display area and 80 kinds of Icon on the Icon display area.
The 18-common and 40-segment drivers operated up to 16-character 1-line with 80 Icon and static segment LCD display.

■PACKAGE OUTLINE



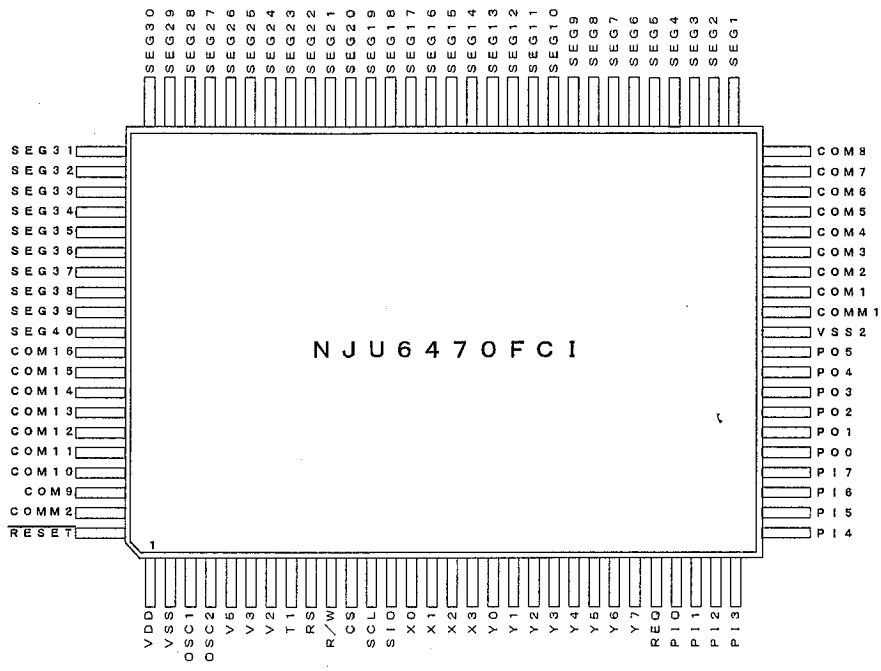
NJU6470F

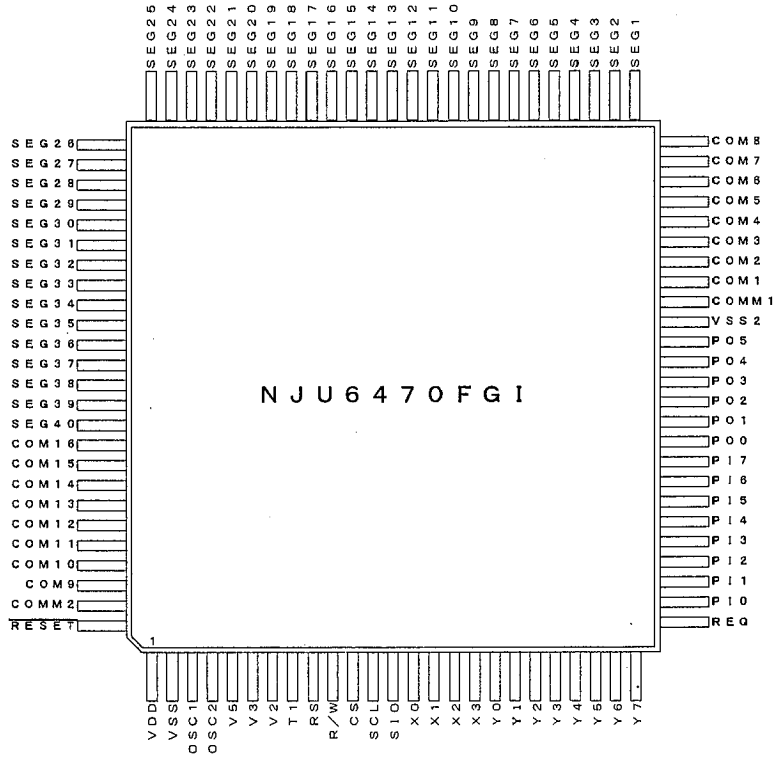
■FEATURES

- 16-character 1-line Dot Matrix LCD Controller Driver
- Maximum 80 Icon Display
- Serial Direct Interface with Microprocessor
- Display Data RAM - 16 x 8 bits : Maximum 16-character 1-line Display
- Character Generator ROM - 7,680 bits : 192 Characters for 5 x 8 Dots
- Character Generator RAM - 32 x 5 bits : 4 Patterns(5 x 8 Dots)
- Icon Display RAM - 16 x 5 bits : Maximum 80 Icon
- High Voltage LCD Driver : 18-common / 40-segment
- Duty and Bias Ratio : 1/18 duty and 1/5 bias
- Useful Instruction Set : Clear Display, Return Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift
- 32key input (4x8 keyscan)
- Bleeder resistance on-chip
- Low Power Consumption
- Operating Voltage --- 4.5 to 5.5 V (Except LCD Driving Voltage)
- Package Outline --- QFP100
- C-MOS Technology

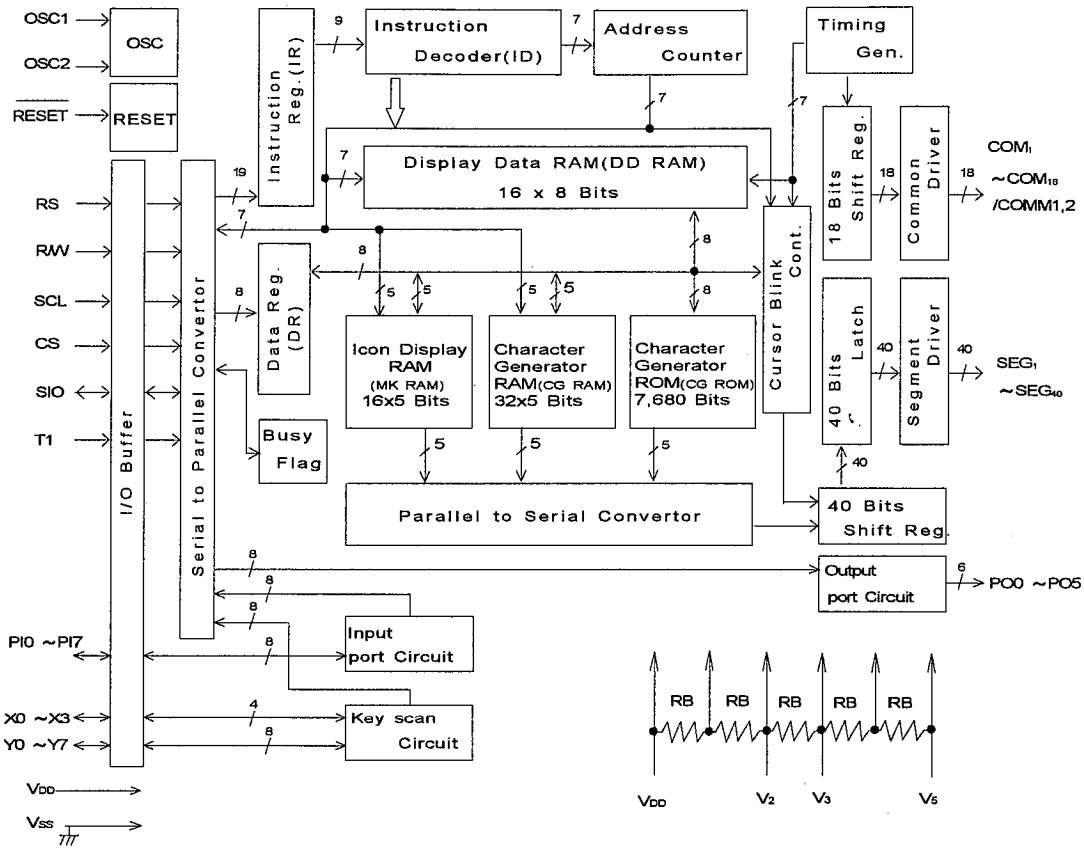
Jun.1999
Ver.1

■PIN CONFIGURATION





■ BLOCK DIAGRAM



■TERMINAL DESCRIPTION

PAD No.	SYMBOL	I/O	FUNCTION
1	VDD	I	Power Source (+5V)
2	VSS	I	Power Source (GND)
3 4	OSC1 OSC2	I O	Oscillation terminal : External R connects to these terminals For external clock operation, the clock should be input on OSC1 terminal and OSC2 terminal should be open.
5 6 7	V5 V3 V2	I	LCD Driving Power Sourse
8	T1	I	Maker test terminal "1" : Busy or address or RAM data read "0" : Normally
9	RS	I	Register selection signal input terminal
10	R/W	I	Read / Write selection signal input terminal
11	$\overline{CS}$	I	Chip select signal input terminal
12	SCL	I	Sift clock input terminal
13	SIO	I/O	Serial Data I/O terminal
14∽17	X0∽X3	I/O	Keyscanning terminal When this terminal is not used ,should be open .
18∽25	Y0∽Y7	I/O	Keyscanning terminal When this terminal is not used ,should be open .
26	REQ	O	Keyscan request signal terminal "1" : Push any key "0" : Normally
27∽34	PI0∽PI7	I	Input port terminal
35∽40	PO0∽PO5	O	Output port terminal Terminal structure is Nch open-drain.
41	VSS2	I	Output port use GND Same voltage to VSS and VSS2
42	COMM1	O	Icon Common Driving Signal terminal
43∽50	COM1∽8	O	LCD Common Driving Signal terminals
51∽90	SEG1∽40	O	LCD Segment Driving Signal terminals
91∽98	COM16∽9	O	LCD Common Driving Signal terminals
99	COMM2	O	Icon Common Driving Signal terminal
100	$\overline{RESET}$	I	Reset terminal When the "L" level is input over 1.8uS to this terminal, the system is reset.

■ FUNCTIONAL DESCRIPTION

(1-1)Register

The NJU6470 incorporates 8-bit registers, an Instruction Register(IR), a Data Register(DR) a Key Register(KR), an Output port Register(LR) and an Input port Register(PR). The Register(IR) stores instruction codes such as "Clear Display" and "Cursor Shift" or address data for Display Data RAM(DD RAM), Character Generator RAM(CG RAM) and Icon Display RAM (MK RAM).
The MPU writes the instruction code and address data to the Register(IR), but it does not read out from the Register(IR).
The Register(DR) is a temporary stored register, the data stored in the Register(DR) is written into the DD RAM, CG RAM or MK RAM and read out from the DD RAM, CG RAM or MK RAM.
The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM, CG RAM or MK RAM by internal operation. The Register(KR,LR,PR) is a temporary stored register, the key scan data(KR), output port data(LR) and input port data(PR) are stored in the each Register.
These registers are selected by the selection signal T1 and RS as shown below.
Table 1. shows register operation controlled by T1, RS and R/W signals.

Table 1. Register Operation

T1	RS	R/W	Selected Register	Operation
0	0	0	IR	Write
0	0	1	PR	Read (Input port data)
0	1	0	DR,LR	Write (DR to DD RAM, CG RAM or MK RAM) (LR:Output port data)
0	1	1	KR	Read (Key scan data)
1	0	1	IR	Read busy flag and address counter
1	1	1	DR	Read (DD RAM, CG RAM or MK RAM to DR)

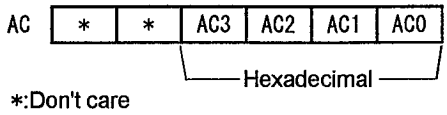
(1-2)Address Counter(AC)

The address counter(AC) addresses the DD RAM, CG RAM or MK RAM.
When the address setting instruction is written into the Register(IR), the address information is transferred from Register(IR) to the Counter(AC). The selection of either the DD RAM, CG RAM or MK RAM is also determined by this instruction.
After writing (or reading) the display data to (or from) the DD RAM, CG RAM or MK RAM, the Counter(AC) increments (or decrements) automatically.
The address data in the Counter(AC) is output from SIO when T1="1", RS="0" and R/W="1" as shown in Table 1.

(1-3)Display Data RAM(DD RAM)

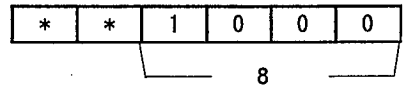
The display data RAM (DD RAM) consists of 16 x 8 bits, stores up to 16-character display data represented in 8-bit code.

The DD RAM address data set in the address counter(AC) is represented in Hexadecimal.



*:Don't care

(Example) DD RAM address "8"



(1-3-1)The relation between DD RAM address and display position on the LCD

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	←Display Position
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	←DDRAM Address(Hex.)

When the display shift is performed,the DD RAM address changes as follows:

(Left Shift Display)

(0)←	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0

(Right Shift Display)

F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	→(F)

(1-4)Character Generator ROM(CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 8 dots character pattern represented in 8-bit character code.The storage capacity is up to 192 kinds of 5 x 8 dots character pattern.

The correspondence between character code and standard character pattern of NJU6470 is shown in Table 2.

User-defined character patterns (Custom Font) are also available by mask option.

Table 2. CG ROM Character Pattern (ROM version 02)

Lower 4bit (Hexadecimal) \ Upper 4bit (Hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

※Character code (10)H～(1F)H, (80)H～(9F)H don't exist.

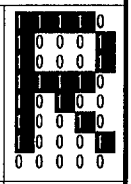
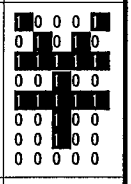
(1-5)Character Generator RAM(CG RAM)

The character generator RAM (CG RAM) stores any kind of character pattern in 5 x 8 dots written by the user program to display user's original character pattern. The CG RAM stores 4 kinds of character in 5 x 8 dots mode.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$-$(03)_H$ should be written to the DD RAM as shown in Table 2.

Table 3. shows the correspondence among the character pattern, CG RAM address and Data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern (5 x 7 dots)

Character Code (DDRAM Data)	CGRAM Address			Character Pattern (CGRAM Data)	
7 6 5 4 3 2 1 0 ← → Upper bit Lower bit	4 3 ← → Upper bit	2 1 0 → Lower bit		4 3 2 1 0 ← → Upperbit Lowerbit	
0 0 0 0 * * 0 0	0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1			Character Pattern Example(1) ←Cursor Position
0 0 0 0 * * 0 1	0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1			Character Pattern Example(2) ←Cursor Position
. . . . .	. . . . .	. . . . .		. . . . .	
0 0 0 0 * * 1 1	1 1	1 0 0 1 0 1 1 1 0 1 1 1			

Notes : 1. Character code bit 0,1 correspond to the CG RAM address bit 3,4(2bits:4 patterns).

2. CG RAM address bits 0 to 2 designate character pattern line position. The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 8th line should be "0". If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position corresponded to the CG RAM data bits 0 to 4 are shown above.
4. CG RAM character patterns are selected when character code bits 4 to 7 are all "0" and these are addressed by character code bits 0 and 1.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.
6. CG RAM address is linked with MK RAM address. MK RAM first address(20)H is next to CG RAM last address(1F)H. And CG RAM first address(00)H is next to MK RAM last address(2F)H.

(1-6)Icon Display RAM(MK RAM)
The NJU6470 displays maximum 80 Icons.
The Icon Display is controlled by writing the Data into MK RAM corresponds to the Icon.
The relation between MK RAM address and Icon Display position is shown below:

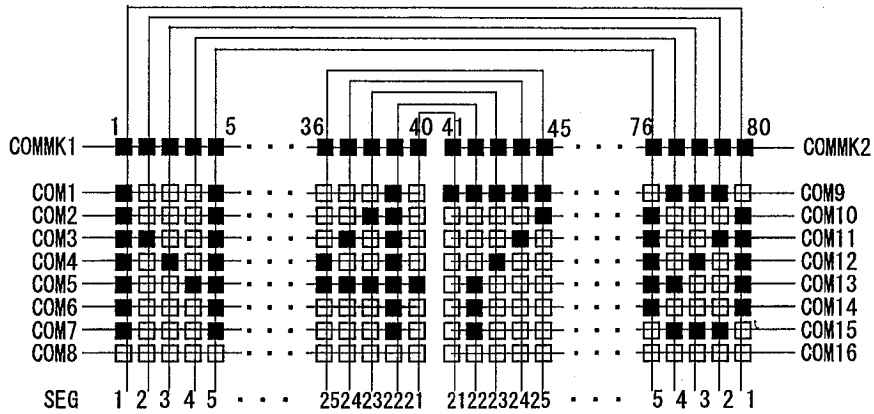


Table 4. Correspondence among Icon Position, MK RAM Address and Data

MK RAM Address (20H~2FH)		Bits for Icon Display Position							
		D7	D6	D5	D4	D3	D2	D1	D0
010 0000	20H	*	*	*	5	4	3	2	1
010 0001	21H	*	*	*	10	9	8	7	6
010 0010	22H	*	*	*	15	14	13	12	11
010 0011	23H	*	*	*	20	19	18	17	16
010 0100	24H	*	*	*	25	24	23	22	21
010 0101	25H	*	*	*	30	29	28	27	26
010 0110	26H	*	*	*	35	34	33	32	31
010 0111	27H	*	*	*	40	39	38	37	36
010 1000	28H	*	*	*	45	44	43	42	41
010 1001	29H	*	*	*	50	49	48	47	46
010 1010	2AH	*	*	*	55	54	53	52	51
010 1011	2BH	*	*	*	60	59	58	57	56
010 1100	2CH	*	*	*	65	64	63	62	61
010 1101	2DH	*	*	*	70	69	68	67	66
010 1110	2EH	*	*	*	75	74	73	72	71
010 1111	2FH	*	*	*	80	79	78	77	76

Notes: 1. When the Icon display function using, the system should be initialized by the software initialization because the MK RAM is not initialized by the power turning on and hardware reset.
2. The Icon display is not shifted by the display shift instruction.
3. MK RAM address is linked with CG RAM address. CG RAM first address(00)H is next to MK RAM last address(2F)H. And MK RAM first address(20)H is next to CG RAM last address(1F)H.

(1-7)Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM and MK RAM and other internal circuits.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

(1-8)LCD Driver

LCD Driver consists of 18-common driver and 40-segment driver.

The character pattern data are latched to the addressed Segment-register respectively. This latched data controls display driver to output LCD driving waveform.

(1-9)Cursor Blinking Control Circuit

This circuits controls cursor On/Off and the cursor position character blinks.

The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).

When the address counter is $(8)_H$, a cursor position is shown as follows:

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
AC	0	0	0	1	0	0	0

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	←Display Position
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	←DDRAM Address(Hex.)

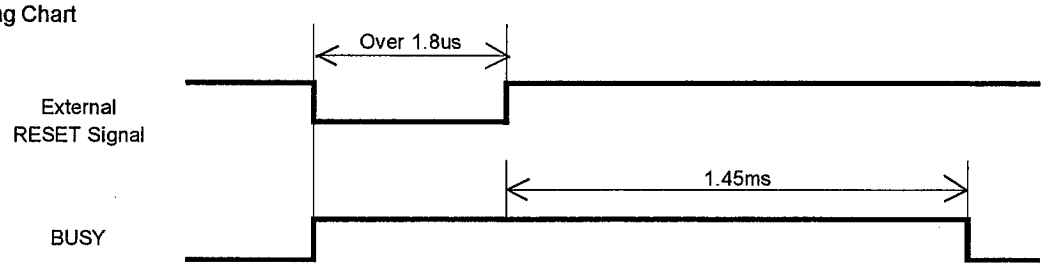
Cursor position

Note : The cursor or blinks also appear when the address counter (AC) selects the CG RAM or the MK RAM. But the displayed cursor and blink are meaningless.
If the AC storing the CG or MK RAM address data, the cursor and blink are displayed in the meaningless position.

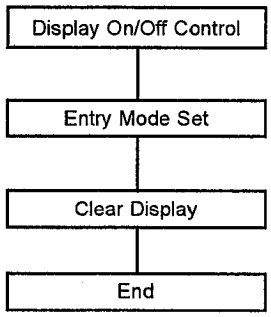
(1-10)Initialization By Hardware

The NJU6470 incorporates $\overline{\text{RESET}}$ terminal to initialize the all system. When the "L" level input over 1.8us to the $\overline{\text{RESET}}$ terminal, reset sequence is executed. In this time, busy signal output during 1.45 ms (fosc=69kHz) after $\overline{\text{RESET}}$ terminal goes to "H".

・Timing Chart



・Initialization flow



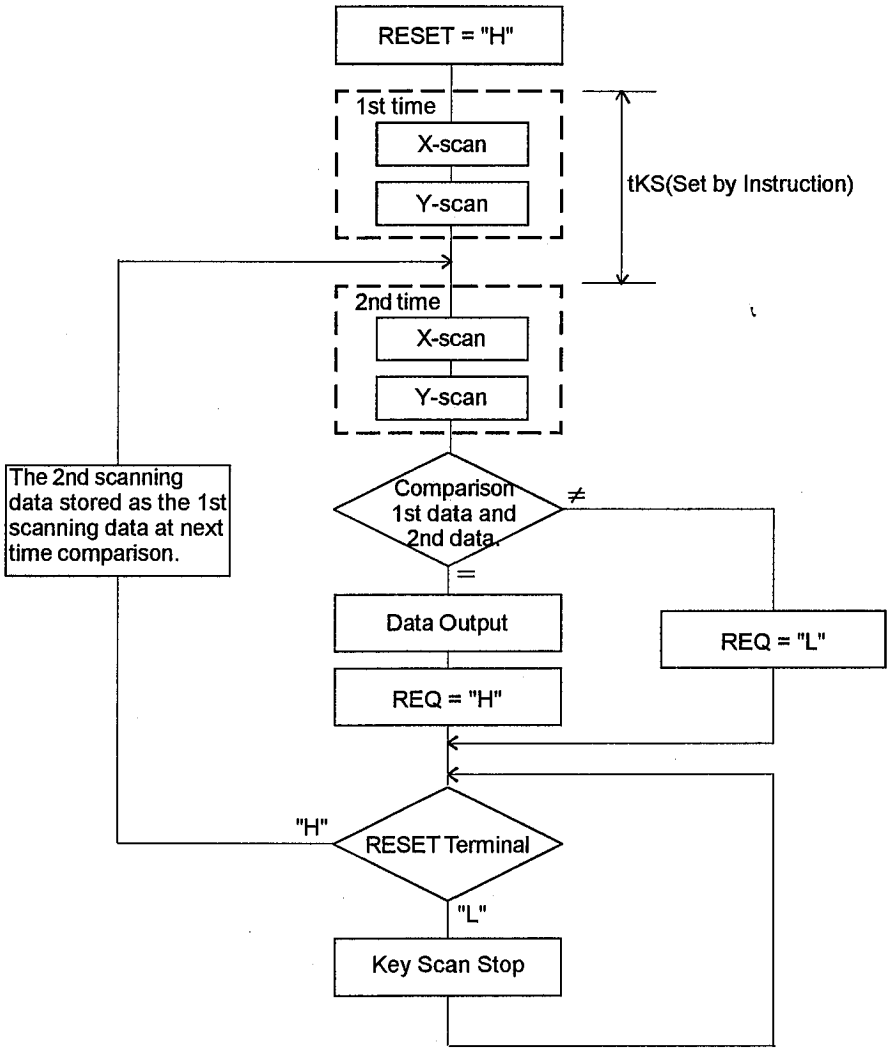
D=0 : Display Off
D=0 : Cursor Off
D=0 : Cursor Blink Off

I/D=1: Increment by 1
Y=0 : No Shift

(1-11)Key Scan

The Key scan function performs scanning 32 keys of the 8x4 matrix and the two times key scanning and data comparison to check key-in. When these data are the same value, the data is output.

(1-11-1)Internal operations of Key Scan Circuit



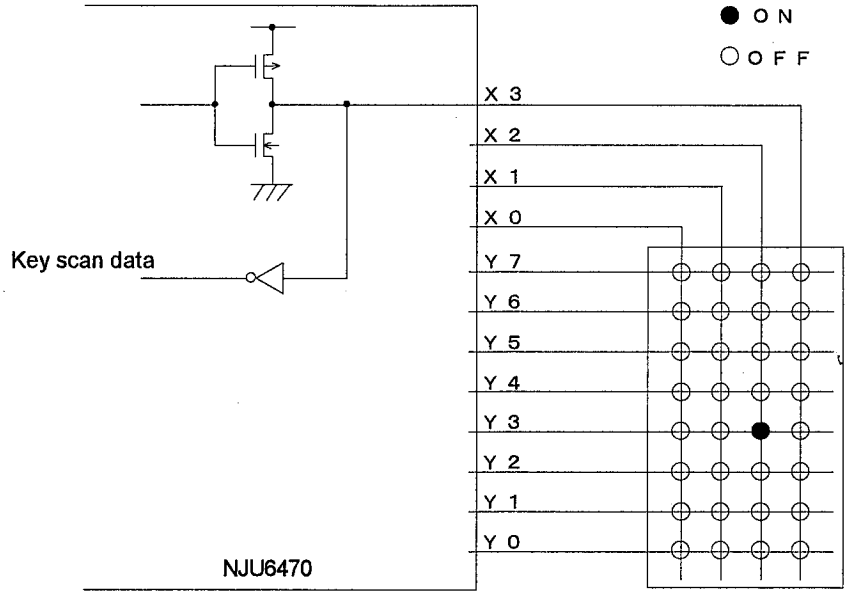
① When the RESET is released (RESET ="H") the scanning starts automatically.
When the initialization is executed, key scan data is "000"H, Sampling Rate is tKS 9.28mS (at fOSC=69kHz).
The key scanning is performed continuously until the RESET is executed (RESET ="L").

② The key scanning circuit executes X-scan and Y-scan in pairs, and executes it 2-time.
When the first scanning data and the second data are the same, the data is output and "H" is output to REQ terminal. When the first and second data are not the same, "L" level is output to REQ terminal.

③ The second scanning data is stored as the first data, and then the next scanning is executed as the second scanning.

(1-11-2)Composition of internal key scan circuit

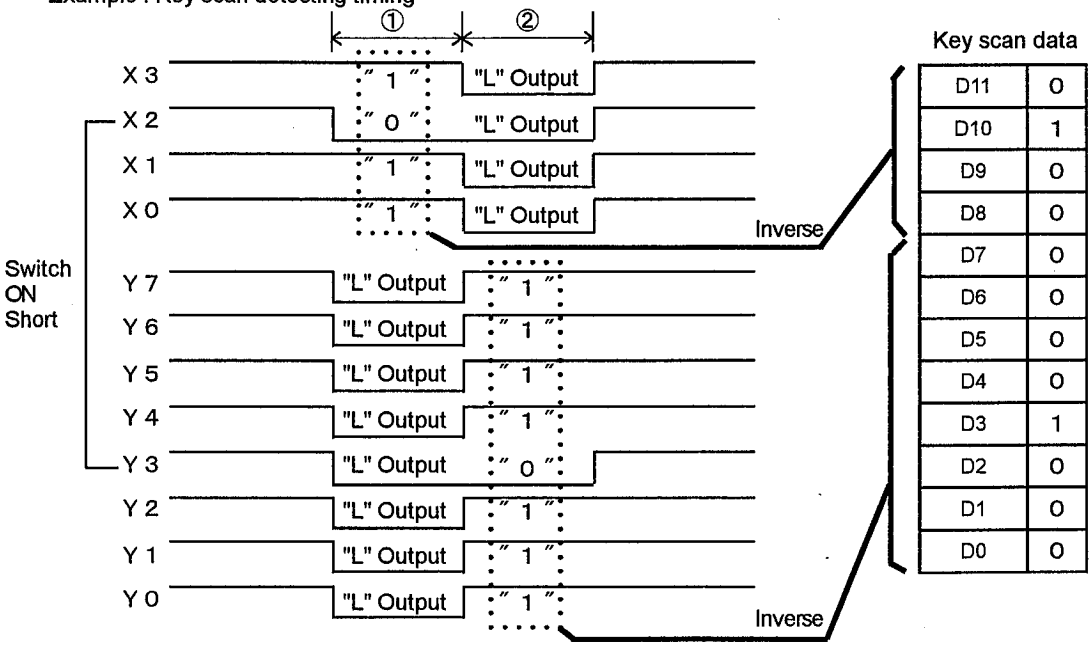
The composition of internal key scan circuit is shown below. X0 to X3 and Y0 to Y7 are the same circuits.
The key switches are connected to Xn wire and Ym wire as shown below. When the key switch is pressed, the Xn wire and Ym wire connected to the key switch should be shorted.



(1-11-3)Key scan detecting timing

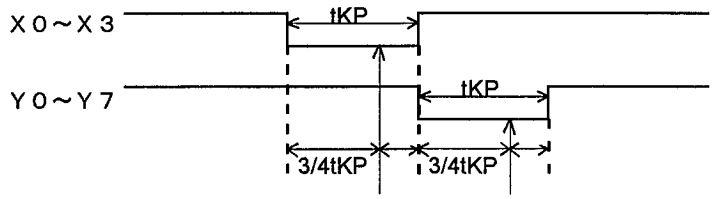
The key scan data detecting is sepalated to (X0 to X3) and (Y0 to Y7) as shown below.
In case of ① timing, (Y0 to Y7) are "L" and the inverted data of (X0 to X3) are detected as the scanning data.
In case of ② timing, (X0 to X3) are "L" and the inverted data of (Y0 to Y7) are detected as the scanning data.

Example : Key scan detecting timing



D11	0
D10	1
D9	0
D8	0
D7	0
D6	0
D5	0
D4	0
D3	1
D2	0
D1	0
D0	0

And key scan data detecting is shown below. Both (X0 to X3) and (Y0 to Y7) key scan data are took-in at the timing of 3/4 tKP (key scan pulse width) shown below.



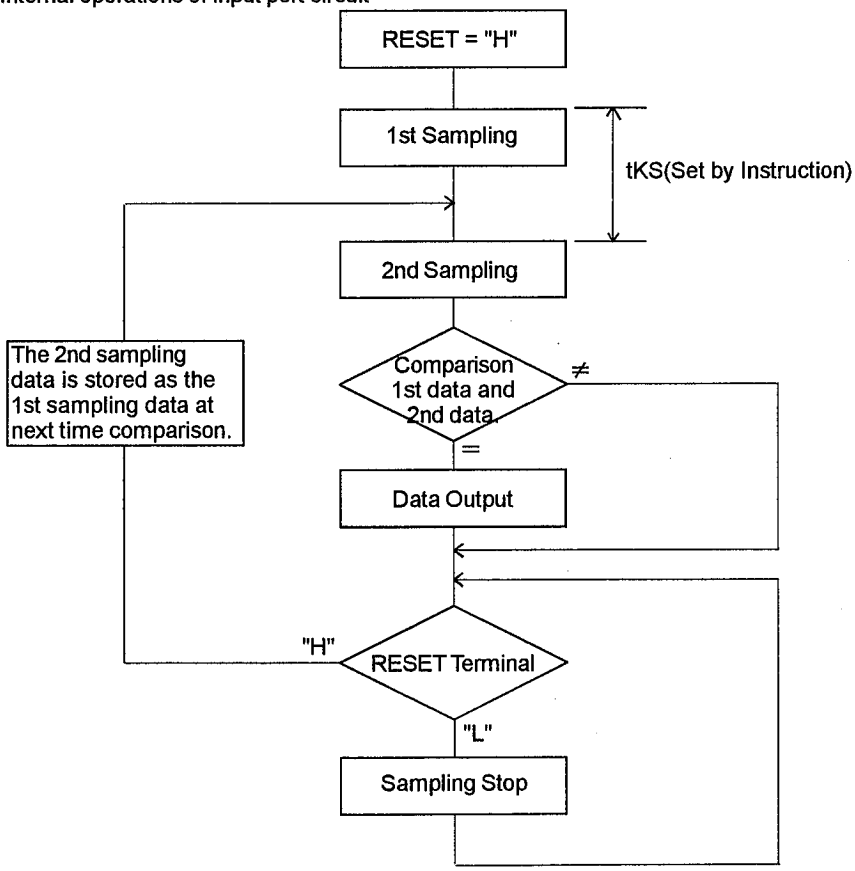
Key scan detecting timing

(1-12)Input port circuit

The input port circuit consists of 8 ports (PI0 to PI7), suitable for various sensor input.

The chattering is prevented by 2-time data sampling and compairing the each data.

(1-12-1)Internal operations of Input port circuit

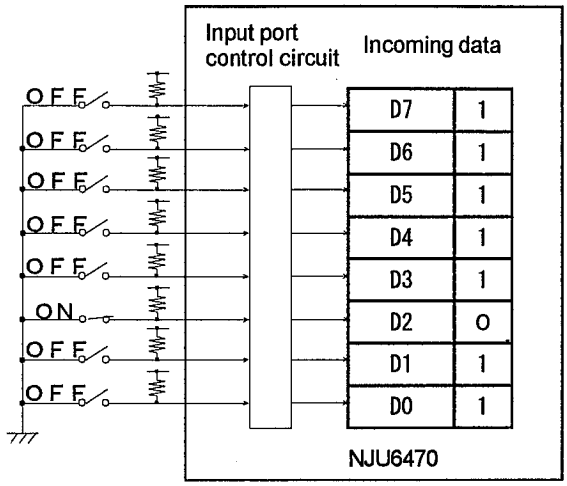


① When the RESET is released (RESET ="H") the sampling starts automatically.
When the initialization is executed, the input data is "00"H, Sampling Rate (tKS) is 9.28mS (at fOSC=69kHz).
The sampling is performed continuously until the RESET is executed (RESET ="L").

② The input port circuit executes data sampling 2-time.
When the first sampling data and the second data are the same, the data is output.

③ The second sampling data is stored as the first data, and then the next data sampling is executed as the second sampling.

(1-12-1)Example : Input port of inner composition



(1-13)Output port circuit

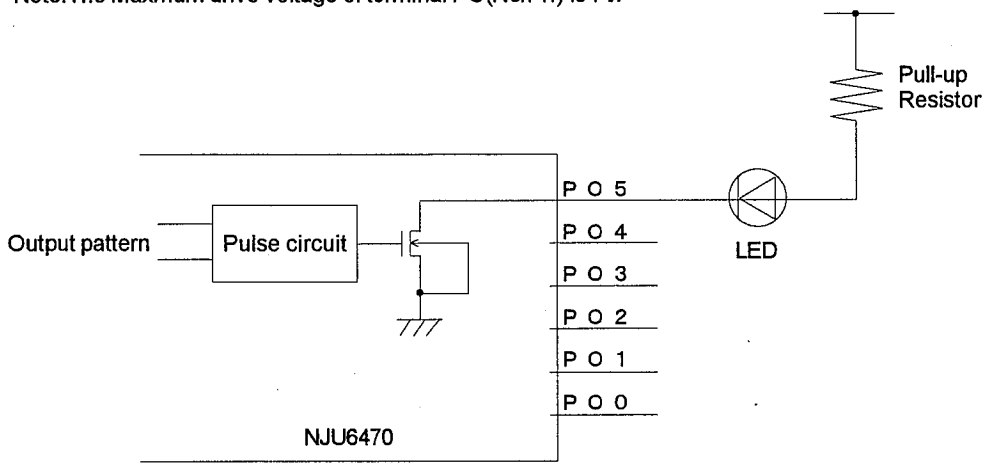
The output circuit consists N-ch open drain structure output port, 6-port (PO0 to PO5), suitable for LED driver. It also consists built in period programable pulse circuit, therefore it is able to blink LED by only 1-instruction.

(1-13-1)Inner composition of output circuit and Example of LED connecting

Inner composition of output circuit is shown below, and PO0 to PO5 are the same circuits.

ON : Turn On ..... "L" level output
OFF : Turn Off ..... High Inpedance
Pulse 1: (Blinking/0.5sec) ... Each 0.5sec repeat cycle (L→High Inpedance)
Pulse 2: (Blinking/1.0sec) ... Each 1.0sec repeat cycle (L→High Inpedance)
Pulse 3: (Blinking/2.0sec) ... Each 2.0sec repeat cycle (L→High Inpedance)

Note:The Maxmum drive voltage of terminal PO(Nch Tr) is 7V.



(2)Instructions

The NJU6470 incorporates two registers, an Instruction Register (IR) and a Data Register(DR).
These two registers store control information temporarily to allow interface between NJU6470 and MPU or peripheral ICs operating different cycles. The operation of NJU6470 is determined by this control signal from MPU. The control information includes register selection signals (RS), read/write signals (R/W), Test terminal and data bus signals (SIO).
Table 5. shows each instruction and its operating time.

Table 5. Table of Instructions

Instructions	Code																		Execute time
	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Maker Testing	0	0	0	*	*	*	*	*	*	*	*	0	0	0	0	0	0	0	0	217uS
Clear Display	0	0	0	*	*	*	*	*	*	*	*	0	0	0	0	0	0	0	1	1.38mS
Return Home	0	0	0	*	*	*	*	*	*	*	*	0	0	0	0	0	0	1	*	217uS
Entry Mode Set	0	0	0	*	*	*	*	*	*	*	*	0	0	0	0	0	1	I/D	S	217uS
Display On/Off Control	0	0	0	*	*	*	*	*	*	*	*	0	0	0	0	1	D	C	B	217uS
Coursor or Display Shift	0	0	0	*	*	*	*	*	*	*	*	0	0	0	1	S/C	R/L	*	*	290uS
Key Input Sampling Rate set	0	0	0	*	*	*	*	*	*	*	*	0	1	Input Port		Key Scan		*	*	217uS
Set DD RAM Address	0	0	0	*	*	*	*	*	*	*	*	1	0	*	*	DD RAM(0～F)H				217uS
Set CG/MK RAM Address	0	0	0	*	*	*	*	*	*	*	*	1	1	CG RAM(00～1F)H MK RAM(20～2F)H						217uS
Write Data to RAM	0	0	1	*	*	*	*	*	*	0	*	Write data(DD RAM)								217uS
												*	*	*	Write data(CG RAM) Write data(MK RAM)					
Write Data to Output Port	0	0	1	*	*	*	*	*	*	1	Output Pattern		*	P05	P04	P03	P02	P01	P00	0uS
Read Data from Input Port	0	1	0	*	*	*	*	*	*	*	*	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	0uS
Read Data from Key Scan	0	1	1	*	*	*	*	KX3	KX2	KX1	KX0	KY7	KY6	KY5	KY4	KY3	KY2	KY1	KY0	0uS
Read Busy Flag & Address	1	1	0	*	*	*	*	*	*	*	*	*	BF	A5	A4	A3	A2	A1	A0	0uS
Read Data from RAM	1	1	1	*	*	*	*	*	*	*	*	Read data(DD RAM)								290uS
												*	*	*	Read data(CG RAM) Read data(MK RAM)					

*:Don't care

Note : fosc=69KHz when the fosc changes, the execute time also changes.

(2-1)Description of each instructions

(a)Maker Testing

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	0	*	*	*	*	*	*	*	*	0	0	0	0	0	0	0	0

All "0" code in 4-bit length is using for device testing mode (only for maker).

(b)Clear Display

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	0	*	*	*	*	*	*	*	*	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code "1" is written into D_0.
When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address $(00)_H$ is set into the address counter and entry mode is set increment.
If the cursor or blink are displayed, they are returned to the left end of the 1st line in the LCD.
The (S) of entry mode, DD RAM, CG RAM, MK RAM do not change.

Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

(c)Return Home

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	0	*	*	*	*	*	*	*	*	0	0	0	0	0	0	1	*

Return home instruction is executed when the code "1" is written into D_1. When this instruction is executed, the DD RAM address $(00)_H$ is set into the address counter. Display is returned its original position if shifted, the cursor or blink are returned to the left end of the 1st line in the LCD if the cursor or blink are on the display.
The DD RAM contents do not change.

(d)Entry Mode Set

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	0	*	*	*	*	*	*	*	*	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into D_2 and the codes of (I/D) and (S) are written into D_1(I/D) and D_0(S), as shown below.
(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	Function
1	Address increment: The address of the DD RAM or CG RAM increment (+1) when the read/write, and the cursor or blink move to the right.
0	Address decrement: The address of the DD RAM or CG RAM decrement (-1) when the read/write, and the cursor or blink move to the left.

S	Function
1	Entire display shift The shift direction is determined by I/D.: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shift.

(e)Display ON/OFF Control

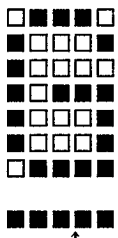
	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	0	*	*	*	*	*	*	*	*	0	0	0	0	1	D	C	B

Display On/Off control instruction which controls the display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into D_3 and the codes of (D), (C) and (B) are written into D_2(D), D_1(C) and D_0(B), as shown below.

D	Function
1	Display On.
0	Display Off.I n this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

C	Function
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

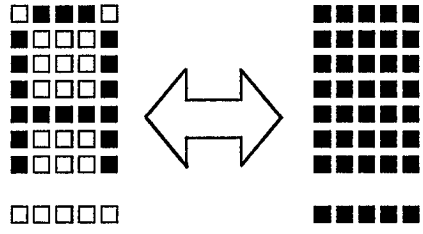
B	Function
1	The cursor position character is blinking. Blinking rate is 500ms at f_{osc}=69kHz. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Cursor

Character Font 5x7dots

(1)Cursor display example



Alternating display

(2)Blink display example

(f)Cursor/Display Shift

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	0	*	*	*	*	*	*	*	*	0	0	0	1	S/C	R/L	*	*

The Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display.
The contents of address counter(AC) does not change by operation of the display shift only.
This instruction is executed when the code "1" is written into D_4 and the codes of (S/C)and (R/L) are written into D_3(S/C) and D_2(R/L), as shown below.

S/C	R/L	Function
0	0	Shift the cursor position to the left ((AC) is decreased by 1)
0	1	Shift the cursor position to the right ((AC) is increased by 1)
1	0	Shift the entire display to the left and the cursor follows it.
1	1	Shift the entire display to the right and the cursor follows it.

(g)Key Input Sampling Rate set

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	0	*	*	*	*	*	*	*	*	0	1	Input port		Key scan		*	*

Key Input Sampling Rate set instruction sets the input data sampling rate (tKS) of Input port and Key scan. NJU6470 prevents the chattering by 2-time data sampling. There are 4 Sampling Rates as follows.
The sampling rate of input port and key scan are selected by writing the code as follows into D5,D4(Input port) and D3,D2(Key scan).

D5 D3	D4 D2	Sampling Rate(tKS) (fOSC=69KHz)
0	0	9.28(mS)
0	1	18.56(mS)
1	0	37.12(mS)
1	1	74.24(mS)

(h)Set DD RAM Address

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	0	*	*	*	*	*	*	*	*	1	0	*	*	DD RAM(0)H~(F)H			

Set DD RAM address instruction is executed when the code "1" is written into D_7, the code "0" is written into D_6 and the address is written into D_3 to D_0 as shown above.
The address data (D_3 to D_0) is written into the address counter (AC) by this instruction. After this instruction execution, the data writing/reading is performed into/from the addressed RAM.
The DD RAM address is set to (0)H automatically at initialization.

(i)Set CG/MK RAM Address

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	0	*	*	*	*	*	*	*	*	1	1	CG RAM(00)H~(1F)H MK RAM(20)H~(2F)H					

Set CG/MK RAM address instruction is executed when the code "1" is written into D_7, the code "1" is written into D_6 and the address is written into D_5 to D_0 as shown above.
The address data (D_5 to D_0) is written into the address counter (AC) by this instruction. After this instruction execution, the data writing/reading is performed into/from the addressed RAM.

(j)Write Data to RAM

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	1	*	*	*	*	*	*	0	*	Write data(DD RAM)							
												*	*	*	Write data(CG RAM) Write data(MK RAM)				

Write Data to RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W) and (T1).
By the execution of this instruction, the binary 8-bit data (D_7 to D_0) are written into the DD RAM, and the binary 5-bit data (D_4 to D_0) are written into the CG or MK RAM. The selection of RAM is determined by the previous instruction. After this instruction execution, the address increment(+1) or decrement(-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

(k)Write Data to Output Port

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	1	*	*	*	*	*	*	1	Output Pattern		*	PO5	PO4	PO3	PO2	PO1	PO0

Write data to output port instruction sets the output pattern of output port (LED drive port : PO5 to PO0). The output pattern is selected by writing the code as follows into D8,D7. When the code "1" is written into D5 to D0, the output ports are on. When the code "0" is written into D5 to D0, the output ports are off.

D8	D7	Output Pattern (fOSC=69kHz)
0	0	Turn on
0	1	Blink(Blinking rate :0.5s)
1	0	Blink(Blinking rate :1.0s)
1	1	Blink(Blinking rate :2.0s)

(l)Read Data from Input Port

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	0	*	*	*	*	*	*	*	*	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0

Read data from input port instruction is executed when the code "1" is written into R/W, and the data of input port (PI7 to PI0) is read out serially through the SIO terminal.
Because the input port data is set into the register by the fall edge of CS signal, the output data is not changed if the input port state is changed.

(m)Read Data from Key Scan

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	1	*	*	*	*	KX3	KX2	KX1	KX0	KY7	KY6	KY5	KY4	KY3	KY2	KY1	KY0

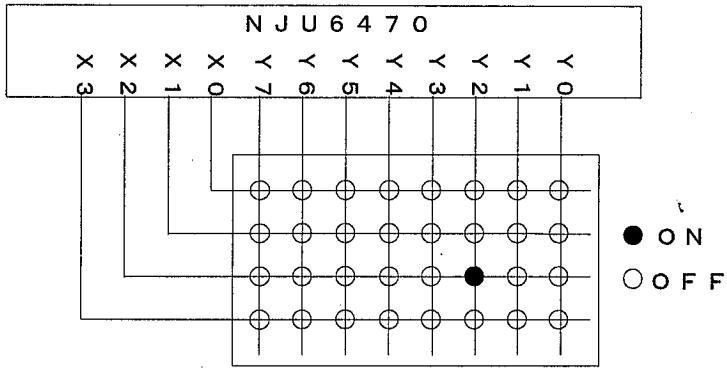
Read data from key scan instruction is executed when the code "1" is written into R/W, RS, and the data of key scan (KX3 to KX0, KY7 to KY0) is read out serially through the SIO terminal.

<Key Scan Data Format>

Key scan data is 12-bit data. Upper 4-bit corresponds to X3 to X0 terminals data, lower 8-bit corresponds to Y7 to Y0 terminals data.

When some key is pressed the bits corresponded to the pressed keys (X3 to X0, Y7 toY0) are "1", and the other bits are all "0". For example, when the key connected to X2 and Y2 is pressed, the key scan data bits of X2 (D10) and Y2 (D2) are "1", and the other bits are all "0".

Example 1. One key is pressed

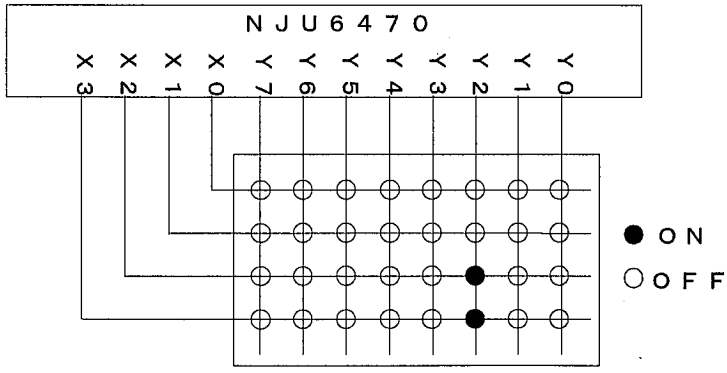


Read out data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	0	1	0	0	0	0	0	0	0	1	0	0
				←	X3~X0	→	←			Y7~Y0					→

In case of Example 2, the key roll over input is available. But in case of Example 3, the key roll over input is not available.

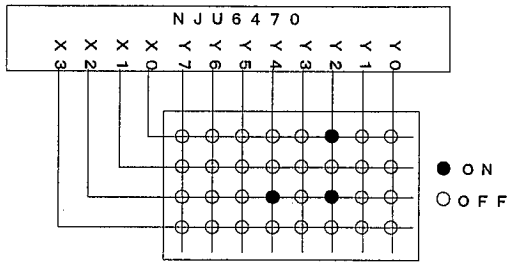
Example 2. The key roll over input①

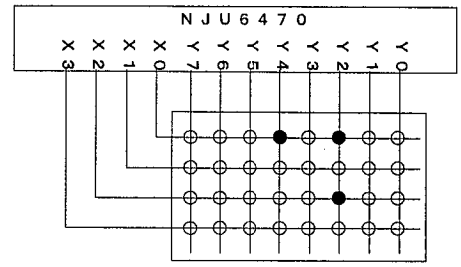


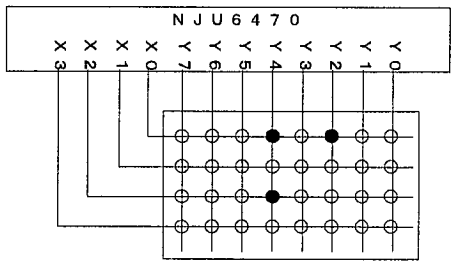
Read out data

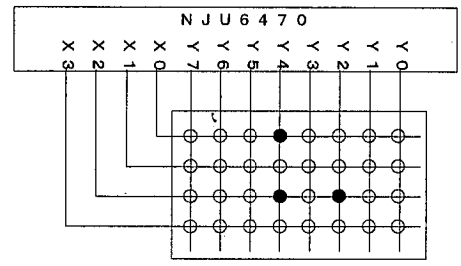
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	1	1	0	0	0	0	0	0	0	1	0	0
				←	X3~X0	→	←			Y7~Y0					→

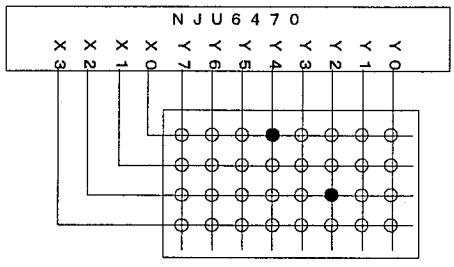
Example 3. The key roll over input②

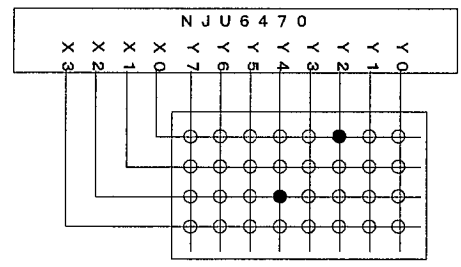


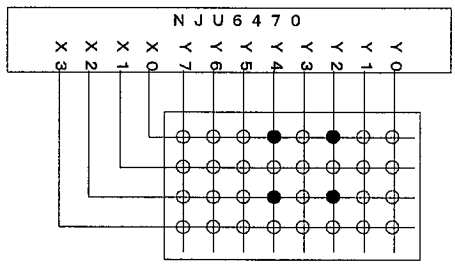












In the above seven cases, each read out key scan data is the same as follows.
Therefore the key scan data should be discriminated carefully, in case of the key roll over input.

Read out data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	0	1	0	1	0	0	0	1	0	1	0	0
				←	X3~X0		→	←			Y7~Y0				→

(n)Read Busy Flag & AC contents

	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	1	0	*	*	*	*	*	*	*	*	*	BF	A5	A4	A3	A2	A1	A0

Read busy flag & AC contents instruction is executed when the code "1" is written into T1, R/W, and the data of busy flag (BF) and address counter (A5 to A0) are read out serially through the SIO terminal.
This instruction reads out the internal status of the NJU6470. When this instruction is executed, the busy flag (BF) stored in D_6 and the address counter(AC) contents stored in D_5 to D_0 are read out.
The (BF)="1" indicates that internal operation is in progress. The next instruction is inhibited when (BF)="1". Check the (BF) status before the next write operation.

(o)Read Data from RAM

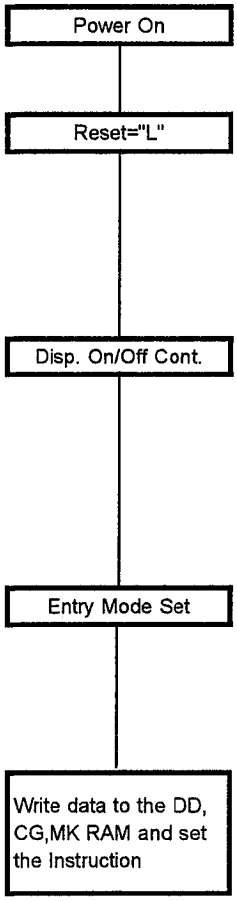
	T1	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	1	1	*	*	*	*	*	*	*	*	Write data (DD RAM)							
												*	*	*	Write data (CG RAM) Write data (MK RAM)				

Read Data from RAM instruction is executed when the code "1" is written into T1, RS and R/W, and DD or CG or MK RAM data is read out serially through the SIO terminal.
By the execution of this instruction, the binary 8-bit data (D_7 to D_0) is read out from the DD RAM, the binary 5-bit data (D_4 to D_0) is read out from the CG or MK RAM. The selection of RAM is determined by previous instruction. Before executing this instruction, RAM address set must be executed, otherwise the read out data is invalidated.
When this instruction is serially executed, the next address data is normally read from the second read.
The RAM address set instruction is not required when the cursor shift instruction is executed just beforehand (only DD RAM reading). The cursor shift instruction has same function as the DD RAM address set, so that after reading the DD RAM, the address increment or decrement is executed automatically according to the entry mode.
But display shift does not occur regardless of the entry mode.

Note : The address counter(AC) is automatically increased or decreased by 1 after write instruction to either of the DD RAM, CG RAM or DD RAM. Even if the read instruction is executed after this write instruction, the addressed data is not read out correctly.
For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

(2-2)The example of initialization using the internal reset circuits

The initialization is shown below from "Power on" to "display on".

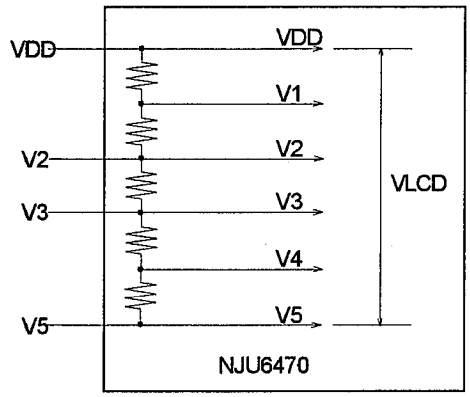


(3)Power Supply for LCD Driving

NJU6470 incorporates bleeder resistance to generate the LCD display driving waveform.
The bleeder resistance is set 1/5 bias suitable for 1/18 duty ratio.

LCD Driving Voltage vs Duty Ratio

Power Supply	Duty Ratio	1/18
	Bias	1/5
V2		VDD - 2/5VLCD
V3		VDD - 3/5VLCD
V5		VDD - VLCD

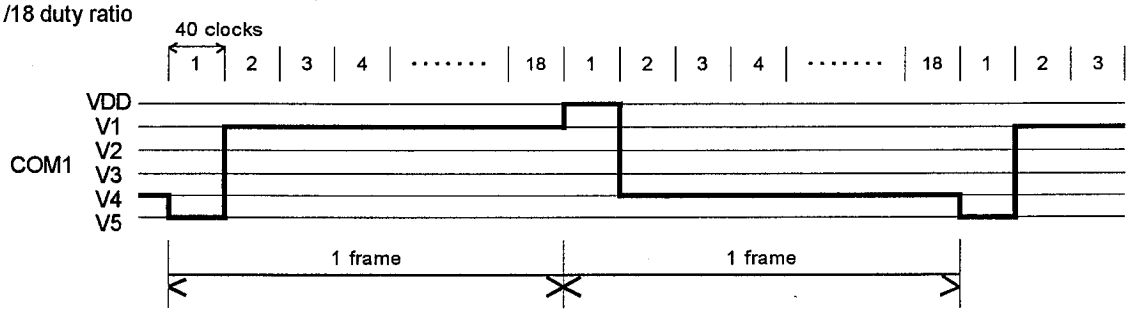


1/5 Bias (1/18 Duty Ratio)

(3-1)Relation between oscillation frequency and LCD frame frequency

The NJU6470 requires either one of the oscillation resistor(RF) for the internal oscillation, or external clock.
The LCD frame frequency example mentioned below is based on 69kHz oscillation.(1clock =14.5us, RF=430kΩ)

1/18 duty ratio

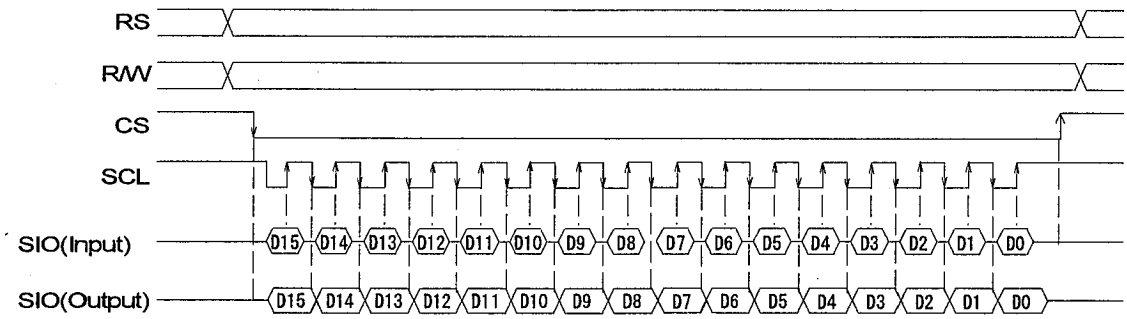


1 frame = 14.5(uS) x 40 x 18 = 10.44(mS)
Frame frequency = 1 / 10.44(mS) = 95.79(Hz)

(4)Interface with MPU

Serial interface circuit is activated when the chip select terminal (CS) goes to "L" level. The data input/output is MSB first like as the order of D_{15}, D_{14} $\cdots$ D_0.
The input data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The shift register converted to parallel data at the CS rise edge input.
In case of entering over than 16-bit data, valid data is last 16-bit data.
The output data is exited from the shift register synchronized at the fall edge of the serial clock SCL.
The time chart for the serial interface is shown below.

Note : The level ("L" or "H") of RS and R/W terminals should be set before CS terminal goes to "L" level.



■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	VDD	-0.3～+7.0	V
Input Voltage	VIN	-0.3～VDD+0.3	V
Operating Temperature	Topr	-30～80	°C
Storage Temperature	Tstg	-55～+125	°C

Note 1 : If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.
Note 2 : Decoupling capacitor should be connected between V_{DD} and V_{SS}, V_{DD} and V_5 due to the stabilized operation for the Voltage converter.
Note 3 : All voltage values are specified as V_{SS} = 0V
Note 4 : The relation : $V_{DD} > V_5 \geqq V_{SS}$, V_{SS}=0V must be maintained.

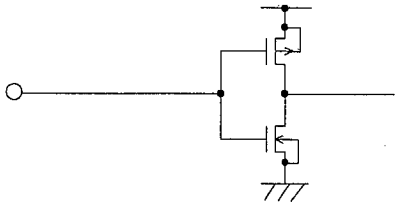
■ELECTRICAL CHARACTERISTICS (VDD=4.5V～5.5V,Ta=-20°C～+75°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	VIH1	Input Terminals (Except for RESET,OSC1 Term.)		2.3	-	VDD	V	5
	VIL1			-	-	0.8	V	5
	VIH2	RESET Terminal		-	-	0.7VDD	V	
	VIL2			0.3VDD	-	-	V	
	VIH3	OSC1 Terminal		-	-	VDD-1.0	V	
	VIL3			VSS+1.0	-	-	V	
Output Voltage	VOH1	SIO,REQ Terminals	-IOH=0.205mA	2.4	-	-	V	
	VOL1		IOL=1.6mA	-	-	0.4	V	
	VOL2	X0-3,Y0-7 Terminals	IOL=300uA	-	-	0.4	V	
	VOL3	PO0-6 Terminals	IOL=20mA	-	-	2.0	V	
Driver On-resist.(COM)	RCOM	±Id=50uA(All COM Term.)		-	-	20	KΩ	6
Driver On-resist.(SEG)	RSEG	±Id=50uA(All SEG Term.)		-	-	30	KΩ	7
Input Leakage Current	ILI	VIN=0～VDD, RESET Terminal		-1.0	-	1.0	uA	
Pull-up Resistance Current	-Ip	X0-3,Y0-7 Terminals, VDD=5V		50	125	250	uA	
Operating Current	IDD	VDD Terminal, fosc=69KHz		-	3.0	-	mA	8
Int. Bleeder Resist. LCD Bias Voltage	V2	VDD=5V,V5=0V,Ta=25°C		2.7	3.0	3.3	V	
	V3			1.7	2.0	2.3	V	
Int. Bleeder Resist. Bleeder resistance	RB	VDD-V5=5V,Ta=25°C		3.7	7.5	11.3	KΩ	9
Oscillation Frequency	fOSC	Rf=430kΩ, VDD=5V, Ta=25°C		48	69	90	kHz	
LCD Driving Voltage	VLCD	V5 Terminal,VDD=5V		VDD-3.0	-	VDD-5.0	V	10

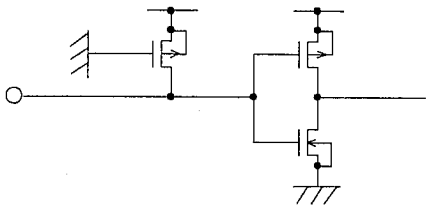
Note 5 : Input/Output structure except LCD driver are shown below:

Input Terminal Structure

REQ Terminal

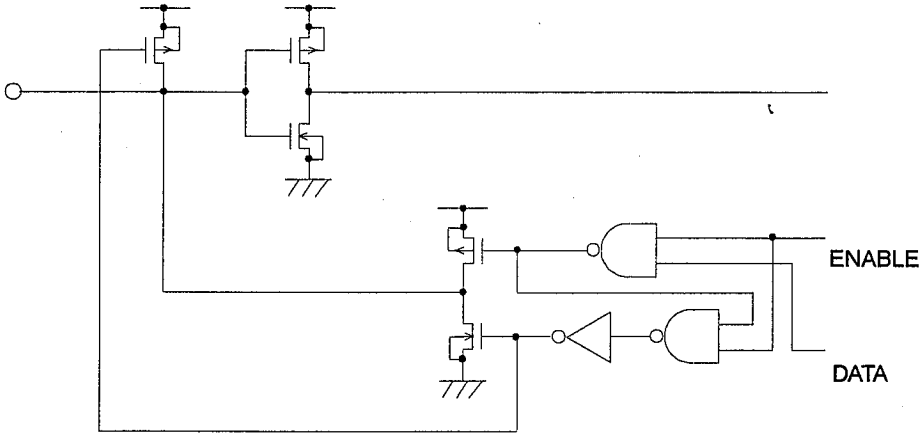


T1,RS,R/W,CS,SCL Terminals



Input/Output Terminal Structure

SIO Terminal



X0 to X3, Y0 to Y7 terminals : Refer to (1-11)Key scan
PO0 to PO5 terminals : Refer to (1-13)Output port circuit

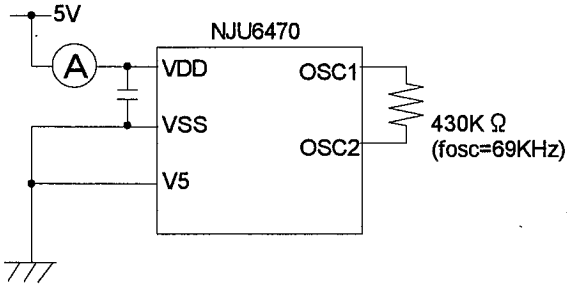
Note 6 : It is the resistance value between power supply terminals (VDD, VSS) and each COM terminals (COM1 to COM16, COMM1, COMM2), when the sink current (Id) is added to COM terminals.

Note 7 : It is the resistance value between power supply terminals (VDD, VSS, V3, V2) and each SEG terminals (SEG1 to SEG40), when the sink current (Id) is added to SEG terminals.

Note 8 : Except Input/output current but including the current flowing on bleeder resistance.
Besides, the following condition must be maintained.

- fosc=69KHz
- Initialization (After the RESET releasing and No instruction)
- Input terminals are VDD
- COM, SEG, X0～X3 and Y0～Y7 are open

- Operating Current Measurement Circuit



Note 9 : RB=(VDD-V5)/IB IB:Bleeder Resistance Current

Note10: Apply to the output voltage from each COM and SEG are less than ±0.15V against the LCD driving constant voltage (V_{DD}, V_5) at no load condition.

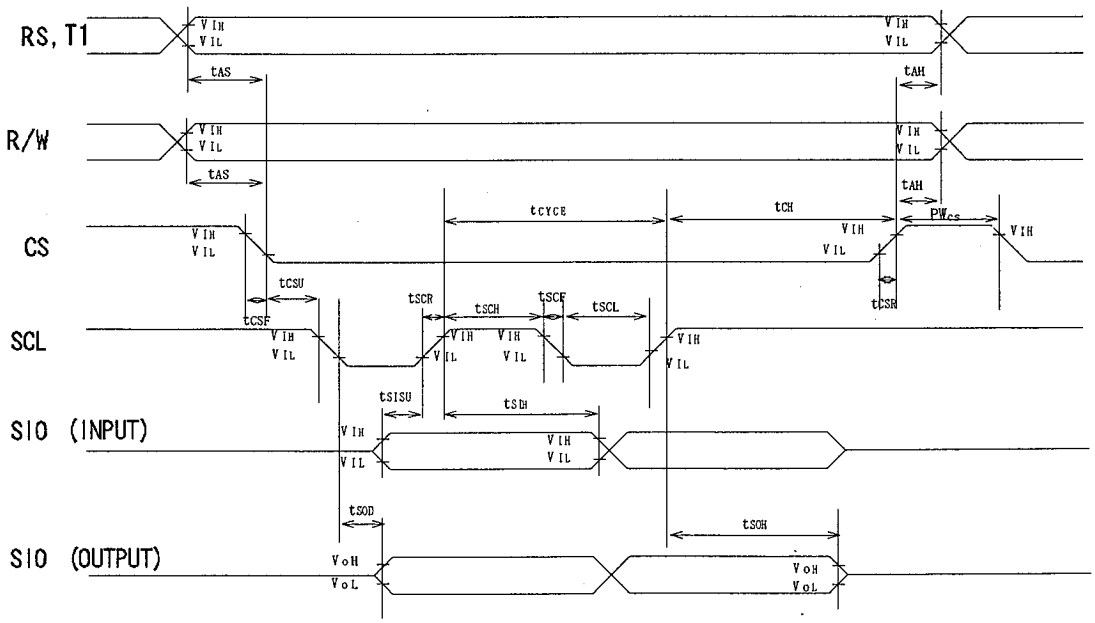
■ Bus timing characteristics

・Serial Interface Sequence (VDD=4.5V～5.5V,VSS=0V,Ta=-20℃～+75℃)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Serial Clock Cycle Time		tCYCE	1	-	uS	
Serial Clock Width	"H" level	tSCH	280	-	nS	
	"L" level	tSCL	680	-	nS	
Serial Clock rise and fall Time		tSCR,tSCF	-	20	nS	
Chip Select "H" level Pulse Width		PWCS	500+ α		nS	11
Chip Select Setup Time		tCSU	200	-	nS	
Chip Select Hold Time		tCH	200	-	nS	
Chip Select rise and fall Time		tCSR,tCSF	-	20	nS	
Setup Time	RS,R/W,T1	tAS	300	-	nS	
Hold Time	RS,R/W,T1	tAH	200	-	nS	
Serial Input Data Setup Time		tSISU	200	-	nS	
Serial Input Data Hold Time		tSIH	200	-	nS	
Serial Output Data Delay Time		tSOD	-	700	nS	
Serial Output Data Hold Time		tSOH	200	-	nS	

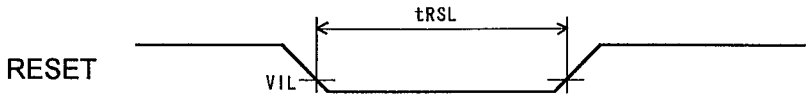
・SIO Load Condition : CL=100pF

Note 11: 500nS + Instruction execute time. Chip select "H" level pulse width (PWCS) is the period from rise edge of CS signal to fall edge of next CS signal. Therefore, the period depends on the instruction execute time.



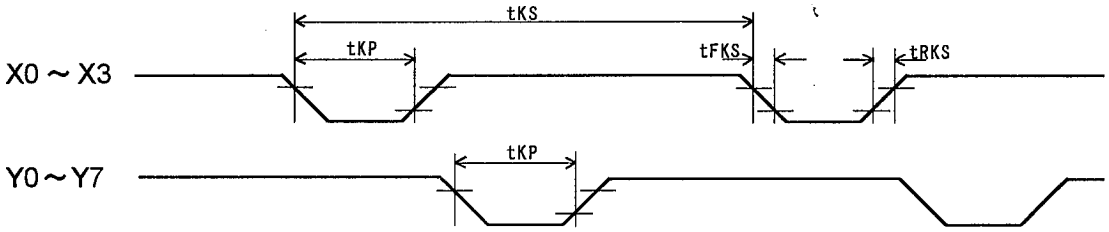
The timing characteristics of the serial bus write/read operating sequence

・The Input Condition when using the Hardware Reset Circuit



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Reset Input "L" Level Width	tRSL	1.8	-	-	uS	

・Key Scan Output Waveform

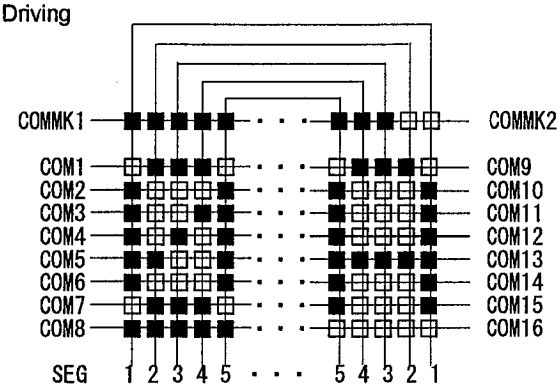


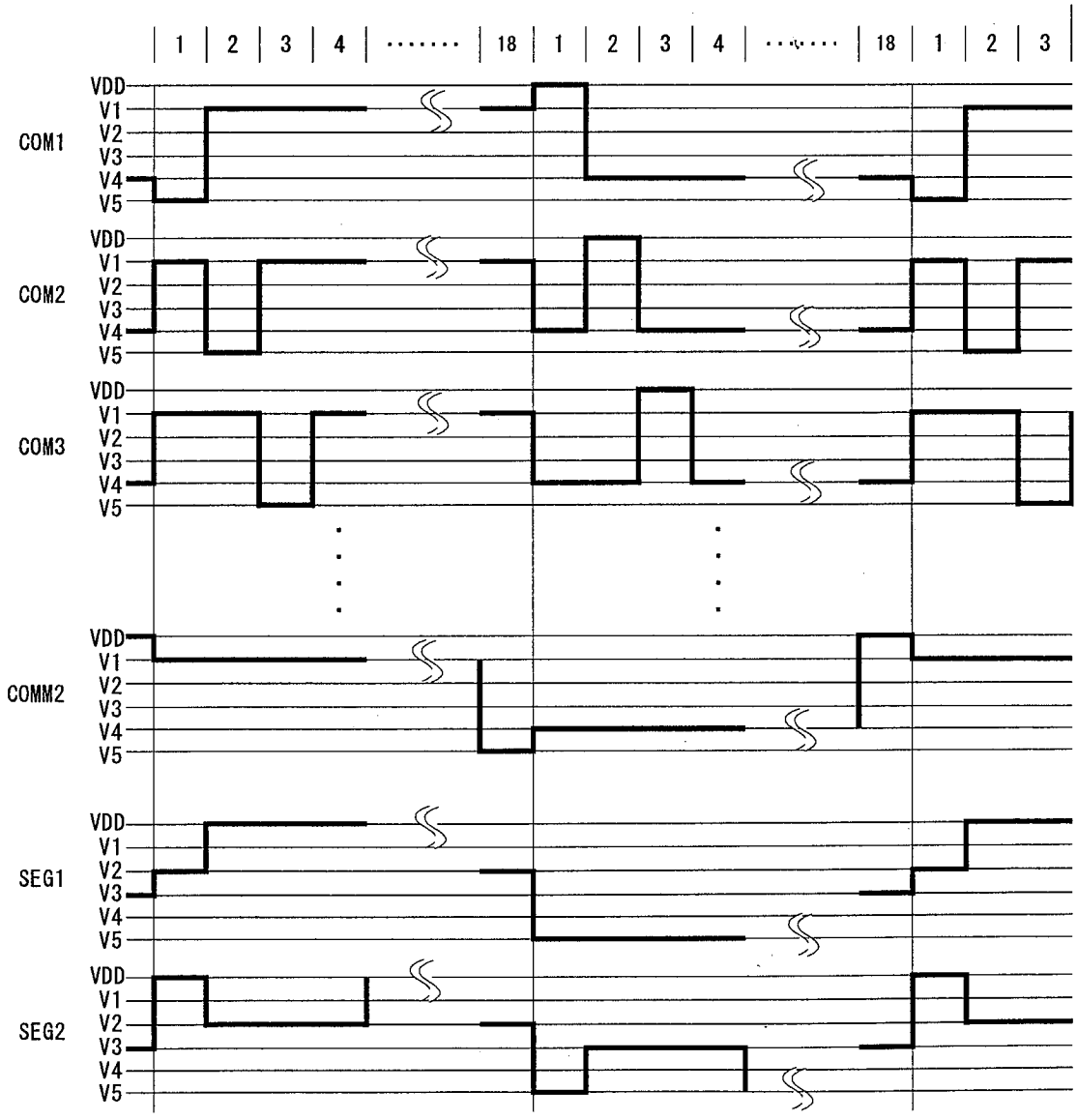
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Keyscan signal fall Time	tFKS	-	-	80	uS	
Keyscan signal rise Time	tRKS	-	-	80	uS	

Key scan sampling rate (tKS) is set by Key Input Sampling Rate set instruction.
The detail is shown in the instruction table.
tKP(key scan pulse width) = tKS / 8
Load Condition of X0 to X3,Y0 to Y7 : CL=100pF

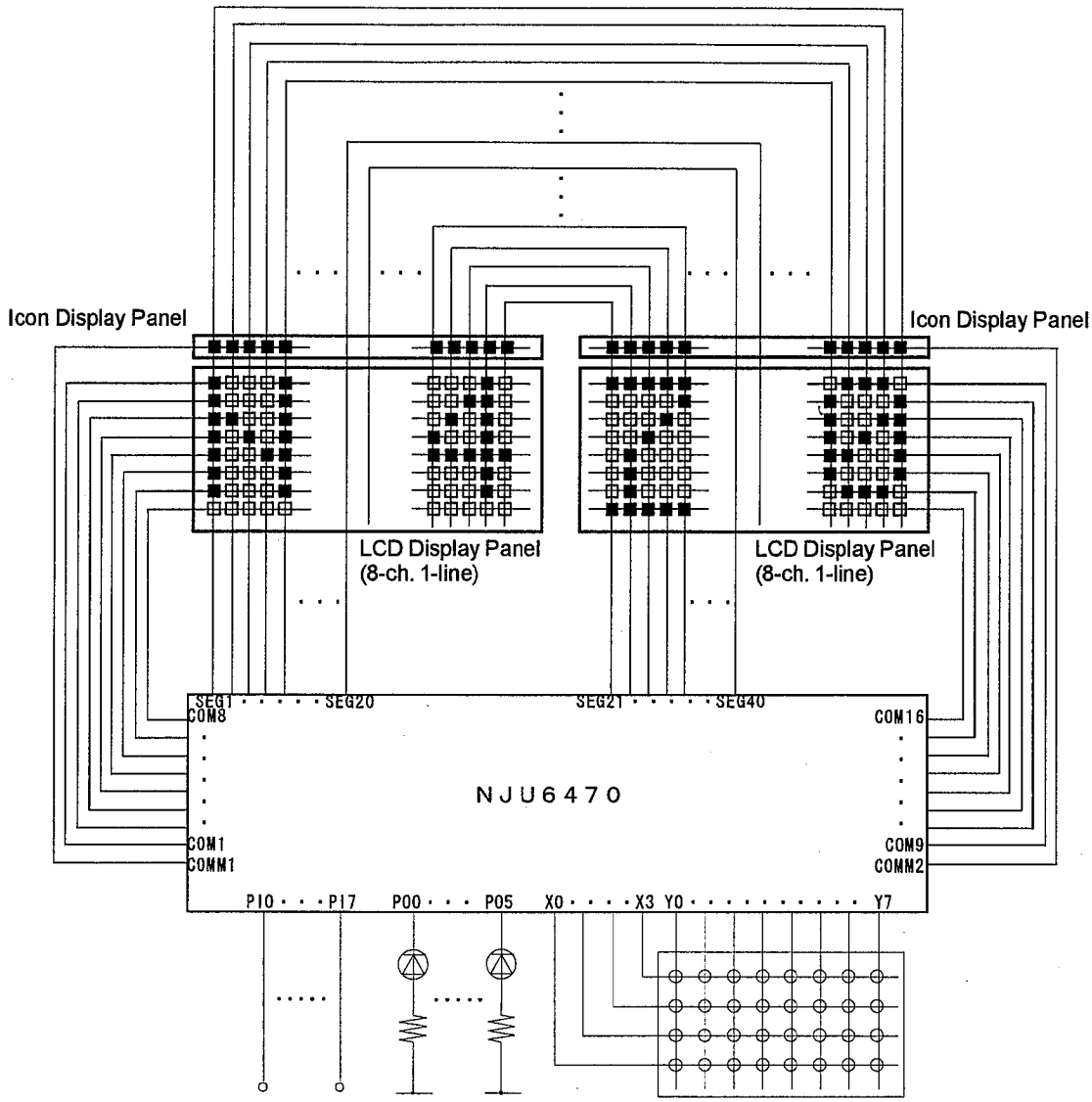
■LCD DRIVING WAVEFORM

1/18 Duty Driving





■APPLICATION CIRCUIT



16-character 1-line Display Example

MEMO

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