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FDP045N10A / FDI045N10A

N 沟道 PowerTrench® MOSFET

100 V、164 A、4.5 mΩ

特性

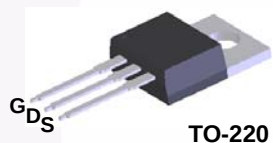
- $R_{DS(on)} = 3.8 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 100 \text{ A}$
- 快速开关速度
- 低栅极电荷, $Q_G = 54 \text{ nC}$ (典型值)
- 高性能沟道技术可实现极低的 $R_{DS(on)}$
- 高功率和高电流处理能力
- 符合 RoHS 标准

说明

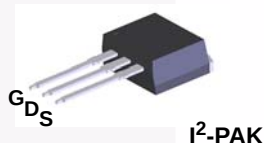
此 N 沟道 MOSFET 采用飞兆半导体先进的 Power Trench® 工艺生产, 这一先进工艺是专为最大限度地降低导通电阻并保持卓越开关性能而定制的。

应用

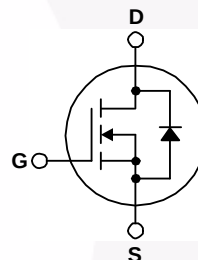
- 用于 ATX/ 服务器 / 电信 PSU 的同步整流
- 电池保护电路
- 电机驱动和不间断电源
- 微型光伏逆变器



TO-220



I²-PAK



MOSFET 最大额定值 $T_C = 25^\circ\text{C}$ 除非另有说明。

符号	参数	FDP045N10A_F102 FDI045N10A_F102	单位
V_{DSS}	漏极-源极电压	100	V
V_{GSS}	栅极-源极电压	± 20	V
I_D	漏极电流	- 连续 ($T_C = 25^\circ\text{C}$, 硅限制)	A
		- 连续 ($T_C = 100^\circ\text{C}$, 硅限制)	
		- 连续 ($T_C = 25^\circ\text{C}$, 封装限制)	
I_{DM}	漏极电流	- 脉冲 (说明 1)	A
E_{AS}	单脉冲雪崩能量	(说明 2)	mJ
dv/dt	二极管恢复 dv/dt 峰值	(说明 3)	V/ns
P_D	功耗	($T_C = 25^\circ\text{C}$)	W
		- 降低至 25°C 以上	W/ $^\circ\text{C}$
T_J, T_{STG}	工作和存储温度范围	-55 至 +175	$^\circ\text{C}$
T_L	用于焊接的最大引线温度, 距离外壳 1/8", 持续 5 秒	300	$^\circ\text{C}$

* 计算连续电流 (基于最高允许结温)。封装限制电流为 120 A。

热性能

符号	参数	FDP045N10A_F102 FDI045N10A_F102	单位
$R_{\theta JC}$	结至外壳热阻最大值	0.57	$^\circ\text{C/W}$
$R_{\theta JA}$	结至环境热阻最大值	62.5	

封装标识与订购信息

器件编号	顶标	封装	包装方法	卷尺寸	带宽	数量
FDP045N10A_F102	FDP045N10A	TO-220	塑料管	N/A	N/A	50 个
FDI045N10A_F102	FDI045N10A	I ² -PAK	塑料管	N/A	N/A	50 个

电气特性 $T_C = 25^\circ\text{C}$ 除非另有说明。

符号	参数	测试条件	最小值	典型值	最大值	单位
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关断特性

BV_{DSS}	漏极-源极击穿电压	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	100	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	击穿电压温度系数	$I_D = 250\ \mu\text{A}$, 参考温度为 25°C	-	0.07	-	V/ $^\circ\text{C}$
I_{DSS}	零栅极电压漏极电流	$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$	-	-	1	μA
		$V_{DS} = 80\ \text{V}$, $T_C = 150^\circ\text{C}$	-	-	500	
I_{GSS}	栅极-体漏电流	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	-	-	± 100	nA

导通特性

$V_{GS(th)}$	栅极阈值电压	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	漏极至源极静态导通电阻	$V_{GS} = 10\ \text{V}$, $I_D = 100\ \text{A}$	-	3.8	4.5	m Ω
g_{FS}	正向跨导	$V_{DS} = 10\ \text{V}$, $I_D = 100\ \text{A}$	-	132	-	S

动态特性

C_{iss}	输入电容	$V_{DS} = 50\ \text{V}$, $V_{GS} = 0\ \text{V}$ $f = 1\ \text{MHz}$	-	3960	5270	pF
C_{oss}	输出电容		-	925	1230	pF
C_{rss}	反向传输电容		-	34	-	pF
$C_{oss(er)}$	能量相关输出电容	$V_{DS} = 50\ \text{V}$, $V_{GS} = 0\ \text{V}$	-	1520	-	pF
$Q_{g(tot)}$	10 V 的栅极电荷总量	$V_{GS} = 10\ \text{V}$, $V_{DS} = 50\ \text{V}$, $I_D = 100\ \text{A}$	-	54	74	nC
Q_{gs}	栅极-源极栅极电荷		-	17	-	nC
Q_{gs2}	栅极平台电荷阈值		-	8	-	nC
Q_{gd}	栅极-漏极“米勒”电荷		-	13	-	nC
ESR	等效串联电阻 (G-S)	$f = 1\ \text{MHz}$	-	1.9	-	Ω

开关特性

$t_{d(on)}$	导通延迟时间	$V_{DD} = 50\ \text{V}$, $I_D = 100\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_G = 4.7\ \Omega$	-	23	56	ns
t_r	开通上升时间		-	26	62	ns
$t_{d(off)}$	关断延迟时间		-	50	110	ns
t_f	关断下降时间		-	15	40	ns

漏极-源极二极管特性

I _S	漏极 - 源极二极管最大正向连续电流		-	-	164*	A
I _{SM}	漏极 - 源极二极管最大正向脉冲电流		-	-	656	A
V _{SD}	漏极 - 源极二极管正向电压	V _{GS} = 0 V, I _{SD} = 100 A	-	-	1.3	V
t _{rr}	反向恢复时间	V _{GS} = 0 V, V _{DD} = 50 V, I _{SD} = 100 A,	-	75	-	ns
Q _{rr}	反向恢复电荷	di _F /dt = 100 A/μs	-	120	-	nC

注意:

- 重复额定值: 脉冲宽度受限于最大结温。
- $L = 3\ \text{mH}$, $I_{AS} = 20.6\ \text{A}$, $R_G = 25\ \Omega$, 开始 $T_J = 25^\circ\text{C}$ 。
- $I_{SD} \leq 100\ \text{A}$, $di/dt \leq 200\ \text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, 开始 $T_J = 25^\circ\text{C}$ 。
- 本质上独立于工作温度的典型特性。

典型性能特征

图 1. 导通区域特性

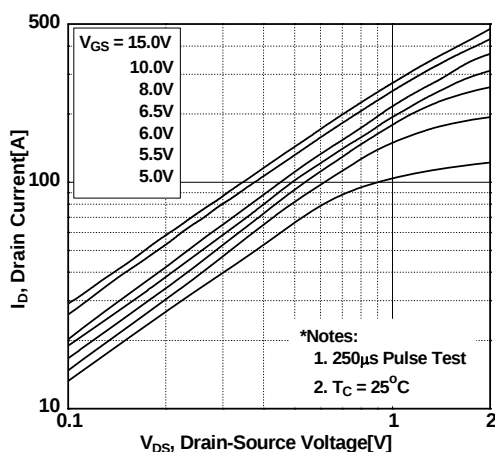


图 2. 传输特性

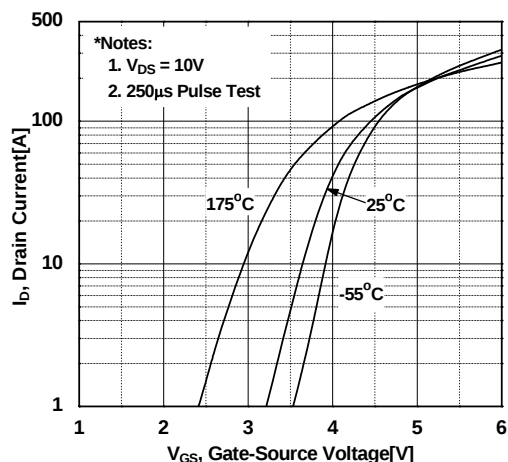


图 3. 导通电阻变化与漏极电流和栅极电压的关系

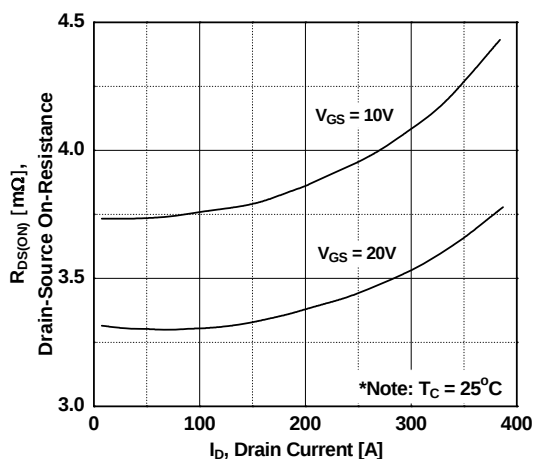


图 4. 体二极管正向电压变化与源极电流和温度的关系

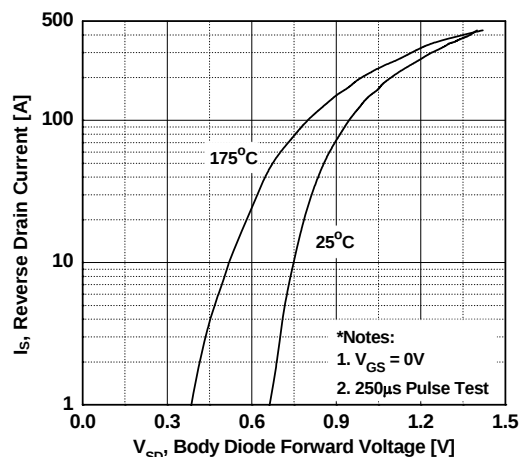


图 5. 电容特性

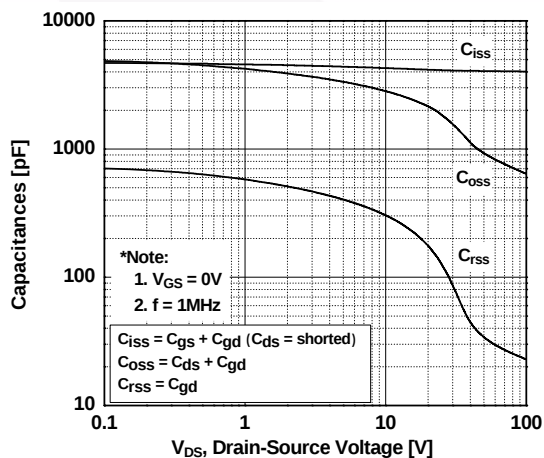
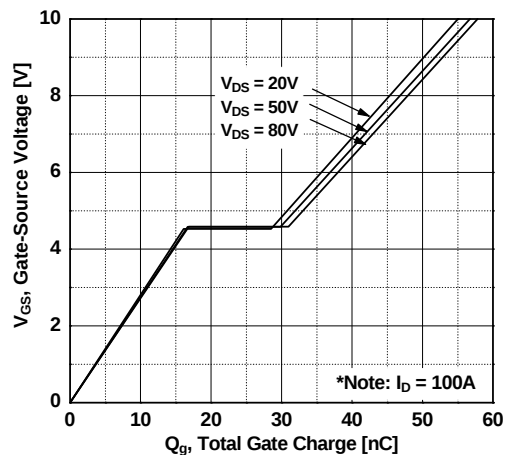


图 6. 栅极电荷特性



典型性能特性 (接上页)

图 7. 击穿电压变化与温度的关系

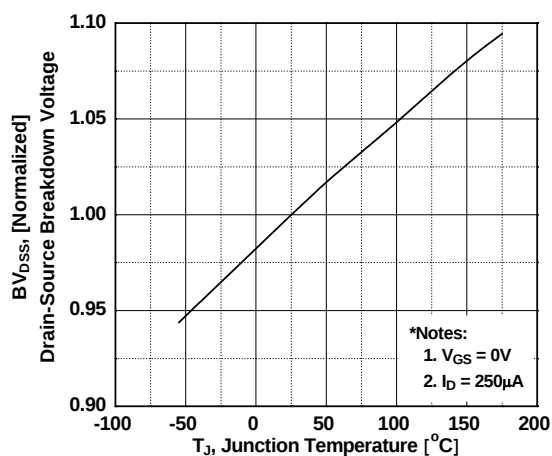


图 8. 导通电阻变化与温度的关系

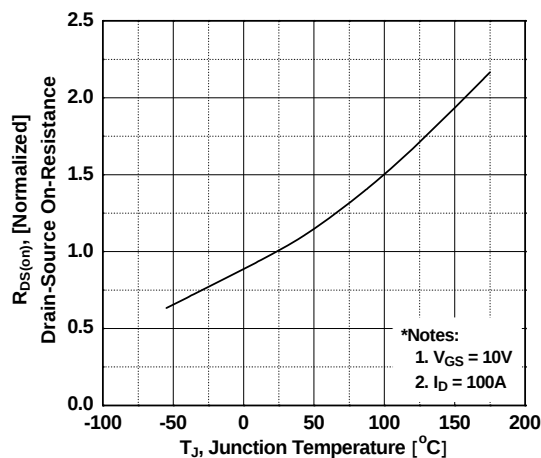


图 9. 最大安全工作区

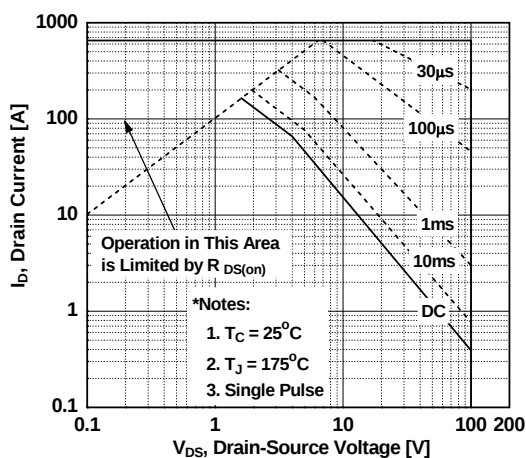


图 10. 最大漏极电流与壳温的关系

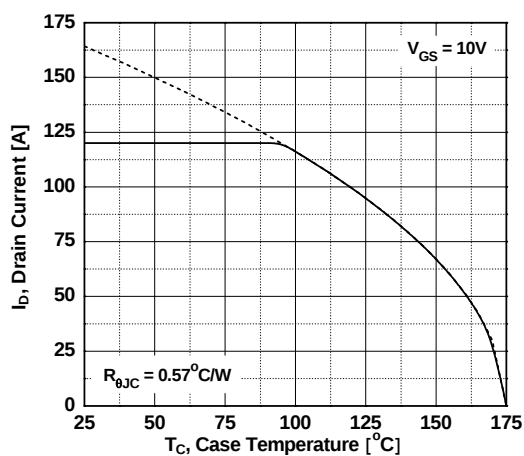


图 11. Eoss 与漏源极电压

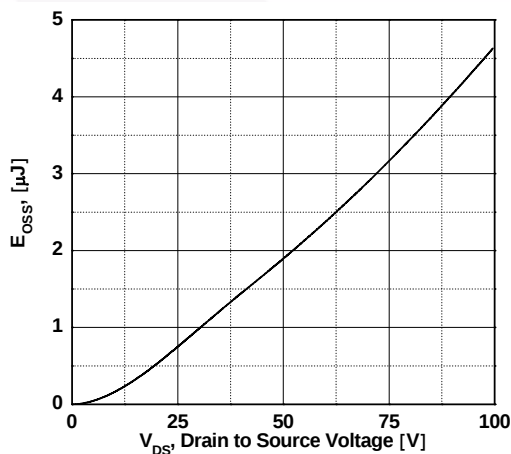
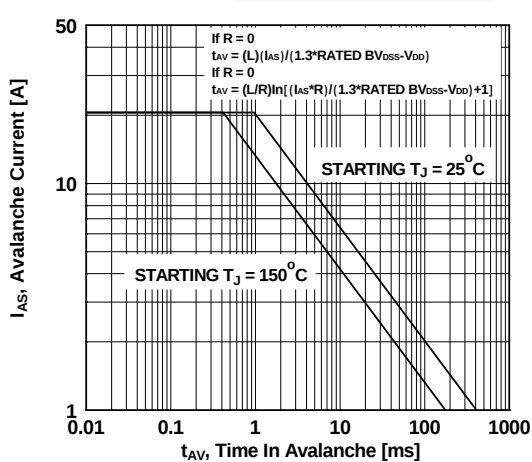
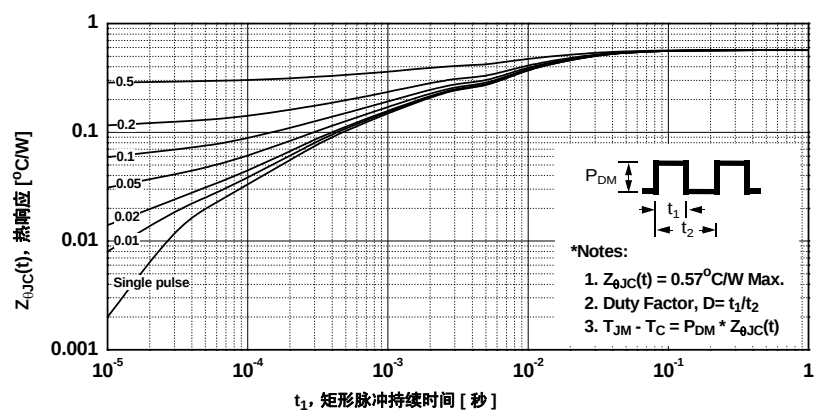


图 12. 非箝位感性开关能力



典型性能特性 (接上页)

图 13. 瞬态热响应曲线



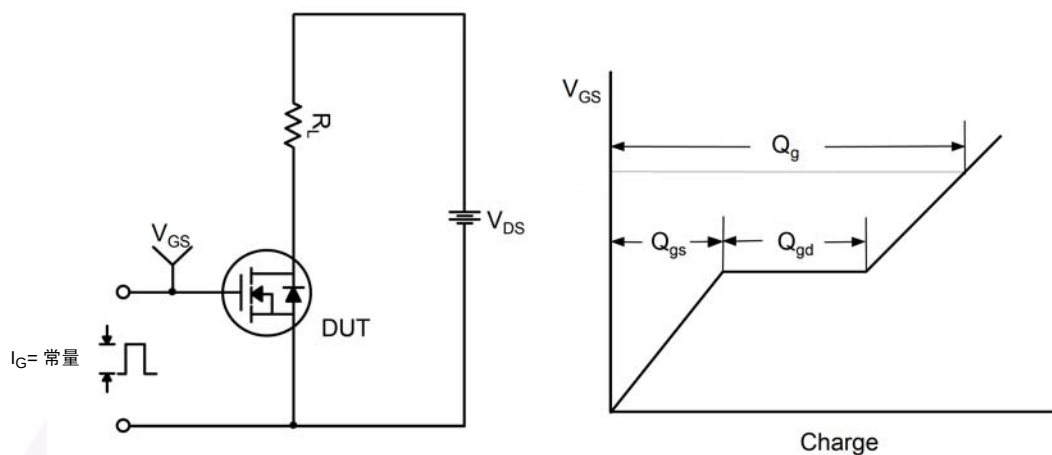


图 14. 栅极电荷测试电路与波形

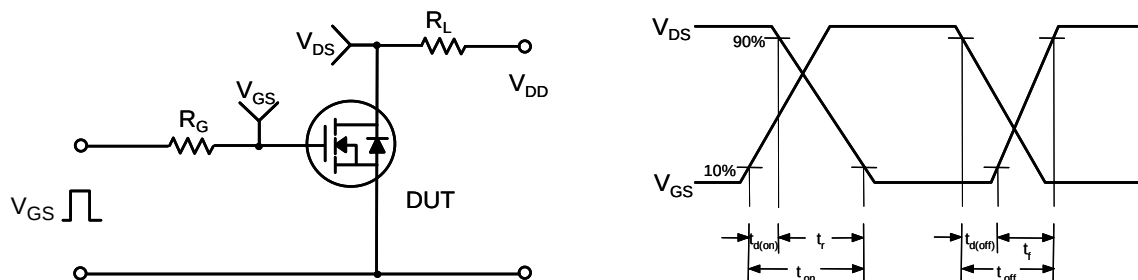


图 15. 阻性开关测试电路与波形

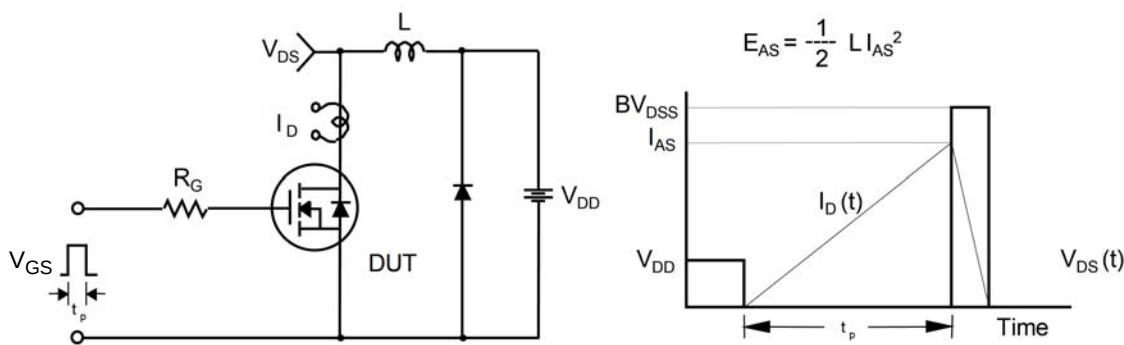


图 16. 非箝位电感开关测试电路与波形

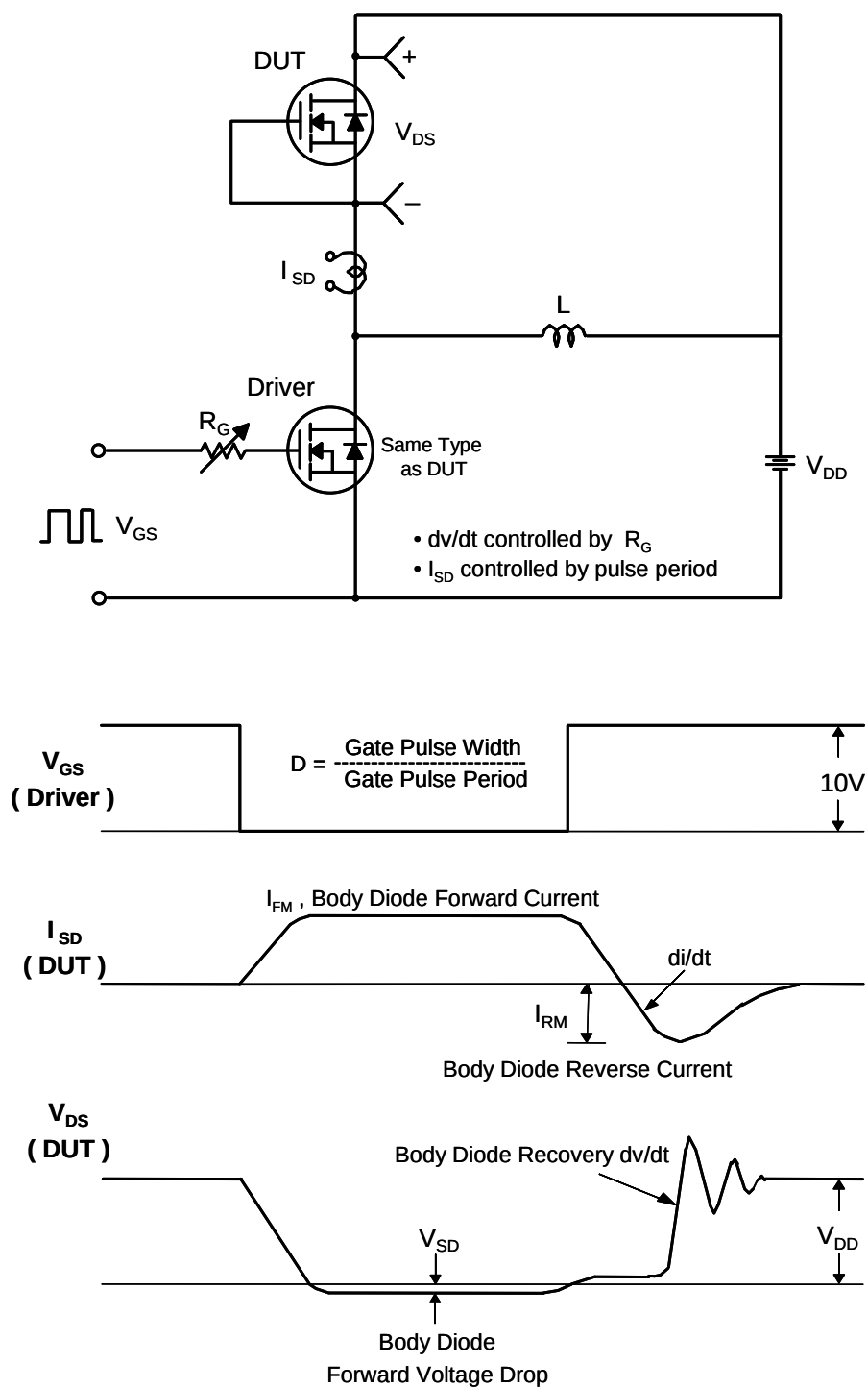


图 17. 二极管恢复 dv/dt 峰值测试电路与波形

机械尺寸

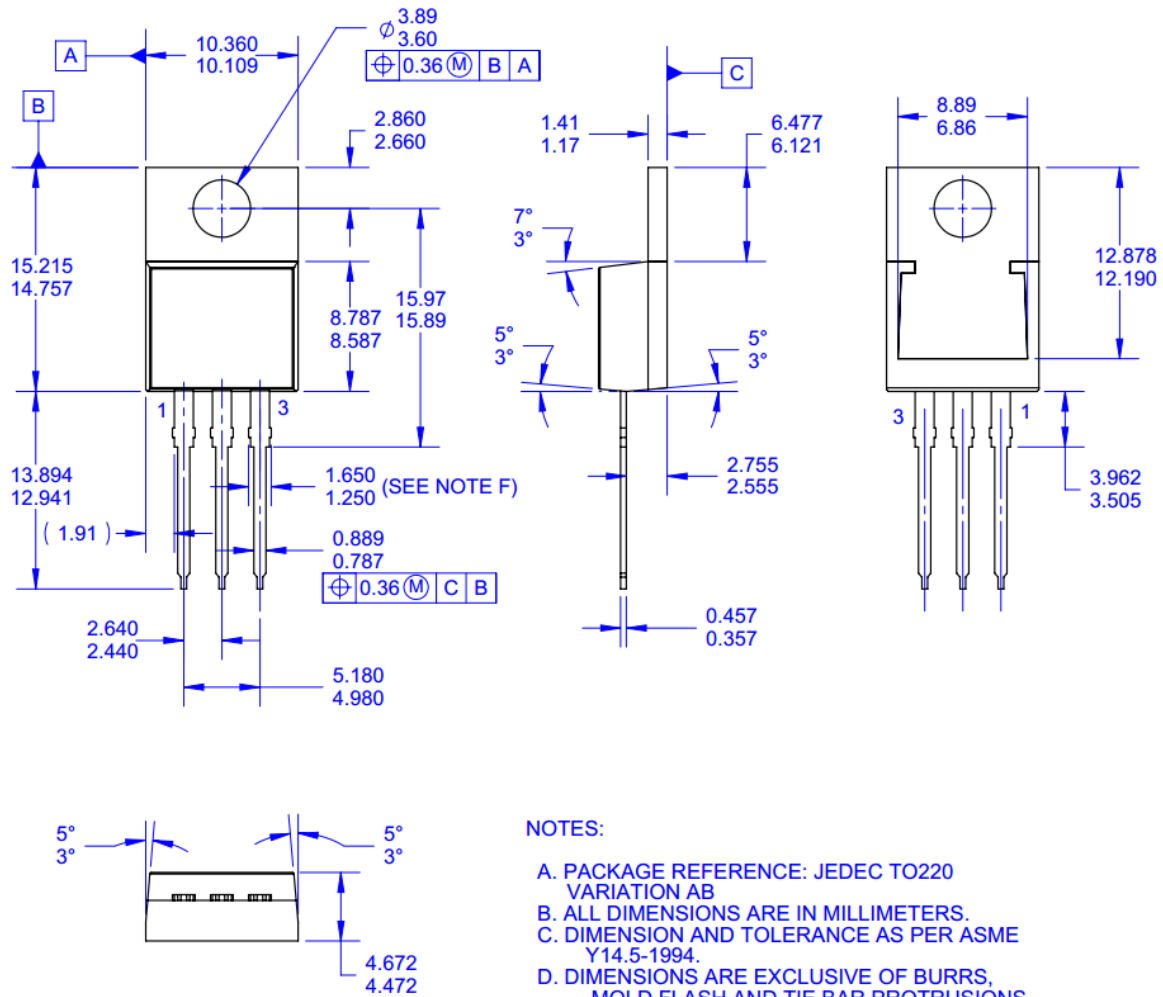


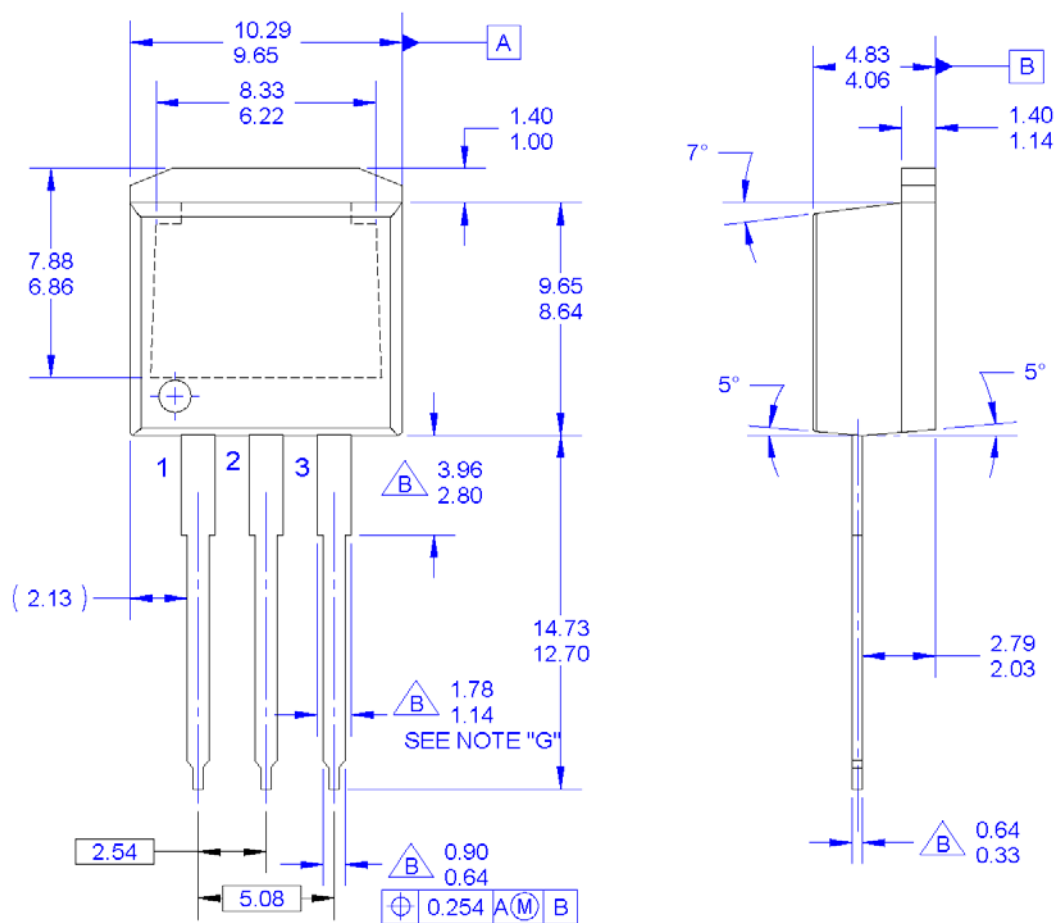
图 18. TO-220 模塑 3 引线 Jedec 变体 AB (Delta)

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机械尺寸



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- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
 B. DOES NOT COMPLY JEDEC STD. VALUE.
 C. ALL DIMENSIONS ARE IN MILLIMETERS.
 D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
 E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
 F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
 G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
 H. DRAWING FILE NAME: TO262A03REV5

图 19. TO262 (I²PAK) 模塑 3 引脚 Jedec 变体 AA

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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