

DS90UR908Q 5 - 65MHz 24 位彩色平面显示器-链路 (FPD-Link) II 至 FPD-Link 转换器

查询样品: [DS90UR908Q-Q1](#)

特性

- 支持 **5 – 65MHz** (**140Mbps** 至 **1.82Gbps** 串行链路)
- **5 通道** (**4 个数据 + 1 个时钟**) **FPD-Link** 驱动器输入
- 长度达 **10 米**的 **AC** 耦合生成树协议 (**STP**) 互连
- 集成型输入端接
- 全速 (**@ Speed**) 链路内置自检 (**BIST**) 模式和报告引脚
- 可选 **I2C** 兼容串行控制总线
- **RGB888 + VS, HS, DE** 支持
- 断电模式大大减少了功率耗散
- 快速随机数据锁定; 无需基准时钟
- 可调输入接收器均衡
- **LOCK** (锁定) (实时链路状态) 报告引脚
- 低电磁干扰 (**EMI**) **FPD-Link** 输出
- 针对低 **EMI** 的展频时钟生成 (**SSCG**) 选项
- **1.8V** 或 **3.3V** 兼容 **LVC MOS I/O** 接口
- 汽车应用级产品: 符合 **AEC-Q100 2** 级要求
- **>8kV** 人体模型 (**HBM**) 和静电放电 (**ESD**) 耐受
- 向后兼容模式以实现与之前生产的器件的共同运行

应用范围

- 汽车导航显示屏
- 汽车娱乐系统显示屏

说明

DS90UR908Q 将 FPD-Link II 转换为 FPD-Link。它将一个单对线 (FPD-Link II) 上具有嵌入时钟的高速串行化接口转换为 4 个低压差分信令 (LVDS) 数据/控制数据流和 1 个 LVDS 时钟对 (FPD-Link)。这个串行总线方案消除了时钟和数据间的偏差问题, 从而大大简化了系统设计, 减少了控制器引脚数量, 并且减少了互连线尺寸、重量和成本, 并从总体上简化了印刷电路板 (PCB) 布局布线。此外, 内部 DC 均衡编码被用来支持 AC 耦合互连。

DS90UR908Q 转换器恢复数据 (RGB) 和控制信号并从一个串行数据流 (FPD-Link II) 中提取时钟。它能够锁定进入数据流, 而无需使用一个协商序列或特别的 SYNC (同步) 模式, 也不需要一个基准时钟。提供了一个链路状态 (LOCK) 输出信号。

串行输入数据流的可调输入均衡为线缆的传输介质损耗提供补偿, 并减少了介质引起的确定性抖动。低压差分信令的使用、输出电压电平选择特性和额外的输出展频生成大大减少了 EMI。

由于连接至显示屏物理接口的接线更少, 使用 LVDS 技术的 FPD-Link 输入非常适合于高速、低功率和低 EMI 数据传输。

DS90UR908Q 采用 48 引脚超薄四方扁平无引线封装 (WQFN) 封装, 并可在 -40°C 至 +105°C 的汽车 AEC-Q100 2 级额定温度范围内运行。



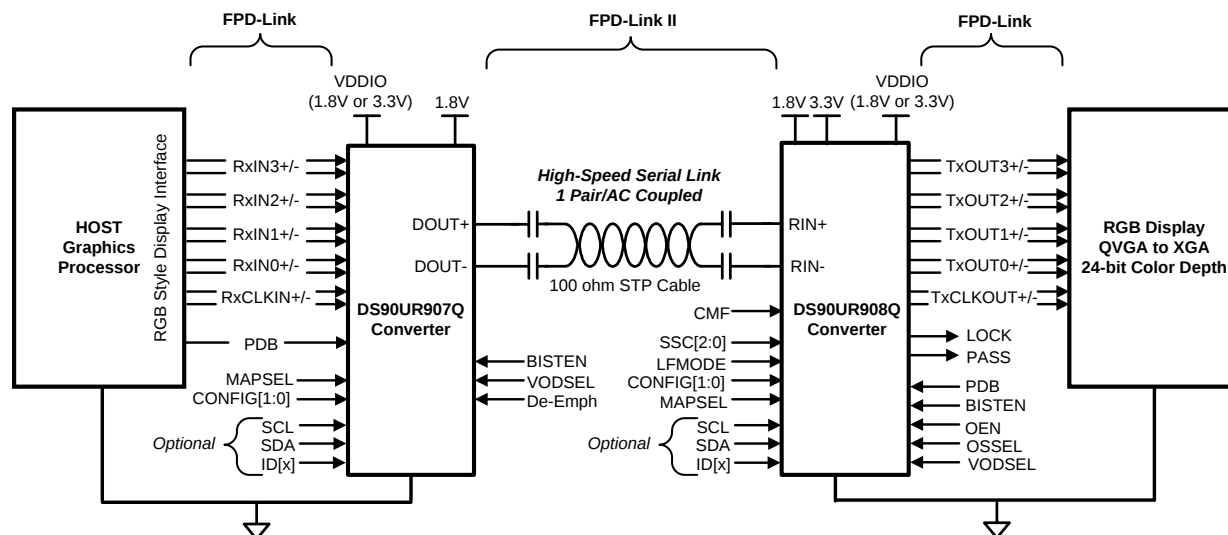
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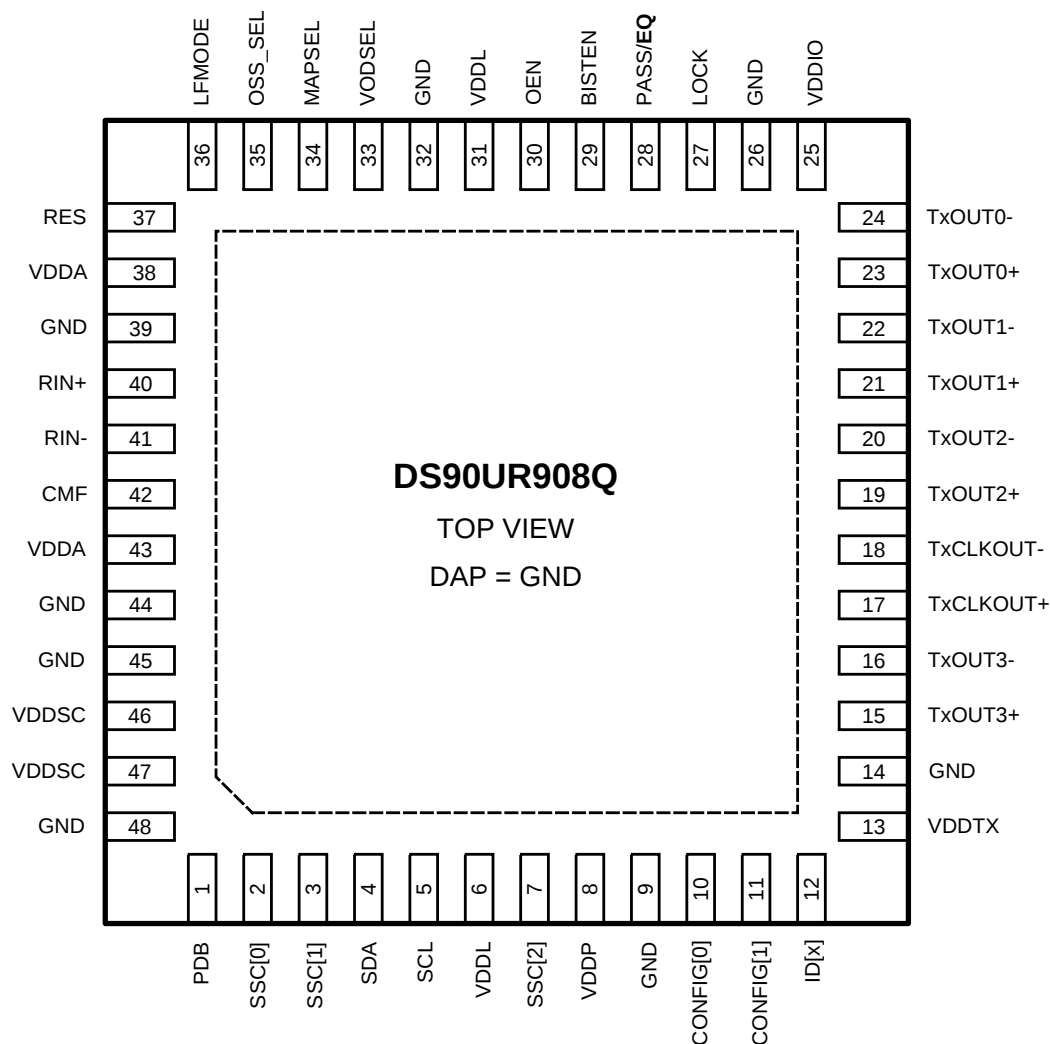
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English Data Sheet: [SNLS317](#)

Applications Diagram



Pin Diagram



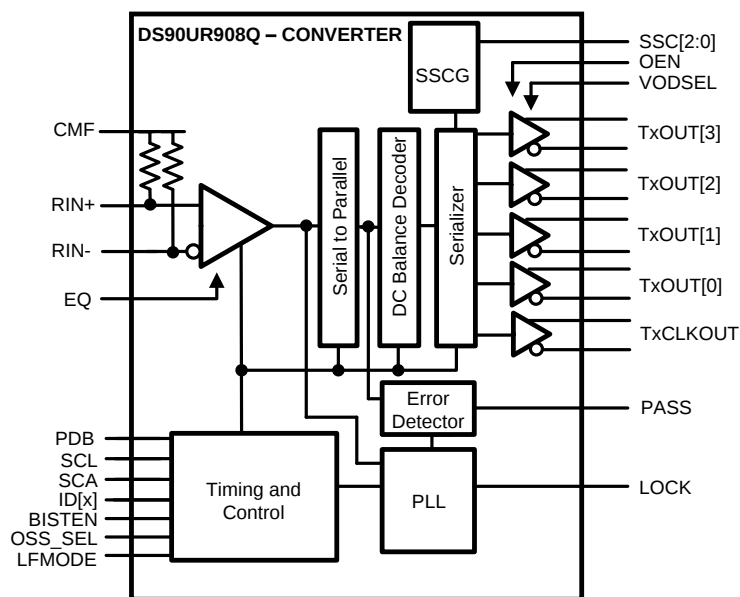
PIN DESCRIPTIONS⁽¹⁾

Pin Name	Pin #	I/O, Type	Description
FPD-Link II Input Interface			
RIN+	40	I, LVDS	True input The input must be AC coupled with a 100 nF capacitor. Internal termination.
RIN-	41	I, LVDS	Inverting input The input must be AC coupled with a 100 nF capacitor. Internal termination.
CMF	42	I, Analog	Common-Mode Filter VCM center-tap is a virtual ground which maybe ac-coupled to ground to increase receiver common mode noise immunity. Recommended value is 4.7 μ F or higher.
FPD-Link Output Interface			
TxOUT[3:0]+	15,19, 21, 23	O, LVDS	True LVDS Data Output
TxOUT[3:0]-	16,20, 22, 24	O, LVDS	Inverting LVDS Data Output
TxCLKOUT+	17	O, LVDS	True LVDS Clock Output
TxCLKOUT-	18	O, LVDS	Inverting LVDS Clock Output
LVC MOS Outputs			
LOCK	27	O, LVMOS	LOCK Status Output LOCK = 1, PLL is locked, output states determined by OEN. LOCK = 0, PLL is unlocked, output states determined by OSS_SEL and OEN, Table 3 May be used as a Link Status or to flag when the Video Data is active (ON/OFF).
Control and Configuration			
PDB	1	I, LVC MOS w/ pull-down	Power Down Mode Input PDB = 1, Device is enabled (normal operation) PDB = 0, Device is in power-down, the outputs are TRI-STATE. Control registers are RESET .
VODSEL	33	I, LVC MOS w/ pull-down	FPD-Link Output Voltage Select, Table 4 VODSEL = 1, LVDS VOD is ± 400 mV, 800 mVp-p (typ) VODSEL = 0, LVDS VOD is ± 250 mV, 500 mVp-p (typ)
OEN	30	I, LVC MOS w/ pull-down	Output Enable Input, Table 3
OSS_SEL	35	I, LVC MOS w/ pull-down	Output Sleep State Select Input, Table 3
LFMODE	36	I, LVC MOS w/ pull-down	Low Frequency Mode — Pin or Register Control LF_MODE = 1, low frequency mode (TxCLKOUT = 5-20 MHz) LF_MODE = 0, high frequency mode (TxCLKOUT = 20-65 MHz)
MAPSEL	34	I, LVC MOS w/ pull-down	FPD-Link Map Select — Pin or Register Control MAPSEL = 1, MSB on TxOUT3+/-, Figure 16 MAPSEL = 0, LSB on TxOUT3+/-, Figure 15
CONFIG[1:0]	11,10	I, LVC MOS w/ pull-down	Operating Modes — Pin or Register Control Determine the device operating mode and interfacing device, Table 1 CONFIG[1:0] = 00: Interfacing to DS90UR905Q or DS90UR907Q, Control Signal Filter DISABLED CONFIG[1:0] = 01: Interfacing to DS90UR905Q or DS90UR907Q, Control Signal Filter ENABLED CONFIG[1:0] = 10: Interfacing to DS90UR241 or DS99R421 CONFIG[1:0] = 11: Interfacing to DS90C241
SSC[2:0]	7, 3, 2	I, LVC MOS w/ pull-down	Spread Spectrum Clock Generation (SSCG) Range Select, See Table 5 and Table 6
RES	37	I, LVC MOS w/ pull-down	Reserved Tie Low
Control and Configuration — STRAP PIN			
For a High State, use a 10 k Ω pull up to VDDIO; for a Low State, the IO includes an internal pull down. The STRAP pin is read upon power-up and set device configuration. Pin number listed along with shared LVC MOS Output name in square bracket.			
EQ	28 [PASS]	STRAP I, LVC MOS w/ pull-down	EQ Gain Control of FPD-Link II Input EQ = 1, EQ gain is enabled (~ 13 dB) EQ = 0, EQ gain is disabled (~ 1.625 dB)

(1) 1 = High, 0 = Low

PIN DESCRIPTIONS⁽¹⁾ (continued)

Pin Name	Pin #	I/O, Type	Description
Optional BIST Mode			
BISTEN	29	I, LVCMOS w/ pull-down	BIST Enable Input – Optional BISTEN = 1, BIST Mode is enabled. BISTEN = 0, normal mode.
PASS	28	O, LVCMOS	PASS Output (BIST Mode) – Optional PASS = 1, no errors detected PASS = 0, errors detected Leave open if unused. Route to a test point (pad) recommended.
Optional Serial Bus Control Interface			
SCL	5	I, LVCMOS	Serial Control Bus Clock Input - Optional SCL requires an external pull-up resistor to V _{DDIO} .
SDA	4	I/O, LVCMOS Open Drain	Serial Control Bus Data Input / Output - Optional SDA requires an external pull-up resistor to V _{DDIO} .
ID[x]	12	I, Analog	Serial Control Bus Device ID Address Select — Optional Resistor to Ground and 10 kΩ pull-up to 1.8V rail, Table 7
Power and Ground			
VDDL	6, 31	Power	Logic Power, 1.8 V ±5%
VDDA	38, 43	Power	Analog Power, 1.8 V ±5%
VDDP	8	Power	PLL Power, 1.8 V ±5%
VDDSC	46, 47	Power	SSC Generator Power, 1.8 V ±5%
VDDTX	13	Power	FPD-Link Power, 3.3 V ±10%
V _{DDIO}	25	Power	LVCMOS I/O Power, 1.8 V ±5% OR 3.3 V ±10%
GND	9, 14, 26, 32, 39, 44, 45, 48	Ground	Ground
DAP	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connect to the ground plane (GND) with at least 9 vias.

Block Diagram**Figure 1. FPD-Link II to FPD-Link Convertor**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

Supply Voltage – V_{DDn} (1.8V)	–0.3V to +2.5V
Supply Voltage – V_{DDTX} (3.3V)	–0.3V to +4.0V
Supply Voltage – V_{DDIO}	–0.3V to +4.0V
LVCMOS I/O Voltage	–0.3V to $(V_{DDIO} + 0.3V)$
Receiver Input Voltage	–0.3V to $(V_{DD} + 0.3V)$
LVDS Output Voltage	–0.3V to $(V_{DDTX} + 0.3V)$
Junction Temperature	+150°C
Storage Temperature	–65°C to +150°C
48L WQFN Package	
Maximum Power Dissipation Capacity at 25°C	
Derate about 25°C	1/ θ_{JA} °C/W
θ_{JA}	27.7 °C/W
θ_{JC}	3.0 °C/W
ESD Rating (IEC, powered-up only), $R_D = 330\Omega$, $C_S = 150pFs$	
Air Discharge (R_{IN+} , R_{IN-})	$\geq \pm 15$ kV
Contact Discharge (R_{IN+} , R_{IN-})	$\geq \pm 8$ kV
ESD Rating (ISO10605), $R_D = 330\Omega$, $C_S = 150/330pF$	
ESD Rating (ISO10605), $R_D = 2k\Omega$, $C_S = 150/330pF$	
Air Discharge (R_{IN+} , R_{IN-})	$\geq \pm 15$ kV
Contact Discharge (R_{IN+} , R_{IN-})	$\geq \pm 8$ kV
ESD Rating (HBM)	$\geq \pm 8$ kV
ESD Rating (HBM)	$\geq \pm 8$ kV
ESD Rating (CDM)	$\geq \pm 1.25$ kV

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
- (2) For soldering specifications see product folder at www.ti.com and [SNOA549](#)
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{DDn})	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO}) OR	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	–40	+25	+105	°C
TxCLKOUT Frequency	5		65	MHz
Supply Noise ⁽¹⁾			100	mV _{p-p}

- (1) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC coupled to the V_{DDn} (1.8V) supply with amplitude = 100 mVp-p measured at the device V_{DDn} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 750 kHz. The Des on the other hand shows no error when the noise frequency is less than 400 kHz.

DC Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Pin/Freq.	Min	Typ	Max	Units
FPD-Link LVDS Output								
V _{OD}	Differential Output Voltage	R _L = 100Ω Figure 8	VODSEL = L	TxCLKOUT+, TxCLKOUT-, TxOUT[3:0]+, TxOUT[3:0]-	100	250	400	mV
			VODSEL = H		200	450	600	mV
V _{ODp-p}	Differential Output Voltage A-B		VODSEL = L			500		mVp-p
			VODSEL = H			900		mVp-p
ΔV _{OD}	Output Voltage Unbalance		VODSEL = H			4	50	mV
V _{OS}	Offset Voltage		VODSEL = L		1.0	1.2	1.5	V
			VODSEL = H			1.2		V
ΔV _{OS}	Offset Voltage Unbalance					1	50	mV
I _{OS}	Output Short Circuit Current	V _{out} = GND				-5		mA
I _{OZ}	Output TRI-STATE® Current	OEN = GND, V _{out} =V _{DDTX} , or GND			-10		+10	μA
3.3 V I/O LVCMOS DC SPECIFICATIONS – V _{DDIO} = 3.0 to 3.6V								
V _{IH}	High Level Input Voltage	PDB, VODSEL, OEN, OSS_SEL, MAPSEL, LFMODE, SSC[2:0], BISTEN			2.2		V _{DDIO}	V
V _{IL}	Low Level Input Voltage				GND		0.8	V
I _{IN}	Input Current				V _{IN} = 0V or V _{DDIO}	-15	±1	+15
V _{OH}	High Level Output Voltage	I _{OH} = -2 mA	LOCK, PASS	V _{DDIO} - 0.25	V _{DDIO}		V	
V _{OL}	Low Level Output Voltage	I _{OL} = +2 mA			GND	0.2	V	
I _{OS}	Output Short Circuit Current	V _{OUT} = 0V			-45		mA	
I _{OZ}	TRI-STATE® Output Current	PDB = 0V, OSS_SEL = 0V, V _{OUT} = 0V or V _{DDIO}		-10		+10	μA	
1.8 V I/O LVCMOS DC SPECIFICATIONS – V _{DDIO} = 1.71 to 1.89V								
V _{IH}	High Level Input Voltage	PDB, VODSEL, OEN, OSS_SEL, MAPSEL, LFMODE, SSC[2:0], BISTEN			0.7* V _{DDIO}		V _{DDIO}	V
V _{IL}	Low Level Input Voltage				GND		0.3* V _{DDIO}	V
I _{IN}	Input Current				V _{IN} = 0V or V _{DDIO}	-10	±1	+10
V _{OH}	High Level Output Voltage	I _{OH} = -2 mA	LOCK, PASS	V _{DDIO} - 0.2	V _{DDIO}		V	
V _{OL}	Low Level Output Voltage	I _{OL} = +2 mA		GND		0.2	V	
I _{OS}	Output Short Circuit Current	V _{OUT} = 0V			-13		mA	
I _{OZ}	TRI-STATE® Output Current	V _{OUT} = 0V or V _{DDIO}		-15		+15	μA	

- (1) The [Electrical Characteristics](#) tables list ensured specifications under the listed [Recommended Operating Conditions](#) except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Typical values represent most likely parametric norms at $V_{DD} = 3.3V$, $T_a = +25$ degC, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (3) When the Serializer output is at TRI-STATE the Deserializer will lose PLL lock. Resynchronization / Relock must occur before data transfer require t_{PLD} .
- (4) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔV_{OD} , V_{TH} and V_{TL} which are differential voltages.

DC Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾ (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units	
FPD-Link II LVDS RECEIVER DC SPECIFICATIONS								
V _{TH}	Differential Input Threshold High Voltage	V _{CM} = +1.2V (Internal V _{BIAS})	RIN+, RIN-			+50	mV	
V _{TL}	Differential Input Threshold Low Voltage			-50			mV	
V _{CM}	Common Mode Voltage, Internal V _{BIAS}				1.2		V	
R _T	Input Termination			80	100	120	Ω	
SUPPLY CURRENT								
I _{DD1}	Supply Current (includes load current) 65 MHz Clock	Checker Board Pattern, VODSEL = H SSC{2:0} = 000 Figure 2	V _{DDn} = 1.89V	All V _{DD(1.8)} pins		85	95	mA
I _{DDTX1}			V _{DDTX} = 3.6V	V _{DDTX}		40	50	mA
I _{DDIO1}			V _{DDIO} =1.89V	V _{DDIO}		0.3	0.8	mA
			V _{DDIO} = 3.6V			0.8	1.5	mA
I _{DD2}	Supply Current (includes load current) 65 MHz Clock	Checker Board Pattern, VODSEL = H SSC[2:0] = 111 Figure 2	V _{DDn} = 1.89V	All V _{DD(1.8)} pins		95		mA
I _{DDTX2}			V _{DDTX} = 3.6V	V _{DDTX}		40		mA
I _{DDIO2}			V _{DDIO} =1.89V	V _{DDIO}		0.3		mA
			V _{DDIO} = 3.6V			0.8		mA
I _{DDZ}	Supply Current Power Down	PDB = 0V, All other LVCMOS Inputs = 0V	V _{DD} = 1.89V	All V _{DD(1.8)} pins		0.15	2.00	mA
I _{DDTXZ}			V _{DDTX} = 3.6V	V _{DDTX}		0.01	0.10	mA
I _{DDIOZ}			V _{DDIO} =1.89V	V _{DDIO}		0.01	0.08	mA
			V _{DDIO} = 3.6V			0.01	0.08	mA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
FPD-Link II							
t _{DDL} T	Lock Time, Figure 7 ⁽¹⁾	SSC[2:0] = 000	5 MHz		7		ms
		SSC[2:0] = 111	5 MHz		14		ms
		SSC[2:0] = 000	65 MHz		6		ms
		SSC[2:0] = 111	65 MHz		8		ms
t _{JIT}	Input Jitter Tolerance, Figure 10	EQ = Off SSC[2:0] = 000 TxCLKOUT± = 65 MHz	Input Jitter Frequency < 2 MHz		>0.9		UI
			Input Jitter Frequency > 6 MHz		> 0.5		UI
FPD-Link Output							
t _{TLHT}	Low to High Transition Time	R _L = 100Ω	TxCLKOUT±, TxOUT[3:0]±		0.3	0.6	ns
t _{THLT}	High to Low Transition Time				0.3	0.6	ns
t _{DCCJ}	Cycle-to-Cycle Output Jitter ⁽²⁾⁽³⁾⁽⁴⁾	5 MHz	TxCLKOUT±		900	2100	ps
		65 MHz			75	125	ps
t _{TTP1}	Transmitter Pulse Position for bit 1	5 - 65 MHz, Figure 9	TxOUT[3:0]±		1		UI
t _{TTP0}	Transmitter Pulse Position for bit 0				2		UI
t _{TPP6}	Transmitter Pulse Position for bit 6				3		UI
t _{TTP5}	Transmitter Pulse Position for bit 5				4		UI
t _{TTP4}	Transmitter Pulse Position for bit 4				5		UI
t _{TTP3}	Transmitter Pulse Position for bit 3				6		UI
t _{TTP2}	Transmitter Pulse Position for bit 2				7		UI
Δt _{TTP}	Offset Transmitter Pulse Position (bit 6— bit 0)	65 MHz, Figure 9			< +0.1		UI
t _{DD}	Delay-Latency	See Figure 4			10*T		T
t _{TPDD}	Power Down Delay, active to OFF	65 MHz, Figure 5			7	12	ns
t _{TXZR}	Enable Delay, OFF to active	65 MHz, Figure 6			40	55	ns
LVCMOS Outputs							
t _{CLH}	Low to High Transition Time	C _L = 8 pF, Figure 3	LOCK, PASS		5	15	ns
t _{CHL}	High to Low Transition Time				5	15	ns
t _{PASS}	BIST PASS Valid Time, BISTEN = 1, Figure 11	5 MHz	PASS		570	580	ns
		65 MHz			50	65	ns
SSCG Mode							
f _{DEV}	Spread Spectrum Clocking Deviation Frequency	See ⁽⁴⁾	TxCLKOUT = 5 to 65 MHz, SSC[2:0] = ON	±0.5		±2	%
f _{MOD}	Spread Spectrum Clocking Modulation Frequency	See ⁽⁴⁾	TxCLKOUT = 5 to 65 MHz, SSC[2:0] = ON	8		100	kHz

- (1) t_{PLD} and $t_{DDL T}$ is the time required by the serializer and deserializer to obtain lock when exiting power-down state with an active PCLK.
- (2) t_{DCCJ} is the maximum amount of jitter between adjacent clock cycles.
- (3) Specification is ensured by characterization and is not tested in production.
- (4) Specification is ensured by design and is not tested in production.

Recommended Timing for the Serial Control Bus

Over 3.3V operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	Standard Mode	0		100	kHz
		Fast Mode	0		400	
t_{LOW}	SCL Low Period	Standard Mode	4.7			μ s
		Fast Mode	1.3			μ s
t_{HIGH}	SCL High Period	Standard Mode	4.0			μ s
		Fast Mode	0.6			μ s
$t_{HD;STA}$	Hold time for a start or a repeated start condition, Figure 12	Standard Mode	4.0			μ s
		Fast Mode	0.6			μ s
$t_{SU;STA}$	Set Up time for a start or a repeated start condition, Figure 12	Standard Mode	4.7			μ s
		Fast Mode	0.6			μ s
$t_{HD;DAT}$	Data Hold Time, Figure 12	Standard Mode	0		3.45	μ s
		Fast Mode	0		0.9	μ s
$t_{SU;DAT}$	Data Set Up Time, Figure 12	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU;STO}$	Set Up Time for STOP Condition, Figure 12	Standard Mode	4.0			μ s
		Fast Mode	0.6			μ s
t_{BUF}	Bus Free Time Between STOP and START, Figure 12	Standard Mode	4.7			μ s
		Fast Mode	1.3			μ s
t_r	SCL & SDA Rise Time, Figure 12	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time, Figure 12	Standard Mode			300	ns
		Fast mode			300	ns

DC and AC Serial Control Bus Characteristics

Over 3.3V supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level	SDA and SCL	0.7* V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.3* V_{DDIO}	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}		SDA, IOL = 0.5mA	0		0.36	V
I_{in}		SDA or SCL, $V_{in} = V_{DDIO}$ or GND	-10		+10	μ A
t_R	SDA RiseTime – READ	SDA, RPU = X, $C_b \leq 400$ pF, Figure 12		800		ns
t_F	SDA Fall Time – READ			50		ns
$t_{SU;DAT}$	Set Up Time — READ	See Figure 12		540		ns
$t_{HD;DAT}$	Hold Up Time — READ			600		ns
t_{SP}	Input Filter			50		ns
C_{in}	Input Capacitance	SDA or SCL		<5		pF

AC Timing Diagrams and Test Circuits

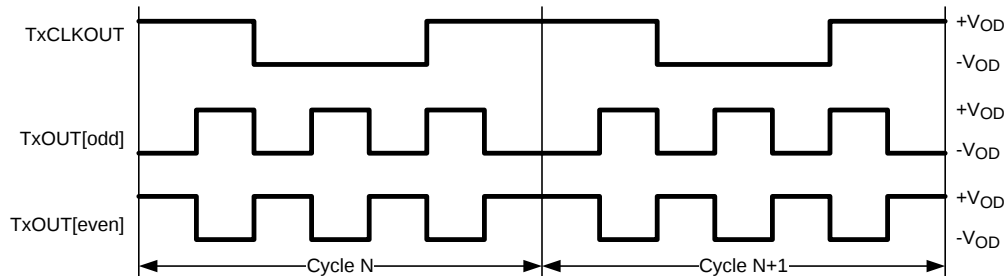


Figure 2. Checkerboard Data Pattern

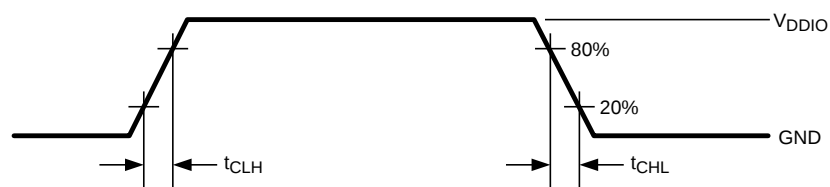


Figure 3. LVCMOS Transition Times

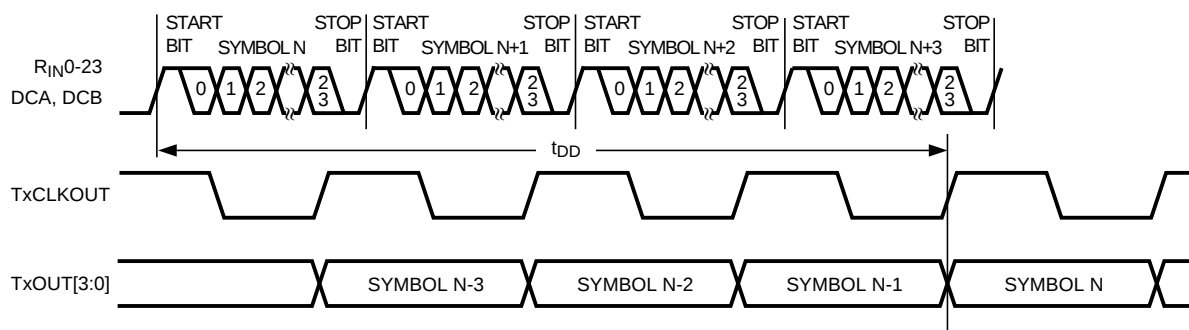


Figure 4. Delay – Latency

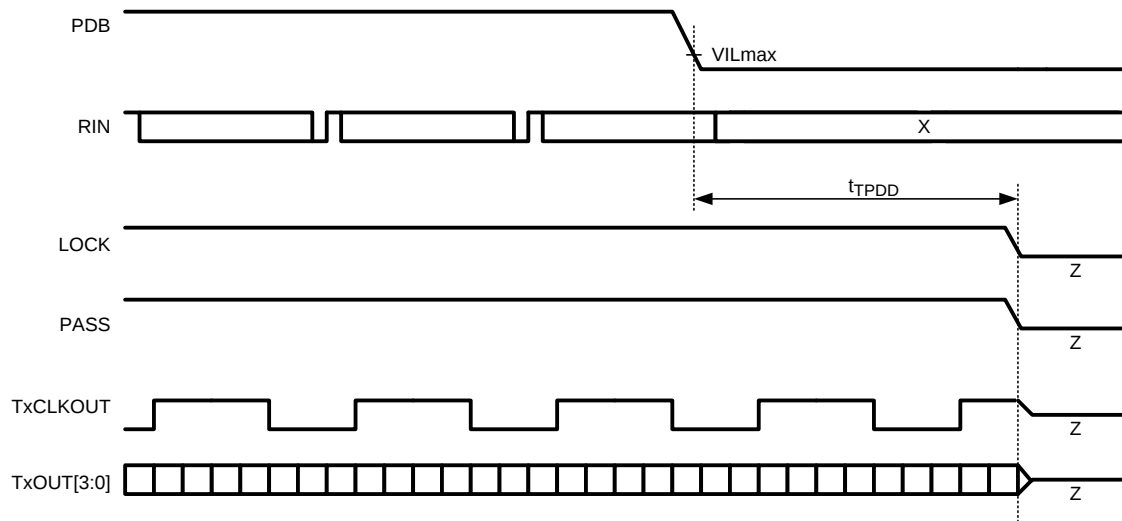


Figure 5. FPD-Link & LVCMOS Powerdown Delay

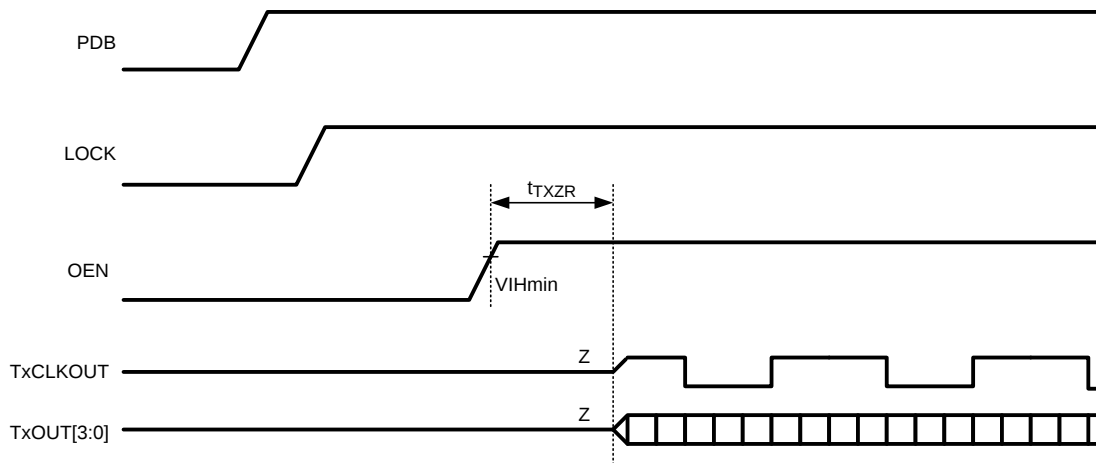


Figure 6. FPD-Link Outputs Enable Delay

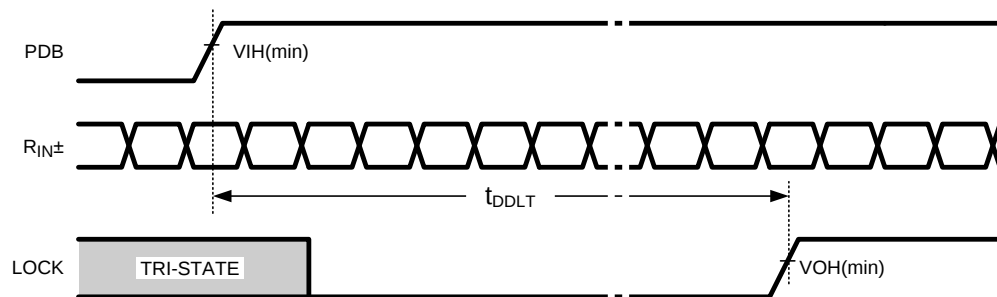


Figure 7. PLL Lock Times

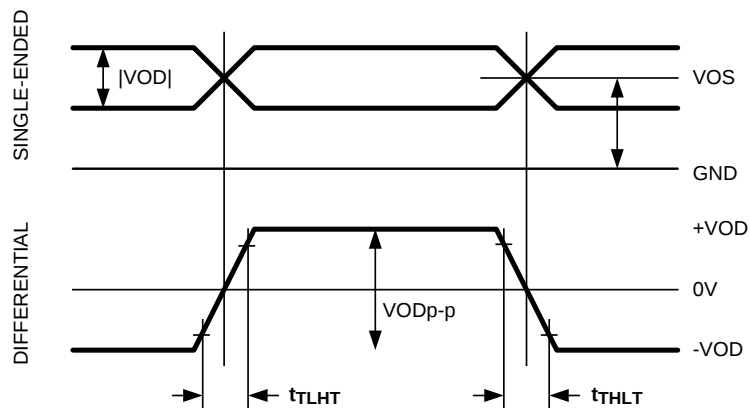


Figure 8. FPD-Link (LVDS) Single-ended and Differential Waveforms

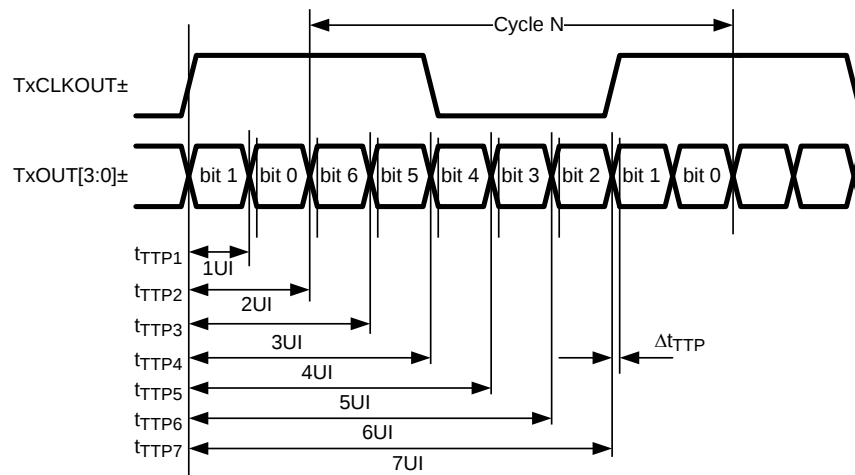


Figure 9. FPD-Link Transmitter Pulse Positions

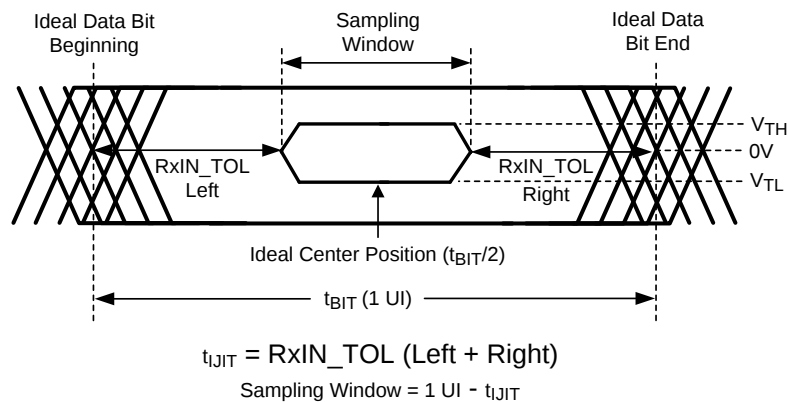


Figure 10. Receiver Input Jitter Tolerance

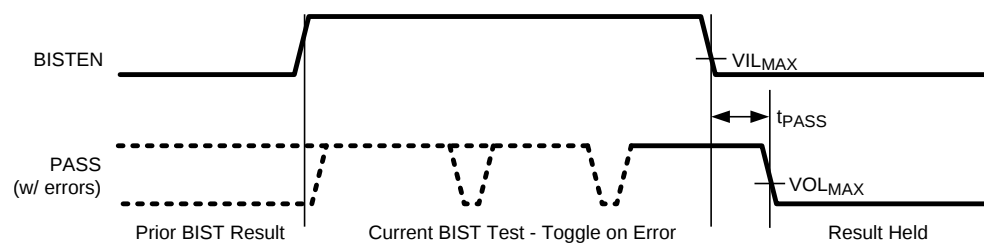


Figure 11. BIST PASS Waveform

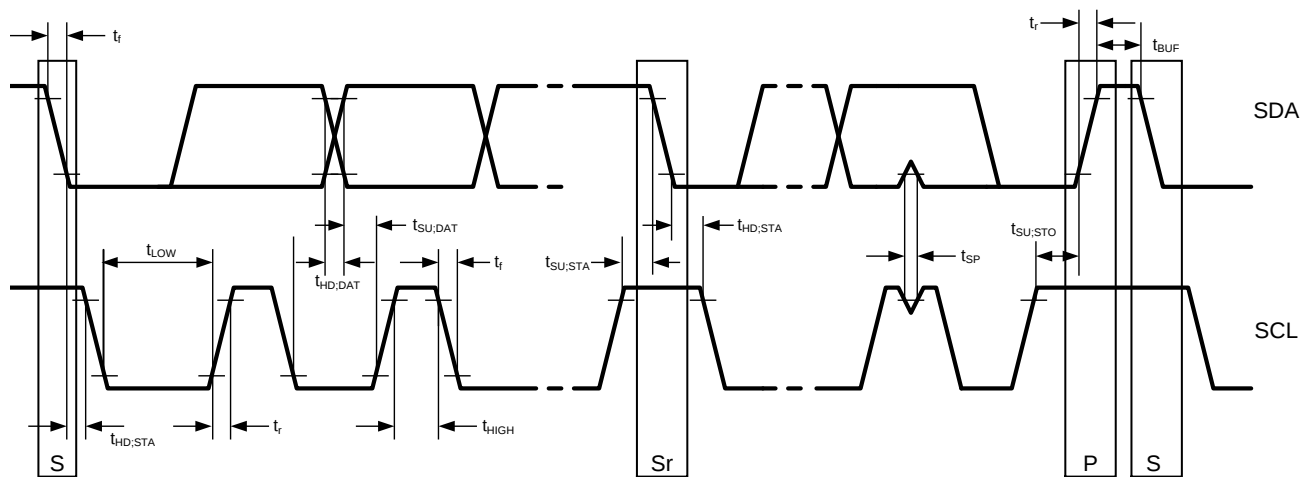


Figure 12. Serial Control Bus Timing Diagram

Functional Description

The DS90UR908Q receives 27-bits of data (24-high speed bits and 3 low speed bits) over a single serial FPD-Link II pair operating at 140Mbps to 1.82Gbps. The serial stream contains an embedded clock, video control signals and the DC-balance information which enhances signal quality and supports AC coupling. The receiver converts the serial stream into a 5-channel (4 data and 1 clock) FPD-Link LVDS Interface. The device is intended to be used with the DS90UR907Q or the DS90UR905Q FPD-Link II serializers, but is backward compatible with previous generation of FPD-Link II as well.

The device converts a single input serial data stream to a FPD-Link output bus, and also provides a signal check for the chipset Built In Self Test (BIST) mode. The device can be configured via external pins or through the optional serial control bus. It features enhance signal quality on the link by supporting the FPD-Link II data coding that provides randomization, scrambling, and DC balancing of the data. It also includes multiple features to reduce EMI associated with display data transmission. This includes the randomization and scrambling of the data, FPD-Link LVDS Output interface, and also the output spread spectrum clock generation (SSCG) support. The power saving features include a power down mode, and optional LVCMOS (1.8 V) interface compatibility.

The DS90UR908Q can lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. It also synchronizes to the serializer regardless of the data pattern, delivering true automatic “plug and lock” performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The DS90UR908Q recovers the clock and data by extracting the embedded clock information, validating and then deserializing the incoming data stream.

The DS90UR907Q / DS90UR908Q chipset supports 24-bit color depth, HS, VS and DE video control signals and up to three over-sampled low-speed (general purpose) data bits.

DATA TRANSFER

The DS90UR908Q will receive a pixel of data in the following format: C1 and C0 represent the embedded clock in the serial stream. C1 is always HIGH and C0 is always LOW. b[23:0] contain the scrambled data. DCB is the DC-Balanced control bit. DCB is used to minimize the short and long-term DC bias on the signal lines. This bit determines if the data is unmodified or inverted. DCA is used to validate data integrity in the embedded data stream. Both DCA and DCB coding schemes are generated by the Ser and decoded by the Des automatically. [Figure 13](#) illustrates the serial stream per PCLK cycle.

Note: The figure only illustrates the bits but does not actually represent the bit location as the bits are scrambled and balanced continuously.

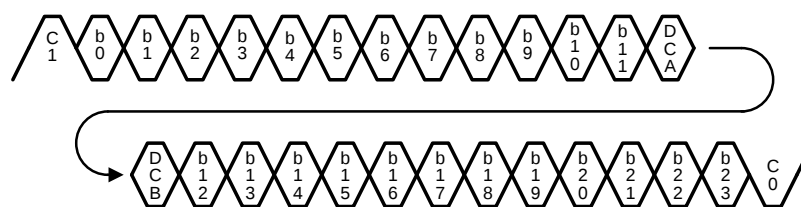


Figure 13. FPD-Link II Serial Stream

The device supports clocks in the range of 5 MHz to 65 MHz. With every clock cycle 24 bits of payload are received along with the four overhead bits. Thus, the line rate is 1.82 Gbps maximum (140 Mbps minimum) with an effective data rate of 1.56 Gbps maximum. The link is extremely efficient at 86% (24/28).

OPERATING MODES AND BACKWARD COMPATIBILITY (CONFIG[1:0])

The DS90UR908Q is backward compatible with previous generations of FPD-Link II serializers. Configuration modes are provided for backwards compatibility with the DS90C241 FPD-Link II Generation 1, and also the DS90UR241 or DS99R421 FPD-Link II Generation 2 serializer by setting the respective mode with the CONFIG[1:0] pins as shown in [Table 1](#). The selection also determine whether the Video Control Signal filter feature is enabled or disabled in Normal mode. This feature may be controlled by pin or by Register.

Table 1. DS90UR908Q Configuration Modes

CONFIG1	CONFIG0	Mode	Des Device
L	L	Normal Mode, Control Signal Filter disabled	DS90UR907Q, DS90UR905Q
L	H	Normal Mode, Control Signal Filter enabled	DS90UR907Q, DS90UR905Q
H	L	Backwards Compatible GEN2	DS90UR241, DS99R421
H	H	Backwards Compatible GEN1	DS90C241

VIDEO CONTROL SIGNAL FILTER

When operating the devices in Normal Mode, the Video Control Signals (DE, HS, VS) have the following restrictions:

- Normal Mode with Control Signal Filter Enabled:
 - DE and HS — Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 PCLK or longer.
- Normal Mode with Control Signal Filter Disabled:
 - DE and HS — Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- VS — Only 1 transition per 130 clock cycles are transmitted, minimum pulse width is 130 clock cycles.

Video Control Signals are defined as low frequency signals with limited transitions. Glitches of a control signal can cause a visual display error. This feature allows for the chipset to validate and filter out any high frequency noise on the control signals. See [Figure 14](#).

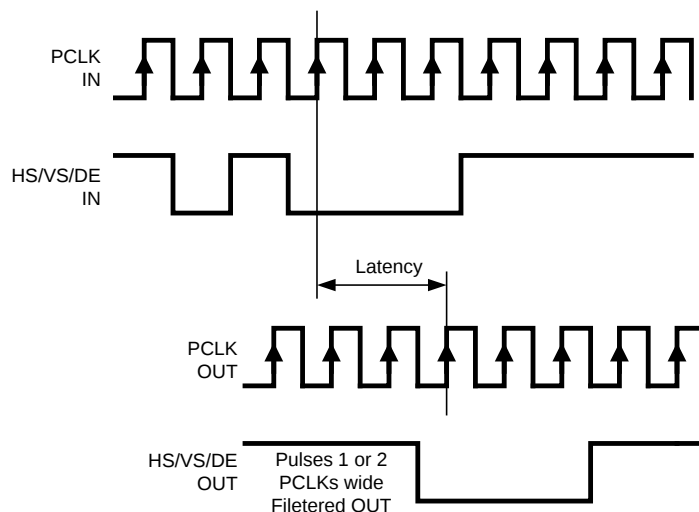


Figure 14. Video Control Signal Filter Waveform

COLOR BIT MAPPING SELECT

The DS90UR908Q can be configured to accept 24-bit color (8-bit RGB) with 2 different mapping schemes: LSBs on TxOUT[3] shown in [Figure 15](#) or MSBs on TxOUT[3] shown in [Figure 16](#). The user selects which mapping scheme is controlled by MAPSEL pin or by Register.

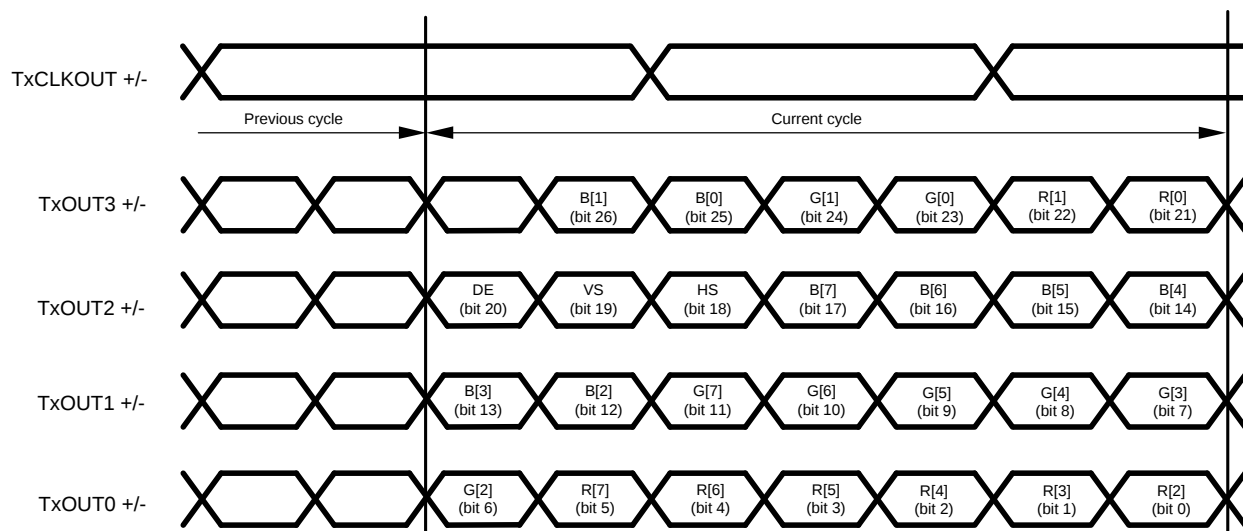


Figure 15. 8-bit FPD-Link Mapping: LSB's on TxOUT3

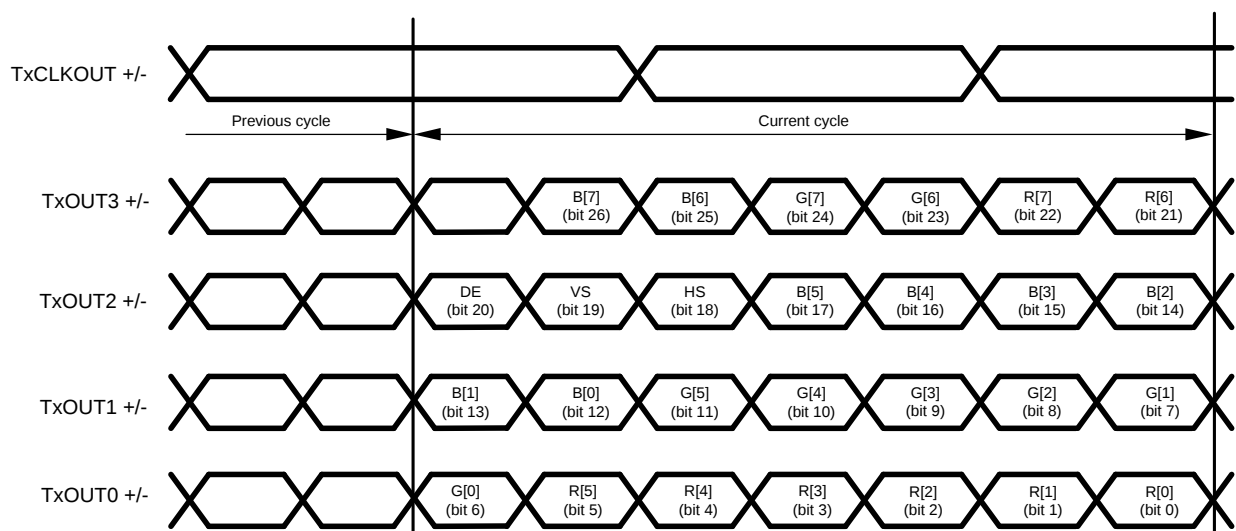


Figure 16. 8-bit FPD-Link Mapping: MSB's on TxOUT3

FPD-LINK II INPUT

Common Mode Filter Pin (CMF) — Optional

The DS90UR908Q provides access to the center tap of the internal termination. A capacitor may be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high noise environments for additional noise rejection capability. A 4.7 μF capacitor may be connected to this pin to Ground.

Input Equalizer Gain (EQ)

The DS90UR908Q can enable receiver input equalization of the serial stream to compensate the cable loss and increase the eye opening to the input. The equalization feature may be controlled by the EQ pin (strap option) [Table 4](#) or by register [Table 8](#).

Table 2. EQ Pin Configuration Table

EQ (Strap Option)	Effect
L	EQ = Off
H	~12 dB

POWER SAVING FEATURES

PowerDown Feature (PDB)

The DS90UR908Q has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the system to save power, disabling the Des when the display is not needed. An auto detect mode is also available. In this mode, the PDB pin is tied High and the Des will enter POWER DOWN when the serial stream stops. When the serial stream starts up again, the Des will lock to the input stream and assert the LOCK pin and output valid data. In POWER DOWN mode, the Data and PCLK output states are determined by the OSS_SEL status. Note – in POWER DOWN, the optional Serial Bus Control Registers are **RESET**.

Stop Stream SLEEP Feature

The DS90UR908Q will enter a low power SLEEP state when the input serial stream is stopped. A STOP condition is detected when the embedded clock bits are not present. When the serial stream starts again, the Des will then lock to the incoming signal and recover the data. Note – in STOP STREAM SLEEP, the optional Serial Bus Control Registers values are **RETAINED**.

OUTPUT INTERFACES (LVCMOS & FPD-LINK)

CLOCK-DATA RECOVERY STATUS FLAG (LOCK), OUTPUT ENABLE (OEN) and OUTPUT STATE SELECT (OSS_SEL)

When PDB is driven HIGH, the CDR PLL begins locking to the serial input, LOCK is Low and the FPD-Link interface state is determined by the state of the OSS_SEL pin.

After the DS90UR908Q completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the FPD-Link outputs. The TxCLK output is held at its current state at the change from OSC_CLK (if this is enabled via OSC_SEL) to the recovered clock (or vice versa). Note that the FPD-Link outputs may be held in an inactive state (TRI-STATE) through the use of the Output Enable pin (OEN).

If there is a loss of clock from the input serial stream, LOCK is driven Low and the state of the outputs are based on the OSS_SEL setting (configuration pin or register).

Table 3. Output State Table

INPUTS			OUTPUTS	
PDB	OEN	OSS_SEL	LOCK	OTHER OUTPUTS
L	X	X	X	TxCLKOUT is TRI-STATE TxOUT[3:0] are TRI-STATE PASS is TRI-STATE
L	X	L	L	TxCLKOUT is TRI-STATE TxOUT[3:0] are TRI-STATE PASS is HIGH
H	L	H	L	TxCLKOUT is TRI-STATE TxOUT[3:0] are TRI-STATE PASS is TRI-STATE
H	H	H	L	TxCLKOUT is TRI-STATE or OSC Output through Register bit TxOUT[3:0] are TRI-STATE PASS is TRI-STATE
H	L	X	H	TxCLKOUT is TRI-STATE TxOUT[3:0] are TRI-STATE PASS is HIGH
H	H	X	H	TxCLKOUT is Active TxOUT[3:0] are Active PASS is Active (Normal operating mode)

LVC MOS 1.8V / 3.3V VDDIO Operation

The LVCMOS outputs can operate with 1.8 V or 3.3 V levels (V_{DDIO}) for target (Display) compatibility. The 1.8 V levels will offer a system power savings. This applies to the following pins: PASS and LOCK.

FPD-LINK OUTPUT**VODSEL**

The differential output voltage of the FPD-Link interface is controlled by the VODSEL input.

Table 4. VODSEL Configuration Table

VODSEL	Result
L	VOD is 250mV TYP (500mVp-p)
H	VOD is 400mV TYP (800mVp-p)

SSCG GENERATION — OPTIONAL

The Des provides an internally generated spread spectrum clock (SSCG) to modulate its outputs. Both clock and data outputs are modulated. This will aid to lower system EMI. Output SSCG deviations to $\pm 2.0\%$ (4% total) at up to 35kHz modulations nominally are available. See [Table 5](#) and [Table 6](#). This feature may be controlled by pins or by register. The LFMODE should be set appropriately if the SSCG is being used. Set LFMODE High if the clock frequency is between 5 MHz and 20 MHz, set LFMODE Low if the clock frequency is between 20 MHz and 65 MHz.

Table 5. SSCG Configuration (LFMODE = L) — Des Output

SSC[2:0] Inputs LFMODE = L (20 - 65 MHz)			Result	
SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	OFF	OFF
L	L	H	± 0.9	CLK/2168
L	H	L	± 1.2	
L	H	H	± 1.9	
H	L	L	± 2.3	
H	L	H	± 0.7	CLK/1300
H	H	L	± 1.3	
H	H	H	± 1.7	

Table 6. SSCG Configuration (LFMODE = H) — Des Output

SSC[2:0] Inputs LFMODE = H (5 - 20 MHz)			Result	
SSC2	SSC1	SSC0	fdev (%)	fmod (kHz)
L	L	L	OFF	OFF
L	L	H	± 0.7	CLK/625
L	H	L	± 1.3	
L	H	H	± 1.8	
H	L	L	± 2.2	
H	L	H	± 0.7	CLK/385
H	H	L	± 1.2	
H	H	H	± 1.7	

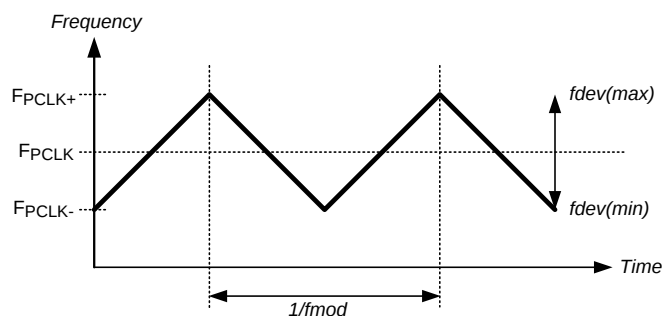
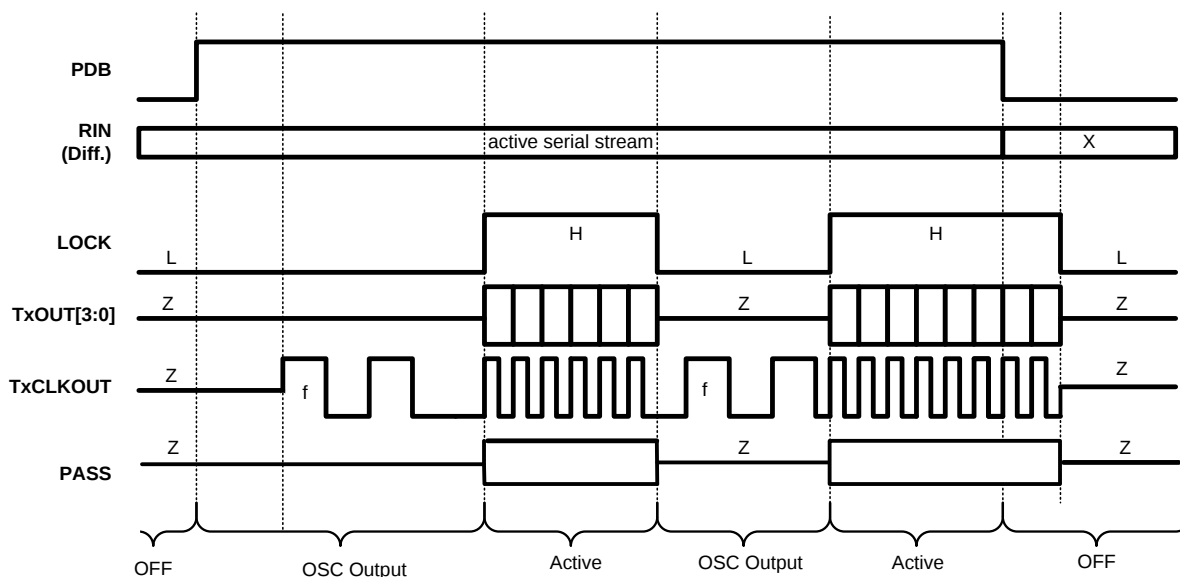


Figure 17. SSCG Waveform

OSCILLATOR OUTPUT — OPTIONAL

The DS90UR908Q provides an optional TxCLKOUT when the input clock (serial stream) has been lost. This is based on an internal oscillator. The frequency of the oscillator may be selected. This feature may be controlled by the external pin and the register. See [Table 3](#), [Table 8](#), and [Figure 18](#).



CONDITIONS: OEN = H, OSS_SEL = H, and OSC_SEL not equal to 000.

Figure 18. TxCLKOUT Output Oscillator Option Enabled

Built In Self Test (BIST) — Optional

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high-speed serial link. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. In the BIST mode only an input clock is required along with control to the Ser and Des BISTEN input pins. The Ser outputs a test pattern (PRBS7) and drives the link at speed. The Des detects the PRBS7 pattern and monitors it for errors. The PASS output pin toggles to flag any payloads that are received with 1 to 24 bit errors. The BISTM pin selects the operational mode of the PASS pin. If BISTM = L, the PASS pins reports the final result only. If BISTM = H, the PASS pins counts payload errors and also results the result. The result of the test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the Des BISTEN pin.

Sample BIST Sequence

See [Figure 19](#) for the BIST mode flow diagram.

Step 1: Place the DS90UR907Q or DS90UR905Q in BIST Mode by setting BISTEN = H. The BIST Mode is enabled via the BISTEN pin. An RxCLKIN or PCLK is required for all the Ser options. When the DS90UR908Q detects the BIST mode pattern and command (DCA and DCB code) the RGB and control signal outputs are shut off.

Step 2: Place the DS90UR908Q in BIST mode by setting the BISTEN = H. The Device is now in the BIST mode and checks the incoming serial payloads for errors. If an error in the payload (1 to 24) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the DS90UR908Q BISTEN pin is set Low. It stops checking the data and the final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: To return the link to normal operation, the serializer BISTEN input is set Low. The Link returns to normal operation.

[Figure 20](#) shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing signal condition enhancements (De-Emphasis, VODSEL, or Rx Equalization).

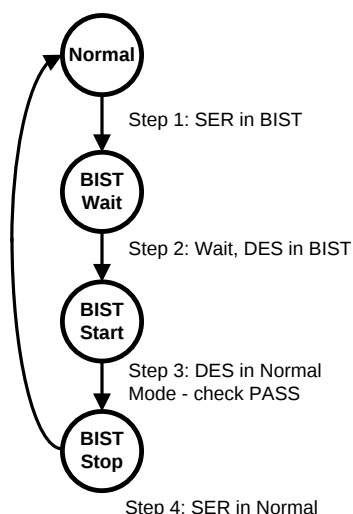


Figure 19. BIST Mode Flow Diagram

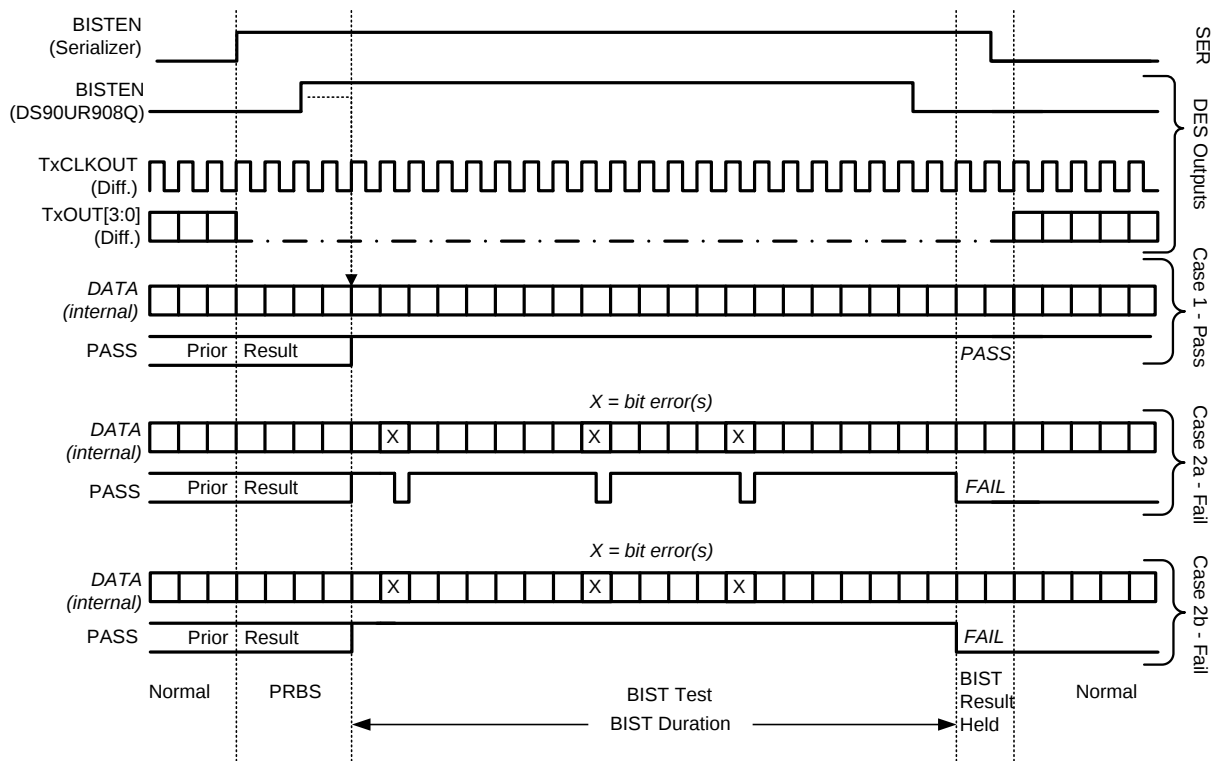


Figure 20. BIST Waveforms

Serial Bus Control — Optional

The DS90UR908Q may also be configured by the use of a serial control bus that is I2C protocol compatible. By default, the I2C reg_0x00'h is set to 00'h and all configuration is set by control/strap pins. A write of 01'h to reg_0x00'h will enable/allow configuration by registers; this will override the control/strap pins. Multiple devices may share the serial control bus since multiple addresses are supported. See [Figure 21](#).

The serial bus is comprised of three pins. The SCL is a Serial Bus Clock Input. The SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull up resistor to V_{DDIO} . For most applications a 4.7 k pull up resistor to V_{DDIO} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

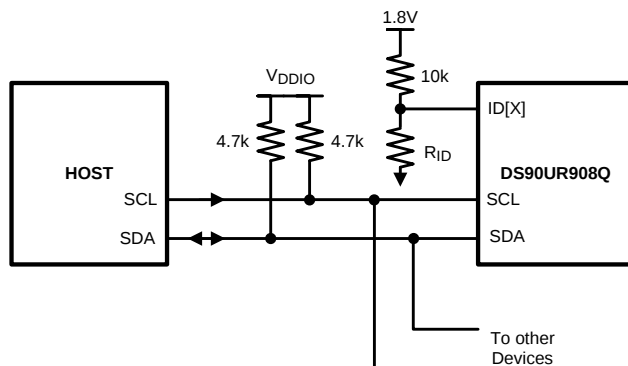


Figure 21. Serial Control Bus Connection

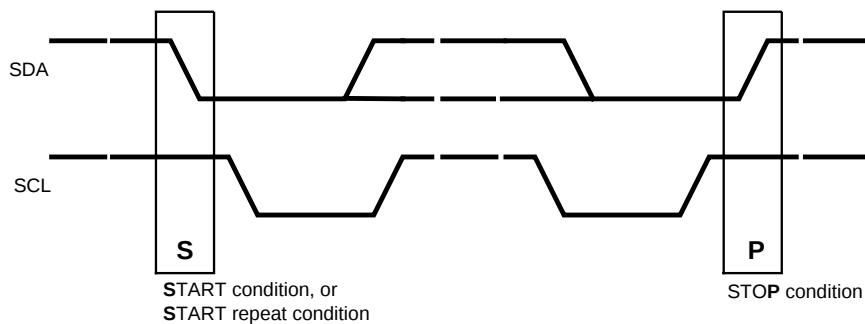


Figure 22. START and STOP Conditions

The third pin is the ID[X] pin. This pin sets one of five possible device addresses. Two different connections are possible. The pin may be pulled to V_{DD} (**1.8V, NOT V_{DDIO}**) with a 10 k Ω resistor. Or a 10 k Ω pull up resistor (to V_{DD} **1.8V, NOT V_{DDIO}**) and a pull down resistor of the recommended value to set other three possible addresses may be used. See [Table 7](#) for the Des. Do not tie ID[x] directly to ground.

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transition High while SCL is also HIGH. See [Figure 22](#).

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus ends with a Stop condition. A READ is shown in [Figure 23](#) and a WRITE is shown in [Figure 24](#).

If the Serial Bus is not required, the three pins may be left open (NC).

Table 7. ID[x] Resistor Value

Resistor RID k Ω (5%tol)	Address 7'b	Address 8'b 0 appended (WRITE)
0.47	7b' 111 0001 (h'71)	8b' 1110 0010 (h'E2)
2.7	7b' 111 0010 (h'72)	8b' 1110 0100 (h'E4)
8.2	7b' 111 0011 (h'73)	8b' 1110 0110 (h'E6)
Open	7b' 111 0110 (h'76)	8b' 1110 1100 (h'EC)

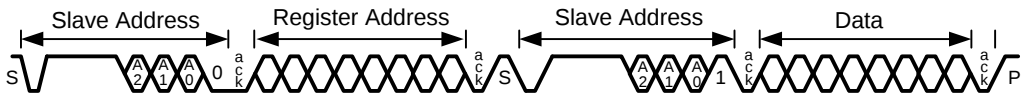


Figure 23. Serial Control Bus — READ

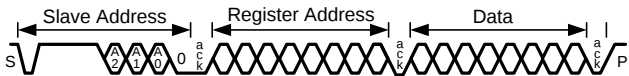


Figure 24. Serial Control Bus — WRITE

Table 8. Serial Bus Control Registers

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
0	0	Des Config 1	7	R/W	0	LFMODE	0: 20 to 65 MHz Operation 1: 5 to 20 MHz Operation
			6	R/W	0	MAPSEL	FPD-Link Map Select 0: LSB on TxOUT3+/- 1: MSB on TxOUT3+/-
			5	R/W	0	Reserved	Reserved
			4	R/W	0	Reserved	Reserved
			3:2	R/W	00	CONFIG	00: Normal Mode, Control Signal Filter Disabled 01: Normal Mode, Control Signal Filter Enabled 10: Backwards Compatible (DS90UR241) 11: Backwards Compatible (DS90C241)
			1	R/W	0	SLEEP	Note – not the same function as PowerDown (PDB) 0: normal mode 1: Sleep Mode – Register settings retained.
			0	R/W	0	REG Control	0: Configurations set from control pins / STRAP pin 1: Configurations set from registers (except I2C_ID)
1	1	Slave ID	7	R/W	0		0: Address from ID[X] Pin 1: Address from Register
			6:0	R/W	1110000	ID[X]	Serial Bus Device ID. Four IDs are: 7b '1110 001 (h'71); 8b ' 1110 0010 (h'E2) 7b '1110 010 (h'72); 8b ' 1110 0100 (h'E4) 7b '1110 011 (h'73); 8b ' 1110 0110 (h'E6) 7b '1110 110 (h'76); 8b ' 1110 1100 (h'EC) All other addresses are Reserved .
2	2	Des Features 1	7	R/W	0	OEN	Output Enable Input, Table 3
			6	R/W	0	OSS_SEL	Output Sleep State Select, Table 3
			5:4	R/W	00	Reserved	Reserved
			3	R/W	0	VODSEL	Differential Driver Output Voltage Select 0: LVDS VOD is ± 250 mV, 500 mVp-p (typ) 1: LVDS VOD is ± 400 mV, 800 mVp-p (typ)
			2:0	R/W	00	OSC_SEL	000: OFF 001: Reserved 010: 25 MHz $\pm 40\%$ 011: 16.7 MHz $\pm 40\%$ 100: 12.5 MHz $\pm 40\%$ 101: 10 MHz $\pm 40\%$ 110: 8.3 MHz $\pm 40\%$ 111: 6.3 MHz $\pm 40\%$

Table 8. Serial Bus Control Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	R/W	Default (bin)	Function	Description
3	3	Des Features 2	7:5	R/W	000	EQ Gain	000: ~1.625 dB 001: ~3.25 dB 010: ~4.87 dB 011: ~6.5 dB 100: ~8.125 dB 101: ~9.75 dB 110: ~11.375 dB 111: ~13 dB
			4	R/W	0	EQ Enable	0: EQ = disabled 1: EQ = enabled
			3	R/W	0	Reserved	Reserved
			2:0	R/W	000	SSC	IF LFMODE = 0, then: 000: SSCG OFF 001: fdev = ±0.9%, fmod = CLK/2168 010: fdev = ±1.2%, fmod = CLK/2168 011: fdev = ±1.9%, fmod = CLK/2168 100: fdev = ±2.3%, fmod = CLK/2168 101: fdev = ±0.7%, fmod = CLK/1300 110: fdev = ±1.3%, fmod = CLK/1300 111: fdev = ±1.57%, fmod = CLK/1300 IF LFMODE = 1, then: 000: SSCG OFF 001: fdev = ±0.7%, fmod = CLK/625 010: fdev = ±1.3%, fmod = CLK/625 011: fdev = ±1.8%, fmod = CLK/625 100: fdev = ±2.2%, fmod = CLK/625 101: fdev = ±0.7%, fmod = CLK/385 110: fdev = ±1.2%, fmod = CLK/385 111: fdev = ±1.7%, fmod = CLK/385

APPLICATIONS INFORMATION

DISPLAY APPLICATION

The DS90UR908Q, in conjunction with the DS90UR907Q or DS90UR905Q, is intended for interfacing between a host (graphics processor) and a Display. It supports an 24-bit color depth (RGB888) and up to 1024 X 768 display formats. In a RGB888 application, 24 color bits (R[7:0], G[7:0], B[7:0]), Pixel Clock (PCLK) and three control bits (VS, HS and DE) are supported across the serial link with PCLK rates from 5 to 65 MHz. The device may also be used in 18-bit color applications. In this application three to six general purpose signals may also be send from host to display.

TYPICAL APPLICATION CONNECTION

Figure 25 shows a typical application of the DS90UR908Q for a 65 MHz XGA Display. The LVDS inputs utilize 100 nF coupling capacitors to the line and the Receiver provides internal termination. Bypass capacitors are placed near the power supply pins. Ferrite beads are placed on the power lines for effective noise suppression.

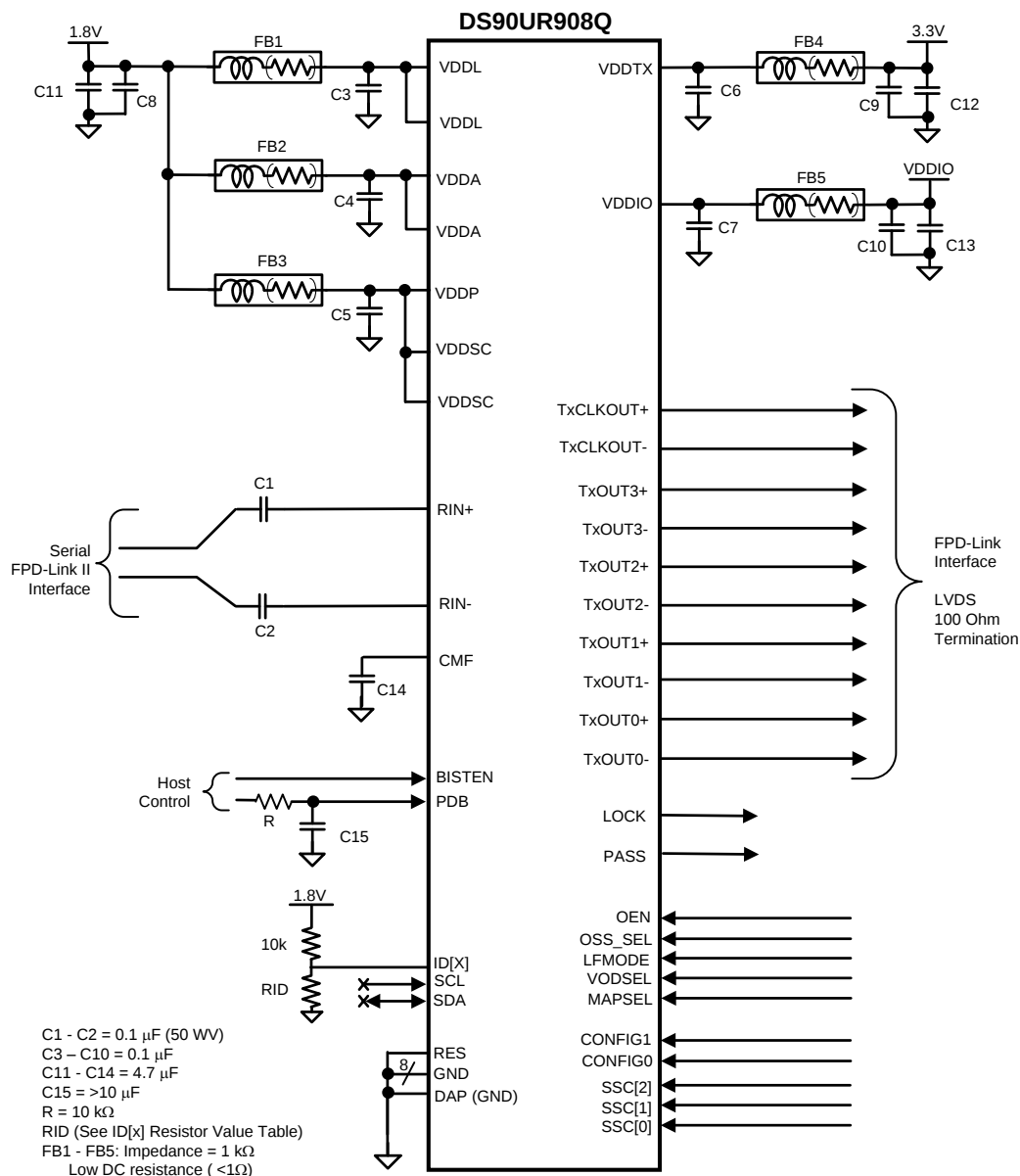


Figure 25. DS90UR908Q Typical Connection Diagram

POWER UP REQUIREMENTS AND PDB PIN

The VDD (V_{DDn}), V_{DDTX} and V_{DDIO} supply ramps should be faster than 1.5 ms with a monotonic rise. Supplies may power up in any order, however device operation should be initiated only after all supplies are in their valid operating ranges. The optional serial bus address selection is done upon power up also. Thus, if using this optional feature, the PDB signal must be delayed to allow time for the ID setting to occur. The delay may be done by simply holding the PDB pin at a Low, or with an external RC delay based off the V_{DDIO} rail which would then need to lag the others in time. If the PDB pin is pulled to V_{DDIO} , it is recommended to use a 10 k Ω pull-up and a 10 μ F cap to GND to delay the PDB input signal.

TRANSMISSION MEDIA

The FPD-Link II chipset is intended to be used in a point-to-point configuration, through a PCB trace, or through twisted pair cable. The serializer and deserializer provide internal terminations providing a clean signaling environment. The interconnect for LVDS should present a differential impedance of 100 Ω . Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Shielded or unshielded cables may be used depending upon the noise environment and application requirements.

LIVE LINK INSERTION

The serializer and deserializer devices support live pluggable applications. The automatic receiver lock to random data “plug & go” hot insertion capability allows the DS90UR908Q to attain lock to the active data stream during a live insertion event.

ALTERNATE COLOR / DATA MAPPING

Color Mapped data Pin names are provided to specify a recommended mapping for 24-bit and 18-bit Applications. When connecting to earlier generations of FPD-Link II serializer devices, a color mapping review is recommended to ensure the correct connectivity is obtained. [Table 9](#) provides examples for interfacing between DS90UR908Q and different deserializers.

Table 9. Alternate Color / Data Mapping

FPD-Link	Bit Number	RGB (LSB Example)	DS90UR905Q	DS90UR241	DS99R421	DS90C241
TxOUT3	Bit 26	B1	B1	N/A		
	Bit 25	B0	B0			
	Bit 24	G1	G1			
	Bit 23	G0	G0			
	Bit 22	R1	R1			
	Bit 21	R0	R0			
TxOUT2	Bit 20	DE	DE	DIN20	RxIN2	DIN20
	Bit 19	VS	VS	DIN19		DIN19
	Bit 18	HS	HS	DIN18		DIN18
	Bit 17	B7	B7	DIN17		DIN17
	Bit 16	B6	B6	DIN16		DIN16
	Bit 15	B5	B5	DIN15		DIN15
	Bit 14	B4	B4	DIN14		DIN14
TxOUT1	Bit 13	B3	B3	DIN13	RxIN1	DIN13
	Bit 12	B2	B2	DIN12		DIN12
	Bit 11	G7	G7	DIN11		DIN11
	Bit 10	G6	G6	DIN10		DIN10
	Bit 9	G5	G5	DIN9		DIN9
	Bit 8	G4	G4	DIN8		DIN8
	Bit 7	G3	G3	DIN7		DIN7

Table 9. Alternate Color / Data Mapping (continued)

FPD-Link	Bit Number	RGB (LSB Example)	DS90UR905Q	DS90UR241	DS99R421	DS90C241
TxOUT0	Bit 6	G2	G2	DIN6	RxIN0	DIN6
	Bit 5	R7	R7	DIN5		DIN5
	Bit 4	R6	R6	DIN4		DIN4
	Bit 3	R5	R5	DIN3		DIN3
	Bit 2	R4	R4	DIN2		DIN2
	Bit 1	R3	R3	DIN1		DIN1
	Bit 0	R2	R2	DIN0		DIN0
N/A			N/ADIN12	DIN23	OS2	DIN23
				DIN22	OS1	DIN22
				DIN21	OS0	DIN21
DS90UR908Q Settings	MAPSEL = 0		CONFIG [1:0] = 00	CONFIG [1:0] = 10		CONFIG [1:0] = 11

PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the LVDS devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 μF to 0.1 μF . Tantalum capacitors may be in the 2.2 μF to 10 μF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50 μF to 100 μF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN style package is provided in TI Application Note: AN-1187 ([SNOA401](#)).

LVDS INTERCONNECT GUIDELINES

See AN-1108 ([SNLA008](#)) and AN-905 ([SNLA035](#)) for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
 - S = space between the pair
 - 2S = space between pairs
 - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the TI web site at: www.ti.com/lvds

Revision History

- **03/30/2010** — Initial Release
- **07/26/2010** — Update all final AC and DC parameter limits
- **08/09/2010** — Update Pin Description of VODSEL
- **04/16/2013** — Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UR908QSQ/NOPB	ACTIVE	WQFN	RHS	48	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	90UR908Q	Samples
DS90UR908QSQE/NOPB	ACTIVE	WQFN	RHS	48	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	90UR908Q	Samples
DS90UR908QSQX/NOPB	ACTIVE	WQFN	RHS	48	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	90UR908Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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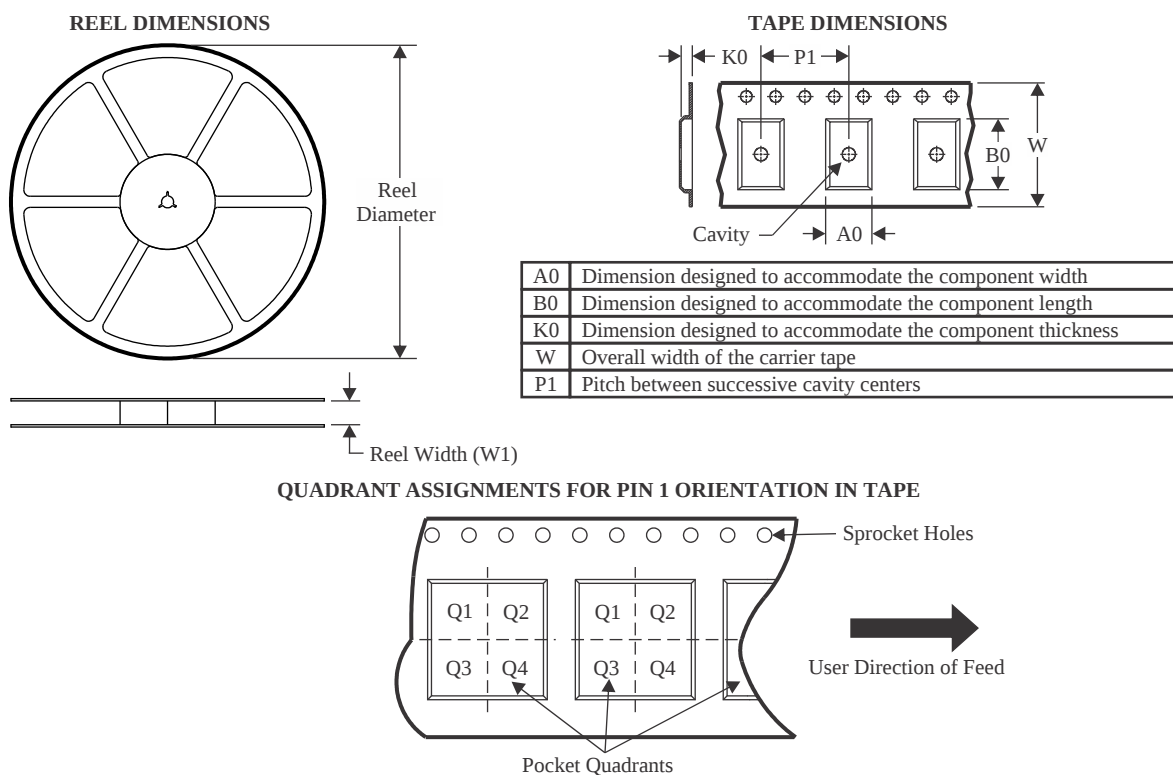
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PACKAGE OPTION ADDENDUM

10-Dec-2020

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

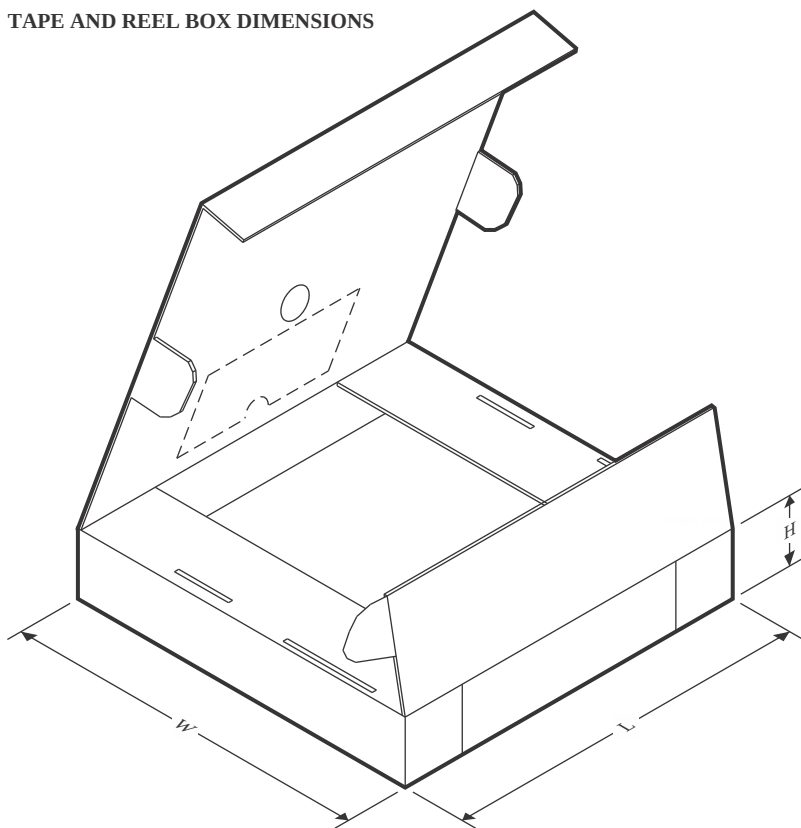
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UR908QSQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UR908QSQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UR908QSQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UR908QSQ/NOPB	WQFN	RHS	48	1000	356.0	356.0	35.0
DS90UR908QSQE/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0
DS90UR908QSQX/NOPB	WQFN	RHS	48	2500	356.0	356.0	35.0

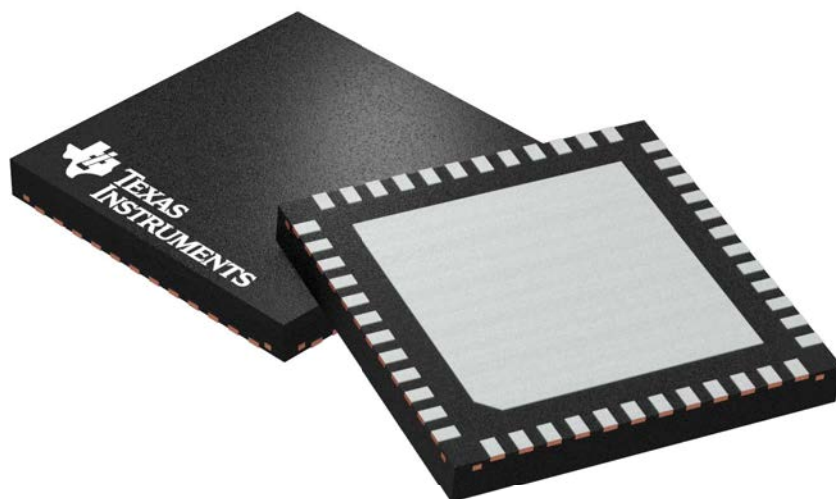
GENERIC PACKAGE VIEW

RHS 48

WQFN - 0.8 mm max height

7 x 7 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4205855/C

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