



LP5907 用于 RF 和模拟电路的超低噪声、250mA 线性稳压器 - 无需旁路电容

1 特性

- 输入电压范围：2.2V 至 5.5V
- 输出电压范围：1.2V 至 4.5V
- 输出电流：250mA
- 与 1 μ F 陶瓷输入和输出电容搭配使用，性能稳定
- 无需噪声旁路电容
- 支持远距离安置输出电容
- 热过载保护和短路保护
- 运行结温范围：-40°C 到 125°C
- 低输出电压噪声：< 10 μ V_{RMS}
- 电源抑制比 (PSRR)：1kHz 频率时为 82dB
- 输出电压容差： $\pm$ 2%
- 几乎零 IQ（禁用时）：< 1 μ A
- 极低 I_Q（使能时）：12 μ A
- 启动时间：80 μ s
- 低压降：120mV（典型值）

2 应用

- 手机
- PDA 手持终端
- 无线局域网 (LAN) 设备

3 说明

LP5907 是一款能够提供 250mA 输出电流的线性稳压器。此器件专门针对 RF 和模拟电路而设计，可满足其低噪声、高 PSRR、低静态电流以及低线路或负载瞬态响应系数等诸多要求。LP5907 采用创新的设计技术，无需噪声旁路电容便可提供出色的噪声性能，并且支持远距离安置输出电容。

此器件设计为与 1 μ F 输入和 1 μ F 输出陶瓷电容搭配使用（无需独立的噪声旁路电容）。

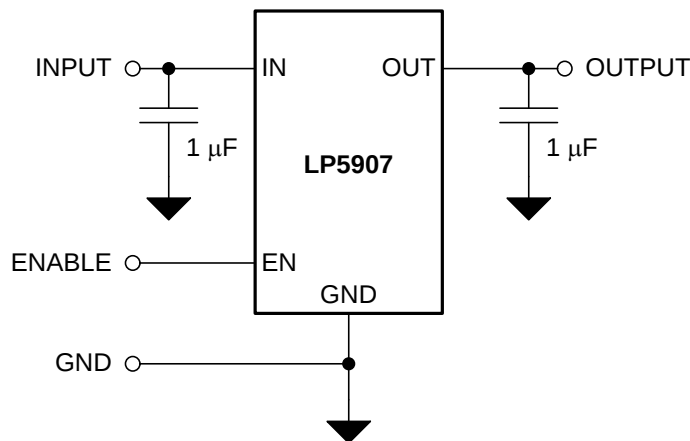
其固定输出电压介于 1.20V 和 4.50V 之间（以 25mV 为单位增量）。如需特定的电压选项，请联系德州仪器 (TI) 销售代表。

器件信息⁽¹⁾

器件型号	封装	封装尺寸
LP5907	DSBGA (4)	0.675mm x 0.675mm（最大值）
	SOT-23 (5)	2.90mm x 1.60mm（标称值）
	X2SON (4)	1.00mm x 1.00mm（标称值）

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



目录

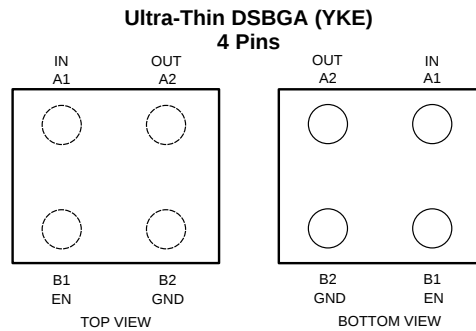
1	特性	1	7.4	Device Functional Modes.....	12
2	应用	1	8	Applications and Implementation	13
3	说明	1	8.1	Application Information.....	13
4	修订历史记录	2	8.2	Typical Application	13
5	Pin Configuration and Functions	3	9	Power Supply Recommendations	16
6	Specifications	4	10	Layout	17
6.1	Absolute Maximum Ratings	4	10.1	Layout Guidelines	17
6.2	Handling Ratings.....	4	10.2	Layout Examples.....	17
6.3	Recommended Operating Conditions.....	4	10.3	X2SON Mounting	18
6.4	Thermal Information	5	10.4	DSBGA Mounting.....	18
6.5	Electrical Characteristics.....	5	10.5	DSBGA Light Sensitivity	18
6.6	Output and Input Capacitors	6	11	器件和文档支持	19
6.7	Typical Characteristics	7	11.1	文档支持	19
7	Detailed Description	11	11.2	商标	19
7.1	Overview	11	11.3	静电放电警告	19
7.2	Functional Block Diagram	11	11.4	术语表	19
7.3	Feature Description.....	11	12	机械封装和可订购信息	19

4 修订历史记录

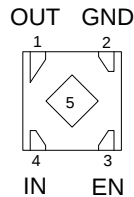
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (October 2013) to Revision H	Page
已添加 器件信息和处理额定值表，特性描述，器件功能模式，应用和实施，电源相关建议，布局，器件和文档支持，以及机械、封装和可订购信息部分；已将一些曲线移至应用曲线部分。	1

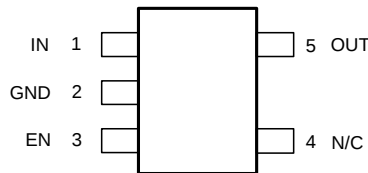
5 Pin Configuration and Functions



X2SON (DQN)
4 Pins
Bottom View



SOT-23 (DBV)
5 Pins
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	DSBGA NUMBER	X2SON NUMBER	SOT-23 NUMBER		
IN	A1	4	1	I	Input voltage supply. A 1- μ F capacitor should be connected at this input.
OUT	A2	1	5	O	Regulated output voltage. A minimum 1- μ F low-ESR capacitor should be connected to this pin. Connect this output to the load circuit. An internal 230- Ω (typical) pull-down resistor prevents a charge remaining on V_{OUT} when the regulator is in the shutdown mode (V_{EN} low).
EN	B1	3	3	I	Enable input. A low voltage ($< V_{IL}$) on this pin turns the regulator off and discharges the output pin to GND through an internal 230- Ω pull-down resistor. A high voltage ($> V_{IH}$) on this pin enables the regulator output. This pin has an internal 1M- Ω pull-down resistor to hold the regulator off by default.
GND	B2	2	2	—	Common ground
N/C	N/A	N/A	4	—	No internal electrical connection.
Thermal Pad	N/A	5	N/A	—	Thermal pad for X2SON package, connect to GND or leave floating. Do not connect to any potential other than GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage	−0.3	6	V
V _{OUT}	Output voltage	−0.3 to (V _{IN} + 0.3 V)	6	
V _{EN}	Enable input voltage	−0.3to (V _{IN} + 0.3 V)	6	
	Continuous power dissipation ⁽⁴⁾	Internally Limited		W
T _{JMAX}	Junction temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military or Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) All voltages are with respect to the GND pin.
- (4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature range		−65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	−2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	−1000	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
V _{IN}	Input supply voltage	2.2	5.5	V
V _{EN}	Enable input voltage	0 to (V _{IN} + 0.3)	5.5	
I _{OUT}	Output current	0	250	mA
T _J	Junction temperature	−40	125	°C
T _A	Ambient temperature ⁽³⁾	−40	85	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the GND pin.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} − (R_{θJA} × P_{D-MAX}). See [Application Information](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LP5907			UNIT
		SOT-23 (DBV)	X2SON (DQN)	DSBGA (YKE)	
		5 PINS	4 PINS	4 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	193.4	216.1	206.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	102.1	161.7	1.5	
R _{θJB}	Junction-to-board thermal resistance	45.8	162.1	37.0	
ψ _{JT}	Junction-to-top characterization parameter	8.4	5.1	15.0	
ψ _{JB}	Junction-to-board characterization parameter	45.3	161.7	36.8	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	123.0	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

V_{IN} = V_{OUT(NOM)} + 1 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 1 μF, unless otherwise stated.⁽¹⁾⁽²⁾⁽³⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN}	Input voltage	T _A = 25°C	2.2		5.5	V
ΔV _{OUT}	Output voltage tolerance	V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA to 250 mA, V _{OUT} ≥ 1.8 V	–2		2	%V _{OUT}
		V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA to 250 mA, V _{OUT} < 1.8 V	–3		3	
	Line regulation	V _{IN} = (V _{OUT(NOM)} + 1 V) to 5.5 V, I _{OUT} = 1 mA		0.02		%/V
	Load regulation	I _{OUT} = 1 mA to 250 mA		0.001		%/mA
I _{LOAD}	Load current	See ⁽⁴⁾	0		250	mA
	Maximum output current		250			
I _Q	Quiescent current ⁽⁵⁾	V _{EN} = 1.2 V, I _{OUT} = 0 mA		12	25	μA
		V _{EN} = 1.2 V, I _{OUT} = 250 mA		250	425	
		V _{EN} = 0.3 V (Disabled)		0.2	1	
I _G	Ground current ⁽⁶⁾	V _{EN} = 1.2 V, I _{OUT} = 0 mA		14		μA
V _{DO}	Dropout voltage ⁽⁷⁾	I _{OUT} = 100 mA		50		mV
		I _{OUT} = 250 mA (DSBGA)		120	200	
		I _{OUT} = 250 mA (SOT-23, X2SON packages)			250	
I _{SC}	Short circuit current limit	T _A = 25°C ⁽⁸⁾	250	500		mA
PSRR	Power supply rejection ratio ⁽⁹⁾	f = 100 Hz, I _{OUT} = 20 mA		90		dB
		f = 1 kHz, I _{OUT} = 20 mA		82		
		f = 10 kHz, I _{OUT} = 20 mA		65		
		f = 100 kHz, I _{OUT} = 20 mA		60		

- (1) All voltages are with respect to the device GND terminal, unless otherwise stated.
- (2) Minimum and maximum limits are ensured through test, design, or statistical correlation over the junction temperature (T_J) range of –40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application R_{θJA}, as given by the following equation: T_{A-MAX} = T_{J-MAX-OP} – (R_{θJA} × P_{D-MAX}). See [Applications and Implementation](#).
- (4) The device maintains a stable, regulated output voltage without a load current.
- (5) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.
- (6) Ground current is defined here as the total current flowing to ground as a result of all input voltages applied to the device.
- (7) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
- (8) Short-circuit current (I_{SC}) for the LP5907 is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100 mV below its nominal voltage.
- (9) This specification is verified by design.

Electrical Characteristics (continued)

 $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$, $V_{EN} = 1.2\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, unless otherwise stated.⁽¹⁾⁽²⁾⁽³⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
e _N	Output noise voltage ⁽⁹⁾	BW = 10 Hz to 100 kHz	I _{OUT} = 1 mA		10		μV _{RMS}
			I _{OUT} = 250 mA		6.5		
R _{AD}	Output Automatic Discharge pull-down resistance	V _{EN} < V _{IL} (output disabled)			230		Ω
T _{SD}	Thermal shutdown	T _J rising			160		°C
	Thermal hysteresis	T _J falling from shutdown			15		
LOGIC INPUT THRESHOLDS							
V _{IL}	Low input threshold	V _{IN} = 2.2 V to 5.5 V V _{EN} falling until the output is disabled				0.4	V
V _{IH}	High input threshold	V _{IN} = 2.2 V to 5.5 V V _{EN} rising until the output is enabled		1.2			V
I _{EN}	Input current at EN pin ⁽¹⁰⁾	V _{EN} = 5.5 V and V _{IN} = 5.5 V			5.5		μA
		V _{EN} = 0 V and V _{IN} = 5.5 V			0.001		
TRANSIENT CHARACTERISTICS							
ΔV _{OUT}	Line transient ⁽⁹⁾	V _{IN} = (V _{OUT(NOM)} + 1 V) to (V _{OUT(NOM)} + 1.6 V) in 30 μs		–1			mV
		V _{IN} = (V _{OUT(NOM)} + 1.6 V) to (V _{OUT(NOM)} + 1.6 V) in 30 μs				1	
	Load transient ⁽⁹⁾	I _{OUT} = 1 mA to 250 mA in 10 μs		–40			mV
		I _{OUT} = 250 mA to 1mA in 10 μs				40	
		Overshoot on start-up ⁽⁹⁾	Stated as a percentage of V _{OUT(NOM)}				5%
t _{ON}	Turnon time	From V _{EN} > V _{IH} to V _{OUT} = 95% of V _{OUT(NOM)} T _A = 25°C			80	150	μs

(10) There is a 1-M Ω resistor between EN and ground on the device.

6.6 Output and Input Capacitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN ⁽¹⁾	TYP	MAX	UNIT
C_{IN}	Input capacitance ⁽²⁾	Capacitance for stability	0.7	1		μF
C_{OUT}	Output capacitance ⁽²⁾		0.7	1	10	
ESR	Output/Input capacitance ⁽²⁾		5		500	m Ω

(1) The minimum capacitance should be greater than 0.5 μF over the full range of operating conditions. The capacitor tolerance should be 30% or better over the full temperature range. The full range of operating conditions for the capacitor in the application should be considered during device selection to ensure this minimum capacitance specification is met. X7R capacitors are recommended however capacitor types X5R, Y5V and Z5U may be used with consideration of the application and conditions.

(2) This specification is verified by design.

6.7 Typical Characteristics

Unless otherwise stated: $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$

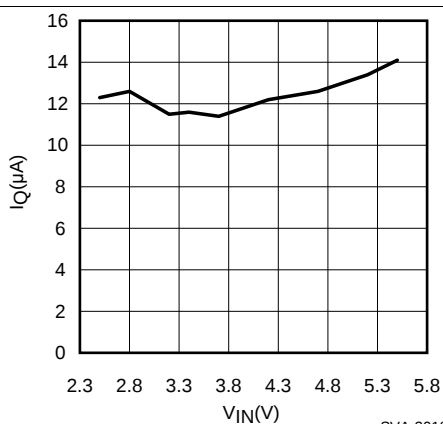


Figure 1. Quiescent Current vs Input Voltage

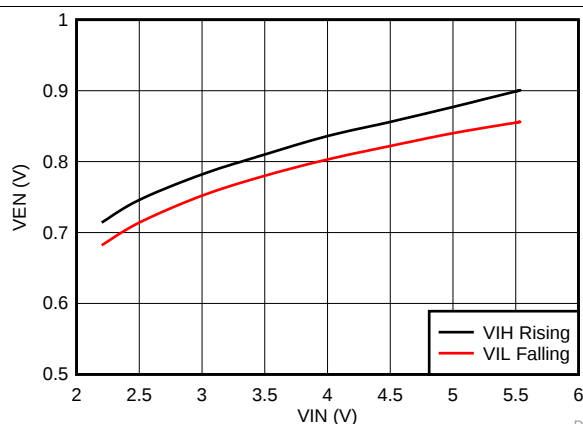


Figure 2. V_{EN} Thresholds vs V_{IN}

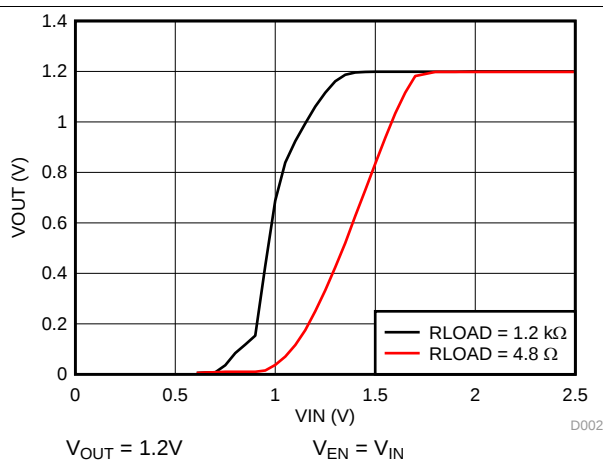


Figure 3. V_{OUT} vs V_{IN}

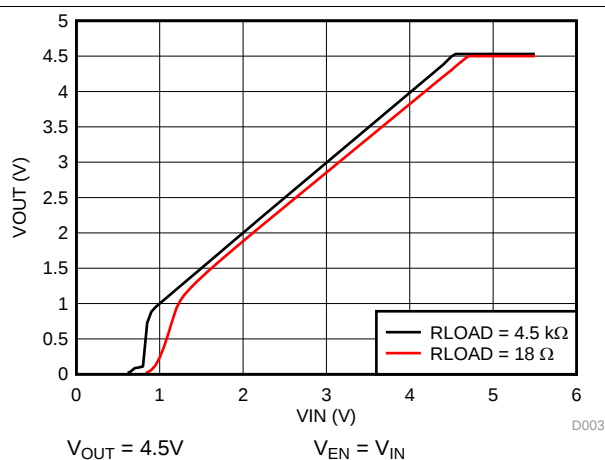


Figure 4. V_{OUT} vs V_{IN}

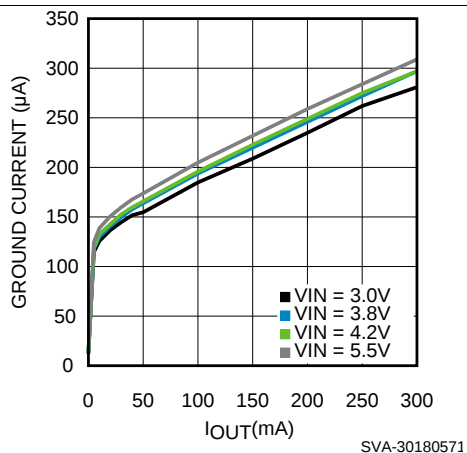


Figure 5. Ground Current vs Output Current

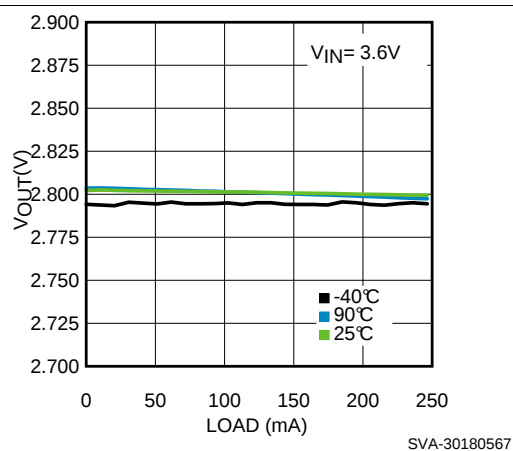


Figure 6. Load Regulation

Typical Characteristics (continued)

Unless otherwise stated: $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$

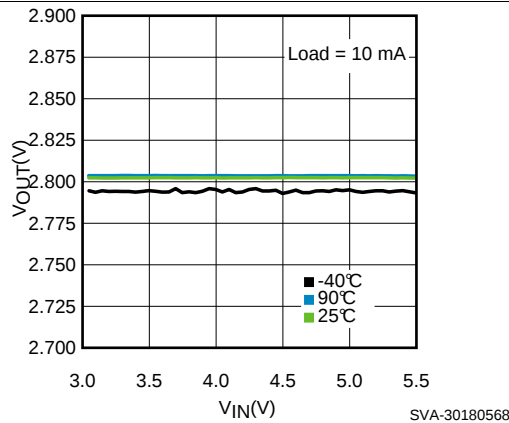


Figure 7. Line Regulation

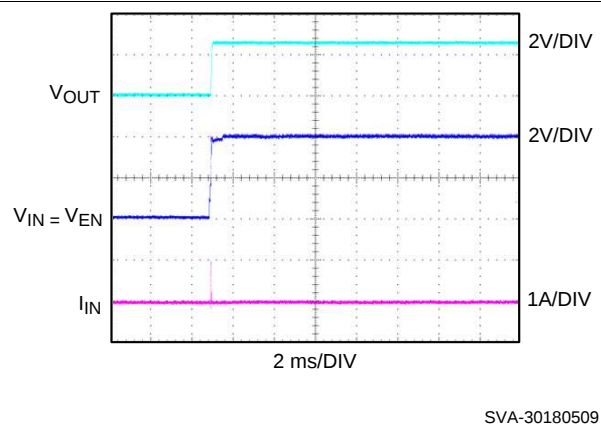


Figure 8. Inrush Current

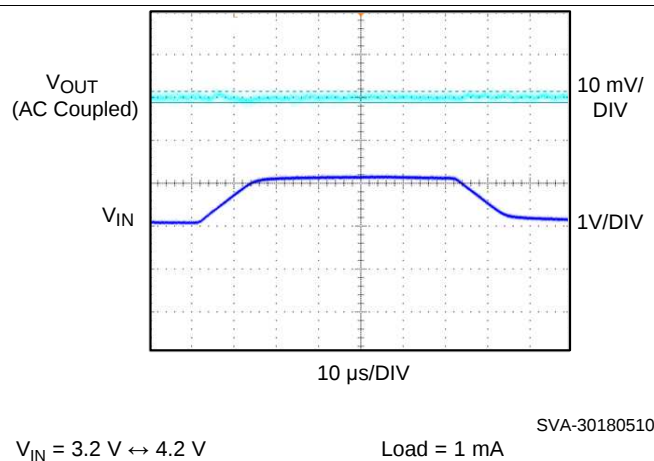


Figure 9. Line Transient

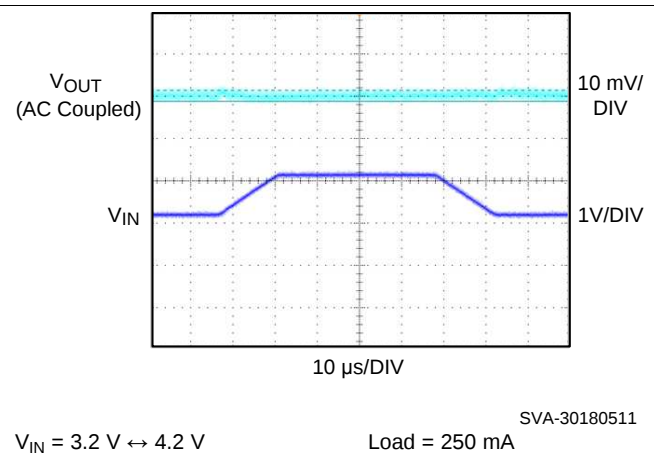


Figure 10. Line Transient

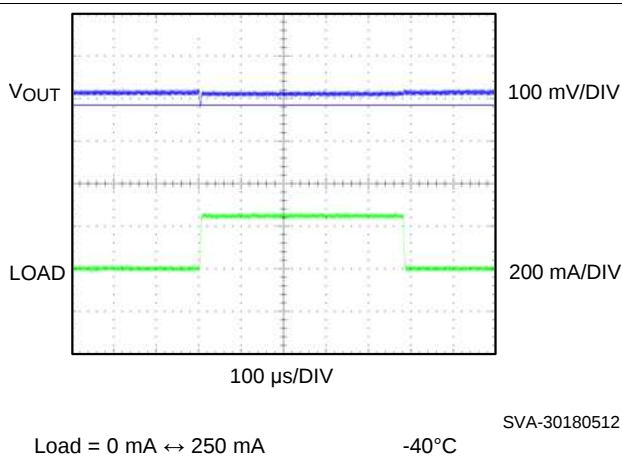


Figure 11. Load Transient

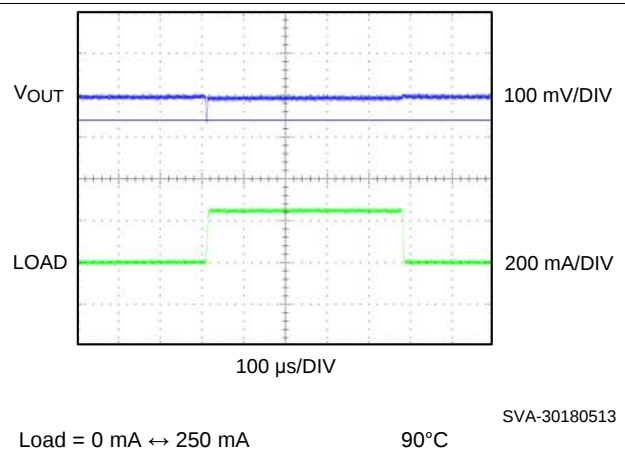


Figure 12. Load Transient

Typical Characteristics (continued)

Unless otherwise stated: $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$

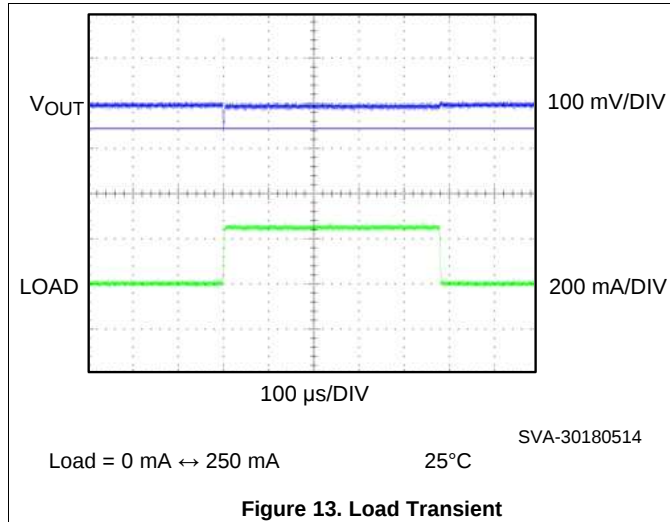


Figure 13. Load Transient

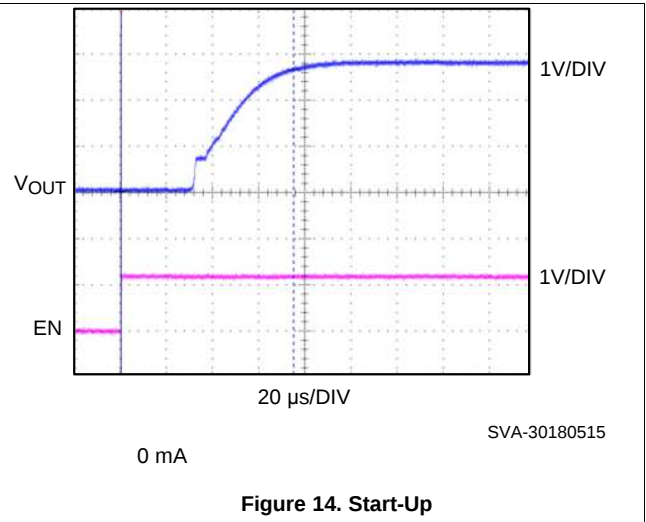


Figure 14. Start-Up

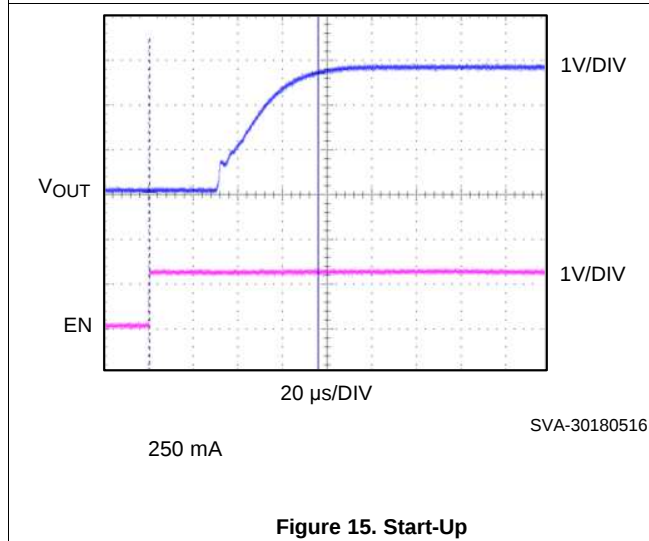


Figure 15. Start-Up

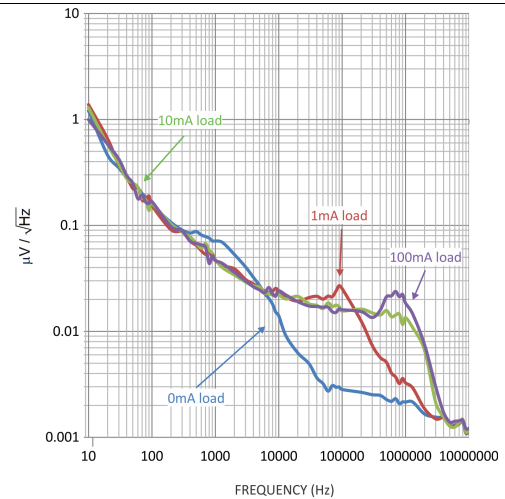


Figure 16. Noise Density Test

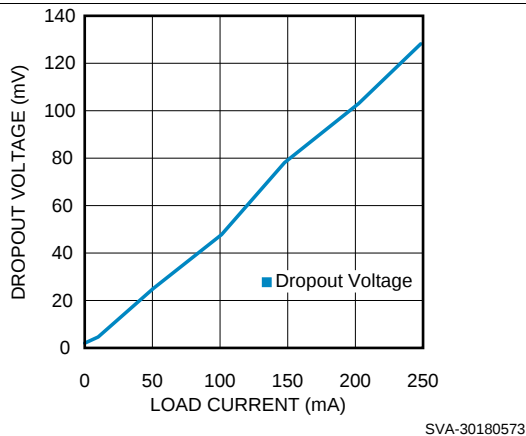


Figure 17. Dropout Voltage vs Load Current

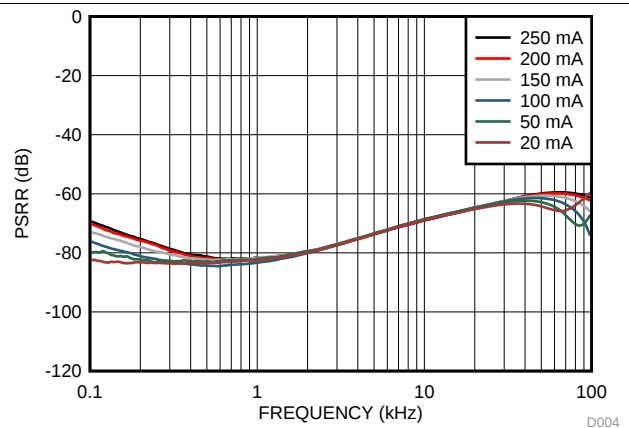


Figure 18. PSRR Loads Averaged 100 Hz To 100 KHz

LP5907

ZHCSD40H –APRIL 2012–REVISED NOVEMBER 2014

www.ti.com.cn

Typical Characteristics (continued)

Unless otherwise stated: $V_{IN} = 3.7\text{ V}$, $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_A = 25^\circ\text{C}$

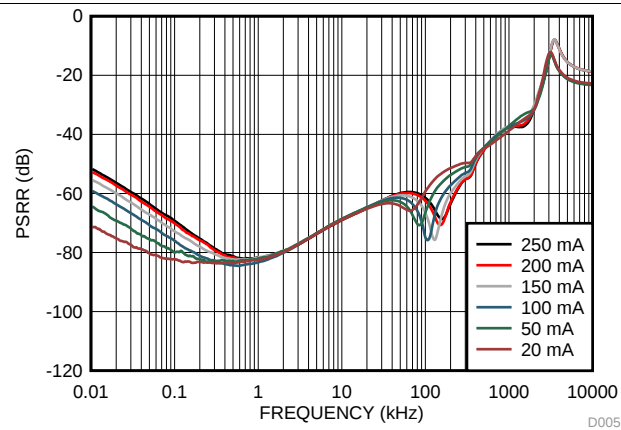


Figure 19. PSRR Loads Averaged 10 Hz To 10 MHz

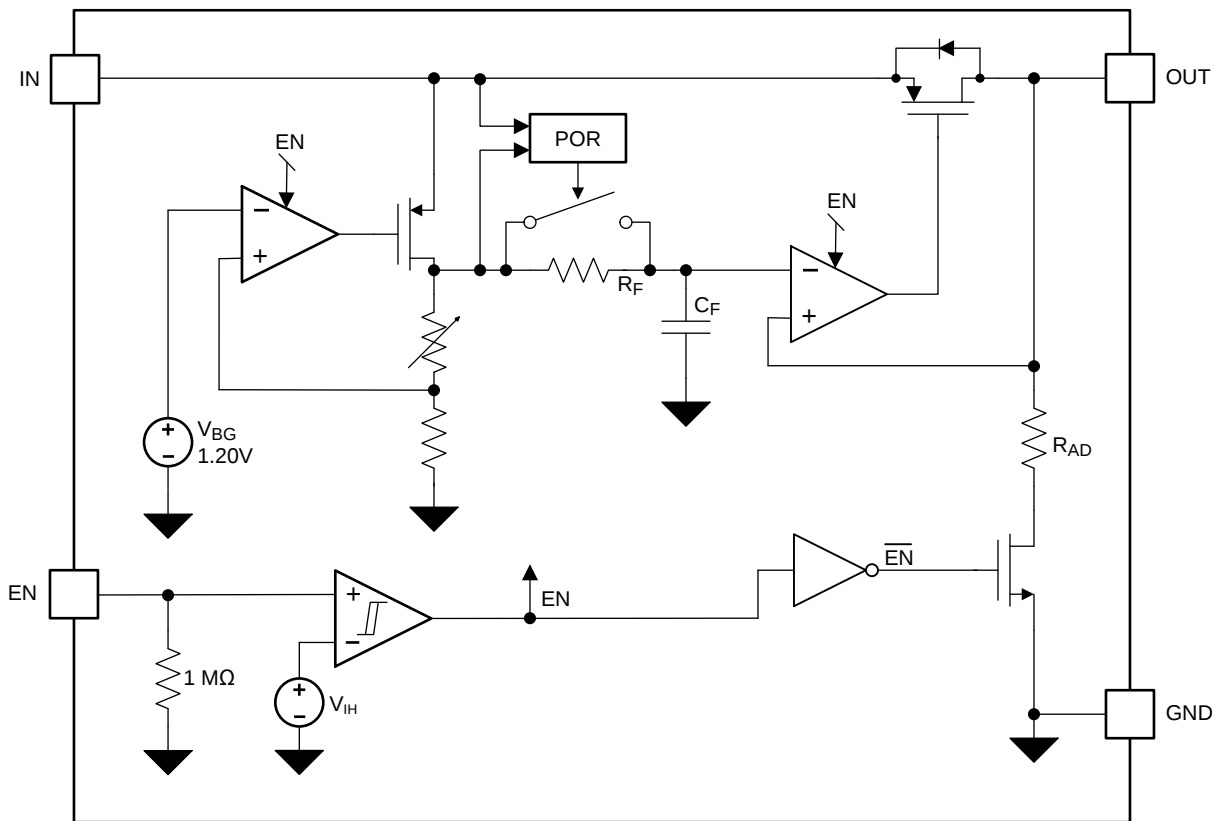
7 Detailed Description

7.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the LP5907 provides low noise, high PSRR, low quiescent current, as well as low line and load transient response figures. Using new innovative design techniques, the LP5907 offers class leading noise performance without the need for a separate noise filter capacitor.

The LP5907 is designed to perform with a single 1- μF input capacitor and a single 1- μF ceramic output capacitor. With a reasonable PCB layout, the single 1- μF ceramic output capacitor can be placed up to 10 cm away from the LP5907 package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The LP5907 EN pin is internally held low by a 1-M Ω resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{IL} threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

7.3.2 Low Output Noise

Any internal noise at the LP5907 reference voltage is reduced by a first order low-pass RC filter before it is passed to the output buffer stage. The low-pass RC filter has a –3 dB cut-off frequency of approximately 0.1 Hz.

Feature Description (continued)

7.3.3 Output Automatic Discharge

The LP5907 output employs an internal 230- Ω (typical) pull-down resistance to discharge the output when the EN pin is low, and the device is disabled.

7.3.4 Remote Output Capacitor Placement

The LP5907 requires at least a 1- μ F capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10 cm away from the LDO.

7.3.5 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the LP5907 has been designed to protect against temporary thermal overload conditions. The Thermal Shutdown circuitry was not intended to replace proper heat-sinking. Continuously running the LP5907 device into thermal shutdown may degrade device reliability.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP5907 Enable (EN) pin is internally held low by a 1-M Ω resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions.

When the EN pin is pulled low, and the output is disabled, the output automatic discharge circuitry is activated. Any charge on the OUT pin is discharged to GND through the internal 230- Ω (typical) pull-down resistance.

7.4.2 Minimum Operating Input Voltage (V_{IN})

The LP5907 does not include any dedicated UVLO circuitry. The LP5907 internal circuitry is not fully functional until V_{IN} is at least 2.2 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2 V or ($V_{OUT} + V_{DO}$).

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP5907 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1 μF . The LP5907 delivers this performance in industry standard packages such as DSBGA, X2SON, and SOT-23 which, for this device, are specified with an operating junction temperature (T_J) of -40°C to 125°C .

8.2 Typical Application

Figure 20 shows the typical application circuit for the LP5907. Input and output capacitances may need to be increased above the 1 μF minimum for some applications.

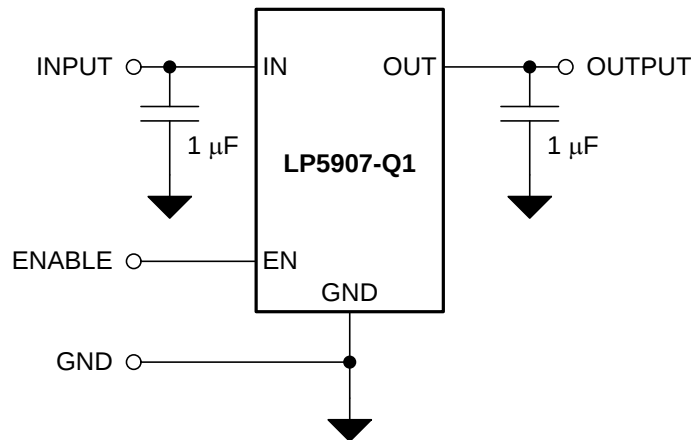


Figure 20. LP5907 Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.2 V to 5.5 V
Output voltage	1.8 V
Output current	200 mA
Output capacitor range	0.7 μF to 10 μF
Input/Output capacitor ESR range	5 to 500 m Ω

8.2.2 Detailed Design Procedure

8.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using [Equation 1](#):

$$P_{D-MAX} = ((T_{J-MAX} - T_A) / R_{\theta JA}) \quad (1)$$

The actual power being dissipated in the device can be represented by [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

These two equations establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature (T_{A-MAX}) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature (T_{A-MAX}) may have to be derated. T_{A-MAX} is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ\text{C}$), the maximum allowable power dissipation in the device package in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by [Equation 3](#):

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})) \quad (3)$$

Alternately, if T_{A-MAX} can not be derated, the P_D value must be reduced. This can be accomplished by reducing V_{IN} in the ' $V_{IN}-V_{OUT}$ ' term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

8.2.2.2 External Capacitors

Like most low-dropout regulators, the LP5907 requires external capacitors for regulator stability. The device is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.3 Input Capacitor

An input capacitor is required for stability. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance. At least a 1 μF capacitor has to be connected between the LP5907 input pin and ground for stable operation over full load current range. Basically, it is ok to have more output capacitance than input, as long as the input is at least 1 μF .

The input capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are to be used to connect the battery or other power source to the LP5907, then it is recommended to increase the input capacitor to at least 10 μF . Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be verified by the manufacturer to have a surge current rating sufficient for the application. The initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 μF over the entire operating range.

8.2.2.4 Output Capacitor

The LP5907 is designed specifically to work with a very small ceramic output capacitor, typically 1 μF . A ceramic capacitor (dielectric types X5R or X7R) in the 1 μF to 10 μF range, and with ESR between 5 m Ω to 500 m Ω , is suitable in the LP5907 application circuit. For this device the output capacitor should be connected between the OUT pin and a good connection back to the GND pin.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT} , but these are not as attractive for reasons of size and cost (see [Capacitor Characteristics](#)).

The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that is within the range 5 m Ω to 500 m Ω for stability. Like the input capacitor, the initial tolerance, applied voltage de-rating, and temperature coefficient must all be considered when selecting the input capacitor to ensure the actual capacitance is never less than 0.7 μF over the entire operating range.

8.2.2.5 Capacitor Characteristics

The LP5907 is designed to work with ceramic capacitors on the input and output to take advantage of the benefits they offer. For capacitance values in the range of 1 μF to 10 μF , ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1 μF ceramic capacitor is in the range of 20 m Ω to 40 m Ω , which easily meets the ESR requirement for stability for the LP5907.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within $\pm 15\%$ over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 μF to 10 μF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

8.2.2.6 Remote Capacitor Operation

The LP5907 requires at least a 1 μF capacitor at the OUT pin, but there is no strict requirements about the location of the capacitor in regards to the pin. In practical designs the output capacitor may be located up to 10 cm away from the LDO. This means that there is no need to have a special capacitor close to the output pin if there is already respective capacitors in the system (like a capacitor at the input of supplied part). The remote capacitor feature helps user to minimize the number of capacitors in the system.

As a good design practice, it is good to keep the wiring parasitic inductance at a minimum, which means to use as wide as possible traces from the LDO output to the capacitors, keeping the LDO output trace layer as close as possible to ground layer and avoiding vias on the path. If there is a need to use vias, implement as many as possible vias between the connection layers. The recommendation is to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, it is recommended to use an input capacitor equal to or larger to the sum of the capacitance at the output node for the best load transient performance.

8.2.2.7 No-Load Stability

The LP5907 remains stable, and in regulation, with no external load.

8.2.2.8 Enable Control

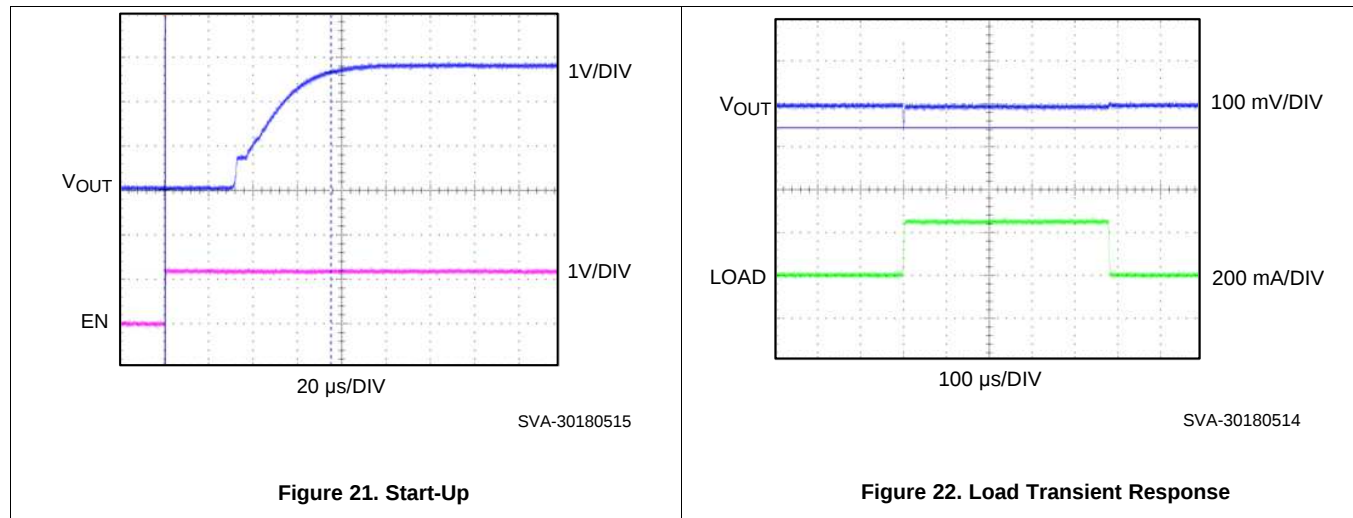
The LP5907 may be switched ON or OFF by a logic input at the EN pin. A voltage on this pin greater than V_{IH} turns the device on, while a voltage less than V_{IL} turns the device off.

When the EN pin is low, the regulator output is off and the device typically consumes less than 1 μA . Additionally, an output pull-down circuit is activated which ensures that any charge stored on C_{OUT} is discharged to ground.

If the application does not require the use of the shutdown feature, the EN pin can be tied directly to the IN pin to keep the regulator output permanently on.

An internal 1-M Ω pull-down resistor ties the EN input to ground, ensuring that the device remains off if the EN pin is left open circuit. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the [Electrical Characteristics](#) under V_{IL} and V_{IH} .

8.2.3 Application Curves



9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2.2 V to 5.5 V. The input supply should be well regulated and free of spurious noise. To ensure that the LP5907 output voltage is well regulated and dynamic performance is optimum, the input supply should be at least $V_{OUT} + 1$ V. A minimum capacitor value of 1 μ F is required to be within 1 cm of the IN pin.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP5907 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP5907.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5907, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} should be back to the LP5907 ground pin using as wide, and as short, of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided. These will add parasitic inductances and resistance that results in inferior performance especially during transient conditions

10.2 Layout Examples

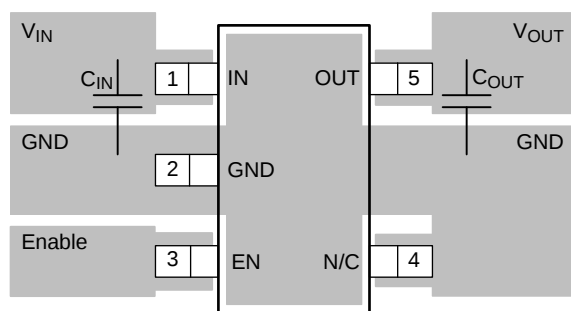


Figure 23. LP5907MF-x.x (SOT-23) Typical Layout

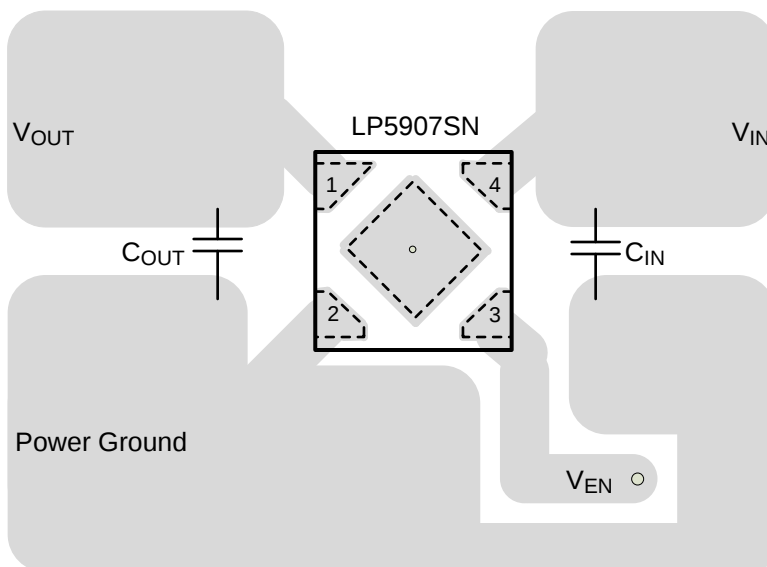


Figure 24. LP5907SN-xx (X2SON) Typical Layout

Layout Examples (continued)

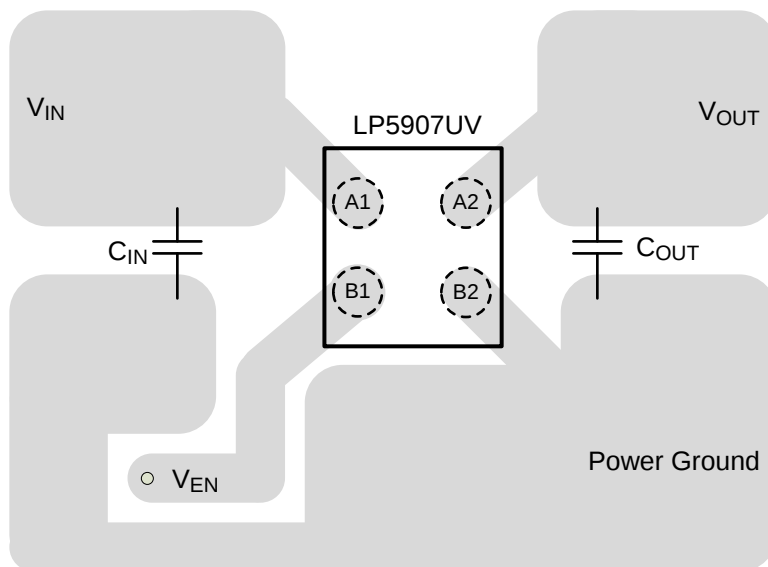


Figure 25. LP5907UV-x.x (DSBGA) Typical Layout

10.3 X2SON Mounting

The X2SON package thermal pad must be soldered to the printed circuit board for proper thermal and mechanical performance. For more information, see the Application Report *QFN/SON PCB Attachment* ([SLUA271](#)).

10.4 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in Texas Instruments Application Note AN-1112, *DSBGA Wafer Level Chip Scale Package* ([SNVA009](#)). For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

10.5 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device. Light with wavelengths in the red and infrared part of the spectrum have the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

德州仪器应用手册 AN-1112 《DSBGA 晶圆级芯片规模封装》（文献编号：SNVA009）。

德州仪器应用手册 《QFN/SON PCB 连接》（文献编号：SLUA271）

11.2 商标

All trademarks are the property of their respective owners.

11.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改, 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内, 且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定, 否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险, 客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息, 不能构成从 TI 获得使用这些产品或服务 的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可, 或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分, 仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时, 如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分, 则会失去相关 TI 组件 或服务的所有明示或暗示授权, 且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意, 尽管任何应用相关信息或支持仍可能由 TI 提供, 但他们将独力负责满足与其产品及其应用中使用的 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意, 他们具备制定与实施安全措施所需的全部专业技术和知识, 可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中, 为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此, 此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备) 的授权许可, 除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意, 对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用, 其风险由客户单独承担, 并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品, 这些产品主要用于汽车。在任何情况下, 因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com.cn/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址: 上海市浦东新区世纪大道1568 号, 中建大厦32 楼邮政编码: 200122
Copyright © 2014, 德州仪器半导体技术(上海)有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907A28YKMR	ACTIVE	DSBGA	YKM	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	Q	Samples
LP5907A33YKMR	ACTIVE	DSBGA	YKM	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-40 to 125	N	Samples
LP5907MFX-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLTB	Samples
LP5907MFX-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN8B	Samples
LP5907MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLUB	Samples
LP5907MFX-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN7B	Samples
LP5907MFX-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLYB	Samples
LP5907MFX-2.85/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN4B	Samples
LP5907MFX-2.9/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	1E5X	Samples
LP5907MFX-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLZB	Samples
LP5907MFX-3.1/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN5B	Samples
LP5907MFX-3.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LN6B	Samples
LP5907MFX-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLVB	Samples
LP5907MFX-4.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LLXB	Samples
LP5907SNX-1.2/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF	Samples
LP5907SNX-1.8/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CG	Samples
LP5907SNX-1.9	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	3Z	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907SNX-2.2/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	EP	Samples
LP5907SNX-2.5/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	F9	Samples
LP5907SNX-2.7/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CH	Samples
LP5907SNX-2.75	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HI	Samples
LP5907SNX-2.8/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CI	Samples
LP5907SNX-2.85/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CJ	Samples
LP5907SNX-2.9/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	GV	Samples
LP5907SNX-3.0/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CK	Samples
LP5907SNX-3.1/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CL	Samples
LP5907SNX-3.2/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CM	Samples
LP5907SNX-3.3/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CN	Samples
LP5907SNX-4.0/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	GU	Samples
LP5907SNX-4.5/NOPB	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CO	Samples
LP5907UVE-1.2/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R	Samples
LP5907UVE-1.8/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples
LP5907UVE-2.8/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples
LP5907UVE-2.85/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V	Samples
LP5907UVE-3.0/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5907UVE-3.1/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X	Samples
LP5907UVE-3.2/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
LP5907UVE-3.3/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP5907UVE-4.5/NOPB	ACTIVE	DSBGA	YKE	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	Samples
LP5907UVX-1.2/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	R	Samples
LP5907UVX-1.8/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples
LP5907UVX-2.5/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E	Samples
LP5907UVX-2.8/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	U	Samples
LP5907UVX-2.85/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	V	Samples
LP5907UVX-3.0/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	B	Samples
LP5907UVX-3.1/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	X	Samples
LP5907UVX-3.2/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	C	Samples
LP5907UVX-3.3/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP5907UVX-4.5/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Z	Samples
LP5907UVX19/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	8	Samples
LP5907UVX37/NOPB	ACTIVE	DSBGA	YKE	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

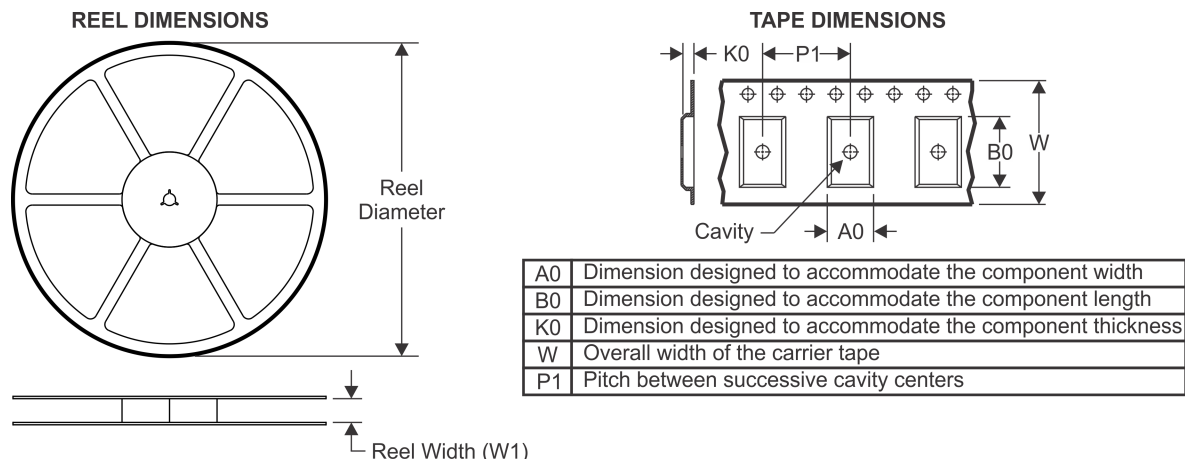
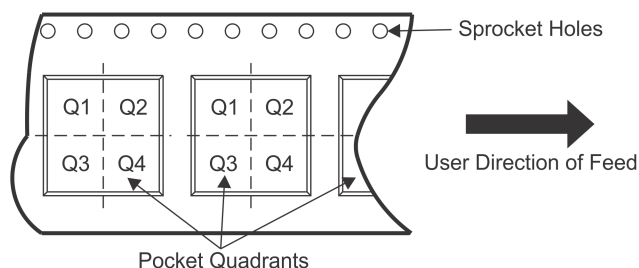
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LP5907 :

- Automotive: [LP5907-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907A28YKMR	DSBGA	YKM	4	3000	178.0	8.4	0.74	0.74	0.54	4.0	8.0	Q1
LP5907A33YKMR	DSBGA	YKM	4	3000	178.0	8.4	0.74	0.74	0.54	4.0	8.0	Q1
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5907SNX-1.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-1.9	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5907SNX-2.5/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.7/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.75	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.8/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.85/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-2.9/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.1/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.2/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-4.0/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907SNX-4.5/NOPB	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.7	0.7	0.48	4.0	8.0	Q1
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.7	0.7	0.48	4.0	8.0	Q1
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	178.0	8.4	0.71	0.71	0.51	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907A28YKMR	DSBGA	YKM	4	3000	220.0	220.0	35.0
LP5907A33YKMR	DSBGA	YKM	4	3000	220.0	220.0	35.0
LP5907MFX-1.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.85/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-2.9/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.1/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907MFX-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5907SNX-1.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-1.8/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-1.9	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.5/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.7/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5907SNX-2.75	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.8/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.85/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-2.9/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.0/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.1/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.2/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-3.3/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-4.0/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907SNX-4.5/NOPB	X2SON	DQN	4	3000	184.0	184.0	19.0
LP5907UVE-1.2/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-1.8/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-2.8/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-2.85/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-3.0/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-3.1/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-3.2/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-3.3/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVE-4.5/NOPB	DSBGA	YKE	4	250	210.0	185.0	35.0
LP5907UVX-1.2/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-1.8/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-2.5/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-2.8/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-2.85/NOPB	DSBGA	YKE	4	3000	220.0	220.0	35.0
LP5907UVX-3.0/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-3.1/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-3.2/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-3.3/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX-4.5/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX19/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0
LP5907UVX37/NOPB	DSBGA	YKE	4	3000	210.0	185.0	35.0

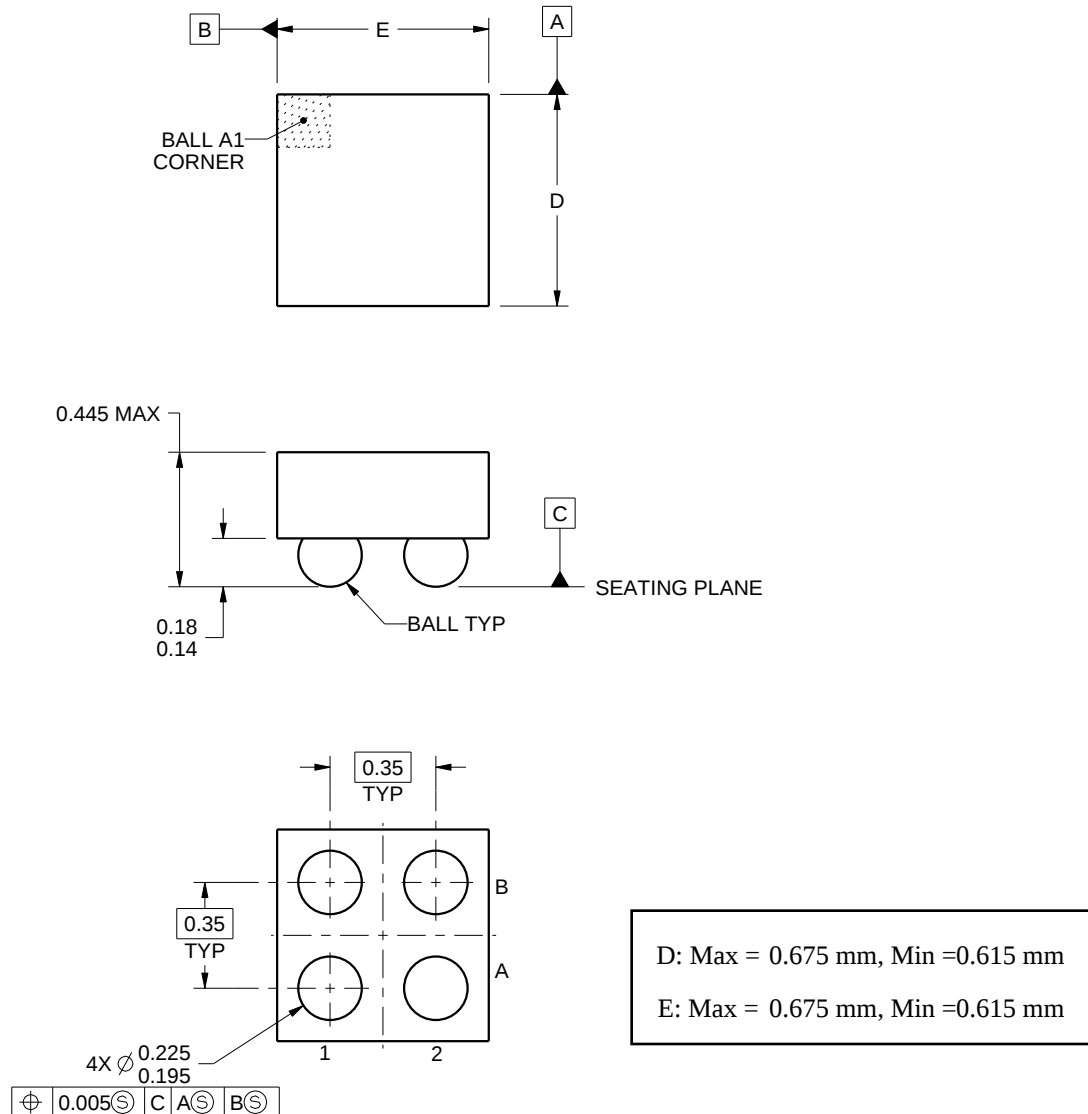


YKE0004

PACKAGE OUTLINE

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



4220102/A 11/2014

NOTES:

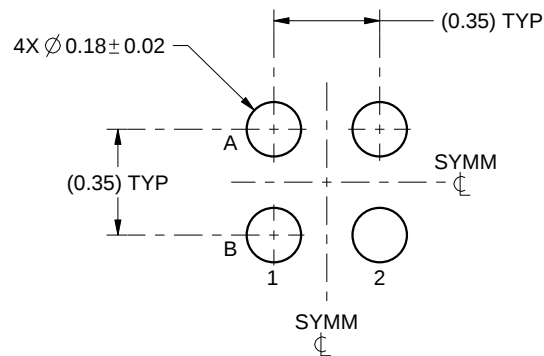
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

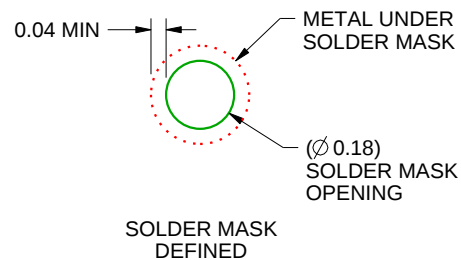
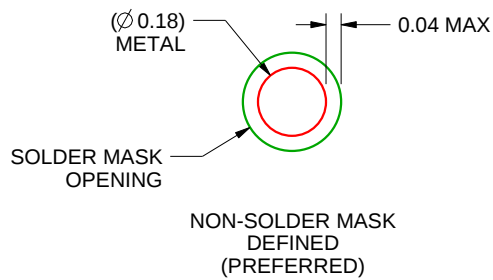
YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4220102/A 11/2014

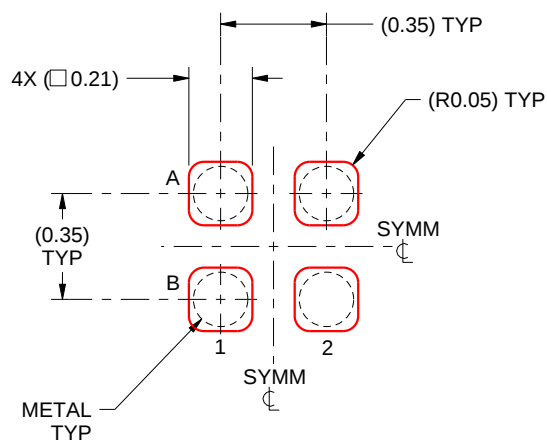
NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

YKE0004

DSBGA - 0.445mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL
SCALE:40X

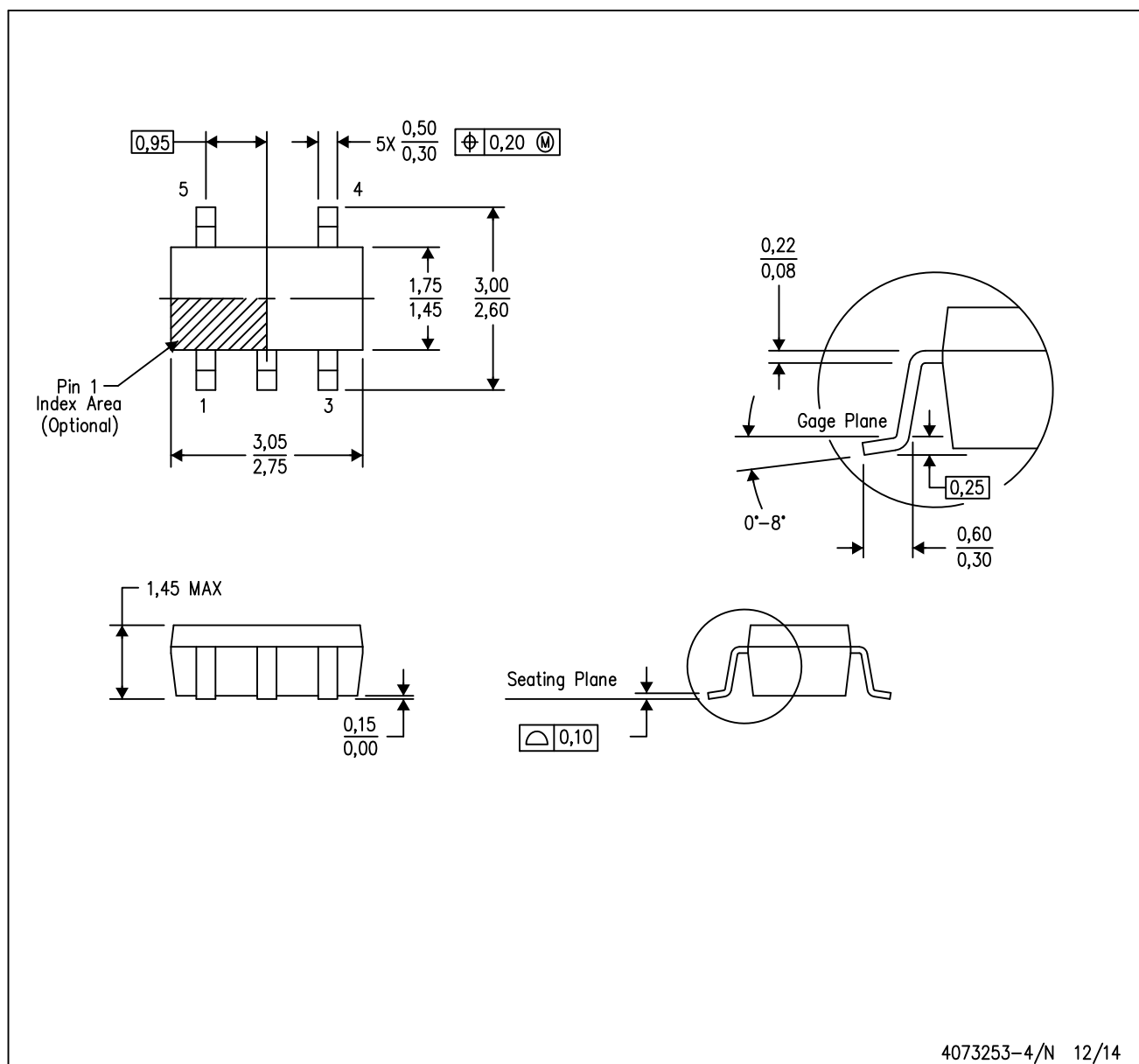
4220102/A 11/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DBV (R-PDSO-G5)

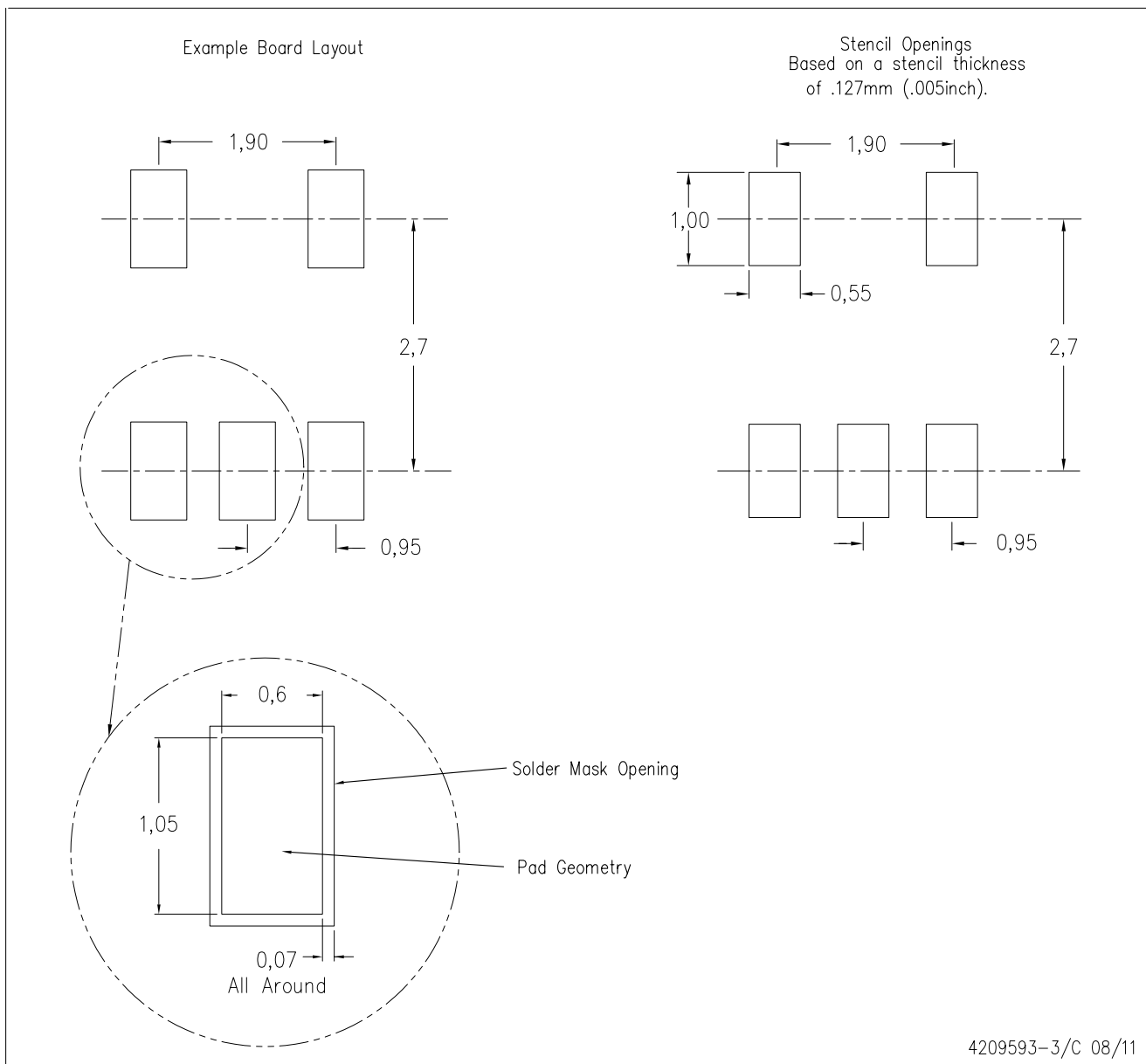
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和该等应用中所用 TI 产品的功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等许可包括但不限于任何专利权、版权、屏蔽作品权或在使用 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默示的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负任何责任，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的的应用。在应用内使用产品的行为本身不会配有安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2017 德州仪器半导体技术（上海）有限公司