Stepping Motor Driver series

High Voltage Series Stepping Motor Drivers

BD6422EFV (PARALLEL-IN type)
BD6425, BD6423EFV (CLK-IN type)

No.12009EAT06

●Description

These products are a low power consumption PWM constant current-drive driver of bipolar stepping motor with power supply's rated voltage of 45V and rated output current of 1.0A, 1.5A.

●Feature

1) Power supply: one system drive (rated voltage of 45V)
2) Rated output current: 1.0A, 1.5A
3) Low ON resistance DMOS output
4) CLK-IN drive mode (BD6425/6423EFV)
5) Parallel IN drive mode (BD6422EFV)
6) PWM constant current control (other oscillation)
7) Built-in spike noise blanking function (external noise filter is unnecessary)
8) FULL STEP & HALF STEP (two kinds), applicable to QUARTER STEP
9) Current decay mode switching function (4 kinds of FAST/SLOW DECAY ratio)
10) Normal rotation & reverse rotation switching function (BD6425/6423EFV)
11) Power save function
12) Built-in logic input pull-down resistor
13) Power-on reset function(BD6425/6423EFV)
14) Thermal shutdown circuit (TSD)
15) Over current protection circuit (OCP)
16) Under voltage lock out circuit (UVLO)
17) Malfunction prevention at the time of no applied power supply (Ghost Supply Prevention)
18) Electrostatic discharge: 8kV (HBM specification)
19) Microminiature, ultra-thin and high heat-radiation (exposed metal type) HTSSOP package

●Application

serial dot impact printer、sewing machine etc.

●Absolute maximum ratings(Ta=25℃)

Item	Symbol	BD6425EFV	BD6423/6422EFV	Unit
Supply voltage	$V_{CC1,2}$	-0.2～+45.0	-0.2～+45.0	V
Power dissipation	Pd	1.45※1	1.1※3	W
		4.70※2	4.0※4	W
Input voltage for control pin	V_{IN}	-0.2～+5.5	-0.2～+5.5	V
RNF maximum voltage	V_{RNF}	0.7	0.7	V
Maximum output current	I_{OUT}	1.5※5	1.0※5	A/phase
Operating temperature range	T_{opr}	-25～+85	-25～+85	℃
Storage temperature range	T_{stg}	-55～+150	-55～+150	℃
Junction temperature	T_{jmax}	+150	+150	℃

※1 70mm×70mm×1.6mm glass epoxy board. Derating in done at 11.6mW/℃ for operating above Ta=25℃.
※2 4-layer recommended board. Derating in done at 37.6mW/℃ for operating above Ta=25℃.
※3 70mm×70mm×1.6mm glass epoxy board. Derating in done at 8.8mW/℃ for operating above Ta=25℃.
※4 4-layer recommended board. Derating in done at 32.0mW/℃ for operating above Ta=25℃.
※5 Do not, however exceed Pd, ASO and Tjmax=150℃.

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●Operating conditions((Ta= -25～+85℃)

Item	Symbol	BD6425EFV	BD6423/6422EFV	Unit
Supply voltage	$V_{CC1,2}$	19~42		V
Maximum Output current (DC)	I_{OUT}	1.2※6	0.7※6	A/phase

※6 Do not however exceed Pd, ASO.

●Electrical characteristics (Unless otherwise specified Ta=25℃、$V_{CC1,2}$=37V)

Item	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Whole						
Circuit current at standby	I_{CCST}	-	1.0	2.5	mA	PS=L
Circuit current	I_{CC}	-	2.0	5.0	mA	PS=H, VREF=3V
Control input						
H level input voltage	V_{INH}	2.0	-	-	V	
L level input voltage	V_{INL}	-	-	0.8	V	
H level input current	I_{INH}	35	50	100	μA	V_{IN}=5V
L level input current	I_{INL}	-10	0	-	μA	V_{IN}=0V
Output (OUT1A, OUT1B, OUT2A, OUT2B)						
Output ON resistance(BD6425EFV)	R_{ON}	-	1.10	1.43	Ω	I_{OUT}=1.0A,Sum of upper and lower
Output ON resistance(BD6423/6422EFV)	R_{ON}	-	2.00	2.60	Ω	I_{OUT}=0.5A,Sum of upper and lower
Output leak current	I_{LEAK}	-	-	10	μA	
Current control						
RNFXS input current (BD6425EFV)	I_{RNFS}	-2.0	-0.1	-	μA	RNFXS=0V
RNFX input current	I_{RNF}	-40	-20	-	μA	RNFX=0V
VREF input current	I_{VREF}	-2.0	-0.1	-	μA	VREF=0V
VREF input voltage range	V_{REF}	0	-	3.0	V	
Minimum on time (Blank time)	t_{ONMIN}	0.5	1.5	3.0	μs	C=470pF, R=82kΩ
BD6425/6423EFV						
Comparator threshold	V_{CTH}	0.57	0.60	0.63	V	VREF=3V
BD6422EFV						
Comparator threshold 100%	V_{CTH100}	0.57	0.60	0.63	V	VREF=3V, (I0X,I1X)=(L,L)
Comparator threshold 67%	V_{CTH67}	0.38	0.40	0.42	V	VREF=3V, (I0X,I1X)=(H,L)
Comparator threshold 33%	V_{CTH33}	0.18	0.20	0.22	V	VREF=3V, (I0X,I1X)=(L,H)

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●Terminal function and Application circuit diagram

1) BD6425EFV

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	GND	Ground terminal	15	CLK	Clock input terminal for advancing the electrical angle.
2	OUT1B	H bridge output terminal	16	CW_CCW	Motor rotating direction setting terminal
3	RNF1	Connection terminal of resistor for output current detection	17	TEST	Terminal for testing (used by connecting with GND)
4	RNF1S	Input terminal of current limit comparator	18	MODE0	Motor excitation mode setting terminal
5	OUT1A	H bridge output terminal	19	MODE1	Motor excitation mode setting terminal
6	NC	Non connection	20	ENABLE	Power supply terminal
7	VCC1	Power supply terminal	21	NC	Non connection
8	NC	Non connection	22	VCC2	Power supply terminal
9	GND	Ground terminal	23	NC	Non connection
10	CR	Connection terminal of CR for setting chopping frequency	24	OUT2A	H bridge output terminal
11	DEC1	Current decay mode setting terminal	25	RNF2S	Input terminal of current limit comparator
12	DEC2	Current decay mode setting terminal	26	RNF2	Connection terminal of resistor for output current detection
13	VREF	Output current value setting terminal	27	OUT2B	H bridge output terminal
14	PS	Power save terminal	28	NC	Non connection

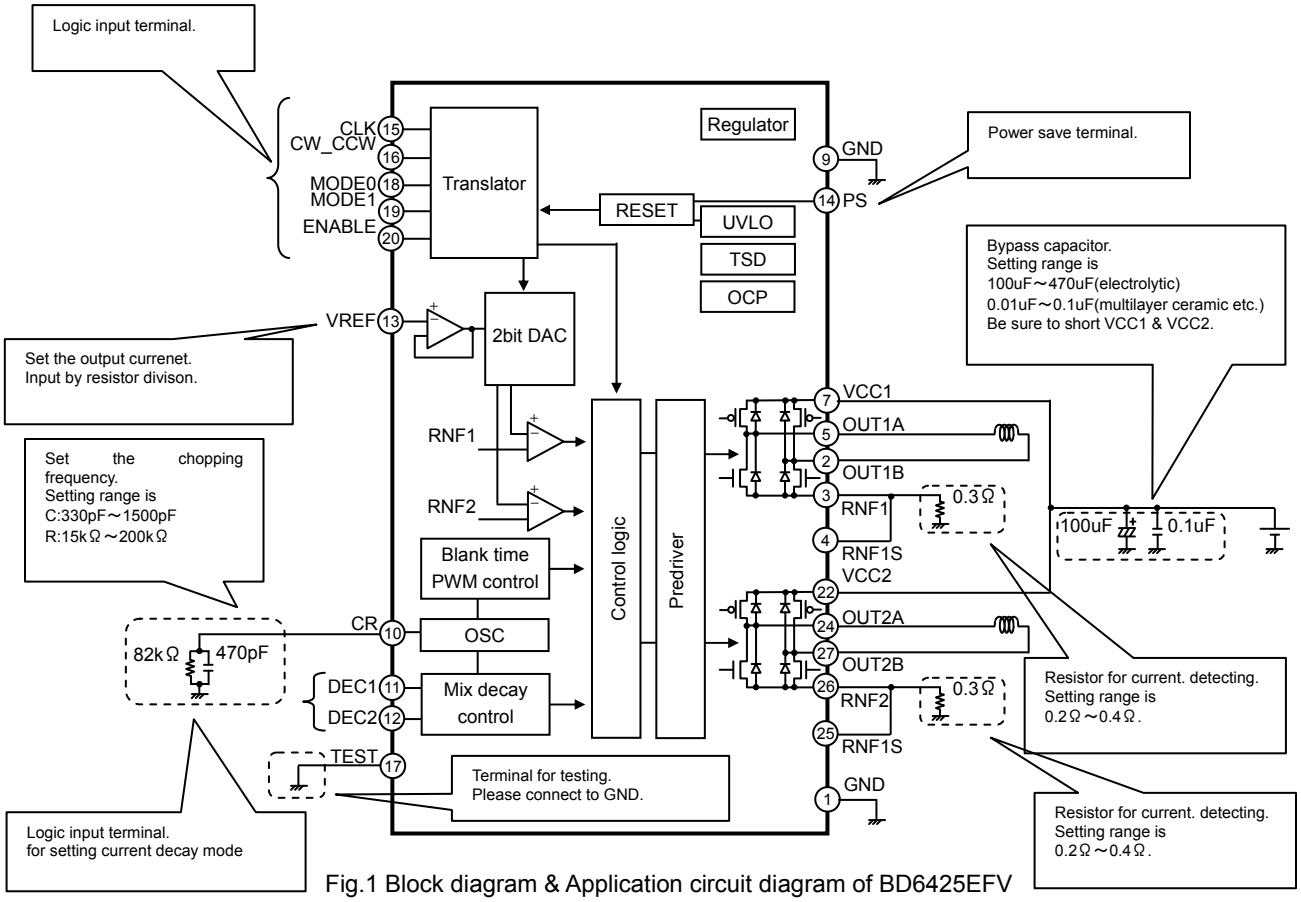

Fig.1 Block diagram & Application circuit diagram of BD6425EFV

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2) BD6423EFV

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	GND	Ground terminal	13	CLK	Clock input terminal for advancing the electrical angle.
2	OUT1B	H bridge output terminal	14	CW_CCW	Motor rotating direction setting terminal
3	RNF1	Connection terminal of resistor for output current detection	15	TEST	Terminal for testing (used by connecting with GND)
4	OUT1A	H bridge output terminal	16	MODE0	Motor excitation mode setting terminal
5	VCC1	Power supply terminal	17	MODE1	Motor excitation mode setting terminal
6	NC	Non connection	18	ENABLE	Output enable terminal
7	GND	Ground terminal	19	NC	Non connection
8	CR	Connection terminal of CR for setting PWM frequency	20	VCC2	Power supply terminal
9	DEC1	Current decay mode setting terminal	21	OUT2A	H bridge output terminal
10	DEC2	Current decay mode setting terminal	22	RNF2	Connection terminal of resistor for output current detection
11	VREF	Output current value setting terminal	23	OUT2B	H bridge output terminal
12	PS	Power save terminal	24	NC	Non connection

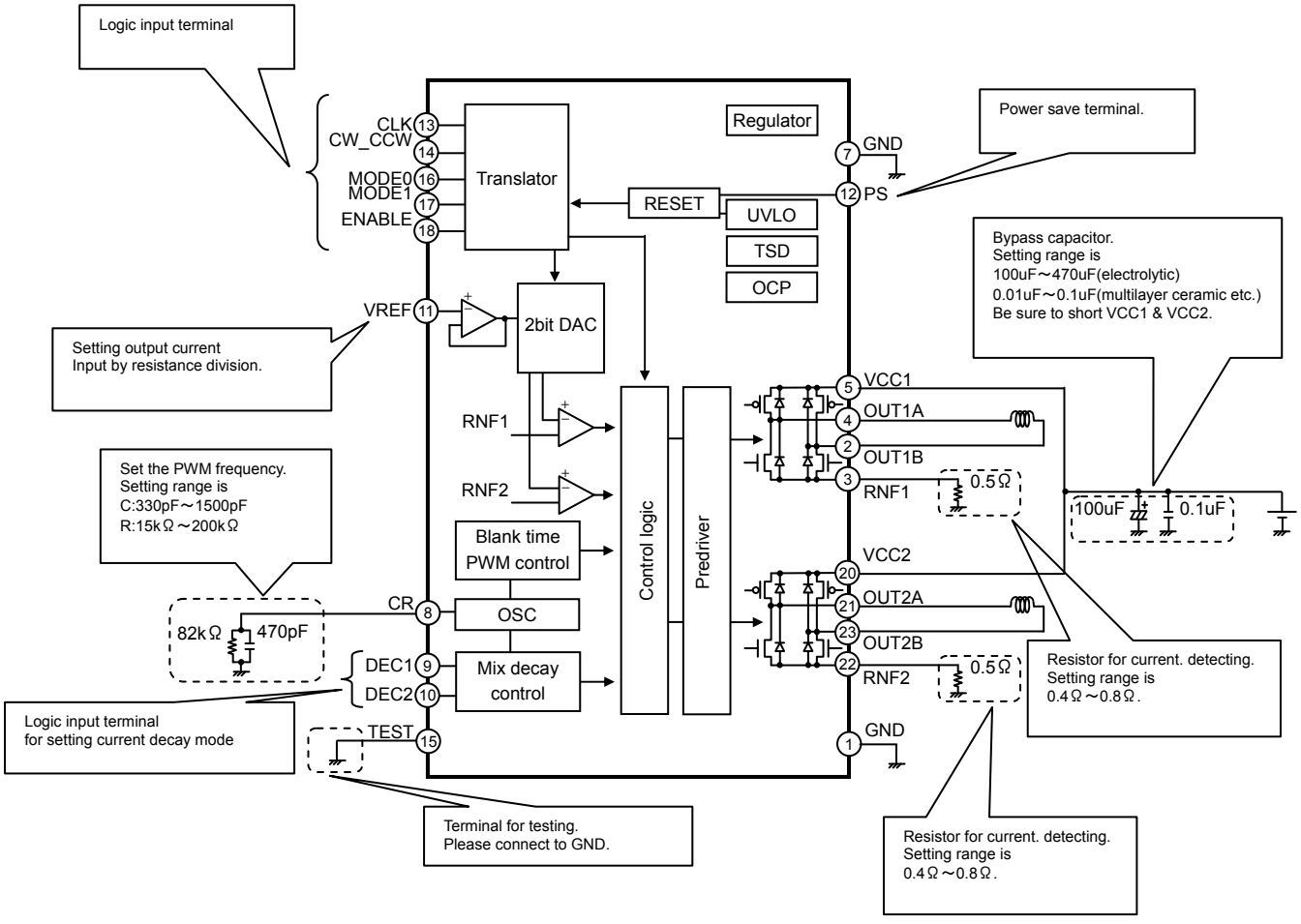

Fig.2 Block diagram & Application circuit diagram of BD6423EFV

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3) BD6422EFV

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	GND	Ground terminal	13	PHASE1	Phase selection terminal
2	OUT1B	H bridge output terminal	14	I01	VREF division ratio setting terminal
3	RNF1	Connection terminal of resistor for output current detection	15	I11	VREF division ratio setting terminal
4	OUT1A	H bridge output terminal	16	PHASE2	Phase selection terminal
5	VCC1	Power supply terminal	17	I02	VREF division ratio setting terminal
6	NC	Non connection	18	I12	VREF division ratio setting terminal
7	GND	Ground terminal	19	NC	Non connection
8	CR	Connection terminal of CR for setting PWM frequency	20	VCC2	Power supply terminal
9	DEC1	Current decay mode setting terminal	21	OUT2A	H bridge output terminal
10	DEC2	Current decay mode setting terminal	22	RNF2	Connection terminal of resistor for output current detection
11	VREF	Output current value setting terminal	23	OUT2B	H bridge output terminal
12	PS	Power save terminal	24	NC	Non connection

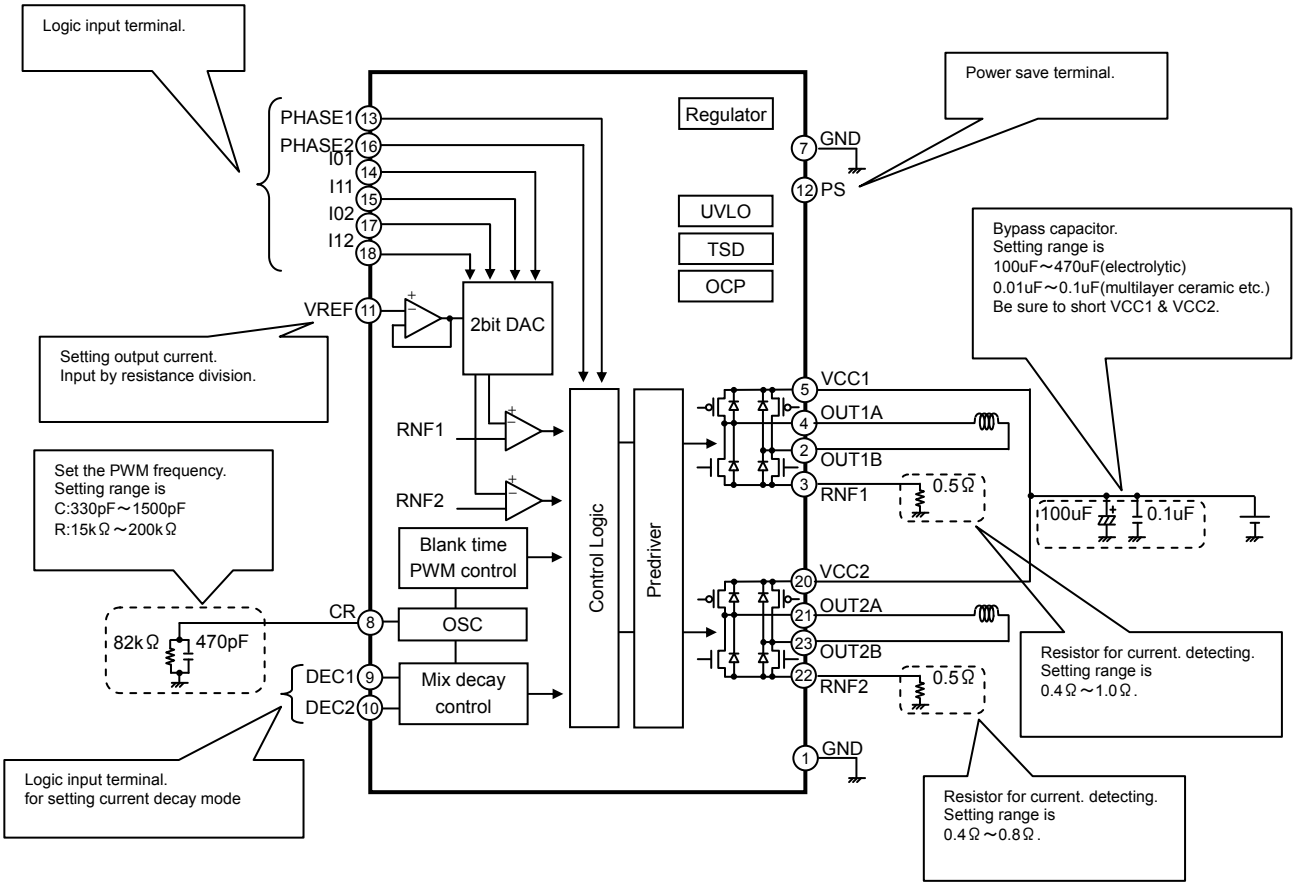

Fig.3 Block diagram & Application circuit diagram of BD6422EFV

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●Usage Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3) Power supply Lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4) GND Potential

The potential of GND pin must be minimum potential in all operating conditions.

(5) Metal on the backside (Define the side where product markings are printed as front)

The metal on the backside is shorted with the backside of IC chip therefore it should be connected to GND. Be aware that there is a possibility of malfunction or destruction if it is shorted with any potential other than GND.

(6) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. Users should be aware that these products have been designed to expose their frames at the back of the package, and should be used with suitable heat dissipation treatment in this area to improve dissipation. As large a dissipation pattern should be taken as possible, not only on the front of the baseboard but also on the back surface. It is important to consider actual usage conditions and to take as large a dissipation pattern as possible.

(7) Inter-pin shorts and mounting errors

When attaching to a printed circuit board, pay close attention to the direction of the IC and displacement. Improper attachment may lead to destruction of the IC. There is also possibility of destruction from short circuits which can be caused by foreign matter entering between outputs or an output and the power supply or GND.

(8) Operation in a strong electric field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(9) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

(10) Thermal shutdown circuit

The IC has a built-in thermal shutdown circuit (TSD circuit). If the chip temperature becomes Tjmax=150℃, and higher, coil output to the motor will be open. The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect or indemnify peripheral equipment. Do not use the TSD function to protect peripheral equipment.

TSD on temperature [℃] (Typ.)	Hysteresis Temperature [℃] (Typ.)
175	25

(11) Inspection of the application board

During inspection of the application board, if a capacitor is connected to a pin with low impedance there is a possibility that it could cause stress to the IC, therefore an electrical discharge should be performed after each process. Also, as a measure again electrostatic discharge, it should be earthed during the assembly process and special care should be taken during transport or storage. Furthermore, when connecting to the jig during the inspection process, the power supply should first be turned off and then removed before the inspection.

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(12) Input terminal of IC

This IC is a monolithic IC, and between each element there is a P+ isolation for element partition and a P substrate.
This P layer and each element's N layer make up the P-N junction, and various parasitic elements are made up.
For example, when the resistance and transistor are connected to the terminal as shown in figure 4,

○When GND＞(Terminal A) at the resistance and GND＞(Terminal B) at the transistor (NPN),
the P-N junction operates as a parasitic diode.

○Also, when GND＞(Terminal B) at the transistor (NPN)
The parasitic NPN transistor operates with the N layers of other elements close to the aforementioned parasitic diode.

Because of the IC's structure, the creation of parasitic elements is inevitable from the electrical potential relationship. The operation of parasitic elements causes interference in circuit operation, and can lead to malfunction and destruction. Therefore, be careful not to use it in a way which causes the parasitic elements to operate, such as by applying voltage that is lower than the GND (P substrate) to the input terminal.

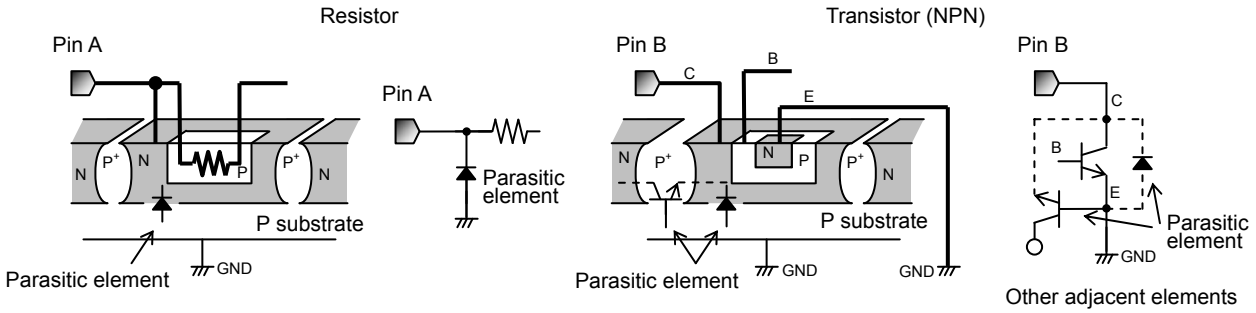

Fig. 4 Pattern Diagram of Parasitic Element

(13) Ground Wiring Patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern potential of any external components, either.

(14) TEST Terminal (BD6425/6423EFV)

Be sure to connect TEST pin to GND.

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●Ordering part number

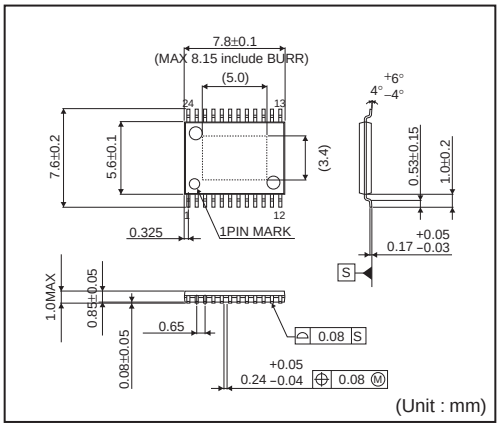
B D 6 4 2 2 E F V	-	E 2

形名

パッケージ
EFV=HTSSOP-B24(BD6423EFV /BD6422EFV)
EFV=HTSSOP-B28(BD6425EFV)

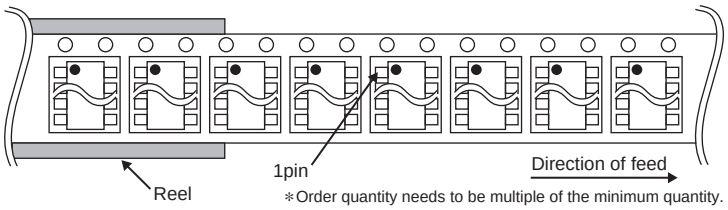
包装、フォーミング仕様
E2: リール状エンボステーピング

HTSSOP-B24



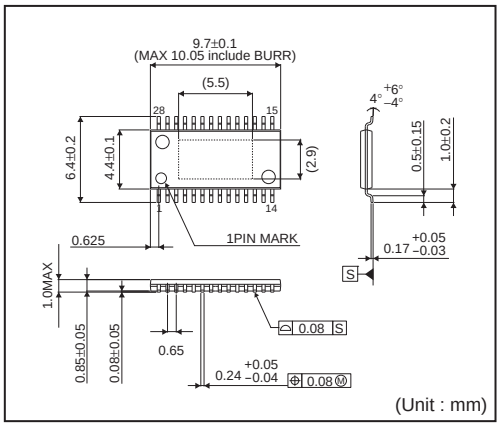
<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



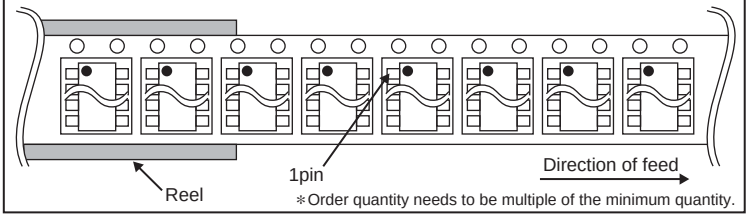
＊Order quantity needs to be multiple of the minimum quantity.

HTSSOP-B28



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



＊Order quantity needs to be multiple of the minimum quantity.

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