EVALUATION KIT AVAILABLE

MAX44006/MAX44008

RGB Color, Infrared, and Temperature Sensors

General Description

The MAX44006/MAX44008 integrate six sensors in two products: red, green, blue (RGB) sensors; an ambient light (clear) sensor; a temperature sensor; and an ambient infrared sensor with an I^2C interface. These highly integrated optical sensors include a temperature sensor to improve reliability and performance.

The devices compute the light information with six parallel data converters allowing simultaneous light measurement in a very short time. The devices consume only 15µA (MAX44006) and 16µA (MAX44008) separately in RGBC + TEMP + IR mode, and also have the ability to operate at 1.7V to 2.0V (MAX44006) and 2.7V to 5.5V supply voltage (MAX44008).

The devices' RGB sensing capability improves the performance of end products by providing robust and precise information for ambient color-sensing and color-temperature measurement.

The devices' superior infrared and 50Hz/60Hz rejection provide robust readings. The wide dynamic range light measurement makes these products perfect candidates for many color measurement applications.

The on-chip ambient sensor has the ability to make wide dynamic range (0.002~8388.61µW/cm^2) lux measurements. The devices' digital computation power provides programmability and flexibility for end-product design. A programmable interrupt pin minimizes the need to poll the devices for data, freeing up microcontroller resources, reducing system software overhead, and ultimately reducing power consumption. All these features are included in a tiny 2mm x 2mm x 0.6mm optical package.

Applications

TVs/Display Systems

Tablet PCs/Notebooks/e-Readers

Printers

LED and Laser Projectors

Digital Light Management

Industrial Sensors

Tablets

Color Correction

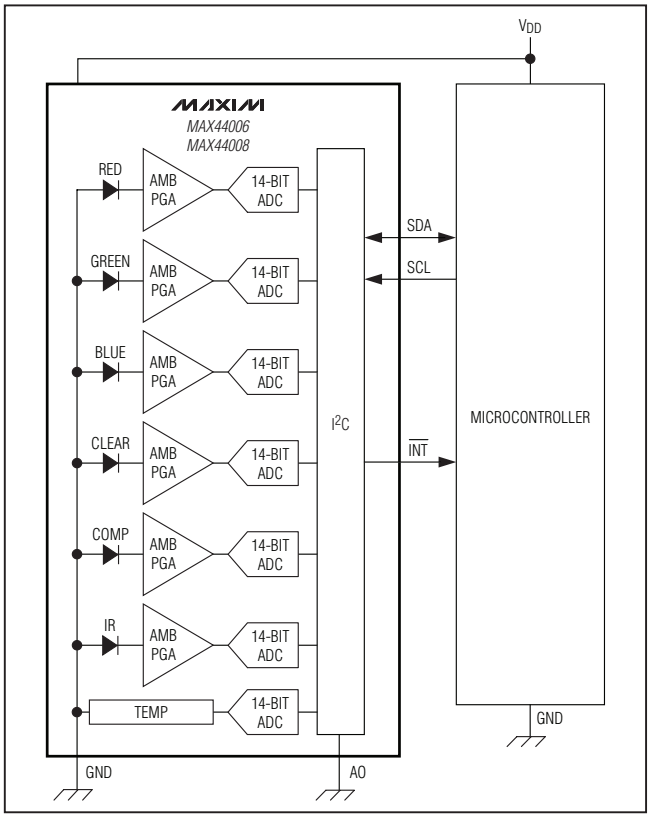
***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX44006.related**.

Features

- **Optical Sensor Fusion for True Color Sensing**
  - **Seven Parallel ADCs**
  - **R, G, B, IR, ALS Sensing**
- **Superior Sensitivity**
  - **0.001 Lux**
- **Optimized for Overall System Power Consumption**
  - **10µA (MAX44006)/10µA (MAX44008) in Ambient Mode**
  - **15µA (MAX44006)/16µA (MAX44008) in RGBC + IR Mode**
  - **0.01µA (MAX44006)/0.5µA (MAX44008) in Shutdown Mode**
- **Digital Functionalities**
  - **Programmable Channel Gains**
  - **Adjustable Interrupt Thresholds**
- **High-Level Integration**
  - **Six Sensors in a 2mm x 2mm x 0.6mm Package**

Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6298; Rev 1; 8/12

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND (MAX44006) .....-0.3V to +2.2V
V_{DD} to GND (MAX44008) .....-0.3V to +6.0V
A0, $\overline{INT}$, SCL, SDA to GND .....-0.3V to +6.0V
Output Short-Circuit Current Duration.....Continuous
Continuous Input Current into Any Terminal..... ±20mA

Continuous Power Dissipation
(derate 11.9mW/°C above +70°C).....953mW
Operating Temperature Range..... -40°C to +85°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

OTDFN (Note 1)
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....+83.9°C/W
Junction-to-Case Thermal Resistance (θ_{JC})..... +37°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.8V (MAX44006), V_{DD} = 3.3V (MAX44008), T_A = +25°C, min/max are from -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COLOR-SENSOR CHARACTERISTICS						
Maximum Sensitivity (Note 3)		Clear = 538nm		0.002		µW/cm^2
		Red = 630nm		0.002		
		Green = 538nm		0.002		
		Blue = 470nm		0.004		
		Infrared = 850nm		0.002		
Maximum Sense Capability		Clear = 538nm		8388		µW/cm^2
		Red = 630nm		8388		
		Green = 538nm		8388		
		Blue = 470nm		16,777		
		Infrared = 850nm		8388		
Total Error	TE	Power = 10µW/cm^2, red = 630nm, green = 538nm, blue = 470nm, T_A = +25°C, clear = 538nm, IR = 850nm		2	15	%
Gain Matching		Red to green to blue, T_A = +25°C		0.5	10	%
Power-Up Time	t_{ON}			10		ms
Dark-Level Counts		6.25ms conversion time, 0 lux, T_A = +25°C			2	Counts
ADC Conversion Time		14-bit resolution (Note 4)		400		ms
		14-bit resolution, T_A = +25°C		100		
		12-bit resolution		25		
		10-bit resolution		6.25		
		8-bit resolution		1.5625		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.8V (MAX44006), V_{DD} = 3.3V (MAX44008), T_A = +25°C, min/max are from -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Conversion Accuracy		T_A = +25°C		1	10	%
		T_A = -40°C to +85°C (Note 5)		2	15	
TEMPERATURE SENSOR						
Accuracy (Note 5)		T_A = +25°C~+55°C		±1	±3	°C
		T_A = 0°C~+70°C		±2	±5	
Resolution				0.25		°C/LSB
POWER SUPPLY						
Power-Supply Voltage	V_{DD}	MAX44006, guaranteed by total error	1.7		2	V
		MAX44008, guaranteed by total error	2.7		5.5	
Quiescent Current	I_{DD}	MAX44006, CLEAR mode		10	18	µA
		MAX44006, RGBC + IR mode		15	30	
		MAX44008, CLEAR mode		10	18	
		MAX44008, RGBC + IR mode		16	30	
Software Shutdown Current	$I_{\overline{SHDN}}$	MAX44006, T_A = +25°C			1	µA
		MAX44008, T_A = +25°C			1.5	
DIGITAL CHARACTERISTICS—SDA, $\overline{INT}$, A0						
Output Low Voltage SDA	V_{OL}	I_{SINK} = 6mA			0.4	V
I^2C Input Voltage High	V_{IH}	SDA, SCL, A0	1.4			V
I^2C Input Voltage Low	V_{IL}	SDA, SCL, A0			0.4	V
Input Hysteresis	V_{HYS}			200		mV
Input Capacitance	C_{IN}			10		pF
Input Leakage Current	I_{IN}	V_{IN} = 0V, T_A = +25°C			0.1	µA
		V_{IN} = 5.5V, T_A = +25°C			0.1	
I^2C TIMING CHARACTERISTICS (Note 6)						
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START	$t_{SU.STA}$		0.6			µs
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		0.9	µs
Data Setup Time	$t_{SU,DAT}$		100			ns
Bus Capacitance	C_B				400	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.8V (MAX44006), V_{DD} = 3.3V (MAX44008), T_A = +25°C, min/max are from -40°C to +85°C, unless otherwise noted.) (Note 2)

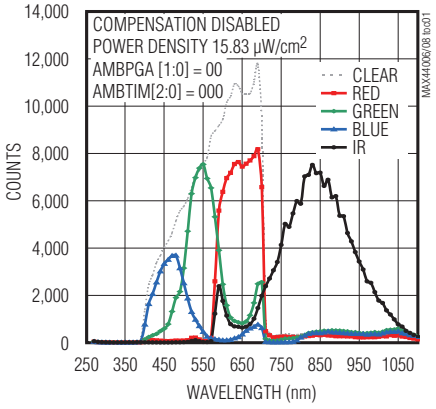
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA and SCL Receiving Rise Time	t_R		20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F		20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_f		20 + 0.1C_B		250	ns
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Note 2: 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by bench or ATE characterization.
Note 3: In AMBTIM[2:0] mode (100ms integration time).
Note 4: At 14-bit resolution mode. Sensitivity is 4 times higher with 400ms integration time than 100ms integration time.
Note 5: Production tested only at +25°C, guaranteed by bench characterization across temperature.
Note 6: Design guidance only, not production tested.

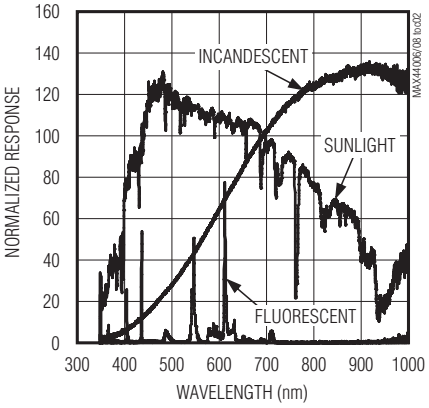
Typical Operating Characteristics

(V_{DD} = 1.8V (MAX44006), V_{DD} = 3.3V (MAX44008), T_A = +25°C, min/max are from -40°C to +85°C, unless otherwise noted.)

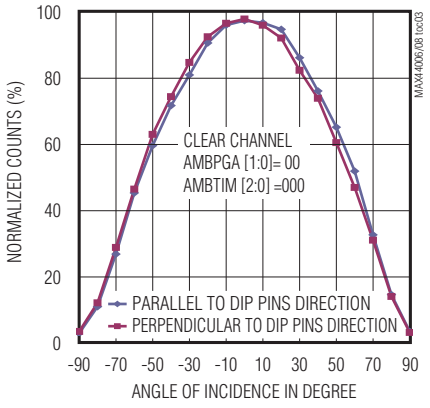
WAVELENGTH vs. COUNTS



SPECTRUM OF LIGHT SOURCES FOR MEASUREMENT



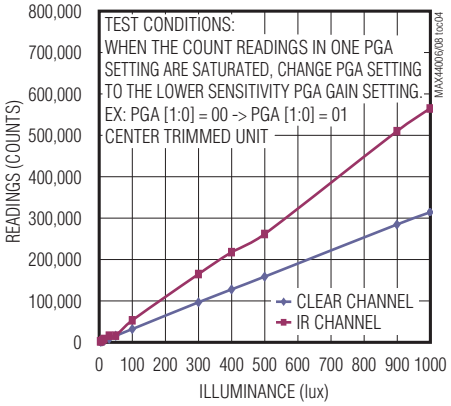
RADIATION PATTERN



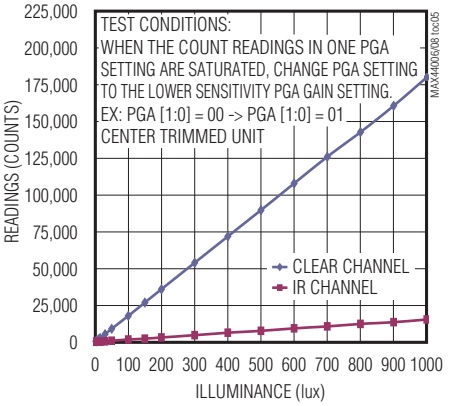
Typical Operating Characteristics (continued)

(V_{DD} = 1.8V (MAX44006), V_{DD} = 3.3V (MAX44008), T_A = +25°C, min/max are from -40°C to +85°C, unless otherwise noted.)

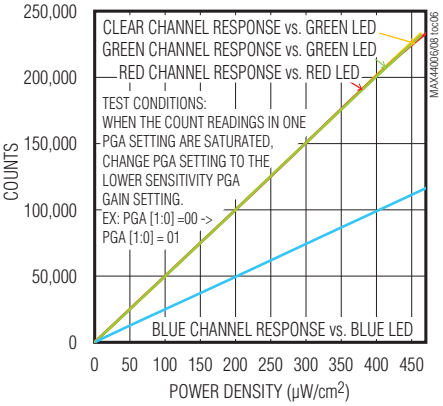
RESPONSE OF CLEAR AND IR CHANNELS WITH INCANDESCENT LIGHT



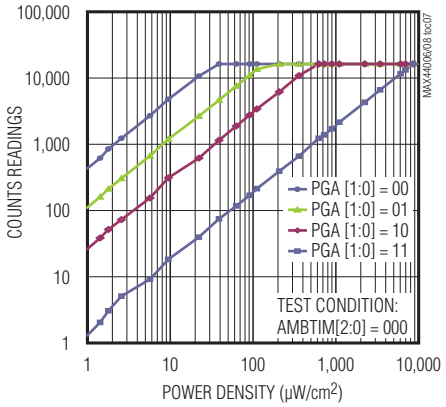
RESPONSE OF CLEAR AND IR CHANNELS WITH FLUROSCENT LIGHT



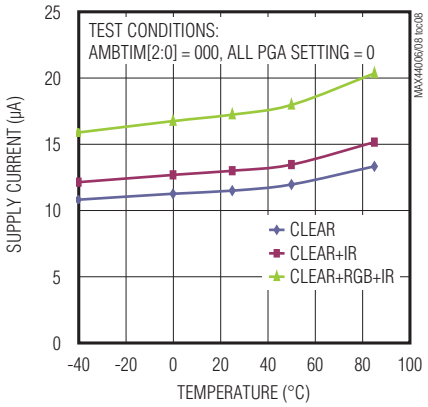
LINIARITY RESPONSE vs. RGB LED



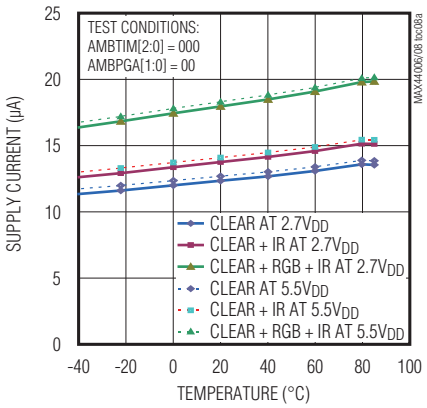
CLEAR CHANNEL RESPONSE TO WHITE LED



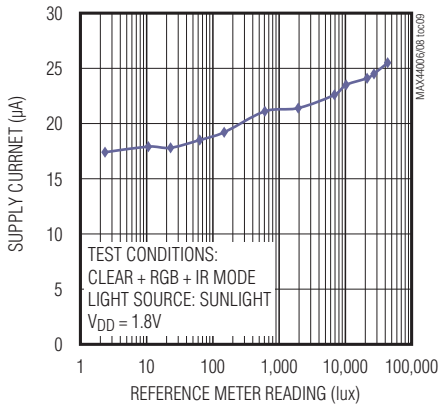
SUPPLY CURRENT vs. TEMPERATURE (MAX44006)



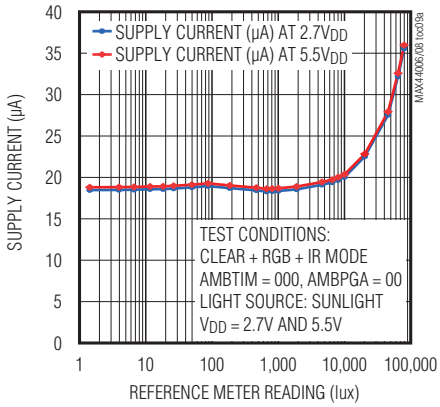
SUPPLY CURRENT vs. TEMPERATURE (MAX44008)



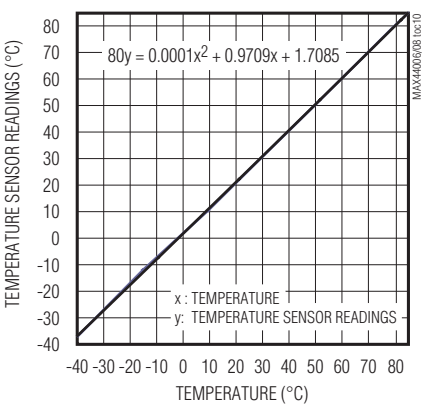
SUPPLY CURRENT vs. LUX (MAX44006)



SUPPLY CURRENT vs. LUX (MAX44008)



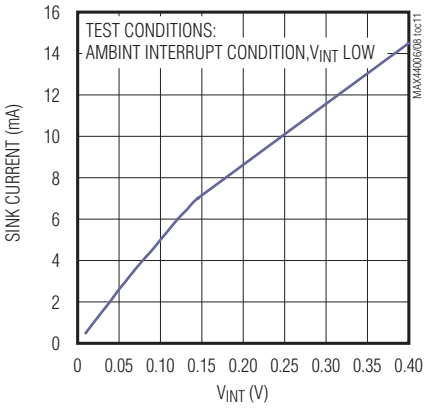
TEMPERATURE SENSOR READINGS vs. TEMPERATURE



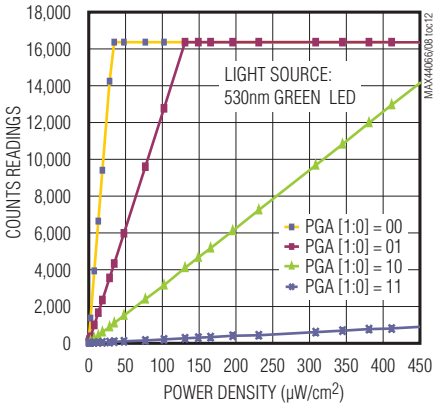
Typical Operating Characteristics (continued)

(V_{CC} = 1.8V (MAX44006), V_{CC} = 3.3V (MAX44008), T_A = +25°C, min/max are from -40°C to +85°C, unless otherwise noted.)

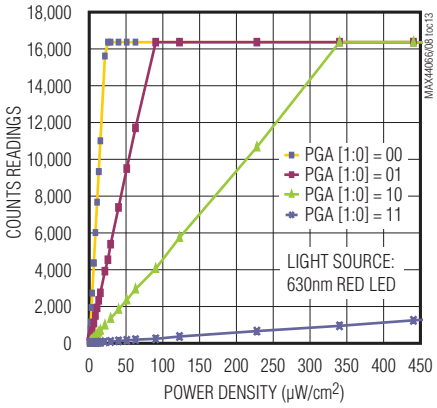
SINK CURRENT vs. V_{INT} LOW



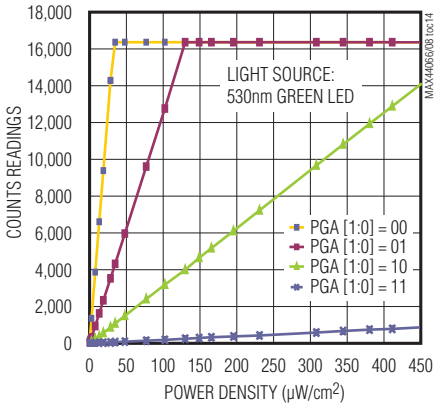
CLEAR CHANNEL LINIARITY RESPONSE



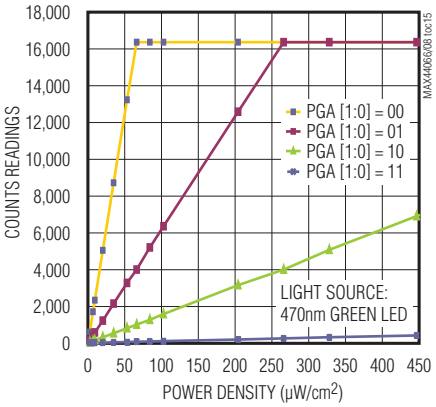
RED CHANNEL LINIARITY RESPONSE



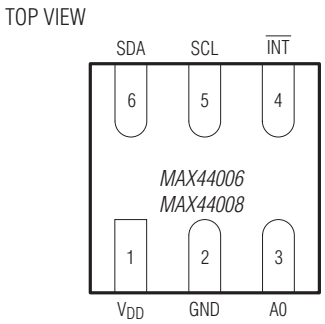
GREEN CHANNEL LINIARITY RESPONSE



BLUE CHANNEL LINIARITY RESPONSE



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power Supply
2	GND	Ground
3	A0	Address Select. Pull high to select address 1000 100x (MAX44006), 1000 000x (MAX44008) or low to select address 1000 101x (MAX44006), 1000 001x (MAX44008).
4	$\overline{INT}$	Interrupt
5	SCL	I^2C Clock
6	SDA	I^2C Data

Detailed Description

The MAX44006/MAX44008 combine a wide-dynamic range color sensor capable of measuring red, green, and blue (RGB) and infrared content of ambient light. The devices also have a digital I^2C interface, advanced TEMP sensor, and interrupt pin functionality to make interfacing with it easy. The die is placed inside an optically transparent (OTDFN) package.

A photodiode array inside the devices converts the light to a current, which is then processed by low-power circuitry and a sigma-delta ADC into a digital bit stream. The data is then stored in an output register that can be read by an I^2C master.

The user can choose whether to read just the clear channel, or clear + IR channel, or clear + RGB + IR channels. Due to parallel conversion by on-chip ADCs, there is no additional delay in making ambient light conversions for multiple channels.

Key features of the devices include high-level integration, low-power design, small packaging, and interrupt pin operation. An on-chip programmable interrupt function eliminates the need to continually poll the devices for data, resulting in a significant power saving.

Ambient Light Sensing

Ambient light sensors are designed to detect brightness the same way human eyes do. To achieve this, the light sensor needs to have a spectral sensitivity that is identical to the photopic curve of the human eye. See Figure 1.

The devices' color sensors are designed to accurately derive the color chromaticity and intensity of ambient light. With parallel ADC conversion circuits, conversion data from multiple channels can be read at the same time. An interrupt signal can also be dynamically configured with higher and lower thresholds, and a persist timer. The interrupt is latched until the master reads the Interrupt Status register. This allows the master to stay in power-efficient sleep mode until a change in lighting condition alerts it.

Variation between light sources can extend beyond the visible spectral range—fluorescent, incandescent, and sunlight, for example, have substantially different IR radiation content. The devices incorporate on-chip measurement of RGBC and IR of compensation of ambient light, allowing accurate lux detection in a variety of lighting conditions, as well as identification of type of light source.

On-chip user-programmable clear, RGB, infrared channel gain registers allow the light sensor response to also be tailored for specific applications, such as when the light sensor is placed under a colored or black glass.

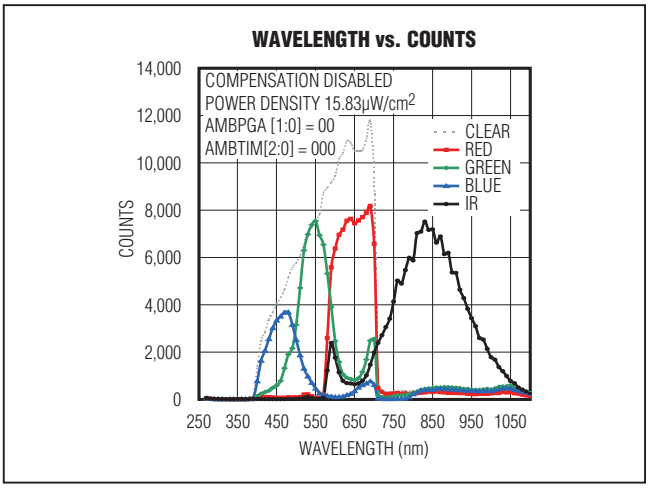


Figure 1. Wavelength vs. Counts

Temperature Sensor

The devices also integrate a temperature sensor that can be used for ambient temperature measurement and compensation. A nonlinear response is designed to replicate the effect of temperature on the photodiodes used on the chip.

Register Description

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	REGISTER ADDRESS	POWER-ON RESET STATE	R/W
STATUS											
Interrupt Status				RESET	SHDN	PWRON		AMBINTS	0x00	0X04	R/W
CONFIGURATION											
Main Configuration			MODE[1:0]		AMBSEL[1:0]			AMBINTE	0x01	0x00	R/W
Ambient Configuration	TRIM	COMPEN	TEMPEN	AMBTIM[2:0]			AMBPGA[1:0]		0x02	0x20	R/W

Register Description (continued)

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	REGISTER ADDRESS	POWER-ON RESET STATE	R/W
AMBIENT READING											
Ambient CLEAR High Byte			AMB_CLEAR[13:8]						0x04	0x00	R
Ambient CLEAR Low Byte	AMB_CLEAR[7:0]								0x05	0x00	R
Ambient RED High Byte			AMB_RED[13:8]						0x06	0x00	R
Ambient RED Low Byte	AMB_RED[7:0]								0x07	0x00	R
Ambient GREEN High Byte			AMB_GREEN[13:8]						0x08	0x00	R
Ambient GREEN Low Byte	AMB_GREEN[7:0]								0x09	0x00	R
Ambient BLUE High Byte			AMB_BLUE[13:8]						0x0A	0x00	R
Ambient BLUE Low Byte	AMB_BLUE[7:0]								0x0B	0x00	R
Ambient INFRARED High Byte			AMB_IR[13:8]						0x0C	0x00	R
Ambient INFRARED Low Byte	AMB_IR[7:0]								0x0D	0x00	R
Ambient IR COMP High Byte			AMB_IRCOMP[13:8]						0x0E	0x00	R
Ambient IR COMP Low Byte	AMB_IRCOMP[7:0]								0x0F	0x00	R
TEMP High Byte			TEMP[13:8]						0x12	0x00	R

Register Description (continued)

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	REGISTER ADDRESS	POWER-ON RESET STATE	R/W
TEMP Low Byte	TEMP[7:0]								0x13	0x00	R
INTERRUPT THRESHOLDS											
AMB Upper Threshold—High Byte			UPTHR[13:8]						0x14	0xFF	R/W
AMB Upper Threshold—Low Byte	UPTHR[7:0]								0x15	0xFF	R/W
AMB Lower Threshold—High Byte			LOTHR[13:8]						0x16	0x00	R/W
AMB Lower Threshold—Low Byte	LOTHR[7:0]								0x17	0x00	R/W
Threshold Persist Timer							AMBPST[1:0]		0x18	0x00	R/W
AMBIENT ADC GAINS											
Digital Gain Trim of CLEAR Channel	TRIM_GAIN_CLEAR[6:0]								0x1D	0xXX	R/W
Digital Gain Trim of RED Channel	TRIM_GAIN_RED[6:0]								0x1E	0xXX	R/W
Digital Gain Trim of GREEN Channel	TRIM_GAIN_GREEN[6:0]								0x1F	0xXX	R/W
Digital Gain Trim of BLUE Channel	TRIM_GAIN_BLUE[6:0]								0x20	0xXX	R/W
Digital Gain Trim of INFRARED Channel	TRIM_GAIN_IR[6:0]								0x21	0xXX	R/W

The individual register bits are explained below.

Interrupt Status (0x00)

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	REGISTER ADDRESS	POWER-ON RESET STATE	R/W
Interrupt Status				RESET	SHDN	PWRON		AMBINTS	0x00	0x04	R/W

The AMBINTS bit in the Interrupt Status register 0x00 is a read-only bit, and indicates that an ambient light-interrupt condition has occurred. If any of these bits (PWRON, AMBINTS) are set to 1, the $\overline{INT}$ pin is pulled low. The PWRON bit in the Interrupt Status register 0x00 is a read-only bit, and if set, indicates that a power-on-reset (POR) condition has occurred, and any user-programmed thresholds may not be valid anymore. The SHDN bit in the Interrupt Status register 0x00 is a read/write bit, and can be used to put the part into and bring out of shutdown for power saving. All register data is retained during this operation. The RESET bit in the Interrupt Status register 0x00 is also a read/write bit, and can be used to reset all the registers back to a power-on default condition.

Reading the Interrupt Status register clears the PWRON and AMBINTS bits if set, and deasserts the $\overline{INT}$ pin ($\overline{INT}$ pin is pulled high by the off-chip pullup resistor). The AMBINTS bits are disabled and set to 0 if the respective INTE Interrupt Enable bits in Register 0x01 are set to 0.

Table 1. Ambient INTERRUPT STATUS Flag (AMBINTS)

BIT0	OPERATION
0	No interrupt trigger event has occurred.
1	The ambient light has exceeded the designated window limits defined by the threshold registers for longer than persist timer count AMBPST[1:0]. It also causes the $\overline{INT}$ pin to be pulled low. Once set, the only way to clear this bit is to read this register. This bit is always set to 0 if AMBINTE bit is set to 0.

Table 2. Power-On INTERRUPT STATUS Flag (PWRON)

BIT2	OPERATION
0	Normal operating mode.
1	The part went through a power-up event, either because the part was turned on, or because there was a power-supply voltage glitch. All interrupt threshold settings in the registers have been reset to power-on default states, and should be examined if necessary. The $\overline{INT}$ pin is also pulled low. Once this bit is set, the only way to clear this bit is to read this register.

Table 3. Shutdown Control (SHDN)

BIT3	OPERATION
0	The part is in normal operation. When the part returns from shutdown, note that the value in data registers is not current until the first conversion cycle is completed.
1	The part can be put into a power-save mode by writing a 1 to this bit. Supply current is reduced to approximately 0.01µA (MAX44006) and 0.5µA (MAX44008) with no I^2C clock activity. While all registers remain accessible and retain data, ADC conversion data contained in them may not be current. Writeable registers also remain accessible in shutdown. All interrupts are cleared.

Table 4. Reset Control (RESET)

BIT4	OPERATION
0	The part is in normal operation.
1	The part undergoes a forced POR sequence. All configuration, threshold, and data registers are reset to a power-on state by writing a 1 to this bit, and an internal hardware reset pulse is generated. This bit then automatically becomes 0 after the RESET sequence is completed. After resetting, the PWRON interrupt is triggered.

Main Configuration (0x01)

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	REGISTER ADDRESS	POWER-ON RESET STATE	R/W
Main Configuration			MODE[1:0]		AMBSEL[1:0]			AMBINTE	0x01	0x20	R/W

Writing to the Main Configuration register does not abort any ambient data conversion (registers 0x04 to 0x0F) if already in progress. It applies the new settings during the next conversion period.

Table 5. Ambient Interrupt Enable (AMBINTE)

BIT0	OPERATION
0	The AMBINTS bit and $\overline{INT}$ pin remain unasserted even if an ambient interrupt event has occurred. The AMBINTS bit is set to 0 if previously set to 1. See Table 1 for more details.
1	Detection of ambient interrupt events is enabled (see the AMBINTS bit for more details). An ambient interrupt can trigger a hardware interrupt ($\overline{INT}$ pin pulled low) and set the AMBINTS bit (register 0x00, BIT0).

Note: Detection of an ambient interrupt event sets the AMBINTS bit (register 0x00, BIT0) only if AMBINTE bit is set to 1. If AMBINTS bits are set to 1, it pulls the interrupt $\overline{INT}$ pin low (asserts it). A read of the Interrupt Status register clears AMBINTS bits if set to 1, and deasserts the $\overline{INT}$ pin if pulled low.

The 2 AMBSEL[1:0] bits define four operating modes for the devices. Ensure that the respective ambient channels also enable use of the MODE[1:0] bits.

Table 6. Ambient Interrupt Select (AMBSEL[1:0])

AMBSEL[1:0]	OPERATION
00	CLEAR channel data is used to compare with ambient interrupt thresholds and ambient timer settings.
01	GREEN channel data is used to compare with ambient interrupt thresholds and ambient timer settings.
10	IR channel data is used to compare with ambient interrupt thresholds and ambient timer settings.
11	TEMP channel data is used to compare with ambient interrupt thresholds and ambient timer settings.

The 2 MODE[1:0] bits define three operating modes for the devices, as shown in Table 7.

Table 7. MODE[1:0]

MODE[1:0]	OPERATING MODE	COMMENTS
00	Clear	CLEAR + TEMP* channels active
01	Clear + IR	CLEAR + TEMP* + IR channels active
10	Clear + RGB + IR	CLEAR + TEMP* + RGB + IR channels active

**When TEMPEN set to 1.*

Ambient Configuration Register (0x02)

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	REGISTER ADDRESS	POWER-ON RESET STATE	R/W
Ambient Configuration	TRIM	COMPEN	TEMPEN	AMBTIM[2:0]			AMBPGA[1:0]		0x02	0x00	R/W

Writing to the Ambient Configuration register aborts any ambient data conversion (registers 0x04 to 0x0F) if already in progress, applies the new settings immediately, and initiates a new conversion.

The 2 AMBPGA[1:0] bits set the gain of the clear/red/green/blue/IR channel measurements according to Table 8.

Table 8. AMBPGA[1:0]

In AMBTIM[2:0] = 000 Mode (100ms integration time)

AMBPGA[1:0]	CLEAR		RED		GREEN	
	nW/cm² per LSB*	FULL SCALE (µW/cm²)	nW/cm² per LSB*	FULL SCALE (µW/cm²)	nW/cm² per LSB*	FULL SCALE (µW/cm²)
00	2	32.768	2	32.768	2	32.768
01	8	131.072	8	131.072	8	131.072
10	32	524.288	32	524.288	32	524.288
11	512	8388.61	512	8388.61	512	8388.61

AMBPGA[1:0]	BLUE		IR	
	nW/cm² per LSB*	FULL SCALE (µW/cm²)	nW/cm² per LSB*	FULL SCALE (µW/cm²)
00	4	65.536	2	32.768
01	16	262.144	8	131.072
10	64	1048.573	32	524.288
11	1024	16777.2	512	8388.61

In AMBTIM[2:0] = 100 Mode (400ms integration time)

AMBPGA[1:0]	CLEAR		RED		GREEN	
	nW/cm² per LSB*	FULL SCALE (µW/cm²)	nW/cm² per LSB*	FULL SCALE (µW/cm²)	nW/cm² per LSB*	FULL SCALE (µW/cm²)
00	0.5	8.192	0.5	8.192	0.5	8.192
01	2	32.768	2	32.768	2	32.768
10	8	131.072	8	131.072	8	131.072
11	128	2097.153	128	2097.153	128	2097.153

AMBPGA[1:0]	BLUE		IR	
	nW/cm² per LSB*	FULL SCALE (µW/cm²)	nW/cm² per LSB*	FULL SCALE (µW/cm²)
00	1	16.384	0.5	8.192
01	4	65.536	2	32.768
10	16	262.1433	8	131.072
11	256	4194.3	128	2097.153

The 3 AMBTIM[2:0] bits set the integration time for the red/green/blue/IR/temp channel ADC conversion, as shown in Table 9.

Table 9. AMBTIM[2:0]

AMBTIM[2:0]	INTEGRATION TIME (ms)	FULL-SCALE ADC (COUNTS)	BIT RESOLUTION	RELATIVE LSB SIZE FOR FIXED AMBPGA[1:0]
000	100	16,384	14	1x
001	25	4,096	12	4x
010	6.25	1,024	10	16x
011	1.5625	256	8	64x
100	400	16,384	14	1/4x
101	Reserved	Not applicable	Not applicable	Not applicable
110	Reserved	Not applicable	Not applicable	Not applicable
111	Reserved	Not applicable	Not applicable	Not applicable

TEMPEN

Table 10. TEMPEN

BIT6	OPERATION
0	Disables temperature sensor.
1	Enables temperature sensor.

The integration time of temperature sensor is controlled by the ambient mode settings. The temperature sensor is enabled only if the clear channel is on.

COMPEN

Table 11. COMPEN

BIT5	OPERATION
0	Disables IR compensation.
1	Enables IR compensation. Only for MODE[1:0] = 00 Mode.

The integration time of compensation channel is controlled by the AMB mode settings. The compensation is enabled only when the clear channel is on. When COMPEN = 1, the CLEAR data is automatically compensated for stray IR leakeds and temperature variations. When COMPEN = 0, the IR compensation is disabled, but the output of the IR compensation data exits.

Table 12. TRIM Adjust Enable (TRIM)

BIT7	OPERATION
0	Use factory-programmed gains for all the channels. Ignore any bytes written to TRIM_GAIN_GREEN[6:0], TRIM_GAIN_RED[6:0], TRIM_GAIN_BLUE[6:0], TRIM_GAIN_CLEAR[6:0], and TRIM_GAIN_IR[6:0] registers.
1	Use bytes written to TRIM_GAIN_GREEN[6:0], TRIM_GAIN_RED[6:0], TRIM_GAIN_BLUE[6:0], TRIM_GAIN_CLEAR[6:0], and TRIM_GAIN_IR[6:0] registers to set the gain for each channel.

AMBIENT Data Register (0x04–0x0F)

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	REGISTER ADDRESS	POWER-ON RESET STATE	R/W
AMBIENT READING											
Ambient CLEAR High Byte			AMB_CLEAR[13:8]						0x04	0x00	R
Ambient CLEAR Low Byte	AMB_CLEAR[7:0]								0x05	0x00	R
Ambient RED High Byte			AMB_RED[13:8]						0x06	0x00	R
Ambient RED Low Byte	AMB_RED[7:0]								0x07	0x00	R
Ambient GREEN High Byte			AMB_GREEN[13:8]						0x08	0x00	R
Ambient GREEN Low Byte	AMB_GREEN[7:0]								0x09	0x00	R
Ambient BLUE High Byte			AMB_BLUE[13:8]						0x0A	0x00	R
Ambient BLUE Low Byte	AMB_BLUE[7:0]								0x0B	0x00	R
Ambient INFRARED High Byte			AMB_IR[13:8]						0x0C	0x00	R
Ambient INFRARED Low Byte	AMB_IR[7:0]								0x0D	0x00	R
Ambient IR COMP High Byte			AMB_IRCOMP[13:8]						0x0E	0x00	R
Ambient IR COMP Low Byte	AMB_IRCOMP[7:0]								0x0F	0x00	R

AMB_CLEAR[13:0], AMB_RED[13:0], AMB_GREEN[13:0],AMB_BLUE[13:0], AMB_IR[13:0], and AMB_IRCOMP[13:0] hold the 14-bit ADC data of the clear/red/green/blue/IR/COMP channels. AMB_IRCOMP[13:0] can be used to enhance overtemperature performance of the devices. The resolution and bit length of the result is controlled by the value of the AMBTIM[2:0] and AMBPGA[1:0] bits. The result is always right justified in the registers, and the unused high bits are set to zero.

Temperature Data Register (0x12–0x13)

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	REGISTER ADDRESS	POWER-ON RESET STATE	R/W
TEMP High Byte			TEMP[13.8]						0x12	0X00	R
TEMP Low Byte	TEMP[7.0]								0x13	0X00	R

Ambient Interrupt Threshold Registers (0x14–0x17)

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	REGISTER ADDRESS	POWER-ON RESET STATE	R/W
AMB Upper Threshold—High Byte			UPTHR[13:8]						0x14	0xFF	R/W
AMB Upper Threshold—Low Byte	UPTHR[7:0]								0x15	0xFF	R/W
AMB Lower Threshold—High Byte			LOTHR[13:8]						0x16	0x00	R/W
AMB Lower Threshold—Low Byte	LOTHR[7:0]								0x17	0x00	R/W

The ambient upper threshold and lower threshold (UPTHR[13:0] and LOTHR[13:0]) set the window limits that are used to trigger an ambient interrupt, AMBINTS. It is important to set these values according to the selected bit resolution/integration time chosen for the ambient measurement based on the AMBTIM[2:0] and AMBPGA[1:0] settings. The upper 2 bits are always ignored. If the AMBINTE bit is set, and the selected ambient channel data is outside the upper or lower thresholds for a period greater than that defined by the AMBPST persist time, the AMBINTS bit in the Status register is set and the $\overline{INT}$ pin is pulled low.

Ambient Threshold Persist Timer Register (0x18)

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	REGISTER ADDRESS	POWER-ON RESET STATE	R/W
Threshold Persist Timer							AMBPST[1:0]		0x18	0x00	R/W

AMBPST[1:0] sets one of four persist values in Table 13 that control a time delay before the interrupt logic reacts to a detected event. This feature is added in order to reduce false or nuisance interrupts.

Table 13. AMBPST[1:0]

AMBPST[1:0]	NO. OF CONSECUTIVE MEASUREMENTS REQUIRED TO TRIGGER AN INTERRUPT
00	1
01	4
10	8
11	16

When AMBPST[1:0] is set to 00, and the AMBINTE bit is set to 1, the first time an AMB interrupt event is detected, the AMBINTS interrupt bit is set and the $\overline{INT}$ pin goes low. If AMBPST[1:0] is set to 01, then four consecutive interrupt events must be detected on four consecutive measurement cycles. Similarly, if AMBPST[1:0] is set to 10 or 11, then 8 or 16 consecutive interrupt events must be detected. If there is an intervening measurement cycle where no interrupt event is detected, then the count is reset to zero.

Gain Trim Registers (0x1D–0x21)

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	REGISTER ADDRESS	POWER-ON RESET STATE	R/W
Digital Gain Trim of CLEAR Channel		TRIM_GAIN_CLEAR[6:0]							0x1D	0xXX	R/W
Digital Gain Trim of RED Channel		TRIM_GAIN_RED[6:0]							0x1E	0xXX	R/W
Digital Gain Trim of GREEN Channel		TRIM_GAIN_GREEN[6:0]							0x1F	0xXX	R/W
Digital Gain Trim of BLUE Channel		TRIM_GAIN_BLUE[6:0]							0x20	0xXX	R/W
Digital Gain Trim of INFRARED Channel		TRIM_GAIN_IR[6:0]							0x21	0xXX	R/W

TRIM_GAIN_CLEAR is used to trim the gain of the clear channel. TRIM_GAIN_RED is used to trim the gain of the red channel, TRIM_GAIN_GREEN is used to trim the gain of the green channel, TRIM_GAIN_BLUE is used to trim the gain of the blue channel, and TRIM_GAIN_IR is used to trim the gain of the IR channel.

These registers are loaded with the factory-trimmed gains on power-up. When the TRIM bit in register 0x02 is set to 1, these registers can be overwritten with user-chosen gains. When the TRIM bit is set back to 0, these registers are automatically reloaded with factory-trimmed values.

Applications Information

Ambient Sensing Applications

Typical applications involve placing the devices behind a glass with a small semitransparent window above it. Use the photodiode sensitive area as shown in Figure 2 to properly position the window above the part.

It is possible to map the RGB color values to an XY coordinate system for ambient color temperature measurement. This information can be used to enhance quality of image display by allowing the instrument to compensate for the human eye's chromatic adaptation—a form of improved autowhite balance. It can also be used to improve the color gamut of RGB LED backlit displays by allowing precise white point adjustment of LED sources.

The part comes equipped with internal gain trim registers for the CLEAR, RGB, and IR AMB photodiodes. By suitably choosing the gains for these channels accurate ambient-light readings can be generated in all lighting conditions irrespective of type of glass the part is used under. This is especially useful for color glass applications where, for cosmetic reasons, the part is placed behind a color film to hide its presence and to blend with the product cosmetic look. This film has the peculiar property of attenuating most ambient light but passing through infrared radiation.

Interrupt Operation

Ambient interrupt is enabled by setting bit 0 of register 0x01 to 1. See Table 5. The interrupt pin, $\overline{INT}$, is an open-drain output and pulls low when an interrupt con-

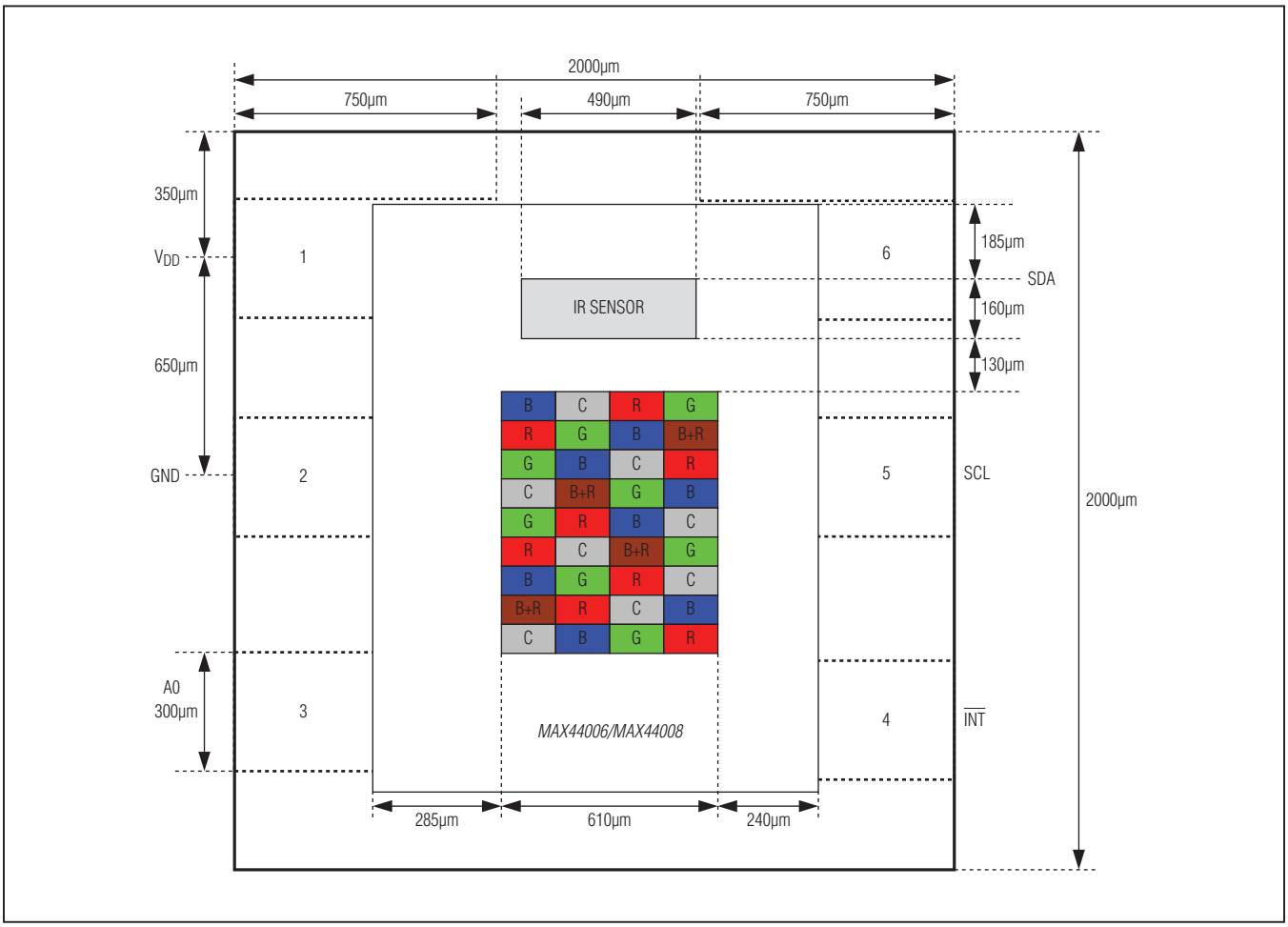


Figure 2. Photodiode Location

dition occurs (e.g., when ambient lux readings exceed threshold limits for a period greater than that set by the Persist Timer register). The interrupt status bit is cleared automatically if register 0x00 is read or if the interrupts are disabled.

A PWRON interrupt bit is set to alert the master of a chip-reset operation in case of a power-supply glitch, as can happen in instruments during vibration or power fluctuations.

It is recommended to utilize the $\overline{INT}$ pin on the devices to alert the master to read measurements from the devices. This eliminates the need for the microcontroller (I^2C master) to continually poll the devices for information. Due to the use of pullup resistors on the I^2C bus, minimizing I^2C bus activity can reduce power consumption substantially. In addition, this frees up the microcontroller resources to service other background processes to improve the devices' performance. The wide variety of smarts available on the chip, such as the ability to set the threshold levels and to count persist timer limits, allow the part to operate in an autonomous mode most of the time.

Typical Operating Sequence

The typical operating sequence for the master to communicate to the devices is shown below:

1) Setup:
   a) Read the Interrupt Status register (0x00) to confirm only the PWRON bit is set (usually at power-up only). This also clears the hardware interrupt.
   b) Set Threshold and Persist Timer registers for ambient measurements.
   c) Write 0x00 to Ambient Configuration register (register 0x02) to set the AMB sensor in the most sensitive gain setting, and the AMB ADCs in 14-bit modes of operation.
   d) Write 0x21 to the Main Configuration register (register 0x01) to set the part in CLEAR + TEMP + RGB + IR mode and to enable AMB interrupt.
   e) (Optional: Set new CLEAR, RGB, and infrared channel gains if necessary and set TRIM bit in register 0x02 to 1).
2) Wait for interrupt.
3) On interrupt:
   a) Read the Interrupt Status register (0x00) to confirm the IC to be the source of interrupt. This should clear the hardware interrupt on the part, if set.
   b) If an AMB interrupt has occurred, read AMB registers (register 0x04–0x0D) and take appropriate action (e.g., sets new backlight strength/change display gamma). Set new AMB thresholds, if necessary.
   c) Return to Step 2.

I²C Serial Interface

The devices feature an I^2C /SMBus™-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the devices and the master at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the devices by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each word transmitted to the devices is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the IC transmits the proper slave address followed by a series of nine SCL

Table 14. Slave Address

A0	SLAVE ADDRESS FOR WRITING	SLAVE ADDRESS FOR READING
MAX44006		
GND	1000 1010	1000 1011
V_{DD}	1000 1000	1000 1001
MAX44008		
GND	1000 0010	1000 0011
V_{DD}	1000 0000	1000 0001

pulses. The devices transmit data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or Repeated START condition, a not acknowledge (NACK), and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on the SDA bus. SCL operates as only an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the devices from high-voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signal.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. See the *START and STOP Conditions* section. SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 4). A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission, and frees the bus by issuing a STOP condition. The bus remains active if a Repeated START condition is generated instead of a STOP condition.

Early STOP Conditions

The devices recognize a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

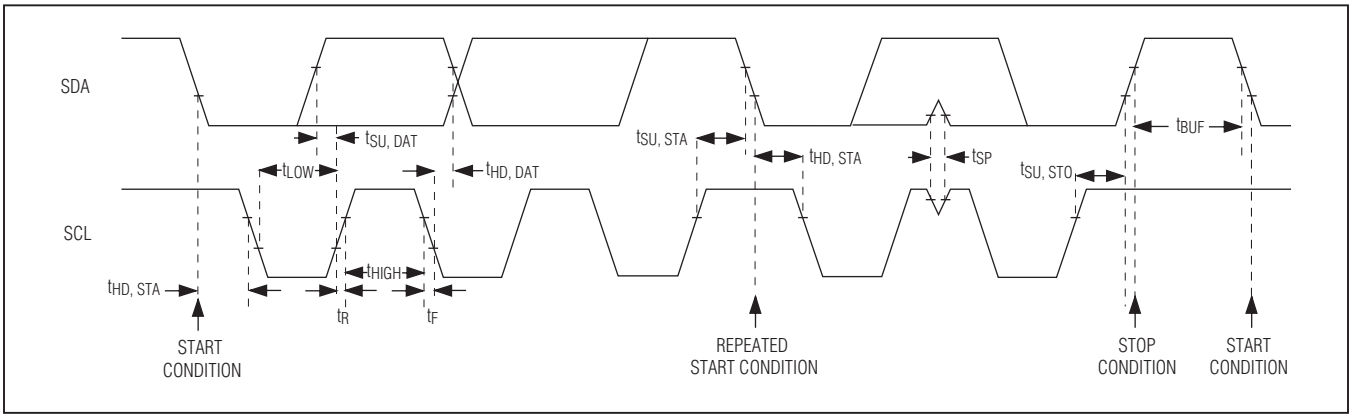


Figure 3. 2-Wire Interface Timing Diagram

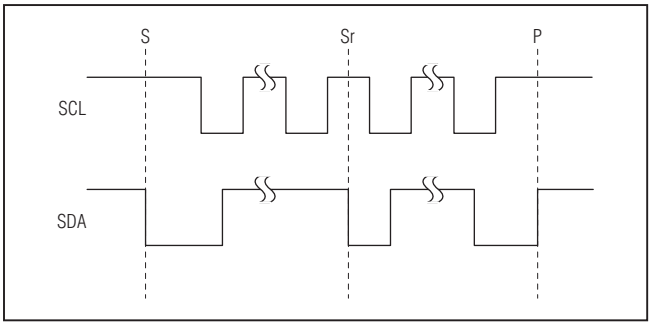


Figure 4. START, STOP, and Repeated START Conditions

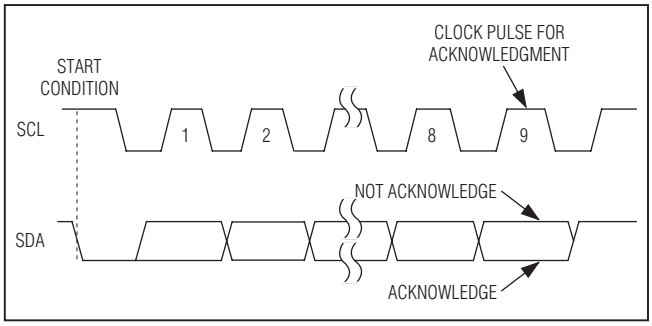


Figure 5. Acknowledge

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the devices use to handshake receipt of each byte of data when in write mode (Figure 5). The devices pull down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can retry communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the devices are in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge (NACK) is sent when the master reads the final byte of data from the device, followed by a STOP condition.

Write Data Format

A write to the devices includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, 1 byte of data to configure the internal register address pointer, 1 or more bytes of data, and a STOP condition. Figure 6 illustrates the proper frame format for writing 1 byte of data to the devices. Figure 7 illustrates the frame format for writing n-bytes of data to the devices.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the devices. The devices acknowledge receipt of the address byte during the master-generated ninth SCL pulse.

The second byte transmitted from the master configures the devices' internal register address pointer. The pointer tells the devices where to write the next byte of data. An acknowledge pulse is sent by the devices upon receipt of the address pointer data.

The third byte sent to the devices contains the data that is written to the chosen register. An acknowledge pulse from the devices signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. Figure 8 illustrates how to write to multiple registers with one frame. The master signals the end of transmission by issuing a STOP condition.

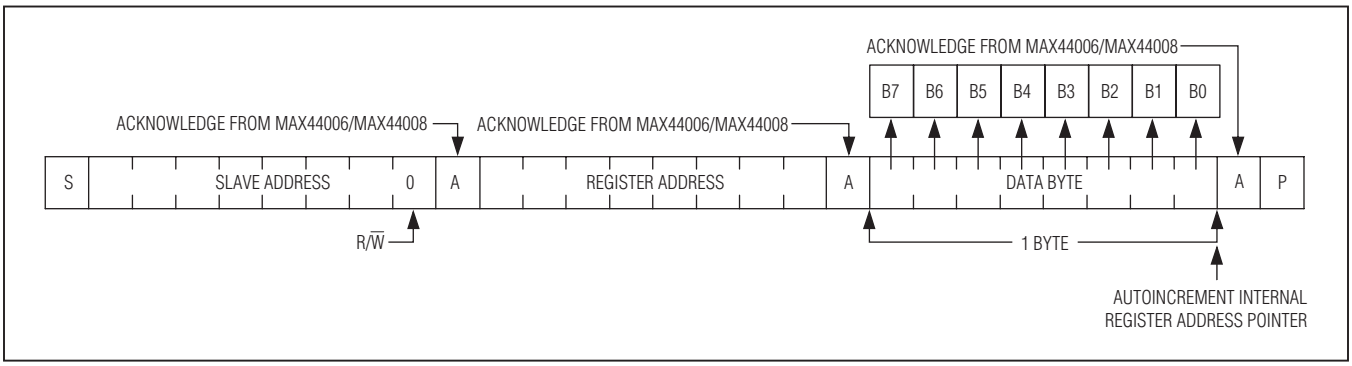


Figure 6. Writing 1 Byte of Data to the MAX44006/MAX44008

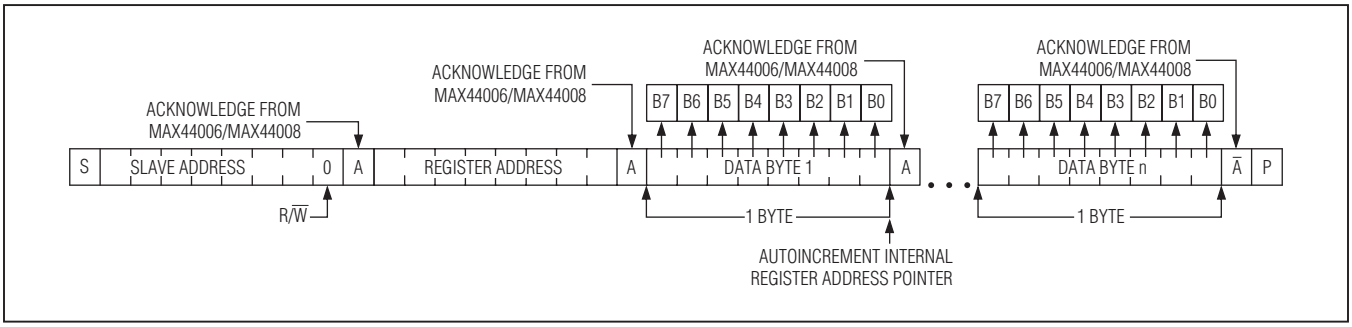


Figure 7. Writing n-Bytes of Data to the MAX44006/MAX44008

Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The devices acknowledge receipt of the slave address by pulling SDA low during the ninth SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00. The first byte transmitted from the devices comprises the contents of register 0x00. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued, followed by another read operation, the first data byte to be read is from register 0x00 and subsequent reads autoincrement the address pointer until the next STOP condition. The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the devices' slave address with the R/$\overline{W}$ bit set to 0, followed by the register address. A Repeated START condition is then sent, followed by the slave address with the R/$\overline{W}$ bit set to 1. The devices transmit the contents of the specified register. The address pointer autoincrements after transmitting the first byte. Attempting to read from register addresses higher than 0xFF results in repeated reads of 0xFF. Note that 0xF6 to 0xFF are reserved registers. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a NACK from the master and then a STOP condition. Figure 8 illustrates the frame format for reading 1 byte from the devices. Figure 9 illustrates the frame format for reading multiple bytes from the devices. Figure 10 illustrates the frame format for reading two registers consecutively without a STOP condition in between reads.

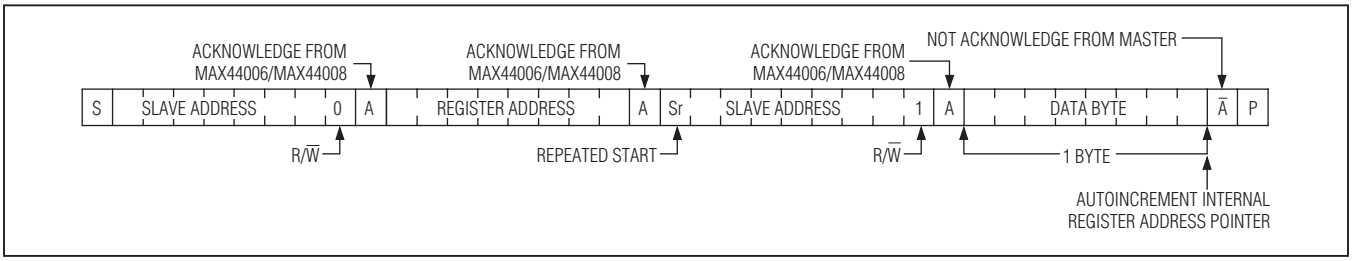


Figure 8. Reading 1 Indexed Byte of Data from the MAX44006/MAX44008

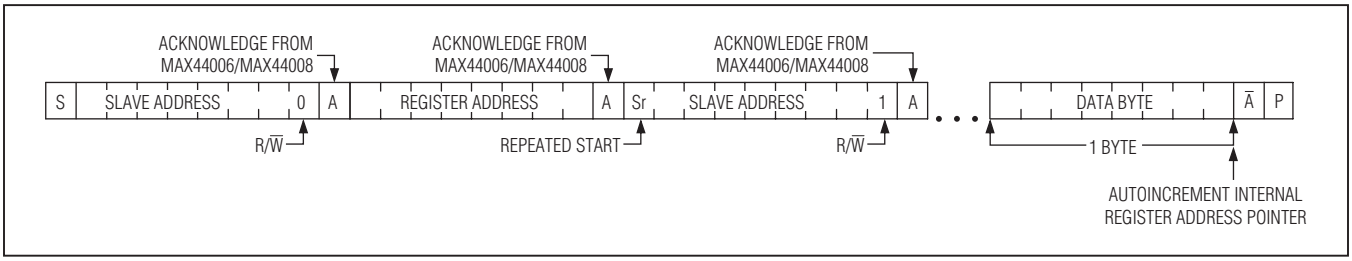


Figure 9. Reading n-Bytes of Indexed Data from the MAX44006/MAX44008

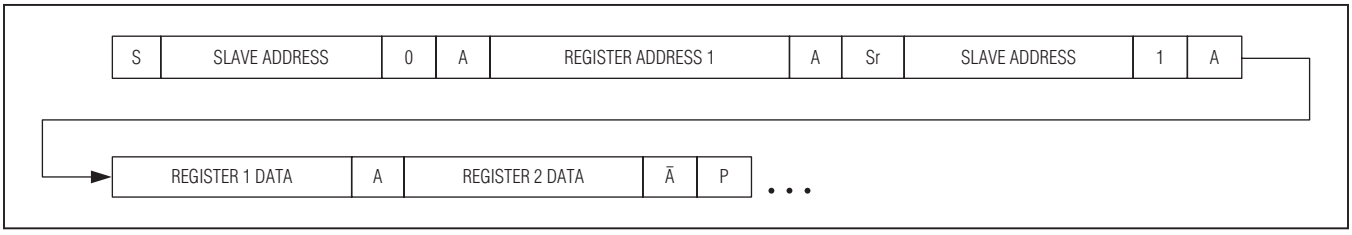
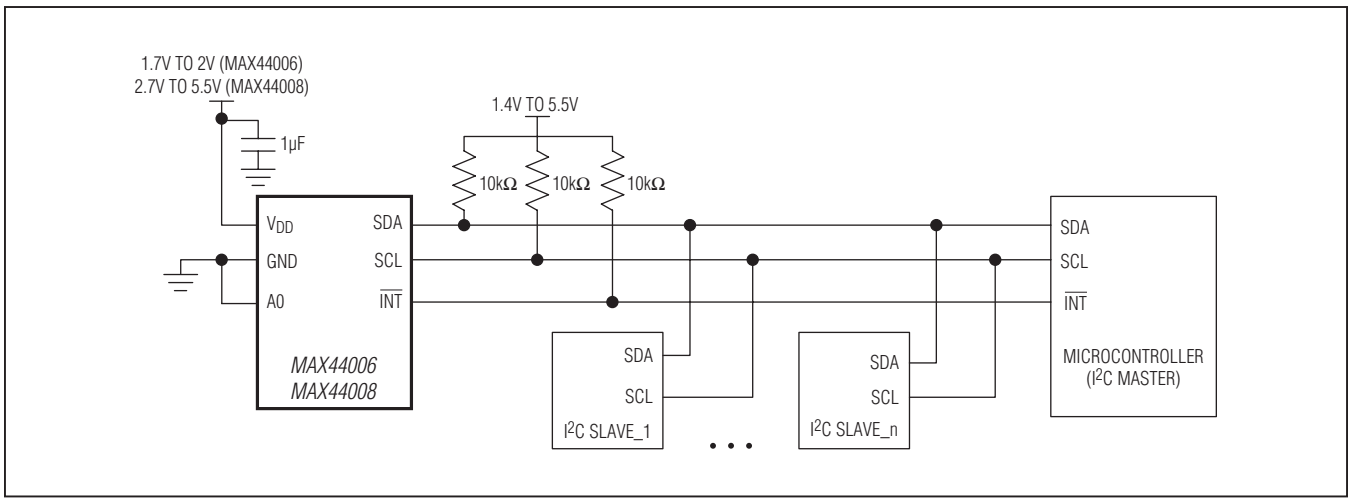


Figure 10. Reading Two Registers Consecutively Without a STOP Condition in Between Reads

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX44006EDT+	-40°C to +85°C	6 OTDFN
MAX44006EDT+T	-40°C to +85°C	6 OTDFN
MAX44008EDT+	-40°C to +85°C	6 OTDFN
MAX44008EDT+T	-40°C to +85°C	6 OTDFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 OTDFN	D622CN+1	21-0606	90-0376

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/12	Initial release	—
1	8/12	Updated the *General Description*, *Features*, *Pin Description*, *AMBIENT Data Register (0x04–0x0F)* sections, and Tables 3 and 14	1, 7, 11, 16, 21

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