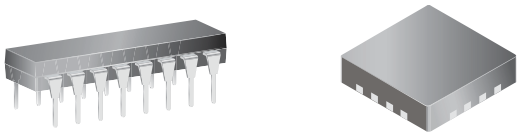
3 Bit Constant Current LED Driver with PWM Control

Features and Benefits

- 5 to 17 V operation
- Wide output current range (10 to 150 mA per output)
- 3 × 7 bit Dot Correction current settings
- 31 bit shift register
- 3 ×10 bit PWM luminance settings
- Buffered output control pins
- Up to 5 MHz serial / PWM clock frequency
- Thermal Shutdown / UVLO

Packages: 16 pin DIP (suffix A), and 16 pin QFN/MLP (suffix ES)



ES, approximate scale 1:1

Description

The A6280 is a 3 bit constant current LED driver that has a wide range of output currents. The A6280 controls LED luminance with a pulse width modulation (PWM) scheme that gives the application the capability of displaying a billion colors. The overall maximum current is set by an external resistor.

The LED luminance is controlled by performing PWM control on the outputs. The luminance data of the PWM signal for each LED is stored in three 10 bit registers. Each LED can be dot corrected by a 7 bit scalar register that scales the maximum current from 100% down to 36.5%. All the internal latched registers are loaded by a 31 bit serial shift register. One bit is used to control the type of data loaded into the registers, either dot correction / clock divider ratio or luminance data. The remaining 30 bits are used for the data. This helps reduce the pin count of the A6280. To further lower the A6280 pin count, the PWM clock and the serial bus clock share the same pin and work concurrently to control LED luminance and to load data.

The A6280 is designed to minimize the number of components needed to drive LEDs with large pixel spacing. Several A6280s can be daisy chained together and controlled by just four control signals (Clock, Serial Data, Latch, and Output Enable). Each of these inputs has buffered outputs on chip. Also, the VIN pin

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Application Diagram

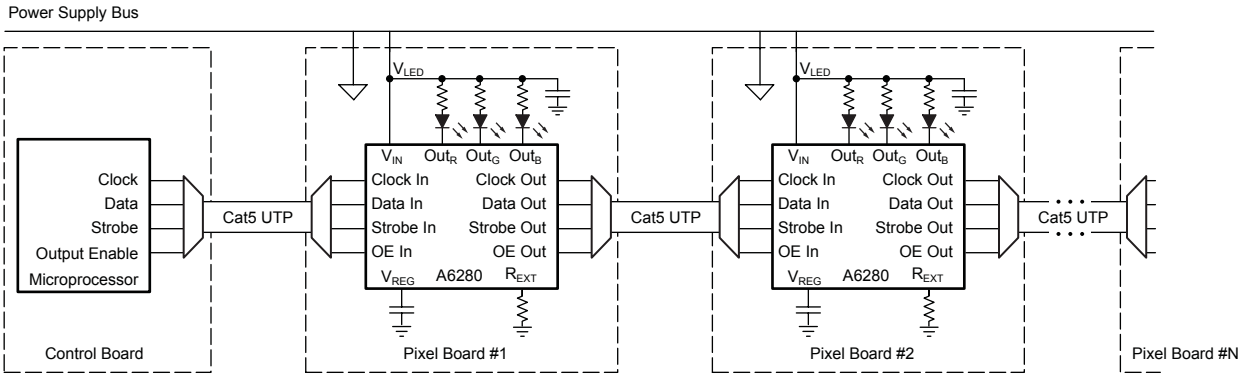


Figure 1. Functional drawing of daisy chained display application. Additional pixel boards with A6280 ICs can be applied.

Description (continued)

can be tied to the LED voltage supply bus, thus eliminating the need for a separate chip supply bus or an external linear regulator.

The A6280 is supplied in a 16 pin dual in line (DIP) package (suffix 'A') package and in a 16 lead QFN/MLP (suffix 'ES') package. The packages are lead (Pb) free with 100% matte-tin leadframe plating.

Selection Guide

Part Number	Packing*	Mounting
A6280EA-T	25 pieces/tube	16 pin DIP
A6280EESTR-T	1500 pieces/reel	16 pin QFN/MLP

*Contact Allegro for additional packing options.

Absolute Maximum Ratings

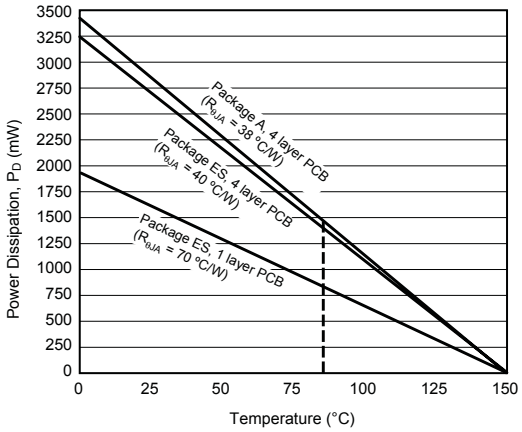
Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{IN}		17	V
Output Voltage	V_O		–0.5 to 17	V
Output Current	I_O		170	mA
Ground Current	I_{GND}		600	mA
Logic Input Voltage Range	V_I		–0.3 to 7	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–40 to 150	ºC

Thermal Characteristics

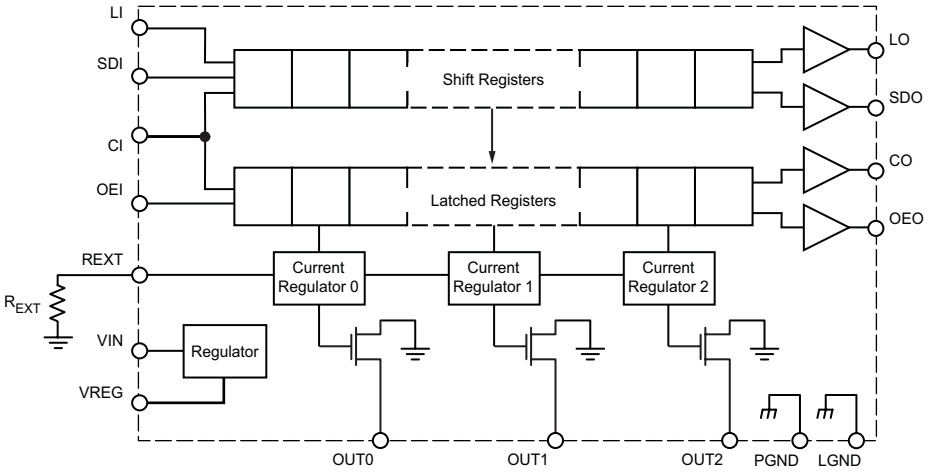
Characteristic	Symbol	Test Conditions*	Rating	Units
Package Thermal Resistance	$R_{\theta JA}$	Package A, 4 layer PCB	38	ºC/W
		Package ES, 4 layer PCB	40	ºC/W
		Package ES, 1 layer PCB with 1 in^2 Cu area	70	ºC/W

*For additional information, refer to the Allegro website.

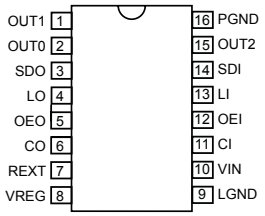
Power Dissipation versus Ambient Temperature



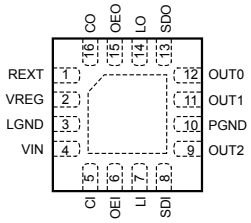
Functional Block Diagram



Pin-out Drawings



Package A



Package ES

Terminal List Table

Name	Number		Description
	A Package	ES Package	
OUT1	1	11	Sinking output terminal
OUT0	2	12	Sinking output terminal
SDO	3	13	Buffered serial data output after shift registers
LO	4	14	Buffered latch output
OEO	5	15	Buffered output enable output
CO	6	16	Buffered clock output
REXT	7	1	An external resistor at this terminal establishes overall output current
VREG	8	2	Regulator decoupling
LGND	9	3	Logic ground
VIN	10	4	Chip power supply voltage
CI	11	5	Serial and PWM clock input
OEI	12	6	Output enable input; when low (active), the output drivers are enabled; when high (inactive), all output drivers are turned off (blanked)
LI	13	7	Latch input terminal; serial data is latched with high-level input
SDI	14	8	Serial data input to shift registers
OUT2	15	9	Sinking output terminal
PGND	16	10	Power ground

OPERATING CHARACTERISTICS, valid at T_A = 25°C, V_{IN} = 4.75 to 17.0 V, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS						
Quiescent Supply Current	I_{DD}	f_{CLKIN} = 0.0 Hz	–	–	5.0	mA
Operating Supply Current	I_{DD}	f_{CLKIN} = 5 Mhz	–	–	15.0	mA
Undervoltage Lockout	$V_{IN(UV)}$	V_{IN} rising	3.5	–	4.5	V
		V_{IN} falling	3.0	–	4.0	V
VREG Voltage Range	V_{REG}	I_O =15 mA, V_{IN} = 17 V	4.6	–	5.4	V
VREG Dropout Voltage	V_{DO}	I_O =15 mA, V_{IN} = 4.75 V	–	200	600	mV
Output Current (any single output)	I_O	R_{EXT} = 5 kΩ, scalar = 100%	135	150.0	165	mA
		R_{EXT} = 15 kΩ	44	–	54	mA
Output to Output Matching Error*	Err	Output to output variation—all outputs on, R_{EXT} = 5 kΩ	7	–	7	%
Output Voltage Range	$V_{DS(min)}$		1.0	–	3.0	V
Load Regulation		$I_{\%Diff}$ / V_{DS}	–	±1	±3	%
Output Leakage Current	I_{DSX}	V_{OH} = 17 V	–	–	1.0	µA
Logic Input Voltage	V_{IH}		2.0	–	–	V
	V_{IL}		–	–	0.8	V
Logic Input Voltage Hysteresis		All digital inputs	–	150	–	mV
Logic Input Current	I_{IN}	V_{IN} = 0 to 5 V	–20	–	20	µA
Logic Output Voltage	V_{OL}	V_{IN} ≥ 5.0 V, I_O = ±2 mA	–	–	0.4	V
	V_{OH}		3.8	–	–	V
Input Resistance	R_I	OEI pin, pull-up	150	300	600	kΩ
		LI pin, pull-down	100	200	400	kΩ
Output Dot Correction Error		R_{EXT} = 5 kΩ; LSB	–	±1	–	bit
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	T_{Jhys}		–	15	–	°C
SWITCHING CHARACTERISTICS						
Clock Hold Time	$t_{H(CLK)}$		20	–	–	ns
Data Setup Time	$t_{SU(D)}$		20	–	–	ns
Data Hold Time	$t_{H(D)}$		20	–	–	ns
Latch Setup Time	$t_{SU(LE)}$		20	–	–	ns
Latch Hold Time	$t_{H(LE)}$		20	–	–	ns
Output Enable Set Up Time	$t_{SU(OE)}$		40	–	–	ns
Output Enable Falling to Outputs Turning ON Propagation Delay Time	$t_{P(OE)2}$		–	200	–	ns
Clock to Output Propagation Delay Time	$t_{P(OUT)}$	V_{DS} = 1.0 V, I_O = 150 mA	–	200	–	ns
Logic Output Fall Time	t_{BF}	C_{OB} = 50 pF, 4.5 to 0.5 V	–	50	100	ns
Logic Output Rise Time	t_{BR}	C_{OB} = 50 pF, 0.5 to 4.5 V	–	30	60	ns
Output Fall Time (Turn Off)	t_f	C_O = 10 pF, 90% to 10% of I_O = 10 mA	–	10	–	ns
		C_O = 10 pF, 90% to 10% of I_O = 10 mA	–	10	–	ns
Output Rise Time (Turn On)	t_r	C_O = 10 pF, 90% to 10% of I_O = 10 mA	–	50	–	ns
		C_O = 10 pF, 90% to 10% of I_O = 10 mA	–	100	–	ns
Clock Falling Edge to Serial Data Out Propagation Delay Time	$t_{P(SDO)}$		–	50	100	ns
Output Enable In to Output Enable Out Propagation Delay	$t_{P(OE)}$		–	50	100	ns
Latch In to Latch Out Propagation Delay	$t_{P(LE)}$		–	50	100	ns
Clock In to Clock Out Propagation Delay	$t_{P(CLK)}$		–	50	100	ns
Clock Out Pulse Duration	$t_{w(CLK)}$		70	100	130	ns
Maximum CLKIN Frequency	f_{CLKIN}		–	–	6	MHz

*Err = [I_O(min or max) – I_O(av)] / I_O(av).

Timing Diagram

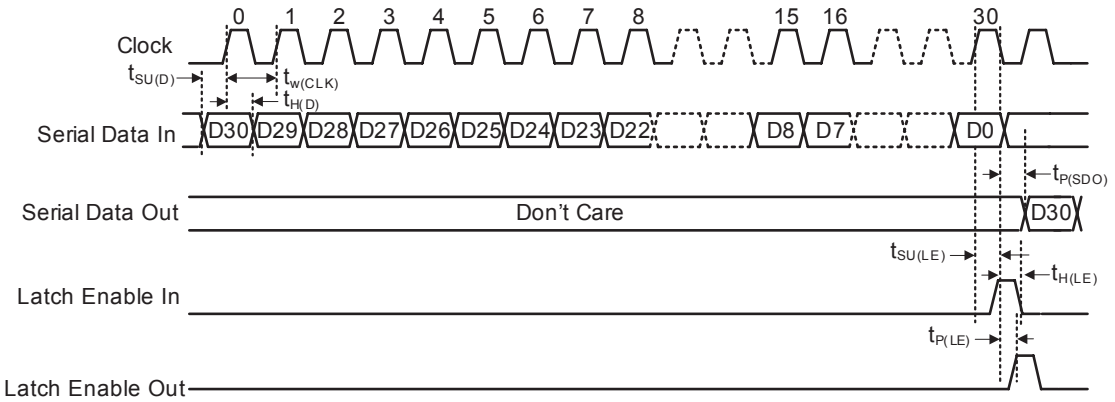


Figure 2. Shift Register Timing

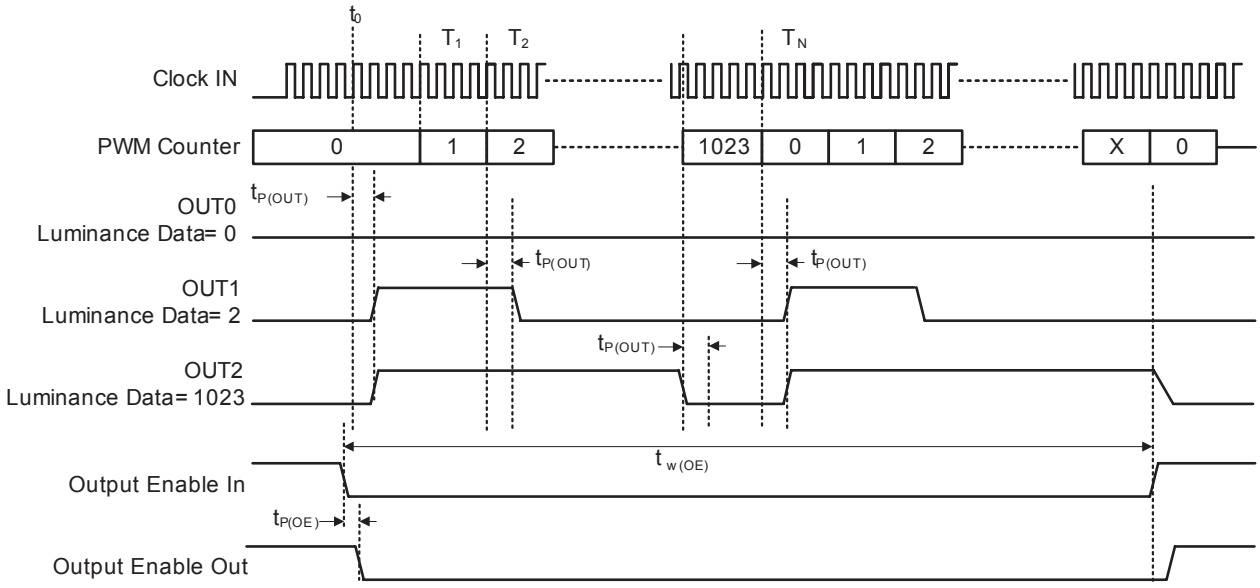


Figure 3. PWM Counter and Output Timing

Functional Description

Shift Registers

The A6280 has a 31 bit shift register that loads data through the Serial Data In (SDI) pin. The shift registers operate by a first-in first-out (FIFO) method. The most significant bit (MSB, bit 30) is the first bit shifted in and the least significant bit (LSB, bit 0) is shifted in last. The serial data is clocked by a rising edge of the Clock In (CI) pin. The Serial Data Out (SDO) pin is updated to the state of bit 30 on the falling edge of the CI pin. This will prevent any race conditions and erroneous data that might occur while propagating information through multiple A6280 that are daisy chained together. The contents of the shift registers will continue to propagate on every rising edge of the CI pin. The information in the shift registers is latched on a rising edge of the Latch In (LI) pin. The latched data remains latched on a rising Output Enable In (OEI) signal.

Output Buffers

The A6280 is designed to allow daisy chaining many A6280s together. It has the ability to pass the clock, data, latch, and output enable signals from one A6820 to the next without any loss of data due to duty cycle skewing or signal degradation.

The A6820 is equipped with output buffers that allow the data signals to travel over long distances through strings of A6280s without the need for extra driving hardware. The A6280 drives these signals to TTL levels. Each of the A6280 inputs have a corresponding buffered output:

- Clock In (CI) pin to Clock Out (CO) pin
- Latch In (LI) pin to Latch Out (LO) pin
- Output Enable In (OEI) pin to Output Enable Out (OEO) pin
- Serial Data In (SDI) pin to Serial Data Out (SDO) pin

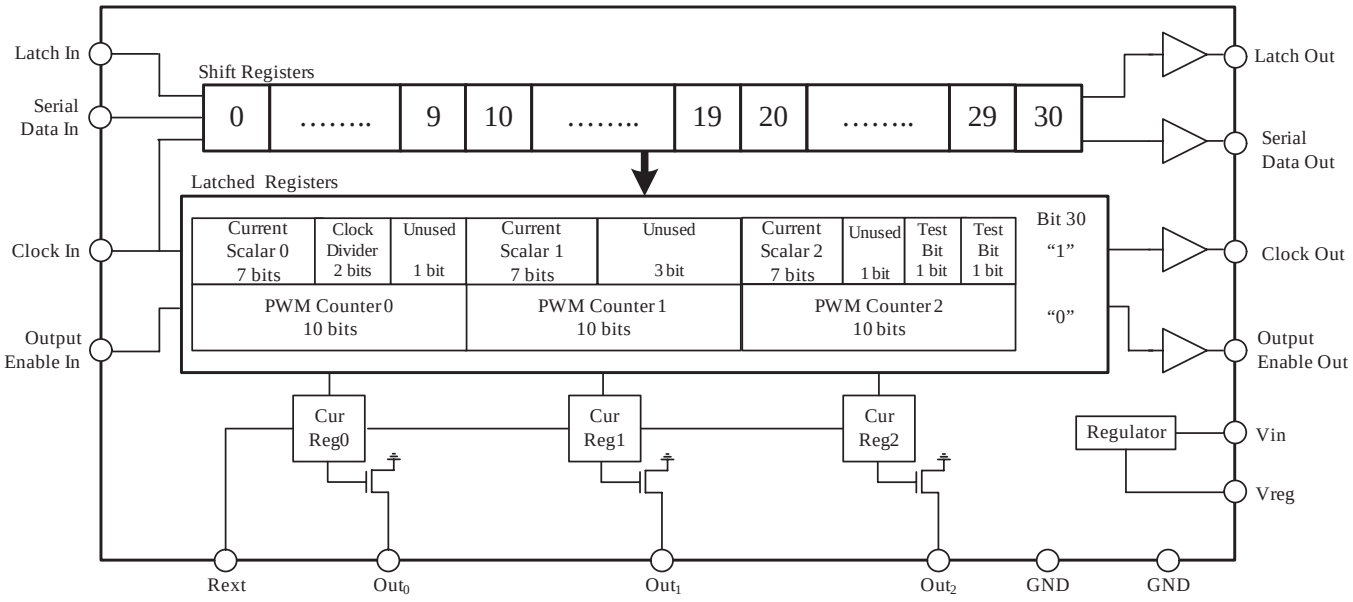


Figure 4. Functional Diagram

PWM Luminance Control

The A6280 controls the intensity of each LED by PWMing the current of each output. The A6280 has three 10 bit luminance registers, one for each output. These luminance registers set the PWM count value at which the outputs switch off during each PWM cycle. Each 10 bit luminance register gives 1023 levels of light intensity. The duty cycle, DC (%), can be determined by the following equation:

$$DC = [(PWM_{n+1})/1024] \times 100 ,$$

where PWM_n is the PWM value greater than zero that is stored in the luminance register. When the luminance register is set to zero, the outputs remain off for the duration of the PWM cycle for a 0% DC. When a luminance register is set to 1023, the LED for that output remains on (100% DC) when OEI is active and begins the PWM cycle. The output remains on when the PWM counter rolls over and begins a new count.

The PWM counter begins counting at zero and increments only when the OEI pin is held low. When the PWM counter reaches the count of 1023, the counter resets to zero and continues incrementing. The counter resets back to zero either on a rising edge of OEI, upon recovery from UVLO, or when powering up. Latching new data into the luminance registers will not reset the PWM counter.

There is a programmable clock divider that attenuates the clock input of the CI pin. See table 1 for bit assignments of the programmable clock divider. The PWM counter is incremented on every rising edge of the CI pin divided by the clock divider count value when the OEI pin is low. For example, if the clock divider is programmed to divide the CI by 2, then the PWM counter will increment once every 2 CI cycles. Given a 5 MHz CI frequency, the clock period would be 200 ns.

Table 1. Clock Divider Configurations

Bits		Divide By Count
7	8	
0	0	×1 (no division)
1	0	×2
0	1	×4
1	1	×8

The clock divider data in the shift registers is latched on a rising edge of the Latch In (LI) pin. The latched clock divider data remains latched on a rising OEI signal.

The total number of possible colors of an RGB pixel is over 1 billion. Refer to figure 6 for the mapping of shift register bits to latches.

Output Current Selection

The overall maximum current is set by the external resistor, R_{EXT}, connected between REXT and LGND. Once set, the maximum current remains constant regardless of the LED voltage variation, supply voltage variation, temperature, or other circuit parameters that could otherwise affect LED current. The maximum output current can be calculated using the following equation:

$$I_O(max) = 753.12 / R_{EXT}.$$

The relationship of the value selected for R_{EXT} and I_O is shown in figure 5.

Internal Linear Regulator

The A6280 has a built-in linear regulator. The regulator operates from 5 to 17 V, and is intended to allow the VIN pin of the A6280 to connect to the same supply as the LEDs. This will simplify board design by eliminating the need for a chip supply bus and external voltage regulators.

The VREG pin is used by the internal liner regulator as an energy reservoir. This pin is for internal use only and is not intended as an external power source. The VREG pin should have a 1.0 µF, 10 V ceramic capacitor connected between the VREG pin and LGND. The capacitor should be located as close to the VREG pin as possible.

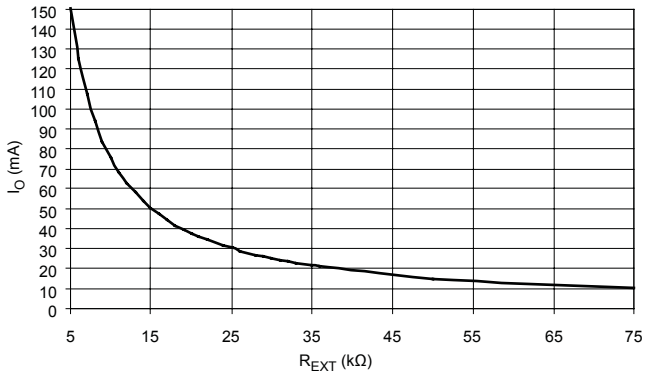


Figure 5. Output Current versus External Resistor, R_{EXT}

Dot Correction Control

The A6280 can further control the maximum output current for each output by setting the three 7 bit dot correction registers with scale data that ranges from 36.5% to 100% of the overall maximum output current that is set by the R_{EXT} resistor. This feature is useful because not every type of LED (red, green, or blue, for example) has the same level of brightness or intensity for any given current, and the brightness could be different even from LED to LED of the same type. By scaling the output currents so that all the LEDs have matched intensities, the application will have full color depth when using the PWM counters. The dot correction current can be calculated by the following equation:

$$I_{On} = I_{On(max)} \times (Scale_n / 2 + 36.5)$$

Refer to figure 6 for the bit configurations for the scalar registers.

The dot correction data in the shift registers is latched on a rising edge of the Latch In (LI) pin. The latched dot correction data remains latched on a rising OEI signal. The default output current when the A6280 is powered up or recovers from a UVLO is 36.5% of the current set by the R_{EXT} resistor.

Package Power Dissipation

The maximum allowable package power dissipation is determined as:

$$P_D(max) = (150 - T_A) / R_{\theta JA} \ .$$

The actual package power dissipation is:

$$P_{D(act)} = DC_0 \times V_{DS0} \times I_{OUT0} + DC_1 \times V_{DS1} \times I_{OUT1} + DC_2 \times V_{DS2} \times I_{OUT2} + V_{IN} \times I_{IN} \ .$$

When calculating power dissipation, the total number of available device outputs is usually used for the worst-case situation (i.e., displaying all 3 LEDs at 100% DC).

Thermal Shutdown (TSD)

When the junction temperature of the A6280 reaches the thermal shutdown temperature threshold, T_{JTSD} (165°C typical), the outputs will shut off until the junction temperature cools down below the recovery threshold, $-T_{JTSD} - \Delta T_J$ (15°C typical). The shift registers and output latches will remain active during the TSD event. Therefore there is no need to reset the data in the output latches.

Undervoltage Lockout

The A6280 includes an internal undervoltage lockout (UVLO) circuit that disables the driver outputs in the event of the logic supply voltage dropping below a minimum acceptable level. This prevents the display of erroneous information, a necessary function for some critical applications. The shift registers will not shift any data in a UVLO condition. Upon recovery of the logic supply voltage and on power up, all internal shift registers and latches will be set to zero.

Ballast Resistors

The voltage on the outputs should be kept in the range 1 to 3 V. If the voltage goes below 1V, the current will begin to rolloff as the driver runs out of headroom. At V_O above 3 V, the power dissipation may become a problem, as each output contributes $V_O \times I_{LED}$ of power loss in the output sink driver. Typically the power supply nominal voltage is chosen to keep the output voltage in this range. Alternatively, series resistors can be added to dissipate the extra power and keep the output voltage within the recommended range.

Bits

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
PWM Counter 0										PWM Counter 1										PWM Counter 2										0
Dot Correction Register 0							Clock Divider		0	Dot Correction Register 1								0	0	0	Dot Correction Register 2							0	ATB*	ATB*	1

*Allegro Test Bit (ATB). Reserved for Allegro internal testing. Always set to zero (0) in the application.

Figure 6. Register Configuration

Applications Drawings

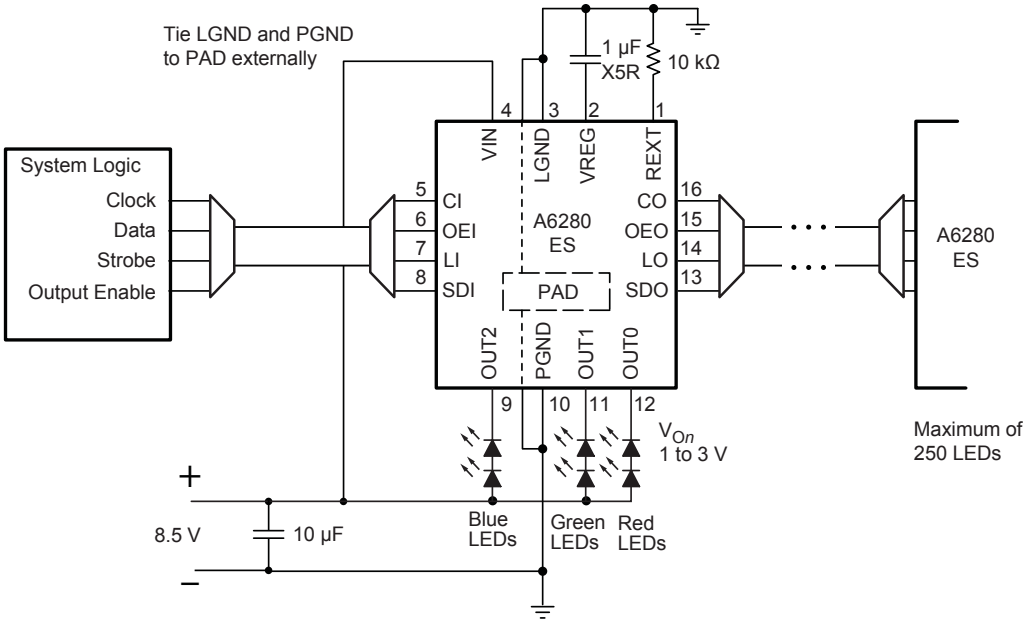


Figure 7. Application Driving 3 RGB LEDs at 75 mA Peak

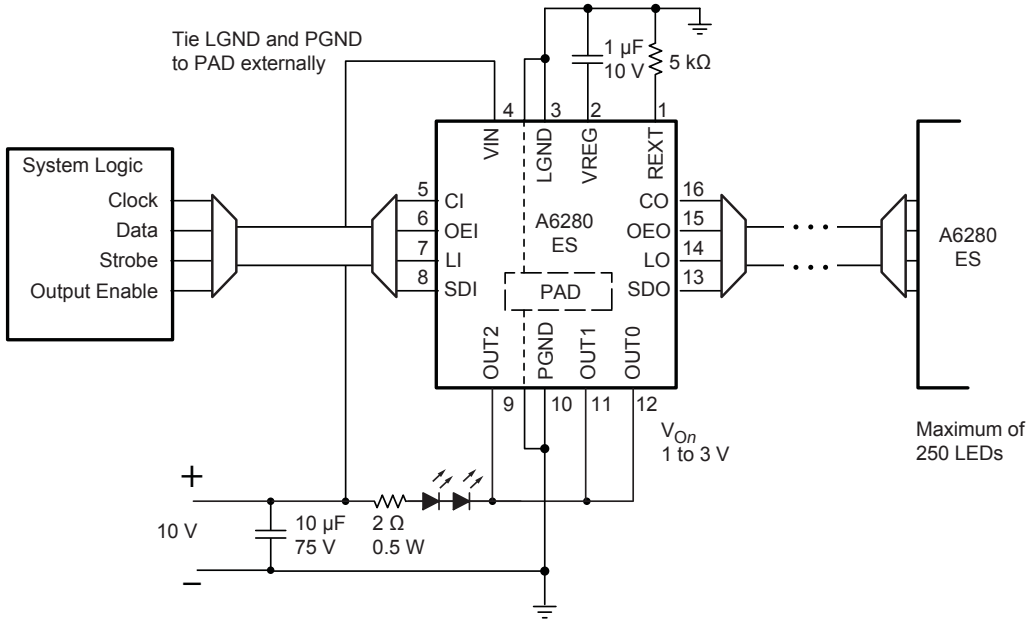
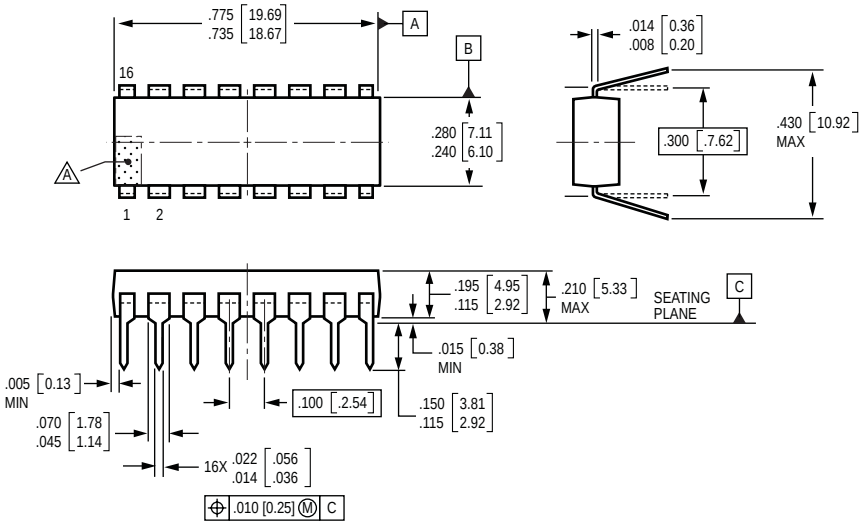


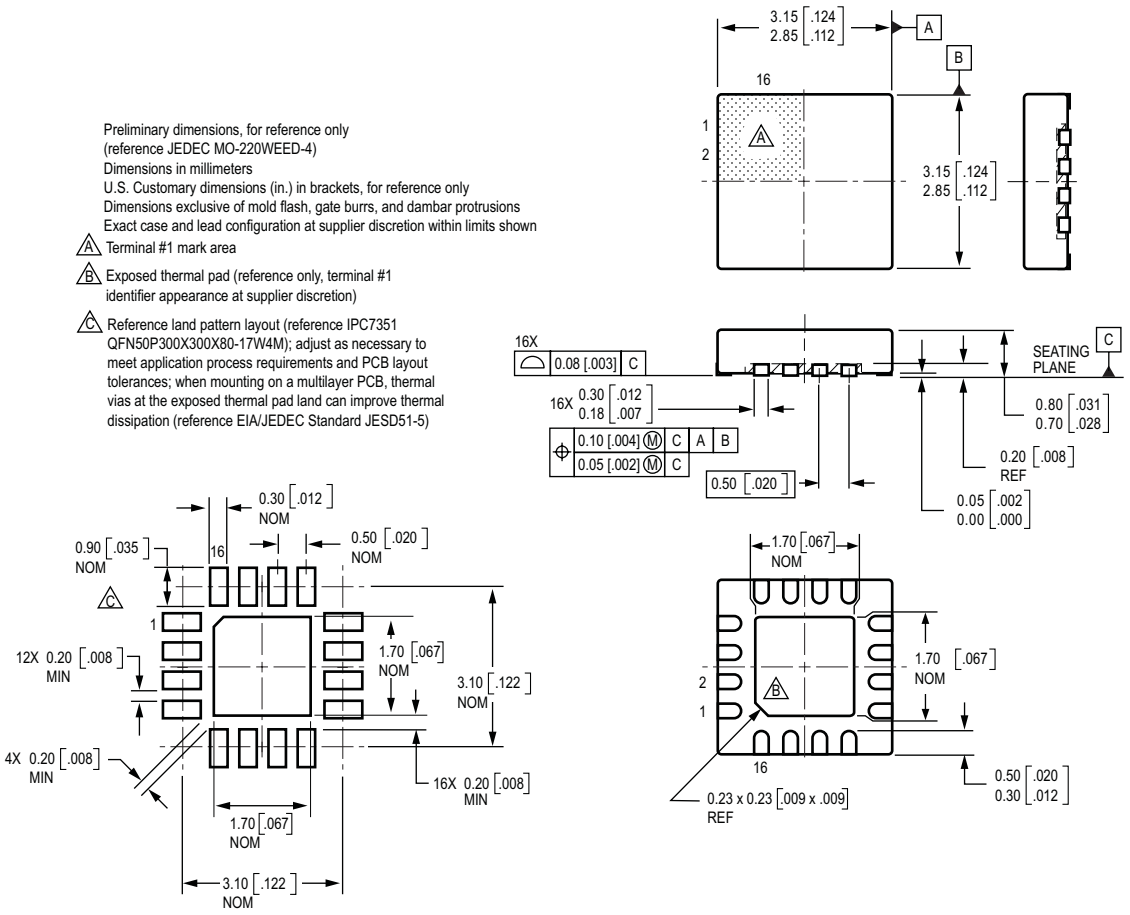
Figure 8. Application Driving High Power LED at 450 mA

A Package, 16 Pin DIP

Preliminary dimensions, for reference only
Dimensions in inches
Metric dimensions (mm) in brackets, for reference only
(reference JEDEC MS-001 BB)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area



ES Package, 16 Pin QFN/MLP



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