A3V26S004N

Airfast RF Power LDMOS Transistor

Rev. 0 — December 2020

Data Sheet: Technical Data

This 26 dBm RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 2496 to 2690 MHz.

2600 MHz

- Typical Single-Carrier W-CDMA Reference Circuit Performance: V_{DD} = 42 Vdc, I_{DQ} = 17 mA, P_{out} = 23.5 dBm Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.(1)

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2515 MHz	23.2	15.1	10.3	–35.0
2595 MHz	23.0	15.5	9.6	–37.0
2675 MHz	22.0	14.8	9.3	–37.7

1. All data measured in reference circuit with device soldered to printed circuit board.

Features

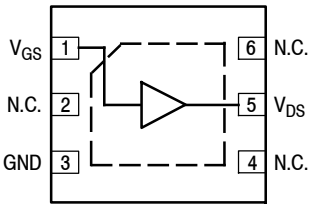
- Designed for low complexity analog or digital linearization systems
- Universal broadband driver
- Optimized for massive MIMO active antenna systems for 5G base stations

A3V26S004N

2496–2690 MHz, 26 dBm Avg., 48 V AIRFAST RF POWER LDMOS TRANSISTOR



DFN 4.5 x 4 PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

NXP reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +105	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 125°C, 26.0 dBm Avg., W-CDMA, 48 Vdc, I_{DQ} = 17 mA, 2595 MHz	$R_{\theta JC}$	8.0	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	1C
Charge Device Model (per JS-002-2014)	C2a

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 8 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 10 μAdc)	$V_{GS(th)}$	0.7	1.2	1.7	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_D = 16 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.6	1.78	1.9	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 75 mAdc)	$V_{DS(on)}$	0.2	0.6	0.9	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

(continued)

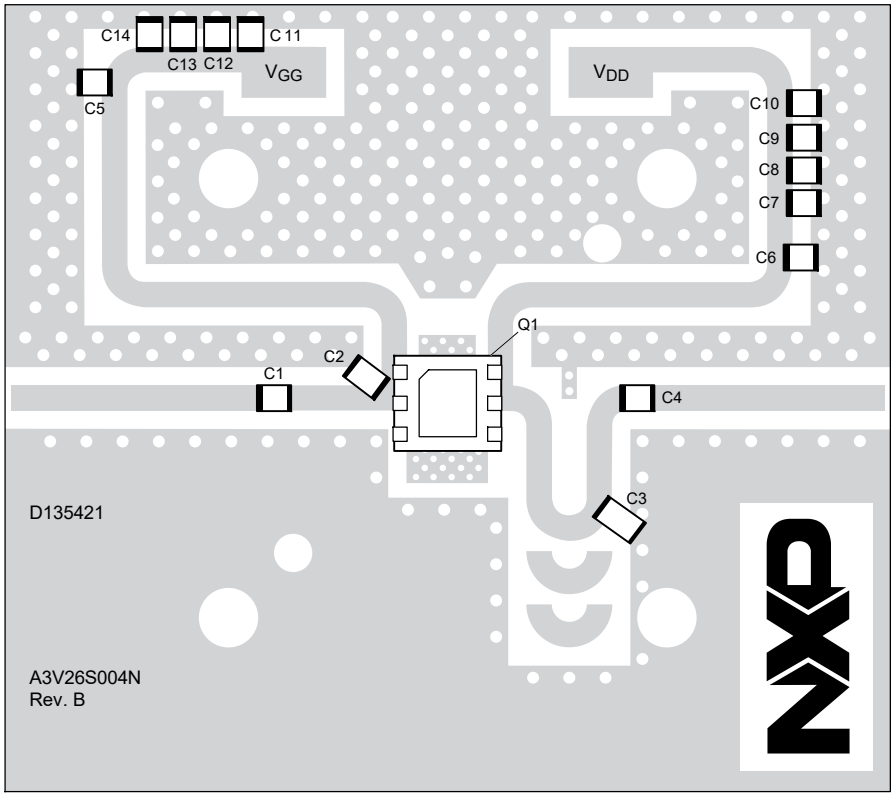
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In NXP Production Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQ} = 16 mA, P_{out} = 26 dBm Avg., f = 2690 MHz, 1-tone CW.					
Power Gain	G_{ps}	19.5	23.3	26.0	dB
Drain Efficiency	η_D	18.0	21.9	—	%
P_{out} @ 6 dB Compression Point	P6dB	33.5	35.0	—	dBm
Wideband Ruggedness (In NXP Reference Circuit, 50 ohm system) I_{DQ} = 17 mA, f = 2595 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 55 Vdc, 1.5 W Avg. Modulated Output Power (3 dB Input Overdrive from 0.7 W Avg. Modulated Output Power)	No Device Degradation				
Typical Performance (2) (In NXP Reference Circuit, 50 ohm system) V_{DD} = 42 Vdc, I_{DQ} = 17 mA, 2515–2675 MHz Bandwidth					
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	170	—	MHz
Gain Flatness in 160 MHz Bandwidth @ P_{out} = 23.5 dBm Avg.	G_F	—	0.7	—	dB
Fast CW, 27 ms Sweep					
P_{out} @ 3 dB Compression Point	P3dB	—	3.1	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2515–2675 MHz bandwidth)	Φ	—	–23	—	°
Gain Variation over Temperature (–40°C to +85°C)	ΔG	—	0.017	—	dB/°C
Output Power Variation over Temperature (–40°C to +85°C)	ΔP1dB	—	0.004	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A3V26S004NT6	T6 Suffix = 5,000 Units, 12 mm Tape Width, 13-inch Reel	DFN 4.5 × 4

1. Part internally input matched.
2. All data measured in fixture with device soldered to printed circuit board.



Note: All data measured in reference circuit with device soldered to printed circuit board. *aaa-037822*

Figure 2. A3V26S004N Reference Circuit Component Layout

Table 7. A3V26S004N Reference Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	6.8 pF Chip Capacitor	600F6R8BW250XT	ATC
C2	1.0 pF Chip Capacitor	600F1R0BW250XT	ATC
C3	1.8 pF Chip Capacitor	600F1R8BW250XT	ATC
C4	10 pF Chip Capacitor	600F100FW250XT	ATC
C5, C6	20 pF Chip Capacitor	600F200FW250XT	ATC
C7	0.1 μF Chip Capacitor	GRM319R71H104KA	Murata
C8	1 μF Chip Capacitor	GRM32ER72A105KA	Murata
C9, C10	10 μF Chip Capacitor	GRM31CR61H106KA	Murata
C11	10 μF Chip Capacitor	GRM21BR61C106KE	Murata
C12	1 μF Chip Capacitor	08055C105KAT2A	AVX
C13	0.1 μF Chip Capacitor	GRM188R71H104KA	Murata
C14	2.2 nF Chip Capacitor	GRM1885C1H222JA	Murata
Q1	RF Power LDMOS Transistor	A3V26S004N	NXP
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D135421	MTL

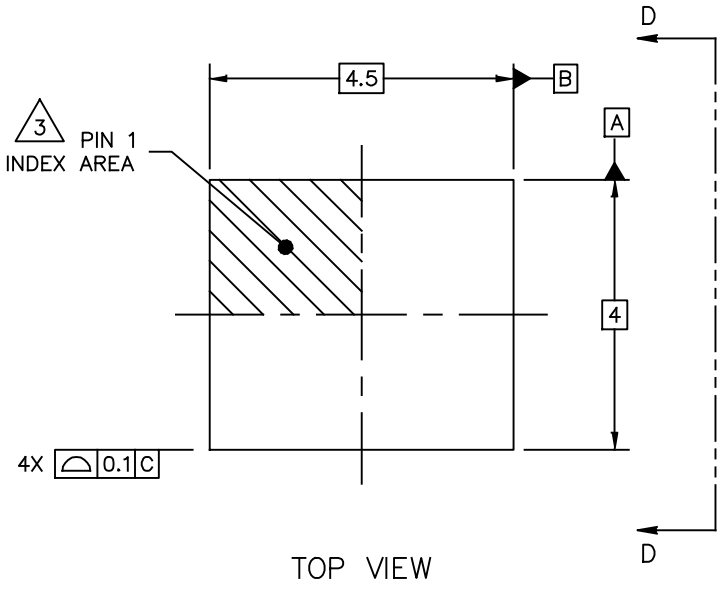


Figure 3. Product Marking

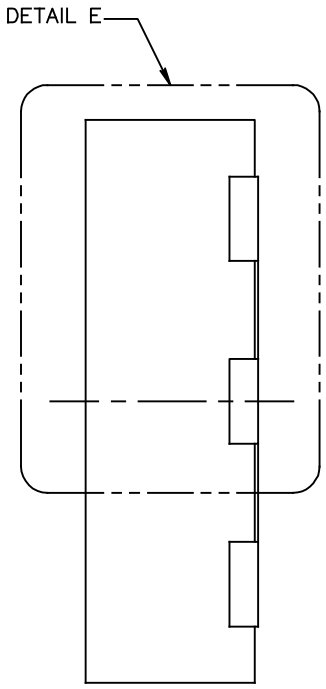
Package Information

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

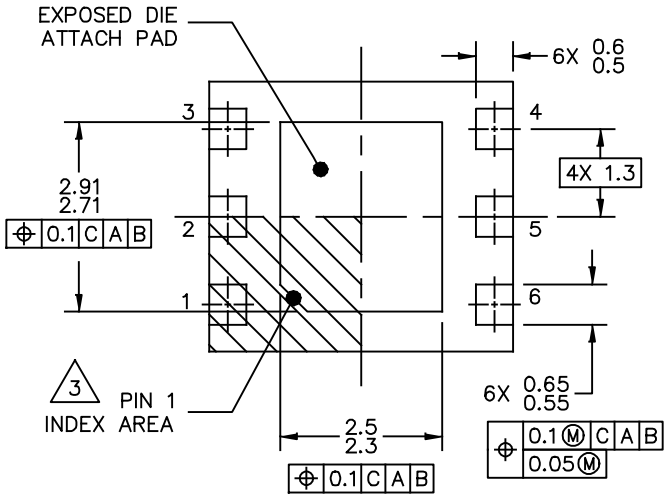
SOT2040–1



TOP VIEW



VIEW D–D



BOTTOM VIEW

RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.

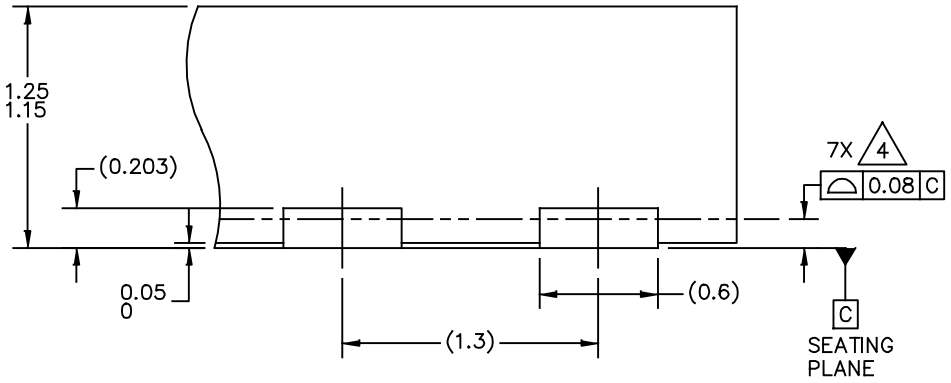
© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: O	PAGE: 1 OF 6

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1



DETAIL E
VIEW ROTATED 90°CW

RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.

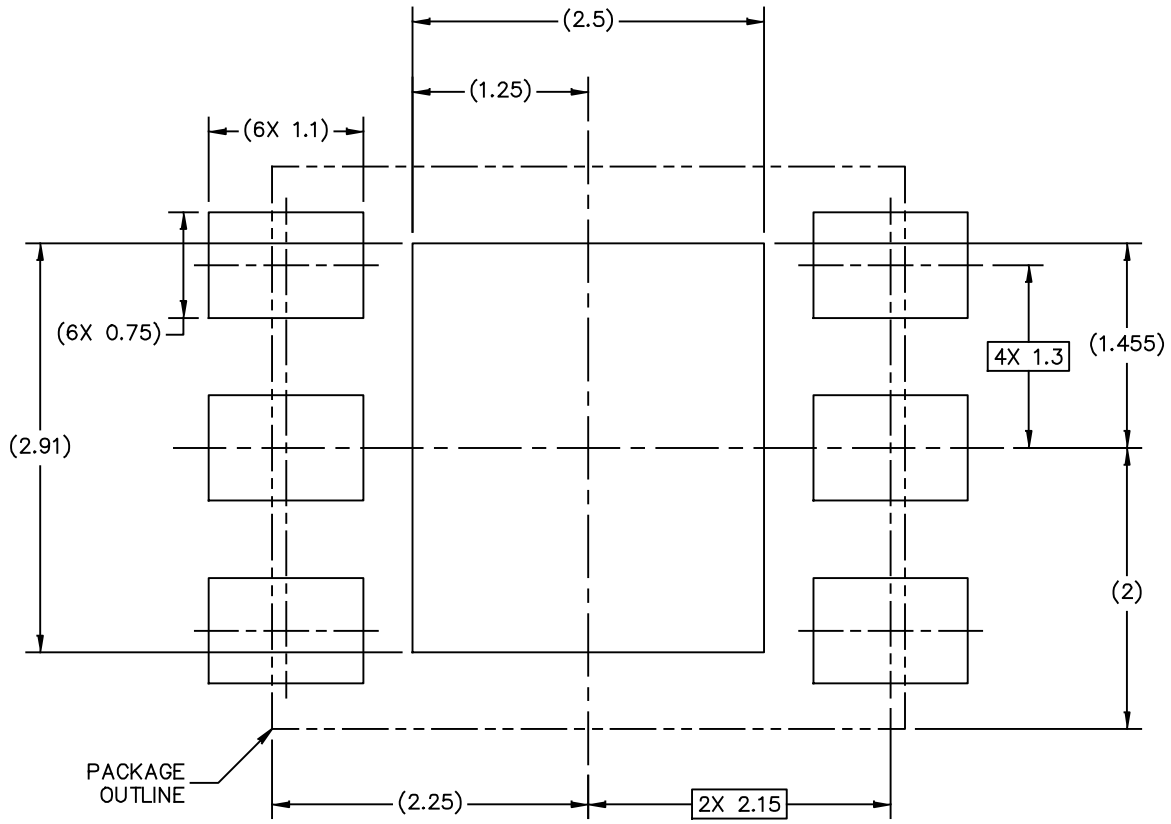
© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: O	PAGE: 2

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

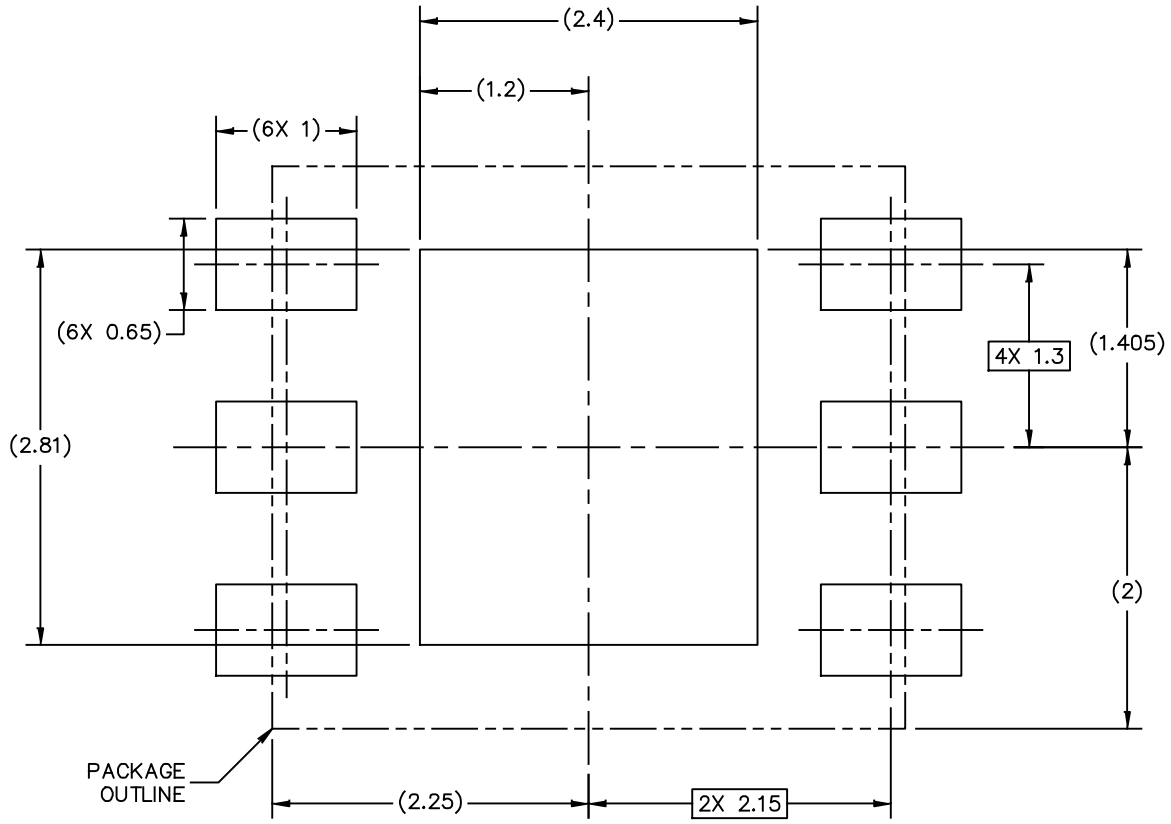
© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: O	PAGE: 3

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

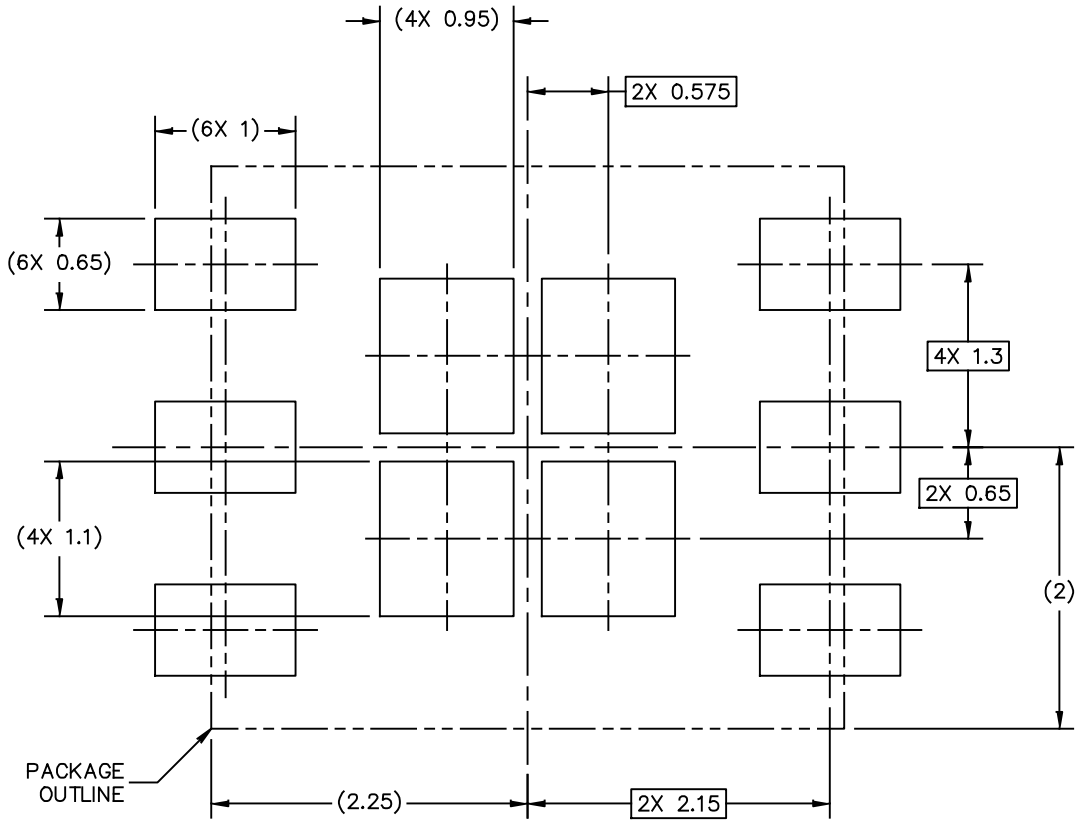
© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: O	PAGE: 4

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1



RECOMMENDED STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: O	PAGE: 5

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: O	PAGE: 6

Product Documentation, Software and Tools

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- Electromigration MTTF Calculator
- .s2p File

Development Tools

- Printed Circuit Boards

Revision History

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2020	• Initial release of data sheet

How to Reach Us

Home Page
nxp.com

Web Support:
nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer’s technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

NXP, the NXP logo, Freescale, the Freescale logo and Airfast are trademarks of NXP B.V. All other product or service names are the property of their respective owners.

© NXP B.V. 2020 **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: December 2020
Document identifier: A3V26S004N