

DATA SHEET

BF1202; BF1202R; BF1202WR N-channel dual-gate PoLo MOS-FETs

Product specification
Supersedes data of 1999 Dec 01

2000 Mar 29

N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R;
BF1202WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier
- Partly internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

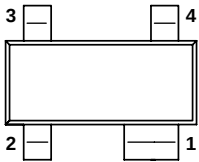
- VHF and UHF applications with 3 to 9 V supply voltage, such as digital and analogue television tuners and professional communications equipment.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1202, BF1202R and BF1202WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

PINNING

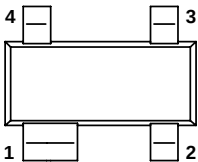
PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



Top view MSB035

BF1202R marking code: LEp

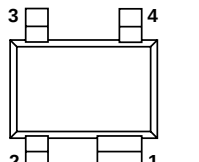
Fig.2 Simplified outline (SOT143R).



Top view MSB014

BF1202 marking code: LDp

Fig.1 Simplified outline (SOT143B).



Top view MSB842

BF1202WR marking code: LE

Fig.3 Simplified outline (SOT343R).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DS}	drain-source voltage		–	–	10	V
I _D	drain current		–	–	30	mA
P _{tot}	total power dissipation		–	–	200	mW
y _{fs}	forward transfer admittance		25	30	40	mS
C _{ig1-ss}	input capacitance at gate 1		–	1.7	2.2	pF
C _{rss}	reverse transfer capacitance	f = 1 MHz	–	15	30	fF
F	noise figure	f = 800 MHz	–	1.1	1.8	dB
X _{mod}	cross-modulation	input level for k = 1% at 40 dB AGC	100	105	–	dBμV
T _j	operating junction temperature		–	–	150	°C

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R;
BF1202WR

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

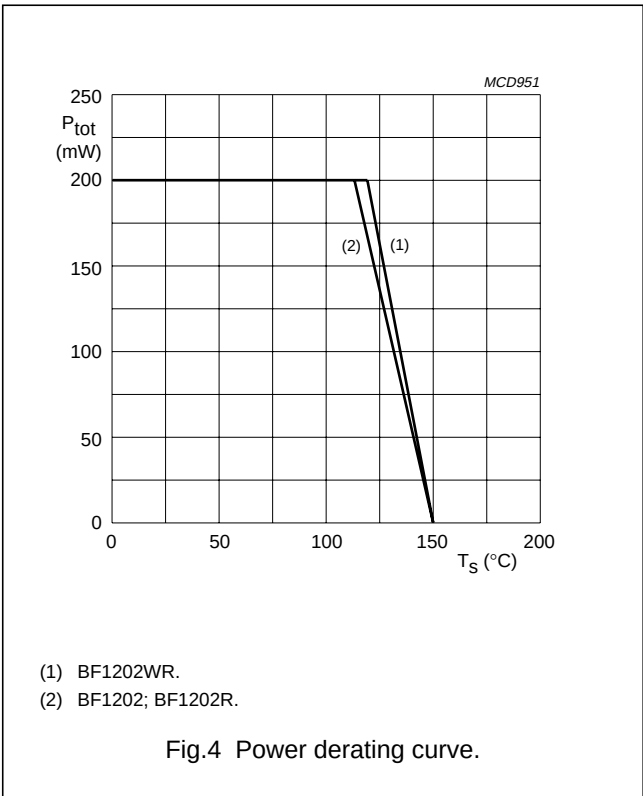
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		–	10	V
I _D	drain current		–	30	mA
I _{G1}	gate 1 current		–	±10	mA
I _{G2}	gate 2 current		–	±10	mA
P _{tot}	total power dissipation				
	BF1202; BF1202R	T _s ≤ 113 °C; note 1	–	200	mW
	BF1202WR	T _s ≤ 119 °C; note 1	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	150	°C

Note

1. T_s is the temperature of the soldering point of the source lead.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-s}	thermal resistance from junction to soldering point		
	BF1202; BF1202R	185	K/W
	BF1202WR	155	K/W



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BF1202WR

STATIC CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; $I_D = 10\text{ }\mu\text{A}$	10	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 10\text{ mA}$	6	–	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10\text{ mA}$	6	–	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1.0	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = 5\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_{G1} = 120\text{ k}\Omega$; note 1	8	16	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; $V_{G1-S} = 5\text{ V}$	–	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 4\text{ V}$	–	20	nA

Note

1. R_{G1} connects G_1 to $V_{GG} = 5\text{ V}$.

DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 12\text{ mA}$; unless otherwise specified.

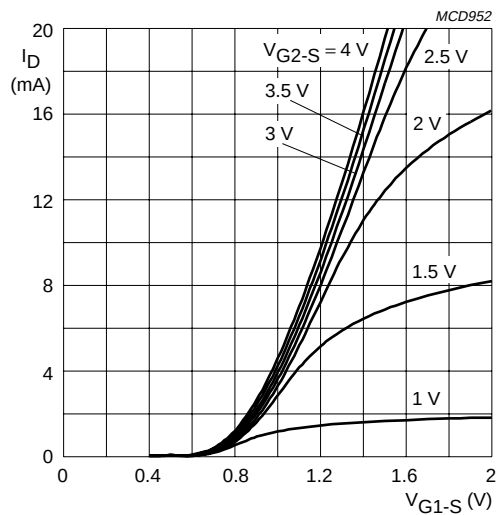
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ }^{\circ}\text{C}$	25	30	40	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1\text{ MHz}$	–	1.7	2.2	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1\text{ MHz}$	–	1	–	pF
C_{oss}	output capacitance	$f = 1\text{ MHz}$	–	0.85	–	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	15	30	fF
F	noise figure	$f = 10.7\text{ MHz}$; $G_S = 20\text{ mS}$; $B_S = 0$	–	9	11	dB
		$f = 400\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	0.9	1.5	dB
		$f = 800\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	1.1	1.8	dB
G_{tr}	power gain	$f = 200\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 0.5\text{ mS}$; $B_L = B_{L\text{ opt}}$	–	34.5	–	dB
		$f = 400\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 1\text{ mS}$; $B_L = B_{L\text{ opt}}$	–	30.5	–	dB
		$f = 800\text{ MHz}$; $G_S = 3.3\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 1\text{ mS}$; $B_L = B_{L\text{ opt}}$	–	26.5	–	dB
X_{mod}	cross-modulation	input level for $k = 1\%$; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 1				
		at 0 dB AGC	90	–	–	dB μ V
		at 10 dB AGC	–	92	–	dB μ V
		at 40 dB AGC	100	105	–	dB μ V

Note

1. Measured in Fig.21 test circuit.

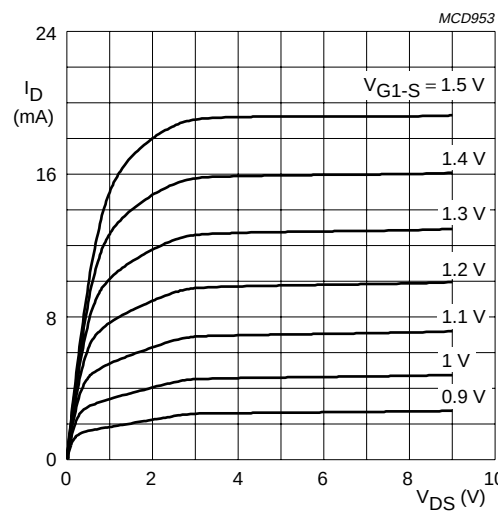
N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R;
BF1202WR



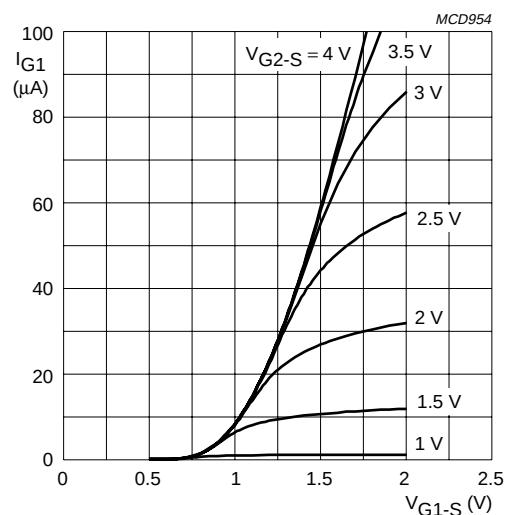
$V_{DS} = 5\text{ V.}$
 $T_j = 25\text{ }^{\circ}\text{C.}$

Fig.5 Transfer characteristics; typical values.



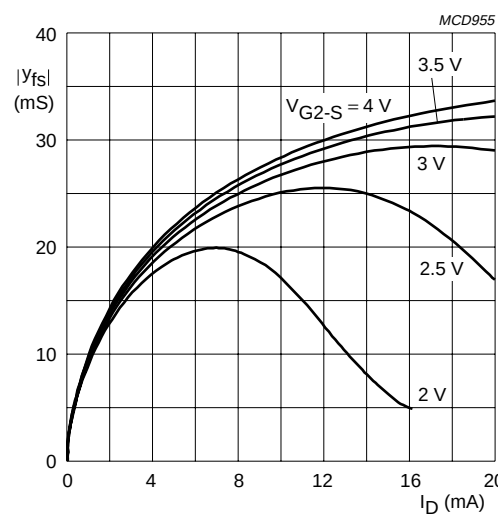
$V_{G2-S} = 4\text{ V.}$
 $T_j = 25\text{ }^{\circ}\text{C.}$

Fig.6 Output characteristics; typical values.



$V_{DS} = 5\text{ V.}$
 $T_j = 25\text{ }^{\circ}\text{C.}$

Fig.7 Gate 1 current as a function of gate 1 voltage; typical values.

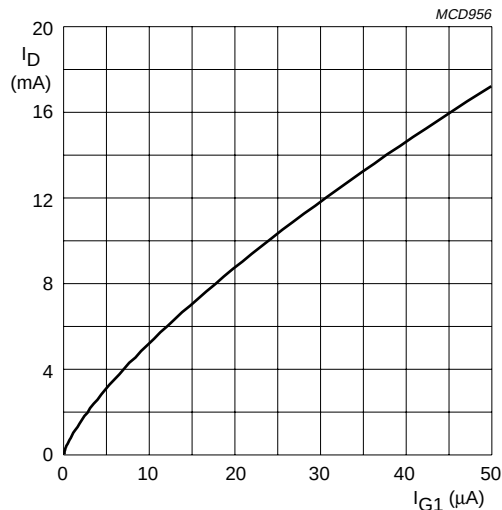


$V_{DS} = 5\text{ V.}$
 $T_j = 25\text{ }^{\circ}\text{C.}$

Fig.8 Forward transfer admittance as a function of drain current; typical values.

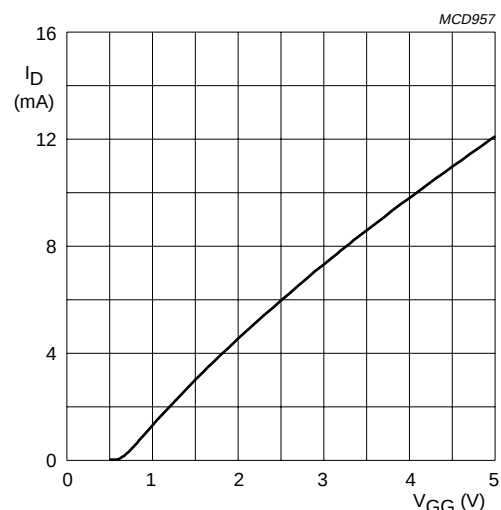
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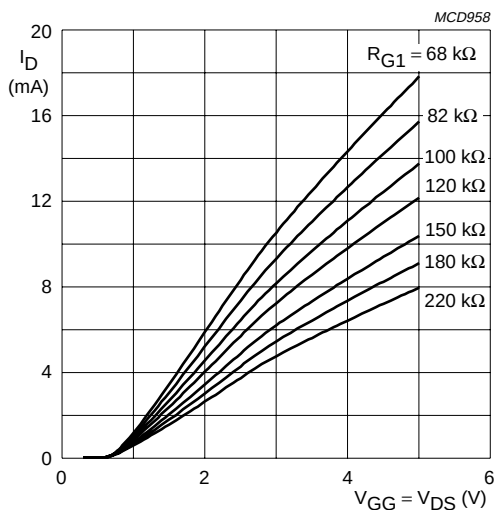
$V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$.
 $T_j = 25\text{ }^{\circ}\text{C}$.

Fig.9 Drain current as a function of gate 1 current; typical values.



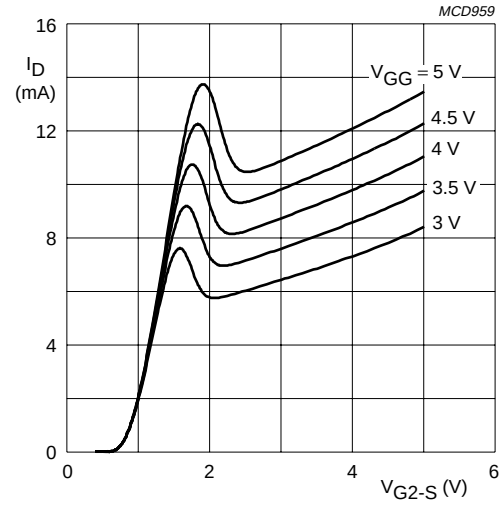
$V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$.
 $R_{G1} = 120\text{ k}\Omega$ (connected to V_{GG}); see Fig.21.

Fig.10 Drain current as a function of gate 1 supply voltage ($= V_{GG}$); typical values.



$V_{G2-S} = 4\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$.
 R_{G1} connected to V_{GG} ; see Fig.21.

Fig.11 Drain current as a function of gate 1 ($= V_{GG}$) and drain supply voltage; typical values.

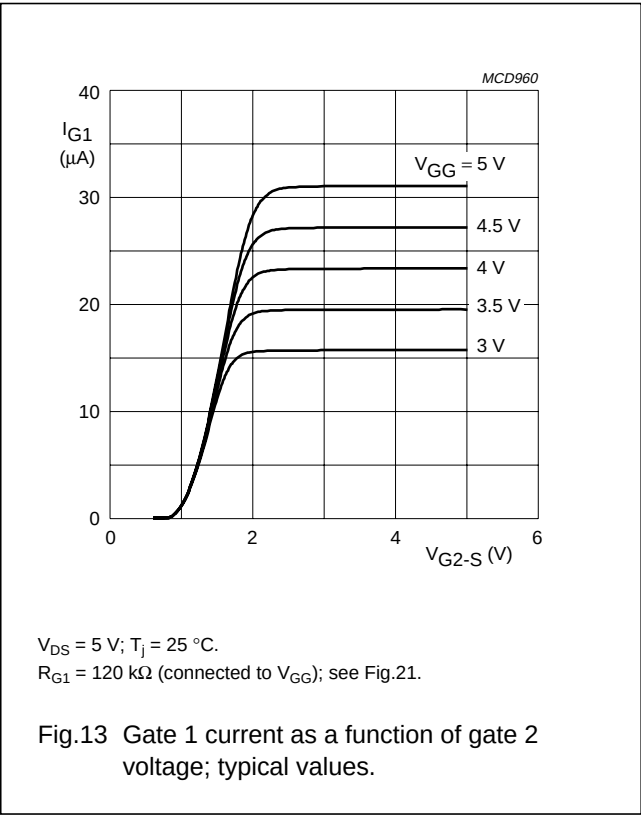
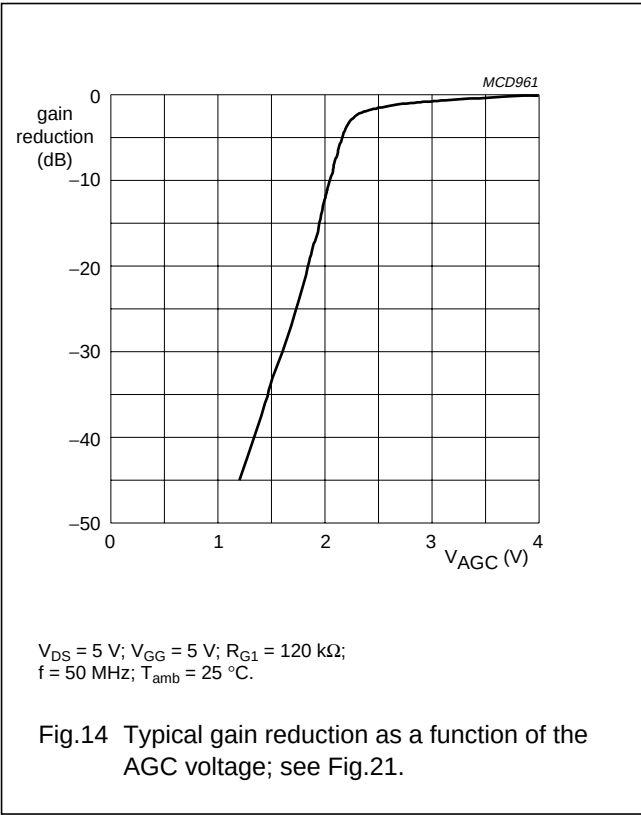
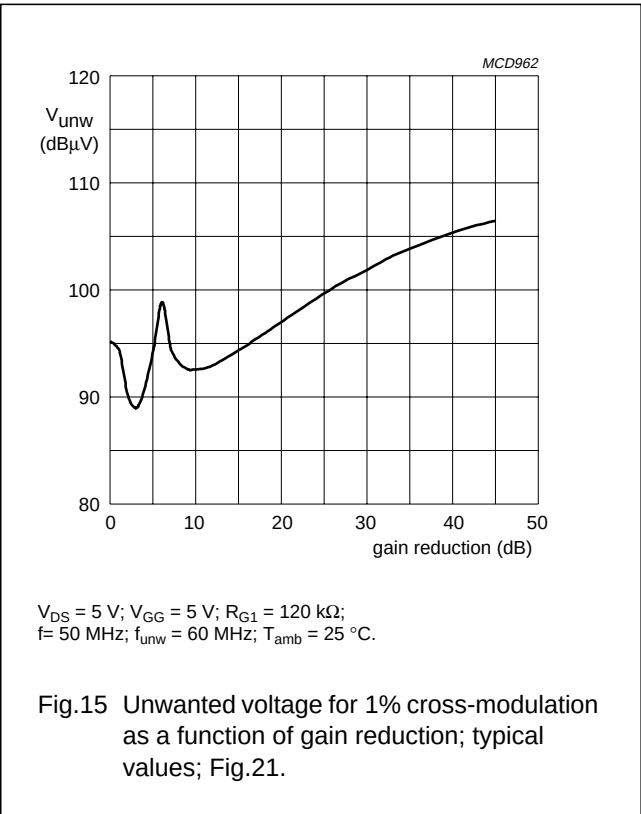
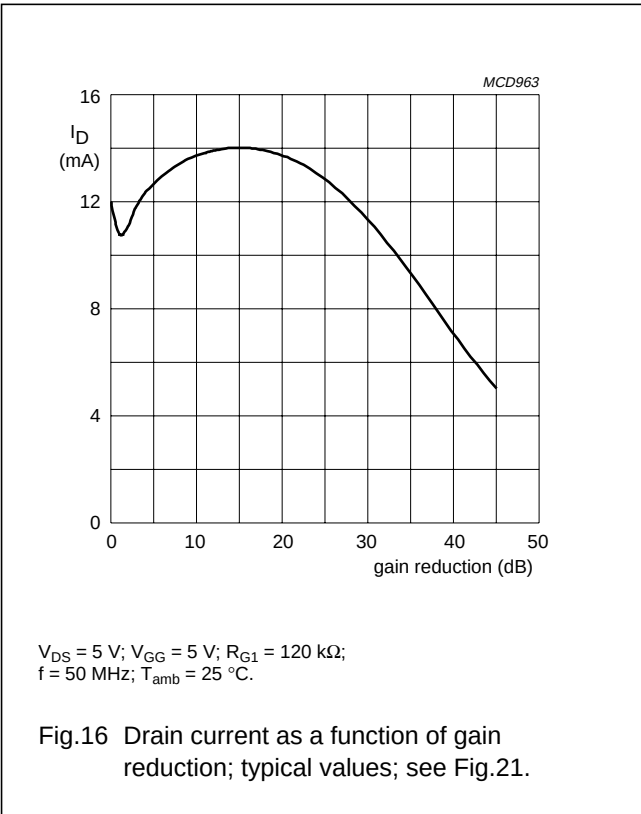


$V_{DS} = 5\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$.
 $R_{G1} = 120\text{ k}\Omega$ (connected to V_{GG}); see Fig.21.

Fig.12 Drain current as a function of gate 2 voltage; typical values.

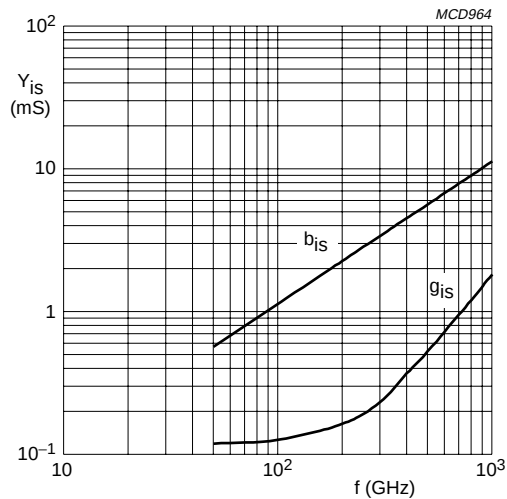
N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R;
BF1202WR



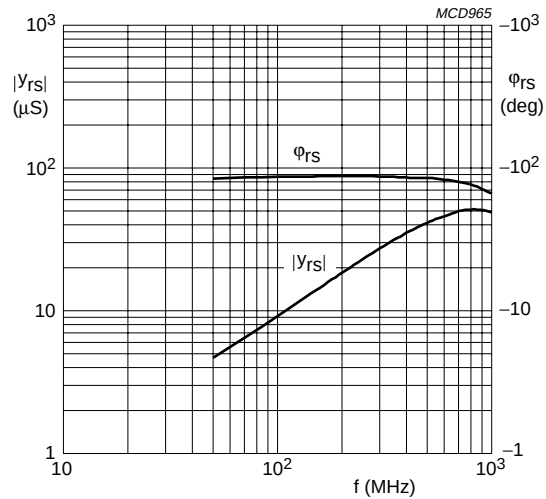
N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R;
BF1202WR



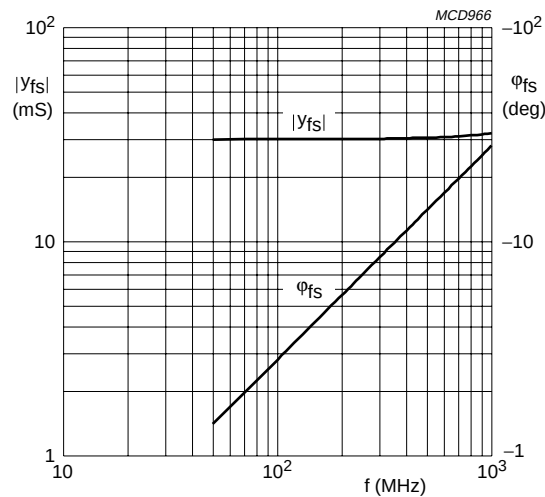
$V_{DS} = 5\text{ V}$; $V_{G2} = 4\text{ V}$.
 $I_D = 12\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.17 Input admittance as a function of frequency; typical values.



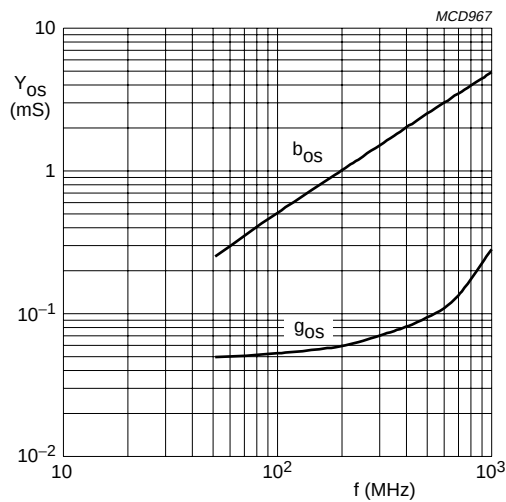
$V_{DS} = 5\text{ V}$; $V_{G2} = 4\text{ V}$.
 $I_D = 12\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.18 Reverse transfer admittance and phase as a function of frequency; typical values.



$V_{DS} = 5\text{ V}$; $V_{G2} = 4\text{ V}$.
 $I_D = 12\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.19 Forward transfer admittance and phase as a function of frequency; typical values.



$V_{DS} = 5\text{ V}$; $V_{G2} = 4\text{ V}$.
 $I_D = 12\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.20 Output admittance as a function of frequency; typical values.

N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R;
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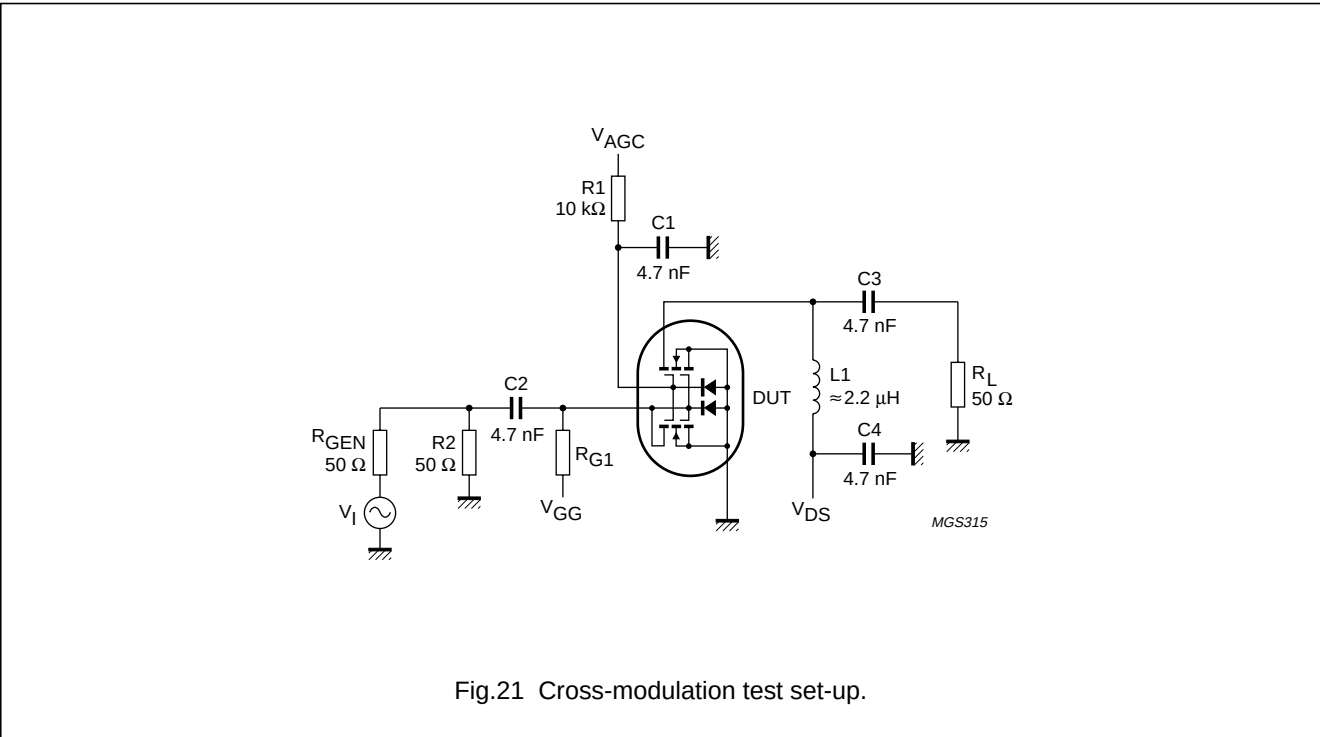


Table 1 Scattering parameters: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 12\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.988	−3.26	2.989	176.2	0.0005	92.6	0.995	−1.50
100	0.988	−6.52	3.017	172.5	0.0009	88.0	0.995	−3.01
200	0.984	−12.99	2.990	165.0	0.0018	82.5	0.994	−5.95
300	0.977	−19.39	2.949	157.6	0.0027	78.2	0.992	−8.86
400	0.965	−25.65	2.913	150.3	0.0036	75.4	0.990	−11.79
500	0.951	−31.76	2.853	143.2	0.0039	71.8	0.988	−14.65
600	0.936	−37.68	2.793	136.3	0.0042	69.9	0.986	−17.41
700	0.919	−43.42	2.727	129.5	0.0044	68.9	0.984	−20.10
800	0.903	−48.94	2.664	123.0	0.0043	68.5	0.980	−22.69
900	0.887	−54.25	2.593	116.7	0.0041	70.7	0.975	−25.27
1000	0.870	−59.34	2.518	110.5	0.0038	72.4	0.970	−27.90

Table 2 Noise data: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 12\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

f (MHz)	F _{min} (dB)	Γ _{opt}		R _n (Ω)
		(ratio)	(deg)	
400	0.9	0.805	28.5	50
800	1.1	0.725	47.2	40

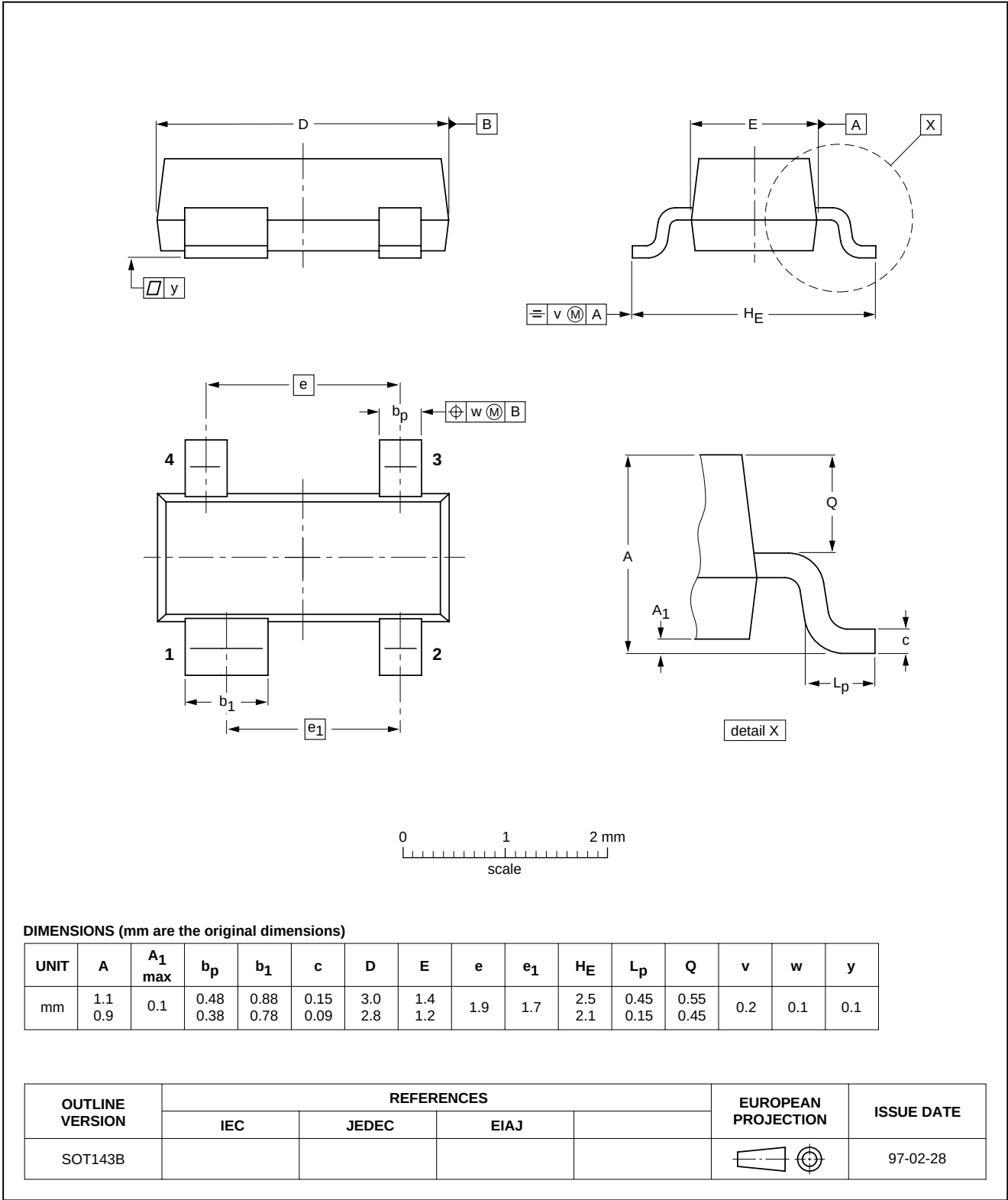
N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R;
BF1202WR

PACKAGE OUTLINES

Plastic surface mounted package; 4 leads

SOT143B

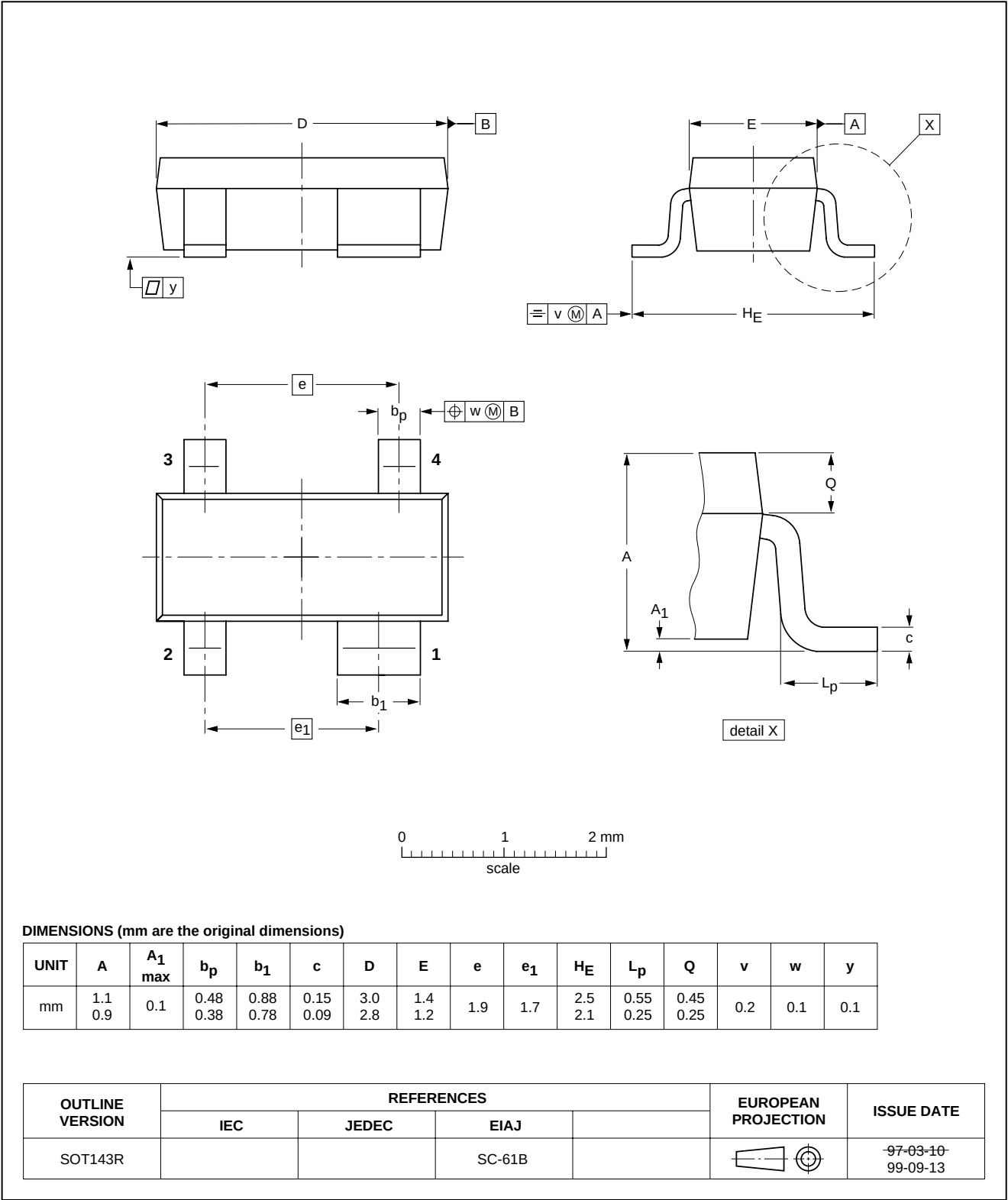


N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R;
BF1202WR

Plastic surface mounted package; reverse pinning; 4 leads

SOT143R

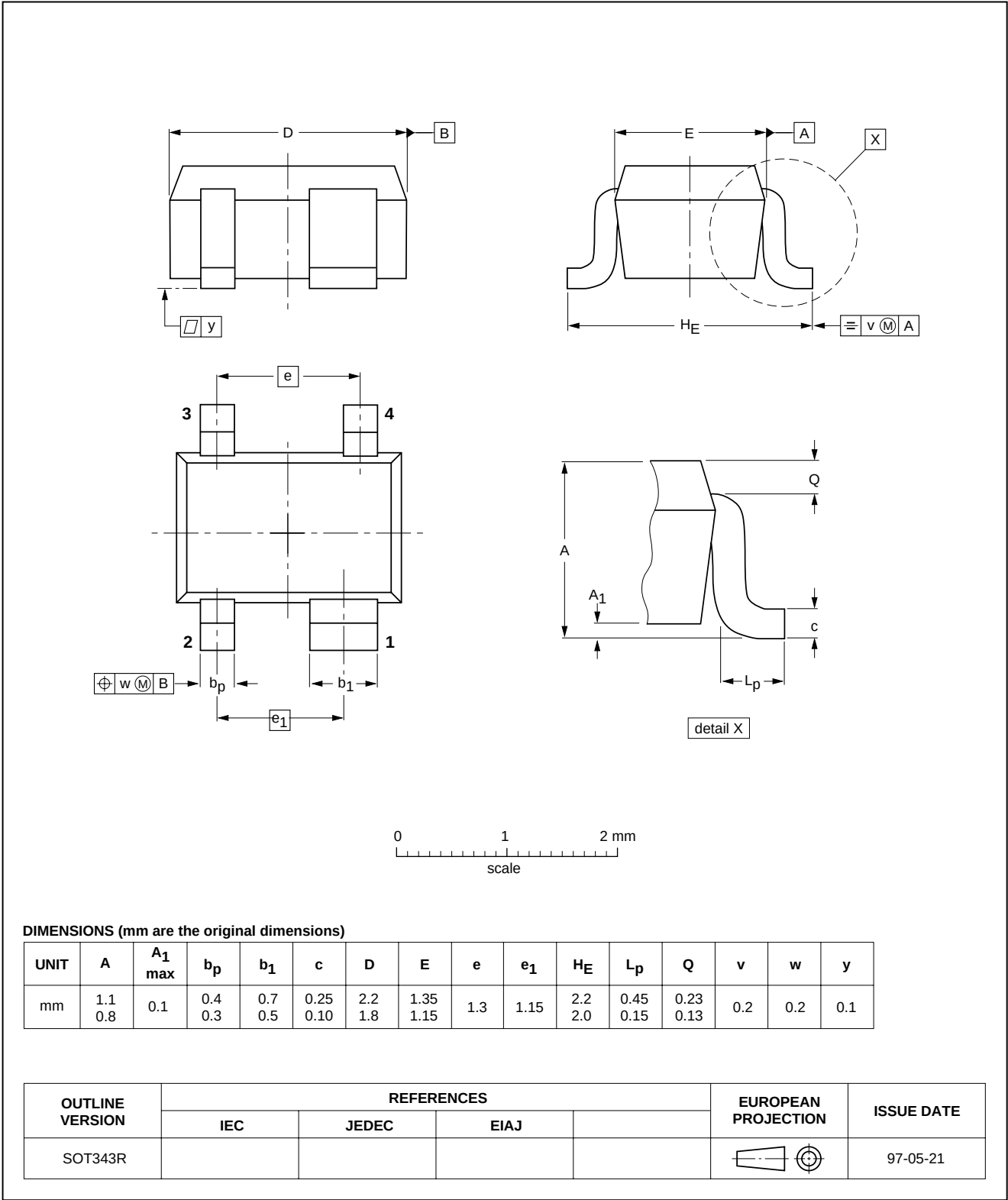


N-channel dual-gate PoLo MOS-FETs

BF1202; BF1202R;
BF1202WR

Plastic surface mounted package; reverse pinning; 4 leads

SOT343R



N-channel dual-gate PoLo MOS-FETs

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BF1202WR

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS ⁽¹⁾
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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NOTES

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BF1202; BF1202R;
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NOTES

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SCA 69

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