



STEVAL-TDR003V1

2-stage RF power amp: PD84001 + PD54008L-E + LPF
N-channel enhancement-mode lateral MOSFETs

Feature

- Excellent thermal stability
- Frequency: 135 - 175 MHz
- Supply voltage: 7.2 V
- Output power: 5 W
- Current < 1.5 A
- Input power < 10 dBm
- Harmonics level < -70 dBc
- Load mismatch 20:1
- V_{APC} 5 V max
- BeO free amplifier
- RoHS compliant

Description

The STEVAL-TDR003V1 is a 2-stage RF power amplifier including output low-pass filter (LPF) for harmonics rejection, specifically designed for portable two-way VHF radio communication.



Mechanical specification:

L = 40 mm, W = 20 mm

Table 1. Device summary

Order code
STEVAL-TDR003V1

Contents

1	Electrical data	3
1.1	Maximum ratings	3
2	Electrical characteristics	3
3	Typical performance	4
4	Circuit layout	9
5	Circuit schematics	10
6	Package mechanical data	12
6.1	PowerFLAT™ mechanical data	13
6.1.1	Mounting indications	15
6.2	Thermal pad and via design - SOT-89	16
6.2.1	Soldering profiles	17
7	Revision history	19

1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	15	V
I_D	Drain current	2.5	A
T_{CASE}	Operating case temperature	-20 to +85	°C
T_A	Max. ambient temperature	+55	°C

2 Electrical characteristics

$T_A = +25\text{ °C}$, $V_{DD} = 7.2\text{ V}$, V_{APC} adjusted

Table 3. Electrical specification

Symbol	Test conditions	Min	Typ	Max	Unit
Freq.	Frequency range	135		175	MHz
P_{IN}	@ $P_{OUT} = 5\text{ W}$	5		10	dBm
I_{TOTAL}	@ $P_{OUT} = 5\text{ W}$ and $P_{IN} = 8\text{ dBm}$			1.5	A
PAE	@ $P_{OUT} = 5\text{ W}$ and $P_{IN} = 8\text{ dBm}$	47% - 52%			
VAPC	@ $P_{OUT} = 5\text{ W}$ and $P_{IN} = 8\text{ dBm}$		4	5	V
Harmonics	@ $P_{OUT} = 5\text{ W}$			-70	dBc

3 Typical performance

Figure 1. Current vs frequency

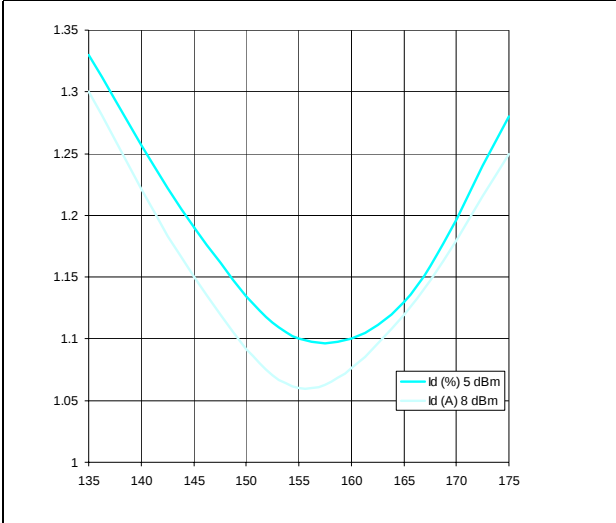


Figure 2. Efficiency vs frequency

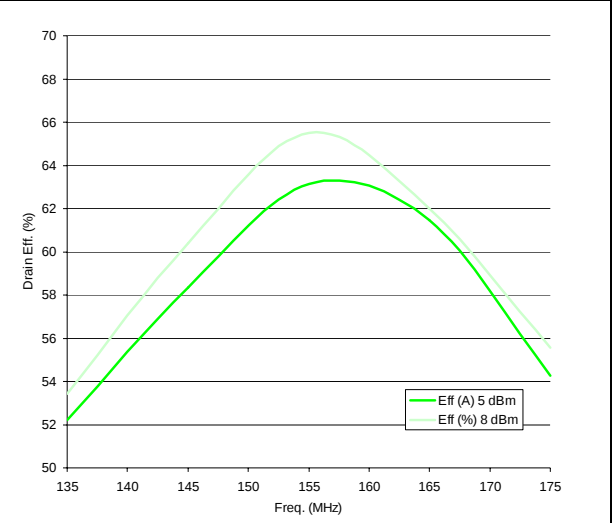


Figure 3. Gain vs frequency

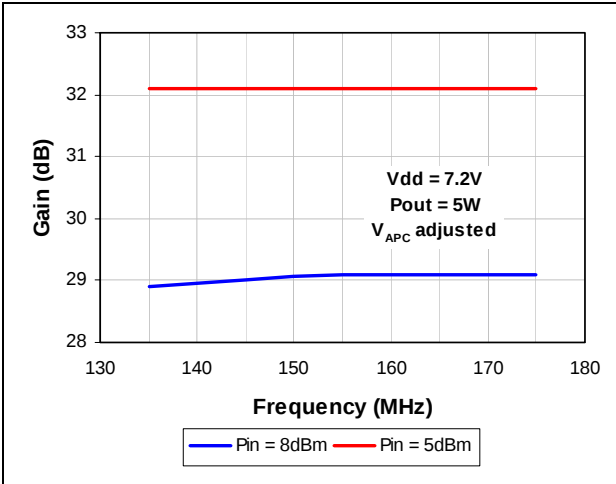


Figure 4. Gain vs input power

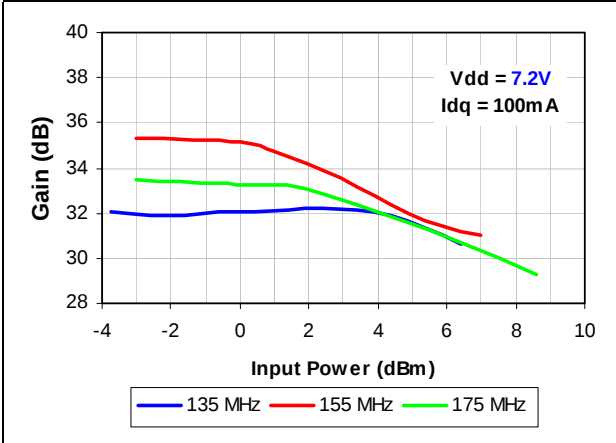


Figure 5. Gain vs input power

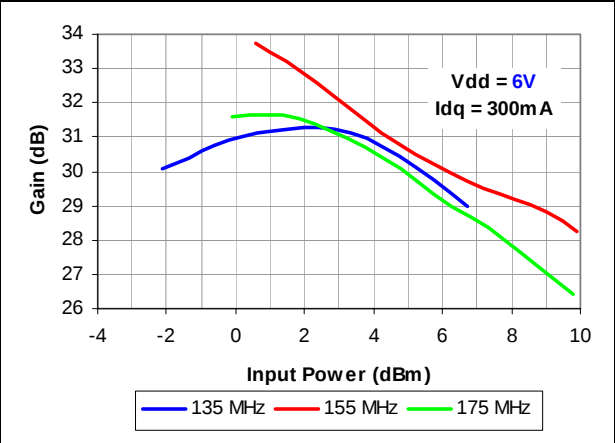


Figure 6. Gain vs input power

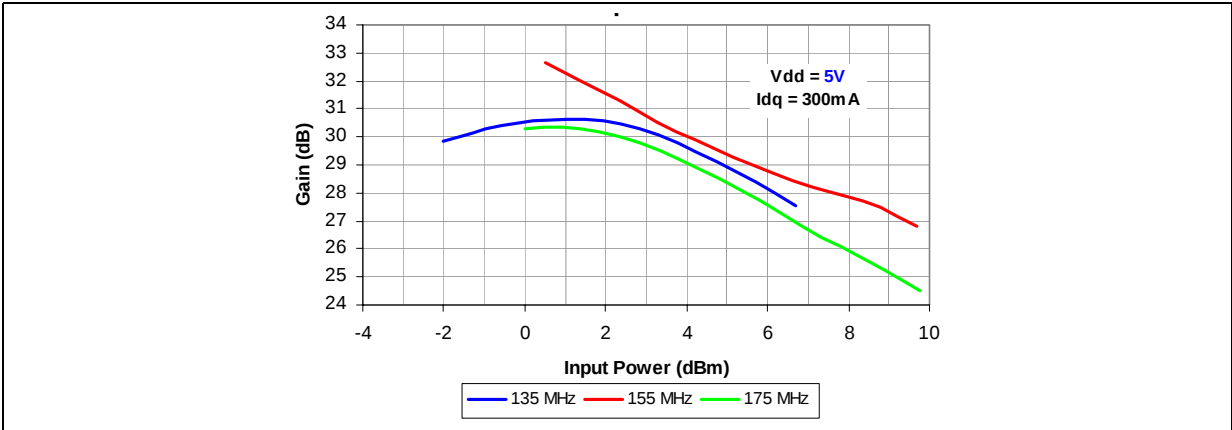


Figure 7. Drain current vs output power

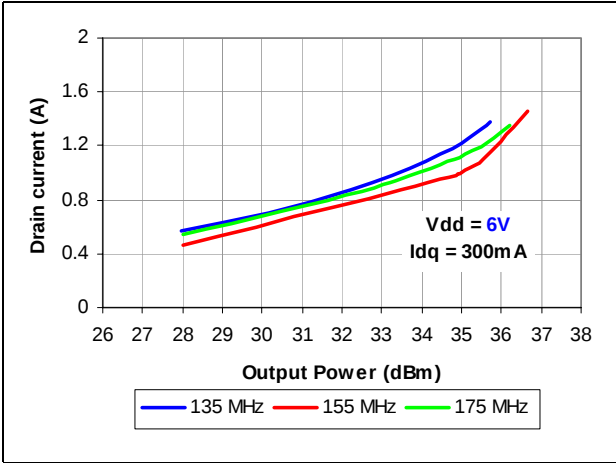


Figure 8. Drain current vs output power

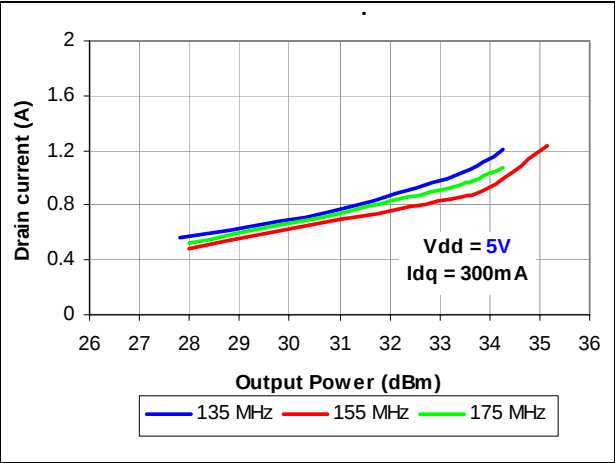


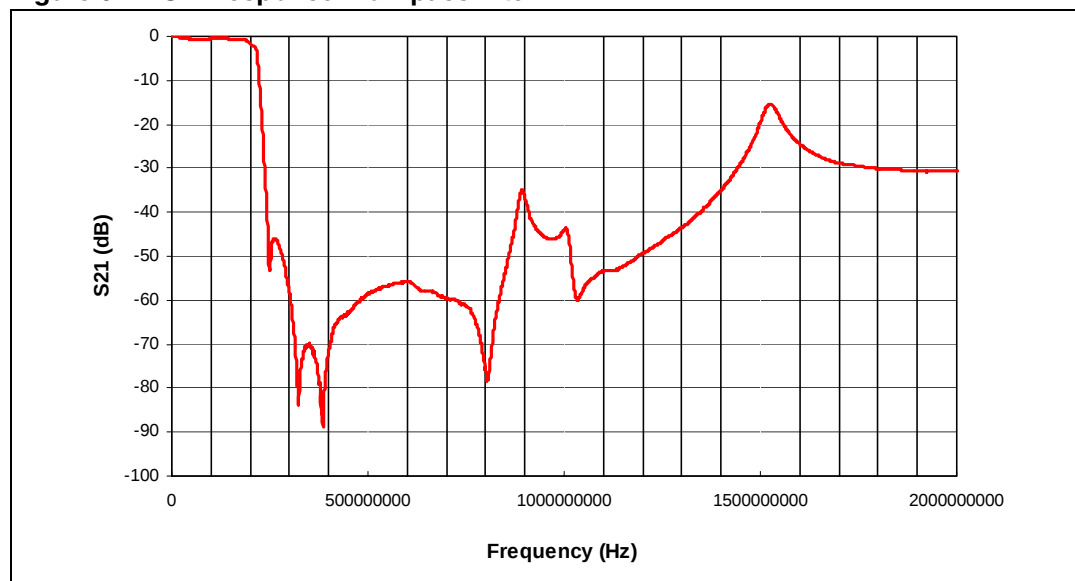
Figure 9. S21 response - low pass filter

Table 4. Component list

Designator	Manufacturer	Size	Value	Comment	Part number
C1, C5, C16	Murata	0603	nc	Capacitor	
C6	Murata	0603	1 μ F	Capacitor	
C1F	Murata	0603	3.3 pF	Capacitor	GRM1885C1H3R3CZ01
C2, C3, C4, C7, C8, C9, C10	Murata	0603	330 pF	Capacitor	GRM1885C1H391JA01
C2F	Murata	0603	18 pF	Capacitor	GRM1885C1H180JA01
C3F	Murata	0603	12 pF	Capacitor	GRM1885C1H120JA01
C4F, C6F	Murata	0603	22 pF	Capacitor	GRM1885C1H220JA01
C5F, C12	Murata	0603	27 pF	Capacitor	GRM1885C1H270JA01
C7F	Murata	0603	15 pF	Capacitor	GRM1885C1H150JA01
C11	Murata	0603	56 pF	Capacitor	GRM1885C1H560JA01
C13	Murata	0603	33 pF	Capacitor	GRM1885C1H330JA01
C14	Murata	0603	100 pF	Capacitor	GRM1885C1H101JA01
C15	Murata	0603	39 pF	Capacitor	GRM1885C1H390JA01
DC-CON1	Phoenix contact	2.54 mm, 5 pole		DC connector	1725685
L1	Coilcraft	1812	24 nH	Inductor	1812SMS-33NJ
L1F	Coilcraft	1008	39 nH	Inductor	1008CS-390NX_BW
L2	Coilcraft	1812	33 nH	Inductor	1812SMS-33NJ
L2F	Coilcraft	1008	22 nH	Inductor	1008CS-220NX_BW
L3	Coilcraft	1812	35.5 nH	Inductor	1812SMS-22NJ
L3F	Coilcraft	1008	27 nH	Inductor	1008CS-270NX_BW
L4	Coilcraft	0603	18 nH	Inductor	0603HC-18NX_BW
L5	Coilcraft	Minispring A	18.5 nH	Inductor	A05T
PD54008L-E	STMicroelectronics	QFN 5x5		RF power transistor	PD54008L-E
PD84001	STMicroelectronics	SOT89		RF power transistor	PD84001
R1, R4	Tyco Electronics / Neohm	0603	62 k Ω	Resistor	CRG series thick film
R2	Tyco Electronics / Neohm	0603	430 k Ω	Resistor	
R3	Tyco Electronics / Neohm	0603	240 Ω	Resistor	
R5	Tyco Electronics / Neohm	0603	150 k Ω	Resistor	
R6	Tyco Electronics / Neohm	0603	11 Ω	Resistor	

Table 4. Component list (continued)

Designator	Manufacturer	Size	Value	Comment	Part number
RF IN, RF OUT amplifier, RF OUT filter	Johnson			SMA	142-0701-801
Substrate		H = 20 mil h = 2 oz		Substrate	FR-4
TL1		W = 0.9 2mm L = 3 mm	Z = 50 Ω	Transmission line	
TL2		W = 0.92 mm L = 7.2 mm	Z = 50 Ω		
TL3		W = 0.92 mm L = 6.2 3mm	Z = 50 Ω		
TL4		W = 0.92 mm L = 6.62 mm	Z = 50 Ω		
TL5		W = 0.92 mm L = 5.8 mm	Z = 50 Ω		
TL6		W = 0.92 mm L = 2.2 mm	Z = 50 Ω		
TL7		W = 0.92 mm L = 11 mm	Z = 50 Ω		
TL8		W = 0.92 mm L = 12.4 mm	Z = 50 Ω		
TL9		W = 0.92 mm L = 2 mm	Z = 50 Ω		

4 Circuit layout

Figure 10. Test fixture component layout

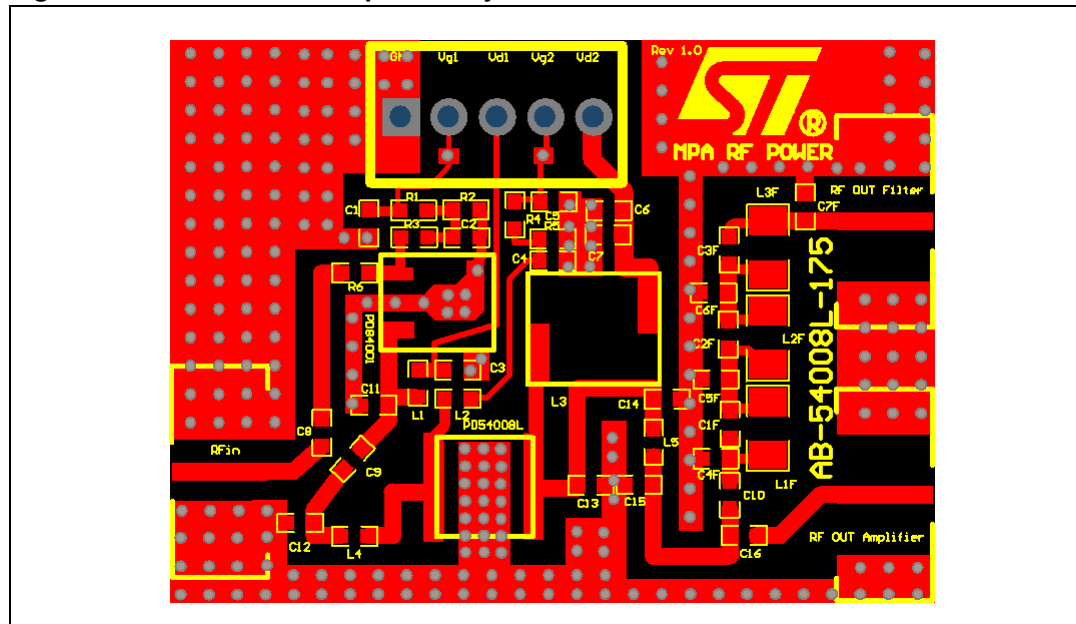
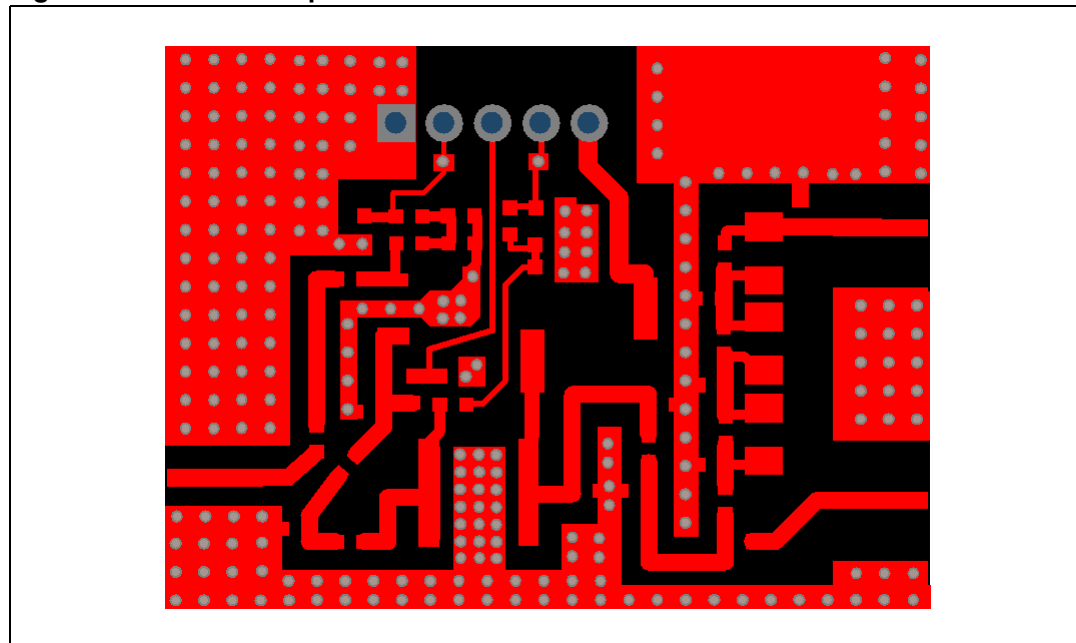


Figure 11. Test circuit photomaster



5 Circuit schematics

Figure 12. Circuit schematic

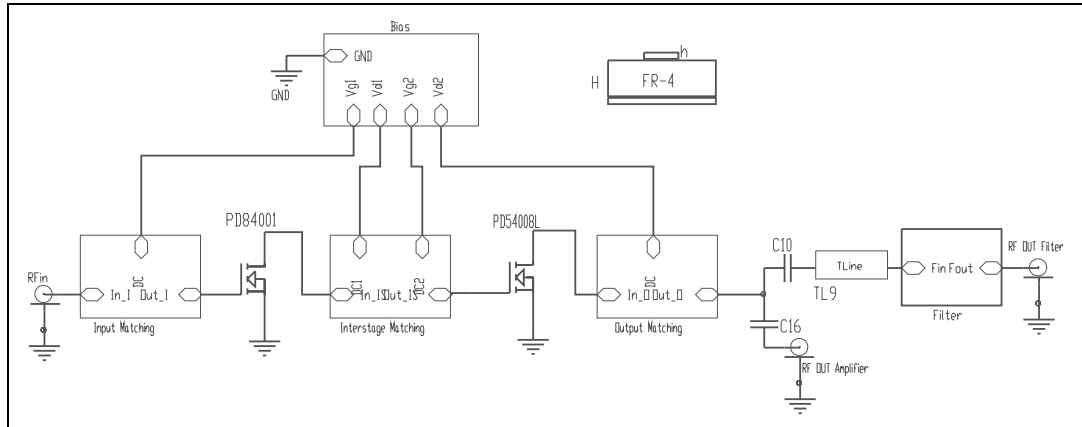


Figure 13. Bias schematic

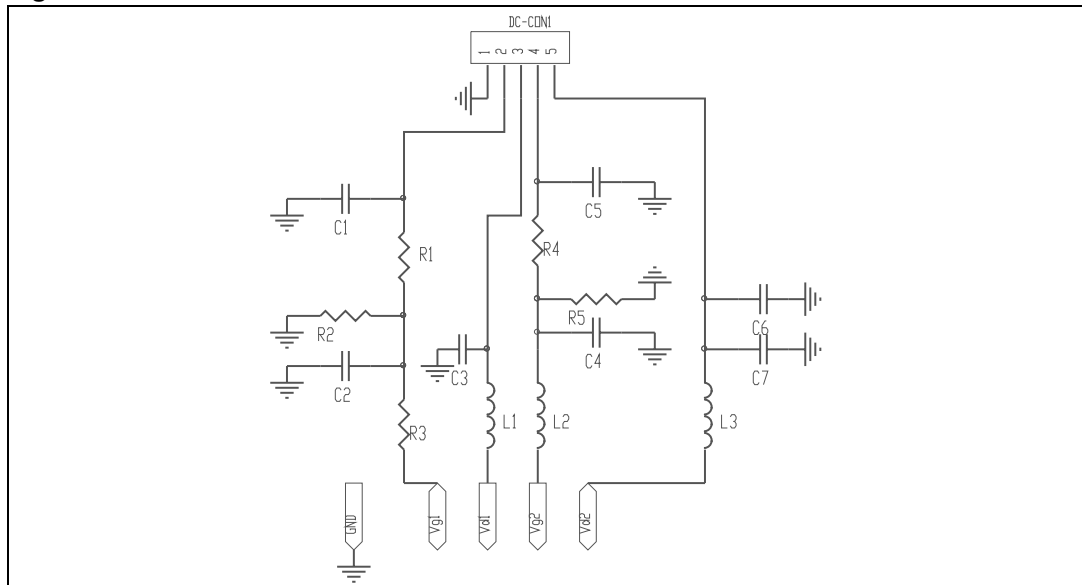


Figure 14. Filter schematic

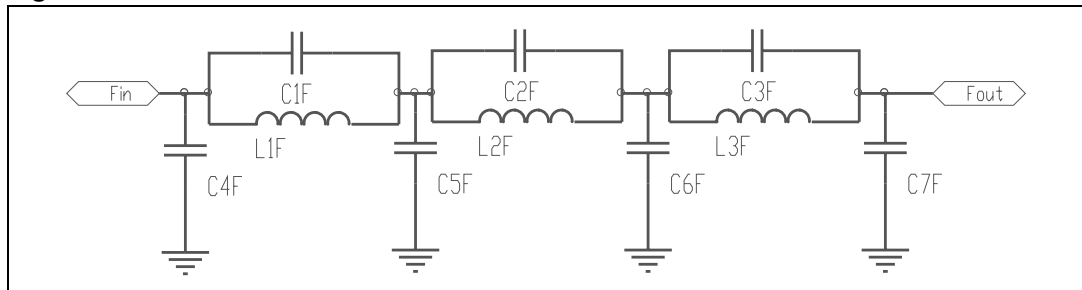


Figure 15. Input matching schematic

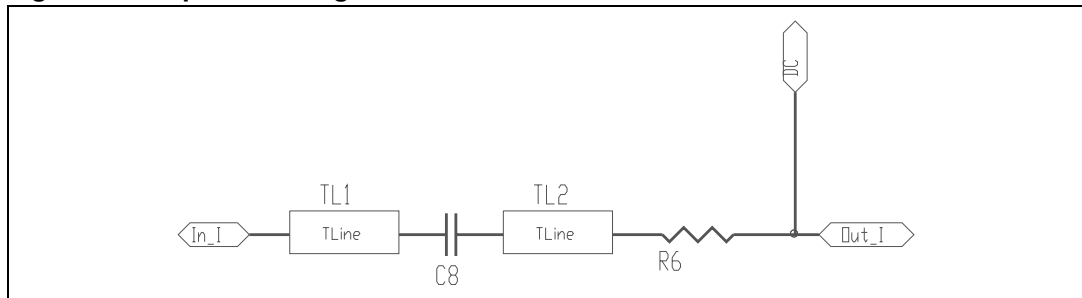


Figure 16. Inter matching schematic

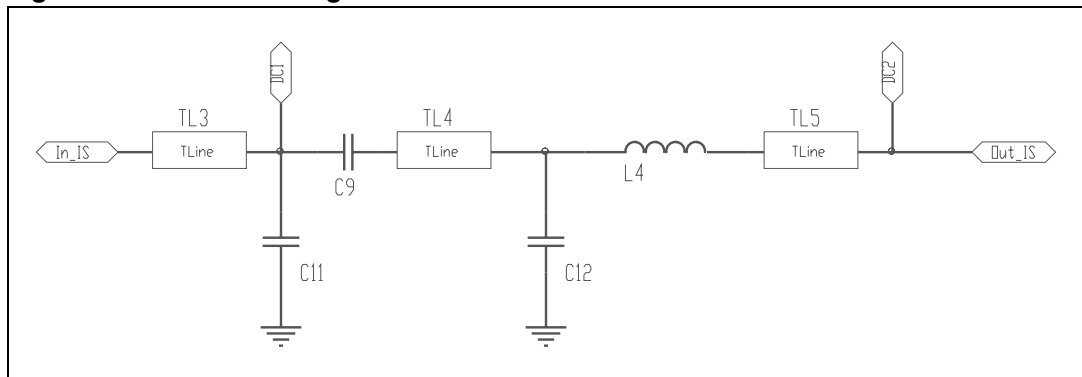
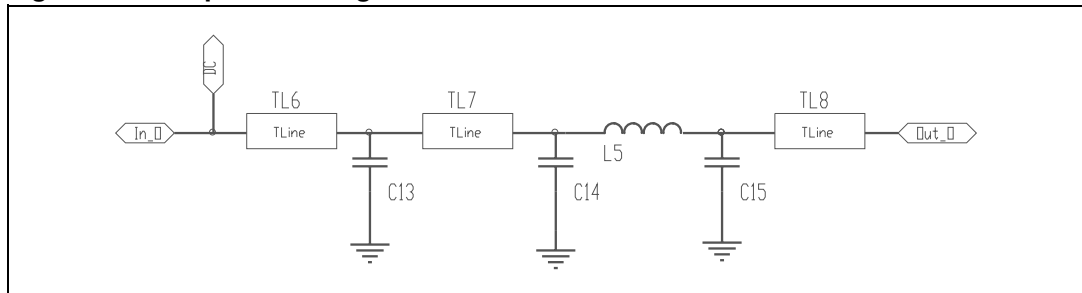


Figure 17. Output matching schematic



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 PowerFLAT™ mechanical data

Table 5. PowerFLAT™ mechanical data

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.24			0.009	
AA	0.15	0.25	0.35	0.006	0.01	0.014
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.64	0.71	0.79	0.025	0.028	0.031
D		5.00			0.197	
d		0.30			0.011	
E		5.00			0.197	
E2	2.49	2.57	2.64	0.098	0.101	0.104
e		1.27			0.050	
f		3.37			0.132	
g		0.74			0.03	
h		0.21			0.008	

Figure 18. PowerFLAT™ package dimensions

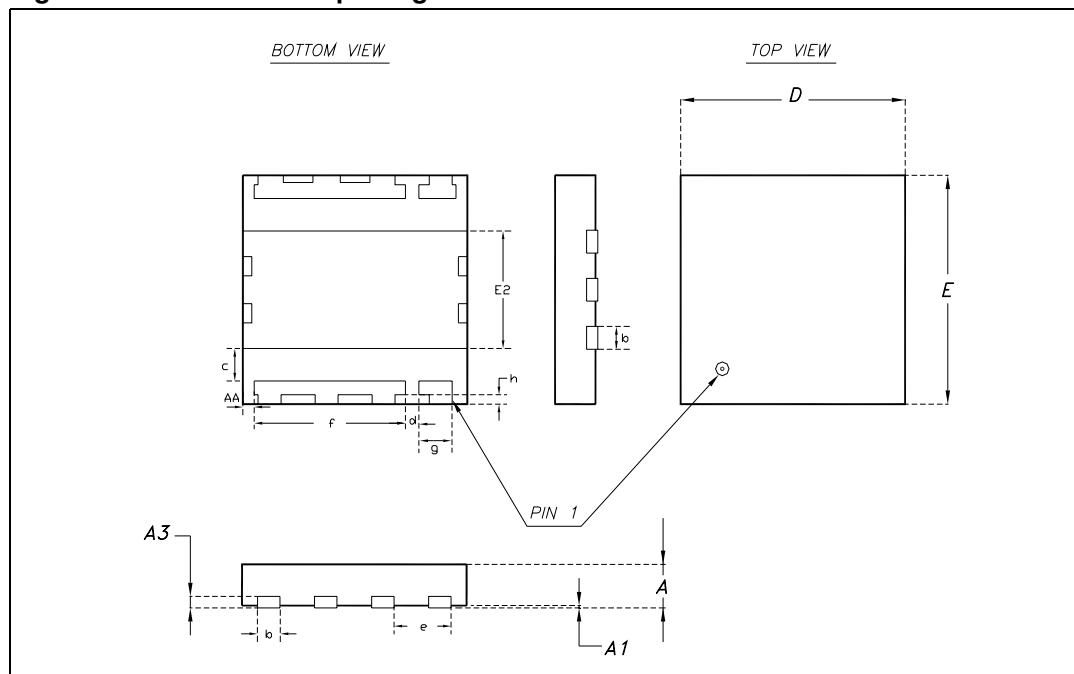
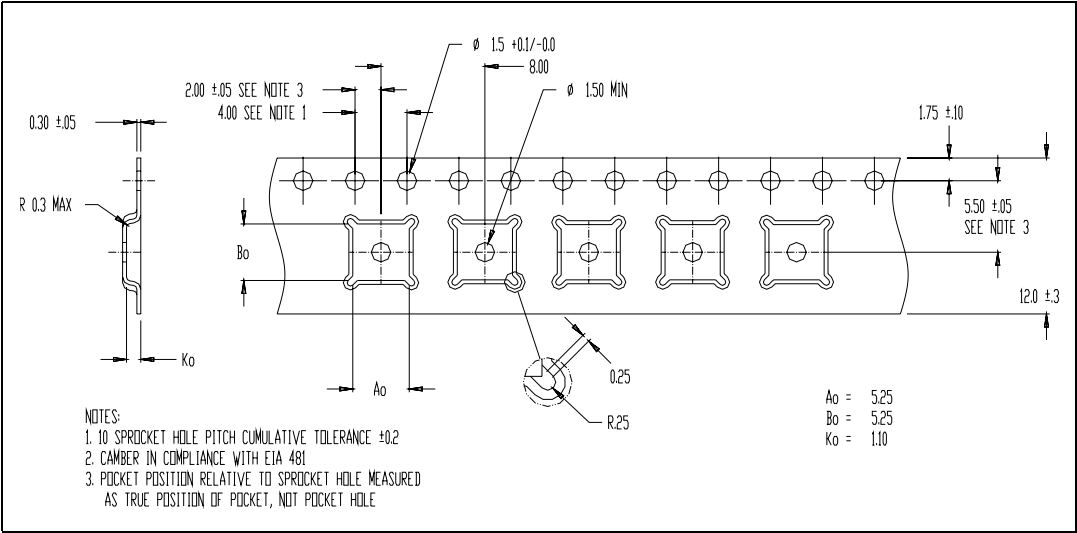


Table 6. PowerFLAT™ tape and reel dimensions

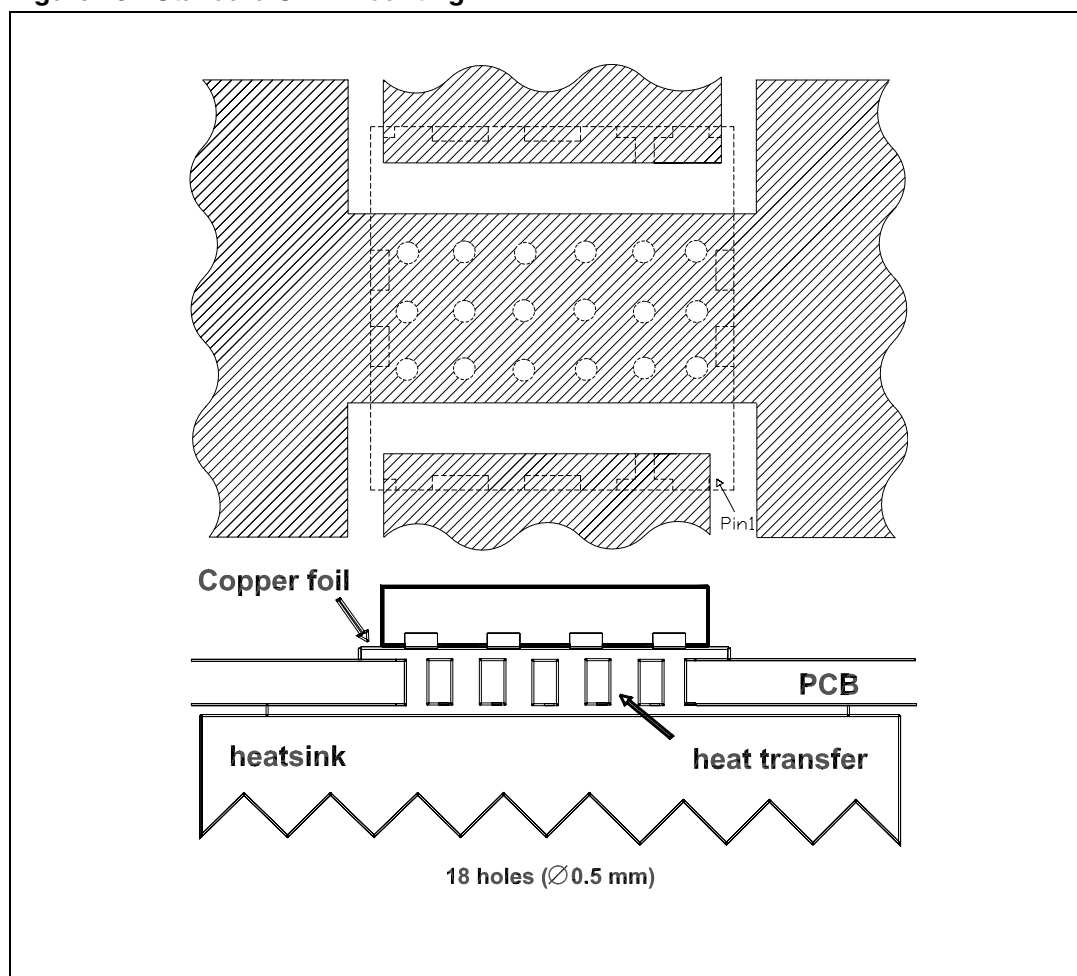
Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
Ao	5.15	5.25	5.35	0.12	0.13	0.13
Bo	5.15	5.25	5.35	0.12	0.13	0.13
Ko	1.0	1.1	1.2	0.02	0.02	0.02

Figure 19. PowerFLAT™ tape and reel



6.1.1 Mounting indications

Figure 20. Standard SMD mounting

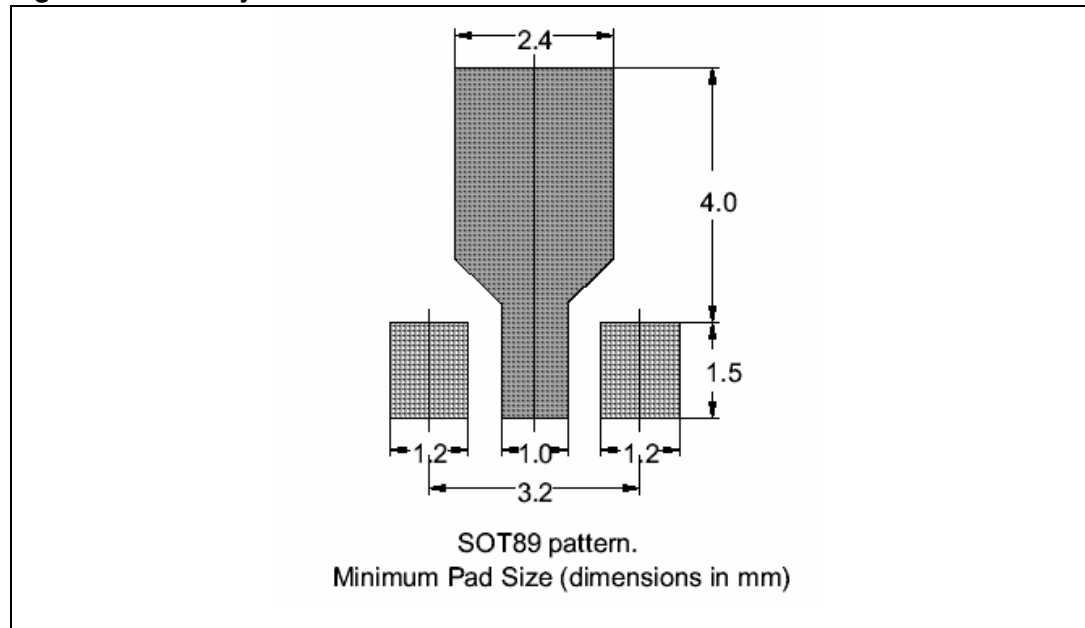


6.2 Thermal pad and via design - SOT-89

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address the thermal, power dissipation and electrical requirements of the device.

The via pattern is based on through-hole vias with 0.203 mm to 0.330 mm finished hole size on a 0.5 mm to 1.2 mm grid pattern with 0.025 plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

Figure 21. Pad layout details



6.2.1 Soldering profiles

Figure 22 shows the recommended solder profile for devices that have lead-free terminal plating and where a lead-free solder is used.

Figure 22. Recommended solder profile - lead-free

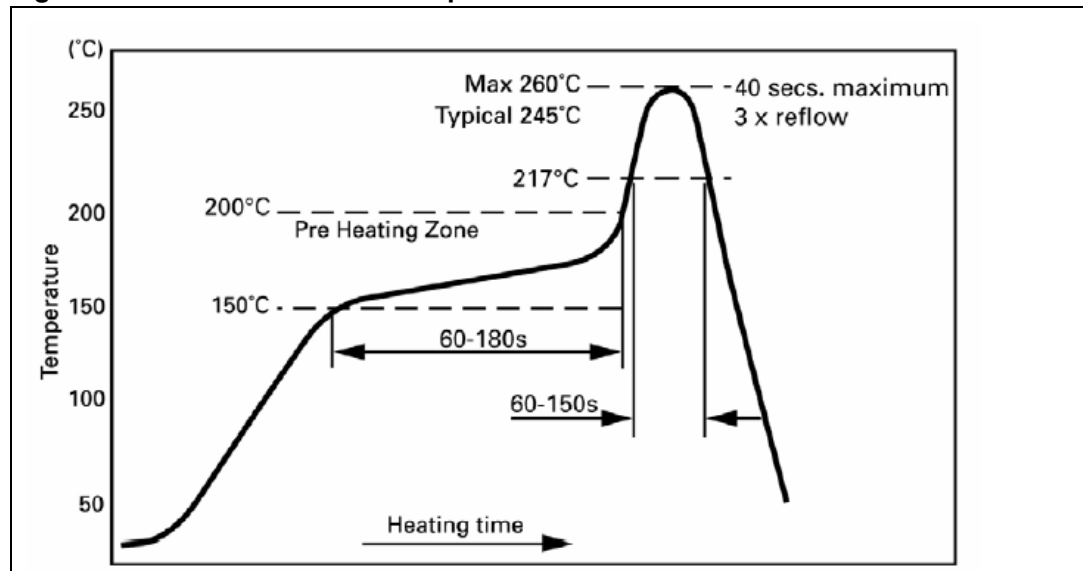


Figure 23 gives the recommended solder profile for devices with lead-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with leaded solder.

Figure 23. Recommended solder profile - leaded

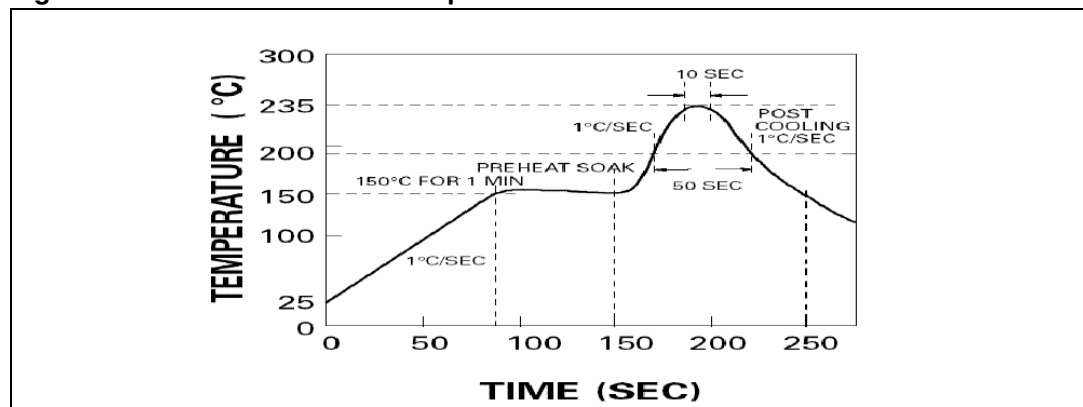
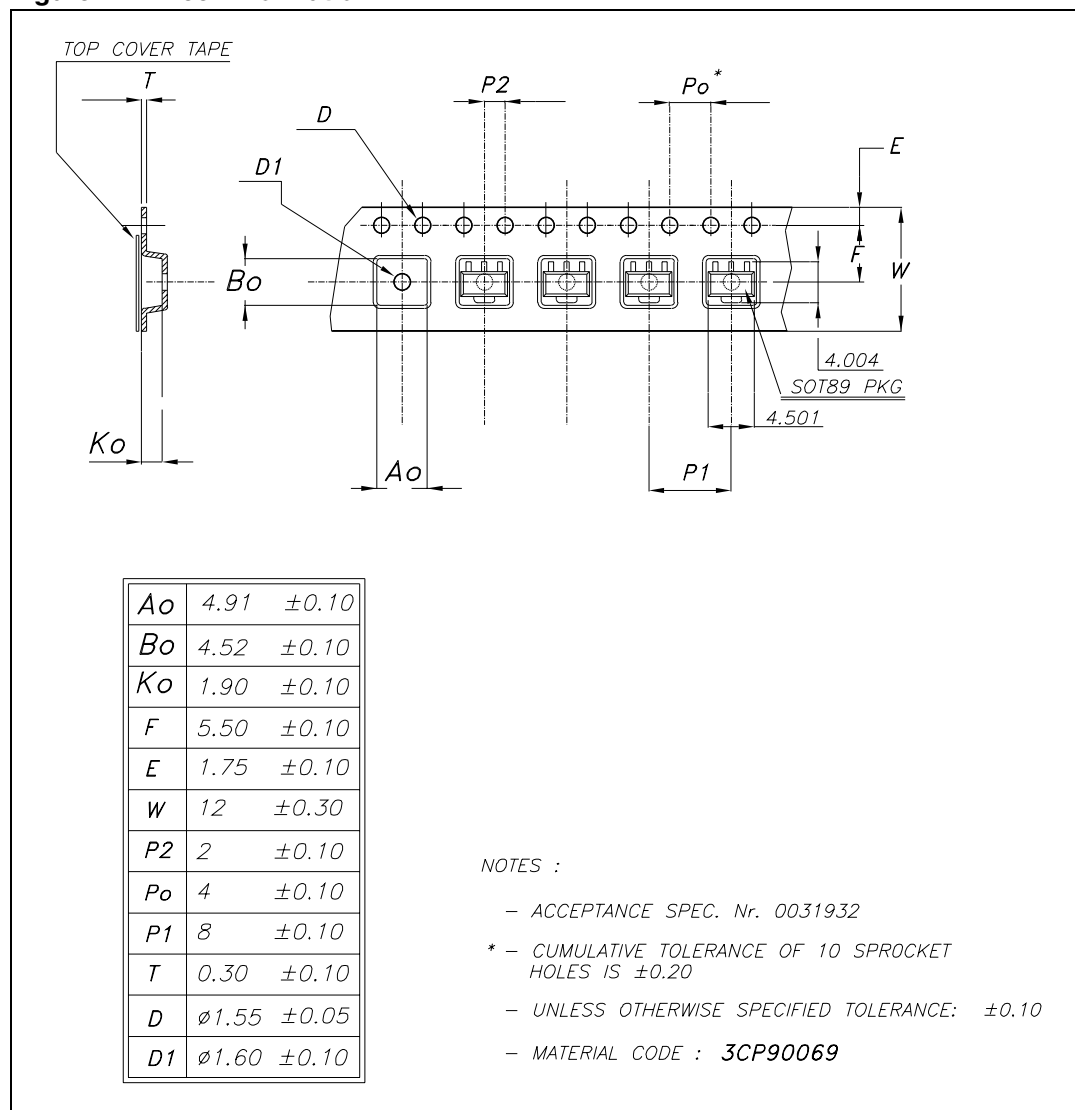


Figure 24. Reel information



7 Revision history

Table 7. Document revision history

Date	Revision	Changes
31-Mar-2010	1	Initial release.

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