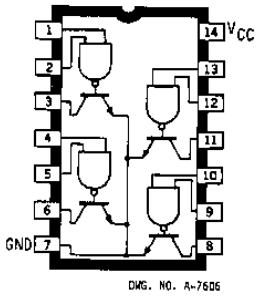
SERIES UHP-400, UHP-400-1, AND UHP-500 POWER AND RELAY DRIVERS

FEATURES

- Inputs Compatible with DTL/TTL
- 500 mA Output Current-Sink Capability
- Pinning Compatible with 54/74 Logic Series
- Transient-Protected Outputs on Relay Drivers
- High-Voltage Output:
  - 100 V Series UHP-500
  - 70 V Series UHP-400-1
  - 40 V Series UHP-400

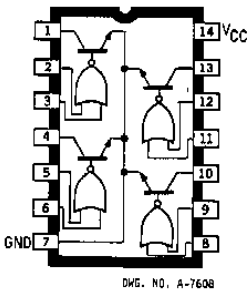
SERIES UHP-400, UHP-400-1, and UHP-500 power and relay drivers are bipolar integrated circuits with logic and high-current switching transistors on the same chip. Each output transistor is capable of sinking 500 mA in the ON state.

UHP Part Numbers			Function
400	400-1	500	Quad 2-Input AND
402	402-1	502	Quad 2-Input OR
403	403-1	503	Quad OR for Inductive Loads
406	406-1	506	Quad AND for Inductive Loads
407	407-1	507	Quad NAND for Inductive Loads
408	408-1	508	Quad 2-Input NAND
432	432-1	532	Quad 2-Input NOR
433	433-1	533	Quad NOR for Inductive Loads



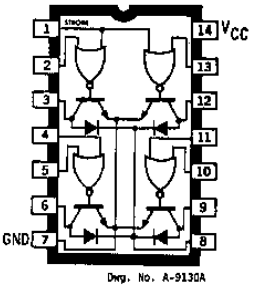
DWG. NO. A-7606

UHP-400
UHP-400-1
UHP-500



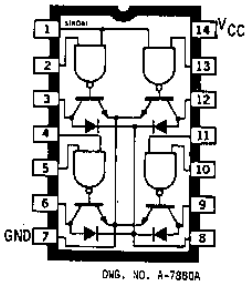
DWG. NO. A-7608

UHP-402
UHP-402-1
UHP-502



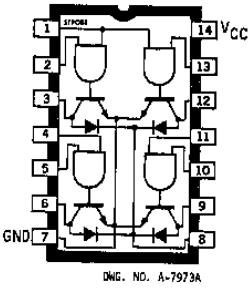
Dwg. No. A-9130A

UHP-403
UHP-403-1
UHP-503



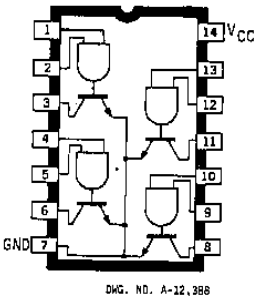
DWG. NO. A-7380A

UHP-406
UHP-406-1
UHP-506



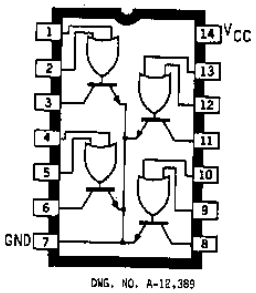
DWG. NO. A-7973A

UHP-407
UHP-407-1
UHP-507



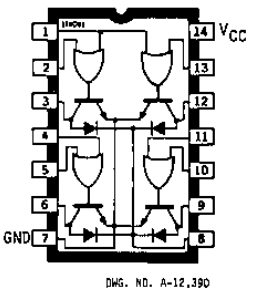
DWG. NO. A-12,388

UHP-408
UHP-408-1
UHP-508



DWG. NO. A-12,389

UHP-432
UHP-432-1
UHP-532



DWG. NO. A-12,390

UHP-433
UHP-433-1
UHP-533

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . 7 V
Input Voltage, V_{IN} . . . . . 5.5 V
Output Off-State Voltage, V_{OFF}
  Series UHP-400 . . . . . 40 V
  Series UHP-400-1 . . . . . 70 V
  Series UHP-500 . . . . . 100 V
Output On-State Sink Current, I_{ON} (one driver) . . . . . 500 mA
  (total package) . . . . . 1 A
Suppression Diode Off-State Voltage, V_R
  Series UHP-400 . . . . . 40 V
  Series UHP-400-1 . . . . . 70 V
  Series UHP-500 . . . . . 100 V
Suppression Diode On-State Current, I_F . . . . . 500 mA
Operating Free-Air Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into Any Output (ON State)	—	—	250	mA

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

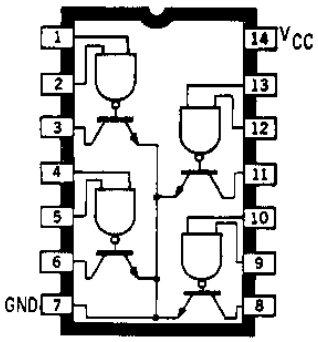
Characteristic	Series	Test Conditions (Note 3)	Limits			
			Min.	Typ.	Max.	Units
Turn-On Delay Time (t_{pdo})	UHP-400	V_S = 40 V, R_L = 265Ω (6 W)	—	200	500	ns
	UHP-400-1	V_S = 70 V, R_L = 465Ω (10 W)	—	200	500	ns
	UHP-500	V_S = 100 V, R_L = 670Ω (15 W)	—	200	500	ns
Turn-Off Delay Time (t_{pd1})	UHP-400	V_S = 40 V, R_L = 265Ω (6 W)	—	300	750	ns
	UHP-400-1	V_S = 70 V, R_L = 465Ω (10 W)	—	300	750	ns
	UHP-500	V_S = 100 V, R_L = 670Ω (15 W)	—	300	750	ns

NOTES:
1. Each input tested separately.
2. Voltage values shown in the test-circuit waveforms are with respect to network ground terminal.
3. C_L = 15 pF. Capacitance value specified includes probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0 V	t_f = 7.0 ns	t_p = 1.0 μs
$V_{in(1)}$ = 3.5 V	t_r = 14 ns	PRR = 500 kHz

UHP-400, UHP-400-1, and UHP-500
Quad 2-Input AND Power Drivers

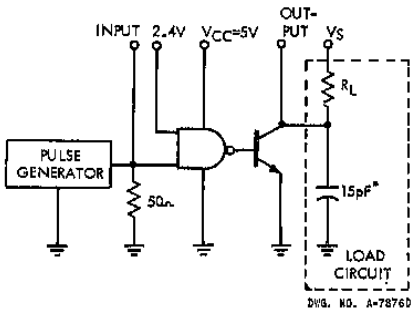


DWG. NO. A-7506

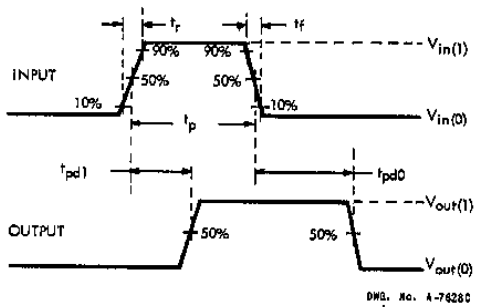
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-400	Min.	2.0 V	2.0 V	40 V	—	—	50	μA
		UHP-400-1	Min.	2.0 V	2.0 V	70 V	—	—	50	μA
		UHP-500	Min.	2.0 V	2.0 V	100 V	—	—	50	μA
Output Voltage	$V_{CE(SAT)}$	All	Min.	0.8 V	4.75 V	150 mA	—	—	0.5	V
			Min.	0.8 V	4.75 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	5.0 V	5.0 V	—	—	4.0	6.0	mA
	$I_{CC(0)}$	All	Max.	0 V	0 V	—	—	17.5	24.5	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at V_{CC} = 5.0 V.
2. Each gate.
3. Each input tested separately.
4. T_A = +25°C.



DWG. NO. A-7876D

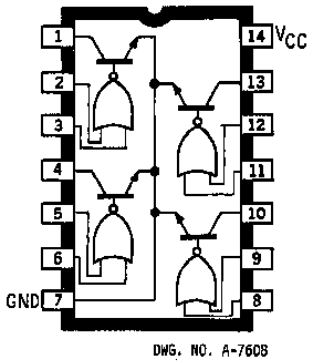


DWG. No. A-7628C

*Includes probe and test fixture capacitance.

UHP-402, UHP-402-1, and UHP-502

Quad 2-Input OR Power Drivers

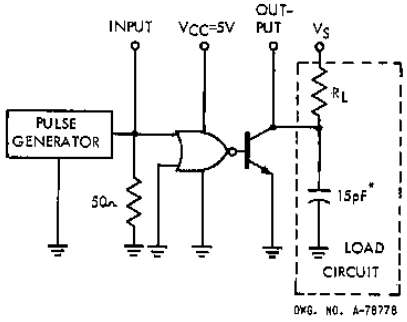


DWG. NO. A-7608

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

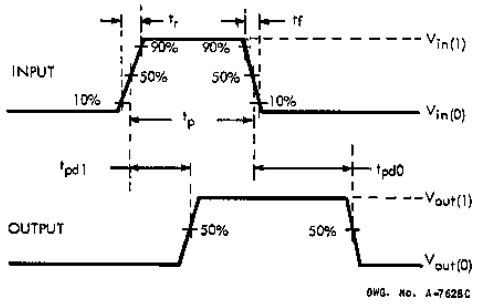
Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-402	Min.	2.0 V	0 V	40 V	—	—	50	μA
		UHP-402-1	Min.	2.0 V	0 V	70 V	—	—	50	μA
		UHP-502	Min.	2.0 V	0 V	100 V	—	—	50	μA
Output Voltage	$V_{CE(SAT)}$	All	Min.	0.8 V	0.8 V	150 mA	—	—	0.5	V
			Min.	0.8 V	0.8 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	5.0 V	5.0 V	—	—	4.1	6.3	mA
	$I_{CC(0)}$	All	Max.	0 V	0 V	—	—	18	25	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at V_{CC} = 5.0 V.
2. Each gate.
3. Each input tested separately.
4. T_A = +25°C.



DWG. NO. A-7877B

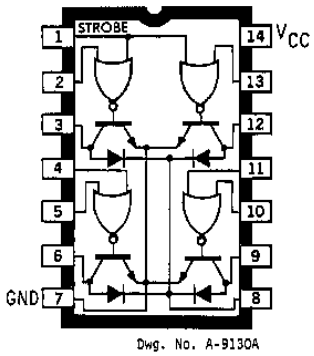
*Includes probe and test fixture capacitance.



DWG. No. A-7628C

UHP-403, UHP-403-1, and UHP-503

Quad OR Relay Drivers

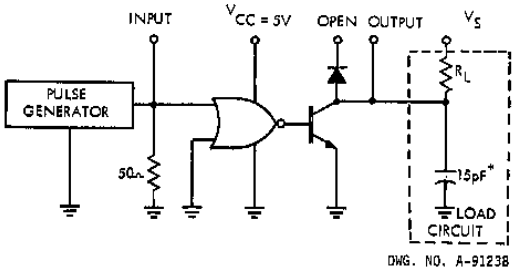


Dwg. No. A-9130A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

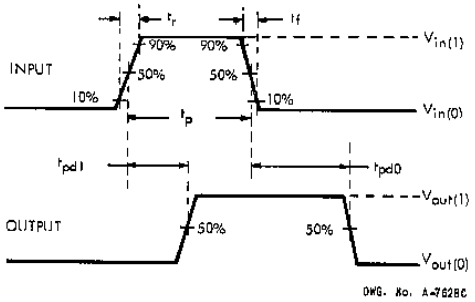
Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-403	Min.	2.0 V	0 V	40 V	—	—	100	μA
		UHP-403-1	Min.	2.0 V	0 V	70 V	—	—	100	μA
		UHP-503	Min.	2.0 V	0 V	100 V	—	—	100	μA
Diode Leakage Current (Note 5)	I_R	All	Nom.	0 V	0 V	Open	—	—	200	μA
Diode Forward Voltage Drop (Note 6)	V_F	All	Nom.	5.0 V	5.0 V	—	—	1.5	1.75	V
Output Voltage	$V_{CE(SAT)}$	All	Min.	0.8 V	0.8 V	150 mA	—	—	0.5	V
			Min.	0.8 V	0.8 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	5.0 V	5.0 V	—	—	4.1	6.3	mA
	$I_{CC(0)}$	All	Max.	0 V	0 V	—	—	18	25	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Max.	—	—	—	—	—	0.8	V
Input Current at All Inputs Except Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA
Input Current at Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−1.1	−1.6	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	100	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at V_{CC} = 5.0 V.
2. Each gate.
3. Each input tested separately.
4. T_A = +25°C.
5. Diode leakage current measured at $V_R = V_{OFF(MIN)}$.
6. Diode forward voltage drop measured at I_F = 200 mA.



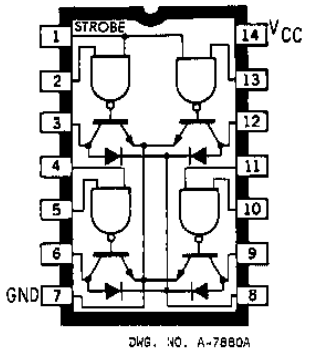
DWG. NO. A-9123B

*Includes probe and test fixture capacitance.



DWG. No. A-7628C

UHP-406, UHP-406-1, and UHP-506
Quad AND Relay Drivers

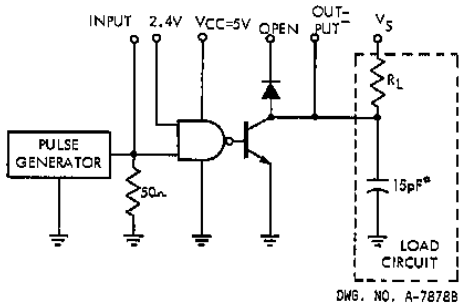


DWG. NO. A-7880A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

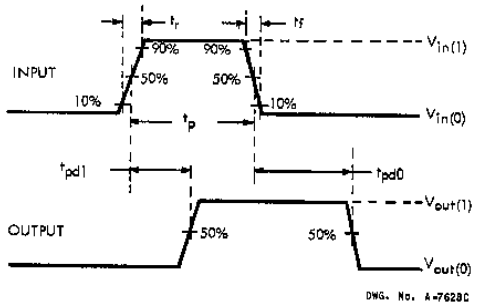
Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-406	Min.	2.0 V	2.0 V	40 V	—	—	100	µA
		UHP-406-1	Min.	2.0 V	2.0 V	70 V	—	—	100	µA
		UHP-506	Min.	2.0 V	2.0 V	100 V	—	—	100	µA
Diode Leakage Current (Note 5)	I_R	All	Nom.	0 V	0 V	Open	—	—	200	µA
Diode Forward Voltage Drop (Note 6)	V_F	All	Nom.	5.0 V	5.0 V	—	—	1.5	1.75	V
Output Voltage	$V_{CE(SAT)}$	All	Min.	0.8 V	4.75 V	150 mA	—	—	0.5	V
			Min.	0.8 V	4.75 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	5.0 V	5.0 V	—	—	4.0	6.0	mA
	$I_{CC(0)}$	All	Max.	0 V	0 V	—	—	17.5	24.5	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current at All Inputs Except Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	µA
			Max.	5.5 V	0 V	—	—	—	1.0	mA
Input Current at Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−1.1	−1.6	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	100	µA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at V_{CC} = 5.0 V.
2. Each gate.
3. Each input tested separately.
4. T_A = +25°C.
5. Diode leakage current measured at $V_R = V_{OFF(MIN)}$.
6. Diode forward voltage drop measured at I_F = 200 mA.



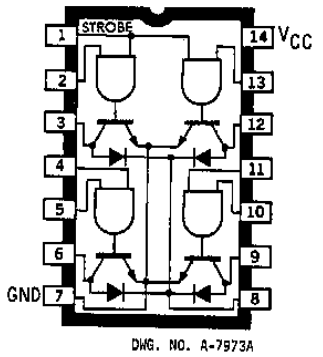
DWG. NO. A-7878B

*Includes probe and test fixture capacitance.



DWG. No. A-7628C

UHP-407, UHP-407-1, and UHP-507
Quad NAND Relay Drivers

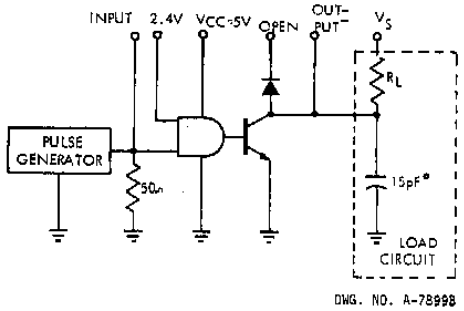


DWG. NO. A-7973A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

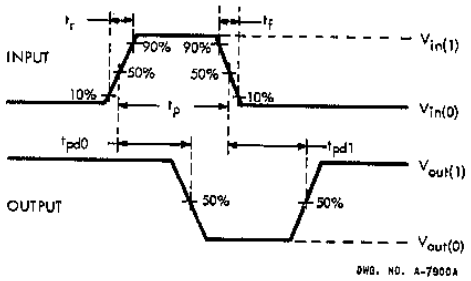
Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-407	Min.	0.8 V	4.75 V	40 V	—	—	100	µA
		UHP-407-1	Min.	0.8 V	4.75 V	70 V	—	—	100	µA
		UHP-507	Min.	0.8 V	4.75 V	100 V	—	—	100	µA
Diode Leakage Current (Note 5)	I_R	All	Nom.	5.0 V	5.0 V	Open	—	—	200	µA
Diode Forward Voltage Drop (Note 6)	V_F	All	Nom.	0 V	0 V	—	—	1.5	1.75	V
Output Voltage	$V_{CE(SAT)}$	All	Min.	2.0 V	2.0 V	150 mA	—	—	0.5	V
			Min.	2.0 V	2.0 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	All	Max.	5.0 V	5.0 V	—	—	20	26.5	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current at All Inputs Except Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	µA
			Max.	5.5 V	0 V	—	—	—	1.0	mA
Input Current at Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−1.1	−1.6	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	100	µA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at V_{CC} = 5.0 V.
2. Each gate.
3. Each input tested separately.
4. $T_A = +25°C$.
5. Diode leakage current measured at $V_R = V_{OFF(MIN)}$.
6. Diode forward voltage drop measured at I_F = 200 mA.



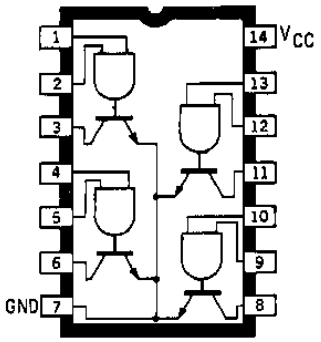
DWG. NO. A-7899B

*Includes probe and test fixture capacitance.



DWG. NO. A-7900A

UHP-408, UHP-408-1, and UHP-508
Quad 2-Input NAND Power Drivers

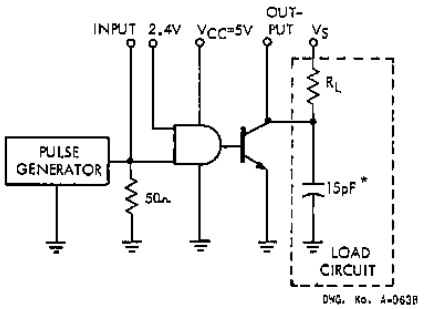


DWG. NO. A-12,388

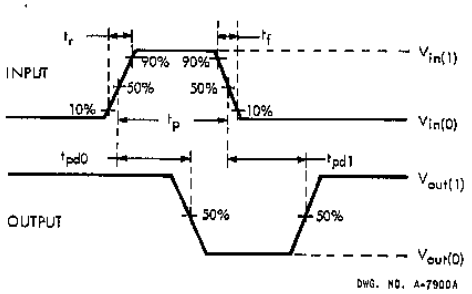
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-408	Min.	0.8 V	4.75 V	40 V	—	—	50	μA
		UHP-408-1	Min.	0.8 V	4.75 V	70 V	—	—	50	μA
		UHP-508	Min.	0.8 V	4.75 V	100 V	—	—	50	μA
Output Voltage	$V_{CE(SAT)}$	All	Min.	2.0 V	2.0 V	150 mA	—	—	0.5	V
			Min.	2.0 V	2.0 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	All	Max.	5.0 V	5.0 V	—	—	20	26.5	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	μA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at V_{CC} = 5.0 V.
2. Each gate.
3. Each input tested separately.
4. T_A = +25°C.



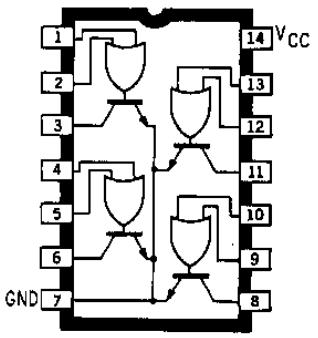
DWG. No. A-0638



DWG. NO. A-7900A

*Includes probe and test fixture capacitance.

UHP-432, UHP-432-1, and UHP-532
Quad 2-Input NOR Power Drivers

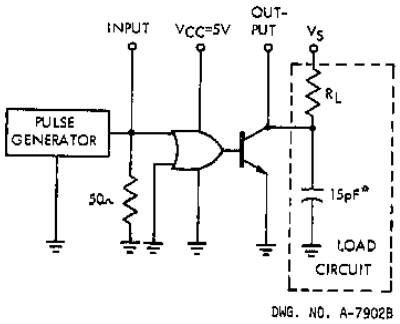


DWG. NO. A-12,389

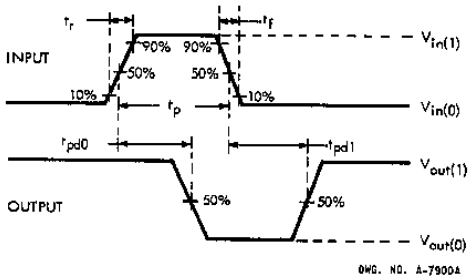
ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-432	Min.	0.8 V	0.8 V	40 V	—	—	50	µA
		UHP-432-1	Min.	0.8 V	0.8 V	70 V	—	—	50	µA
		UHP-532	Min.	0.8 V	0.8 V	100 V	—	—	50	µA
Output Voltage	$V_{CE(SAT)}$	All	Min.	2.0 V	0 V	150 mA	—	—	0.5	V
			Min.	2.0 V	0 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	All	Max.	5.0 V	5.0 V	—	—	20	25	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	µA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at V_{CC} = 5.0 V.
2. Each gate.
3. Each input tested separately.
4. T_A = +25°C.



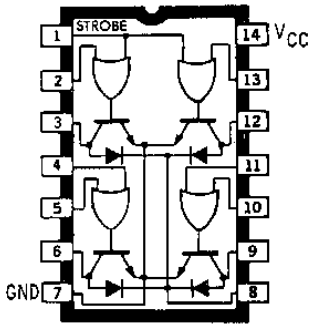
DWG. NO. A-7902B



DWG. NO. A-7900A

*Includes probe and test fixture capacitance.

UHP-433, UHP-433-1, and UHP-533
Quad NOR Relay Drivers

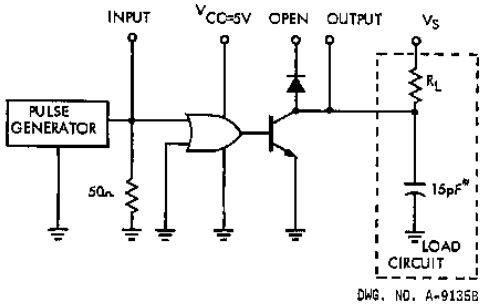


DWG. NO. A-12,390

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

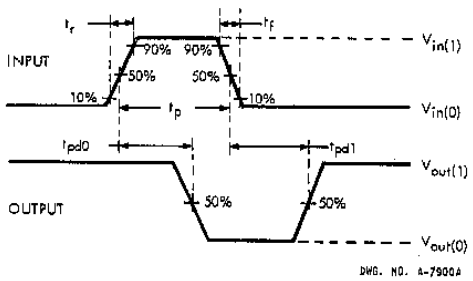
Characteristic	Symbol	Applicable Devices	Test Conditions				Limits			
			V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units
Output Reverse Current	I_{CEX}	UHP-433	Min.	0.8 V	0.8 V	40 V	—	—	100	µA
		UHP-433-1	Min.	0.8 V	0.8 V	70 V	—	—	100	µA
		UHP-533	Min.	0.8 V	0.8 V	100 V	—	—	100	µA
Diode Leakage Current (Note 5)	I_R	All	Nom.	5.0 V	5.0 V	Open	—	—	200	µA
Diode Forward Voltage Drop (Note 6)	V_F	All	Nom.	0 V	0 V	—	—	1.5	1.75	V
Output Voltage	$V_{CE(SAT)}$	All	Min.	2.0 V	0 V	150 mA	—	—	0.5	V
			Min.	2.0 V	0 V	250 mA	—	—	0.7	V
Supply Current (Notes 1, 2 and 4)	$I_{CC(1)}$	All	Max.	0 V	0 V	—	—	6.0	7.5	mA
	$I_{CC(0)}$	All	Max.	5.0 V	5.0 V	—	—	20	25	mA
Input Voltage	$V_{IN(1)}$	All	Min.	—	—	—	2.0	—	—	V
	$V_{IN(0)}$	All	Min.	—	—	—	—	—	0.8	V
Input Current at All Inputs Except Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−0.55	−0.8	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	40	µA
			Max.	5.5 V	0 V	—	—	—	1.0	mA
Input Current at Strobe (Note 3)	$I_{IN(0)}$	All	Max.	0.4 V	4.5 V	—	—	−1.1	−1.6	mA
	$I_{IN(1)}$	All	Max.	2.4 V	0 V	—	—	—	100	µA
			Max.	5.5 V	0 V	—	—	—	1.0	mA

1. Typical values at V_{CC} = 5.0 V.
2. Each gate.
3. Each input tested separately.
4. T_A = +25°C.
5. Diode leakage current measured at $V_R = V_{OFF(MIN)}$.
6. Diode forward voltage drop measured at I_F = 200 mA.



DWG. NO. A-9135B

*Includes probe and test fixture capacitance.



DWG. NO. A-7900A

SERIES ULN-2000A
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

THESE HIGH-VOLTAGE, HIGH-CURRENT Darlington arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units have open-collector outputs and integral diodes for inductive load transient suppression.

Peak inrush currents to 600 mA (Series ULN-2000A and ULN-2020A) or 750 mA (Series ULN-2010A) are permissible, making them ideal for driving tungsten filament lamps.

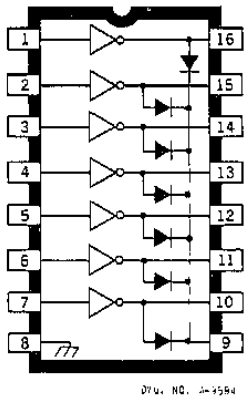
Series ULN-2001A devices are general purpose arrays that may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate printed wiring board layout and are priced to compete directly with discrete transistor alternatives.

Series ULN-2002A is designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also gives these devices excellent noise immunity.

Series ULN-2003A has a 2.7 kΩ series base resistor for each Darlington pair, allowing operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs — particularly those beyond the capabilities of standard logic buffers.

Series ULN-2004A has a 10.5 kΩ series input resistor that permits operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of Series ULN-2003A, while the required input voltage is less than that required by Series ULN-2002A.

Series ULN-2005A is designed for use with standard TTL and Schottky TTL, with which higher output currents are required and loading of the logic



output is not a concern. These devices will sink a minimum of 350 mA when driven from a "totem pole" logic output.

Series ULN-2000A is the original high-voltage, high-current Darlington array. The output transistors are capable of sinking 500 mA and will sustain at

Device Number Designation

$V_{CE(MAX)}$	50 V	50 V	95 V
$I_{C(MAX)}$	500 mA	600 mA	500 mA
Logic	Type Number		
General Purpose PMOS, CMOS	ULN-2001A	ULN-2011A	ULN-2021A
14-25 V PMOS	ULN-2002A	ULN-2012A	ULN-2022A
5 V TTL, CMOS	ULN-2003A	ULN-2013A	ULN-2023A
6-15 V CMOS, PMOS	ULN-2004A	ULN-2014A	ULN-2024A
High-Output TTL	ULN-2005A	ULN-2015A	ULN-2025A

least 50 V in the OFF state. Outputs may be paralleled for higher load-current capability. Series ULN-2010A devices are similar, except that they will sink 600 mA. Series ULN-2020A will sustain 95 V in the OFF state.

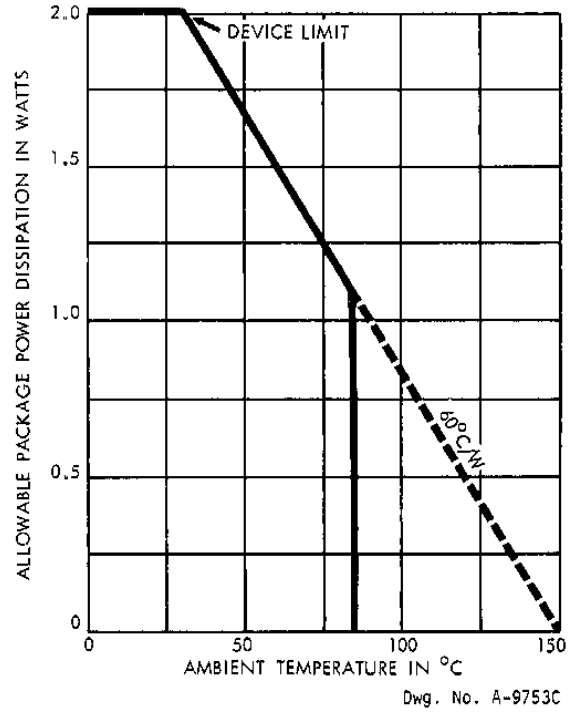
All Series ULN-2000A Darlington arrays are furnished in a 16-pin dual in-line plastic package. These can also be supplied in a hermetic dual in-line package for use in military and aerospace applications.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
for any one Darlington pair
(unless otherwise noted)

Output Voltage, V_{CE} (Series ULN-2000, 2010A)	50 V
(Series ULN-2020A)	95 V
Input Voltage, V_{IN} (Series ULN-2002, 2003, 2004A)	30 V
(Series ULN-2005A)	15 V
Continuous Collector Current, I_C (Series ULN-2000, 2020A)	500 mA
(Series ULN-2010A)	600 mA
Continuous Input Current, I_{IN}	25 mA
Power Dissipation, P_D (one Darlington pair)	1.0 W
(total package)	2.0 W*
Operating Ambient Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

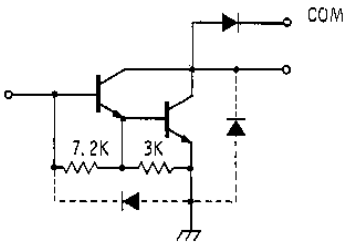
*Derate at the rate of 16.67 mW/°C above +25°C.
Under normal operating conditions, these devices will sustain 350 mA per output with $V_{CE(SAT)}$ = 1.6 V at +70°C with a pulse width of 20 ms and a duty cycle of 34%.

ALLOWABLE AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



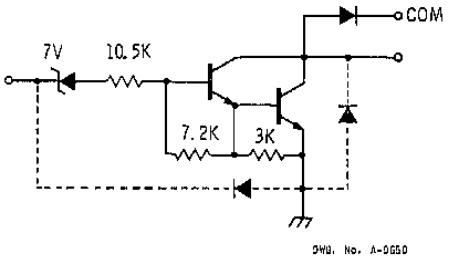
PARTIAL SCHEMATICS

Series ULN-2001A
(each driver)



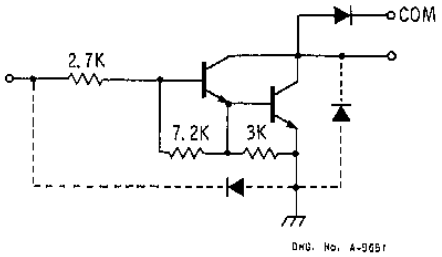
DWG. NO. A-9625

Series ULN-2002A
(each driver)



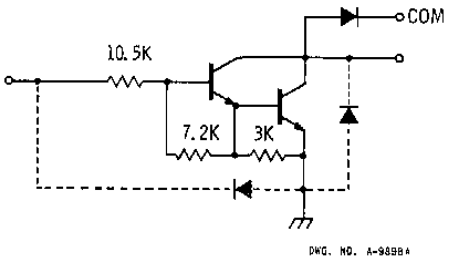
DWG. No. A-9650

Series ULN-2003A
(each driver)



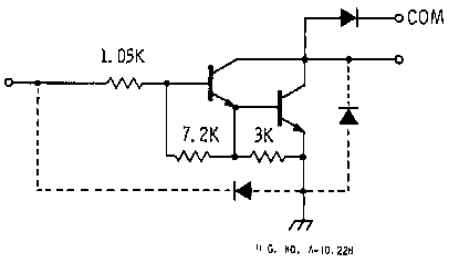
DWG. No. A-9651

Series ULN-2004A
(each driver)



DWG. NO. A-9698A

Series ULN-2005A
(each driver)



DWG. NO. A-10,228

SERIES ULN-2000A

ELECTRICAL CHARACTERISTICS AT +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 50 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2002A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2004A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 μA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2002A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2003A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2004A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2005A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2002A	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
			ULN-2003A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN-2004A	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
			ULN-2005A	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2001A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	μA
				V_R = 50 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

SERIES ULN-2010A

ELECTRICAL CHARACTERISTICS AT +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 50 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2012A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2014A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
				I_C = 500 mA, I_B = 600 μA	—	1.7	1.9	V
Input Current	$I_{IN(ON)}$	3	ULN-2012A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2013A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2014A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2015A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2012A	V_{CE} = 2.0 V, I_C = 500 mA	—	—	17	V
			ULN-2013A	V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	—	—	3.5	V
			ULN-2014A	V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	—	—	9.5	V
			ULN-2015A	V_{CE} = 2.0 V, I_C = 500 mA	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2011A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
				V_{CE} = 2.0 V, I_C = 500 mA	900	—	—	
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	μA
				V_R = 50 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V
				I_F = 500 mA	—	2.1	2.5	V

3

SERIES ULN-2020A

ELECTRICAL CHARACTERISTICS AT +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 95 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 95 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2022A	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2024A	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 μA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2022A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2023A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2024A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2025A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2022A	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
			ULN-2023A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN-2024A	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
			ULN-2025A	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2021A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 95 V, T_A = 25°C	—	—	50	μA
				V_R = 95 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

TEST FIGURES

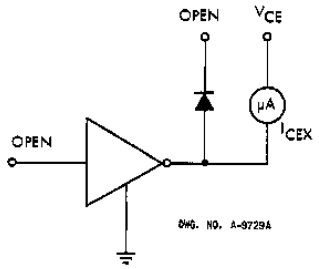


FIGURE 1A

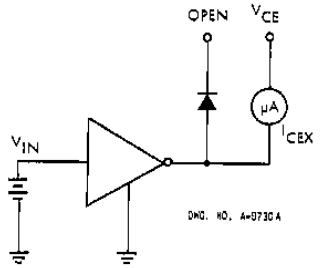


FIGURE 1B

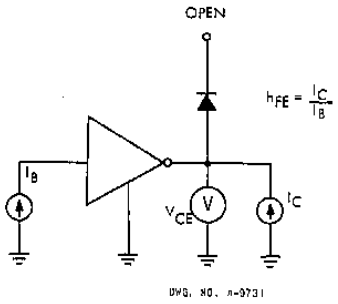


FIGURE 2

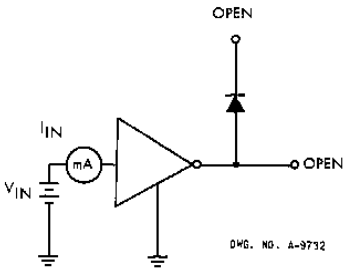


FIGURE 3

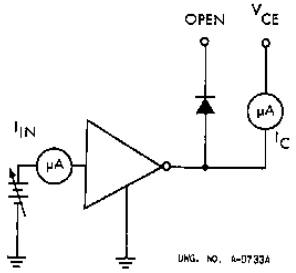


FIGURE 4

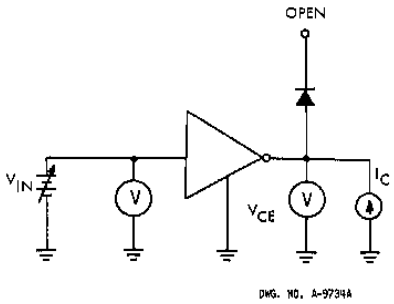


FIGURE 5

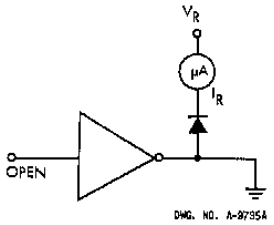


FIGURE 6

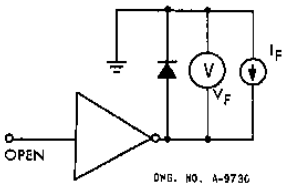
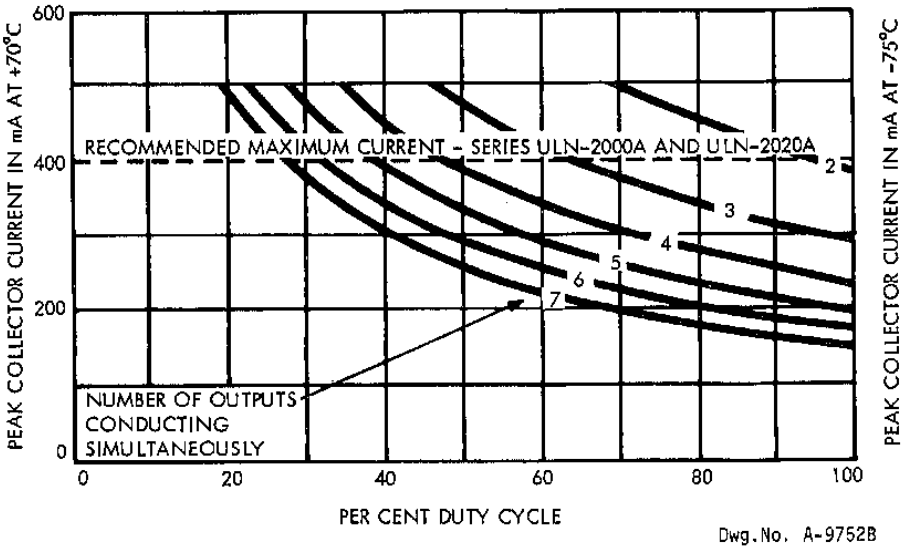


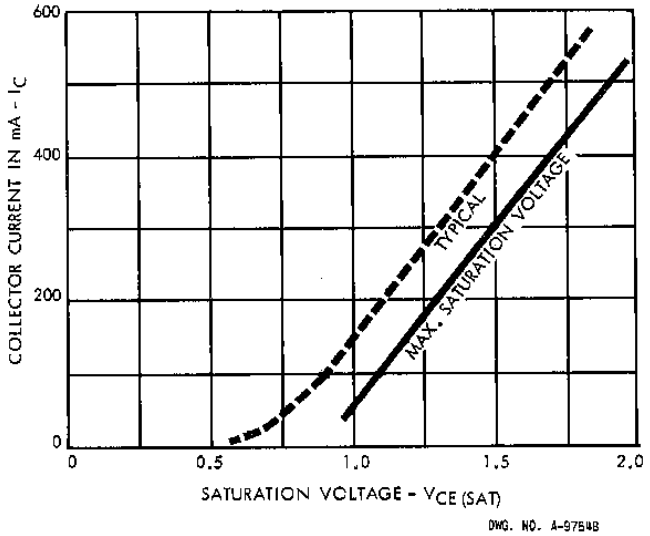
FIGURE 7

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE



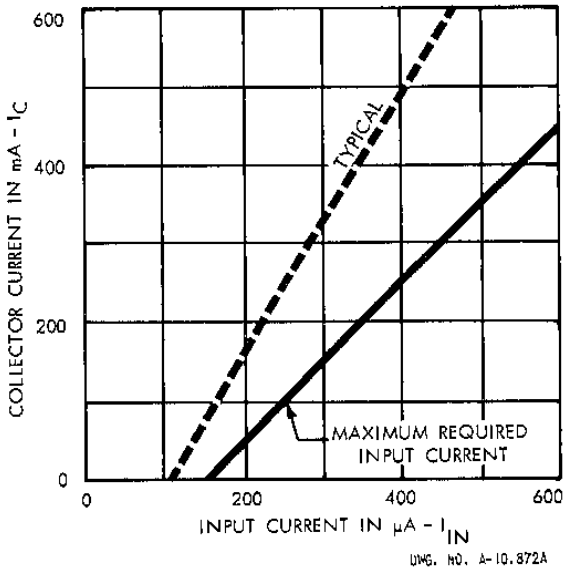
Dwg.No. A-9752B

COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



DWG. NO. A-9754B

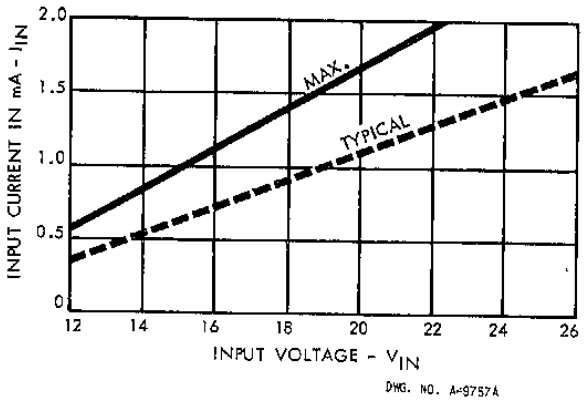
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



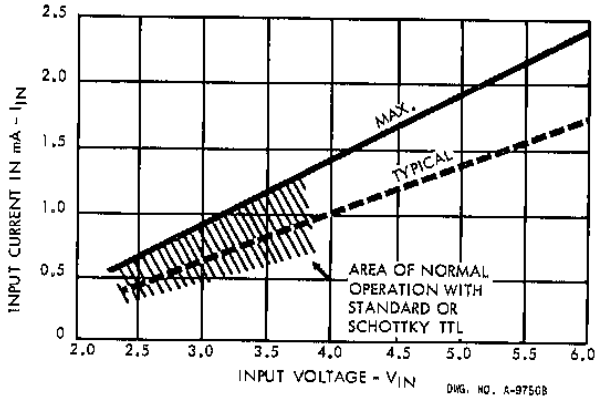
DWG. NO. A-10,872A

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

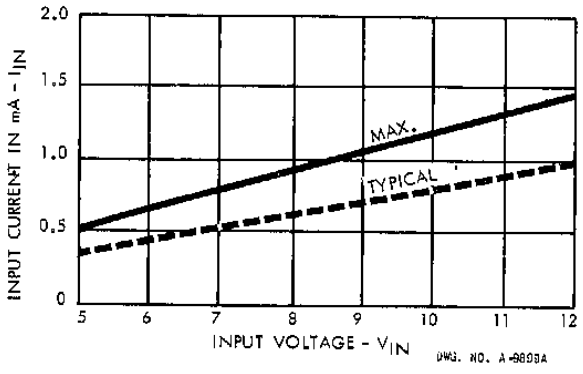
SERIES ULN-2002A



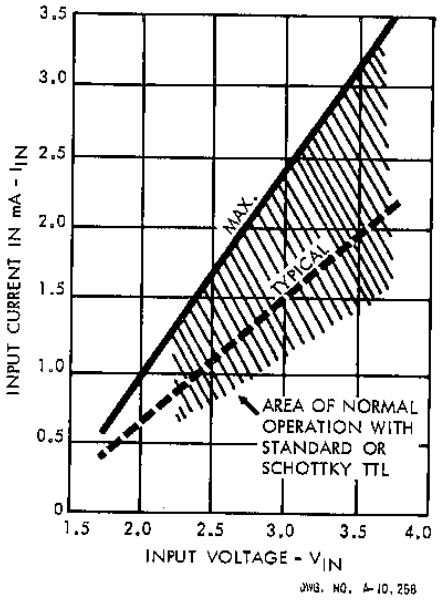
SERIES ULN-2003A



SERIES ULN-2004A



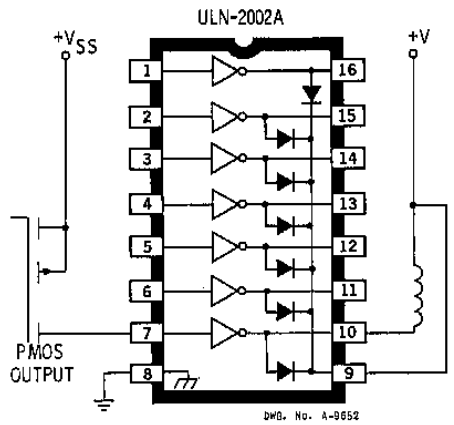
SERIES ULN-2005A



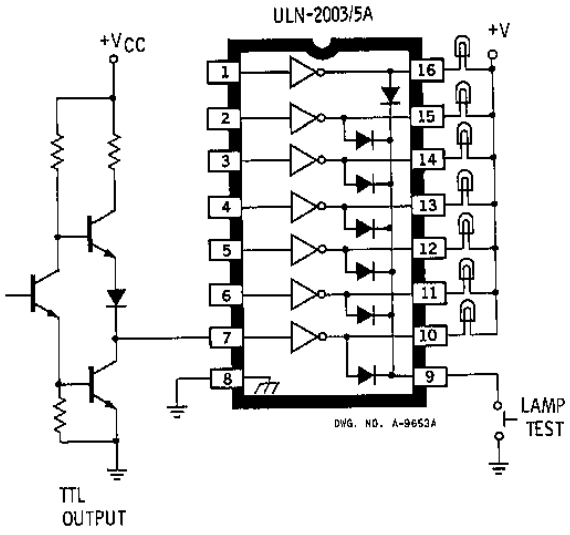
3

TYPICAL APPLICATIONS

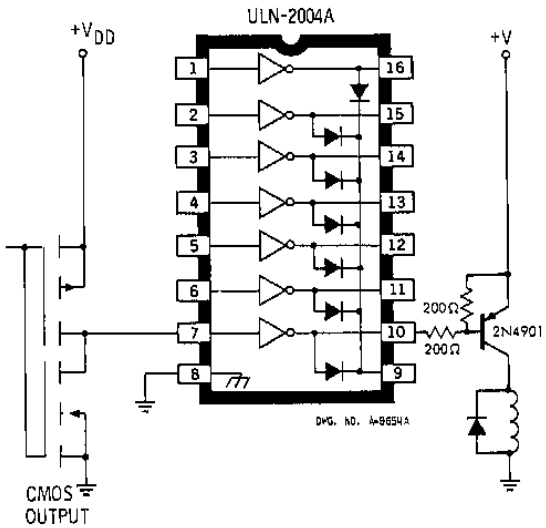
PMOS TO LOAD



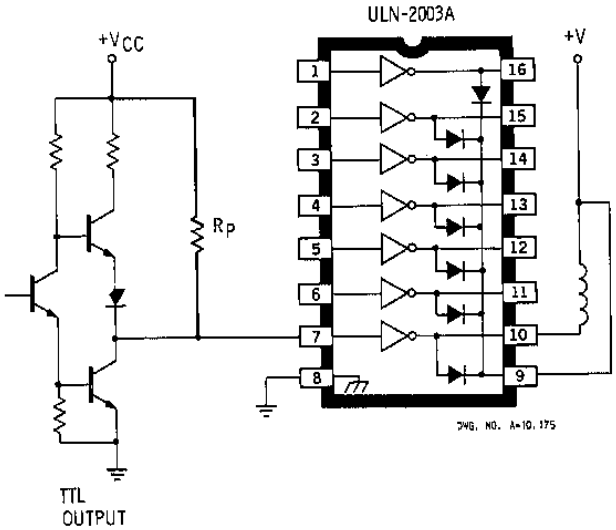
TTL TO LOAD



BUFFER FOR HIGH-CURRENT LOAD



USE OF PULL-UP RESISTORS TO INCREASE DRIVE CURRENT



SERIES ULN-2000L
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

These high-voltage, high-current Darlington arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units have open-collector outputs and integral diodes for inductive load transient suppression.

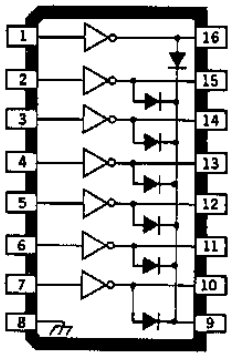
The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Outputs may be paralleled for higher load-current capability. All devices are packaged in the SOIC package.

Output pins are opposite input pins to facilitate printed wiring board layout. The ICs are priced to compete directly with discrete transistor alternatives.

The ULN-2001L is a general-purpose array that can be used with standard bipolar digital logic using external current limiting, or directly with most PMOS or CMOS.

The ULN-2002L is designed for use with 14 V to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also gives these devices excellent noise immunity.

The ULN-2003L has a 2.7 kΩ series base resistor for each Darlingon pair, allowing operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs—particularly those beyond the capabilities of standard logic buffers.



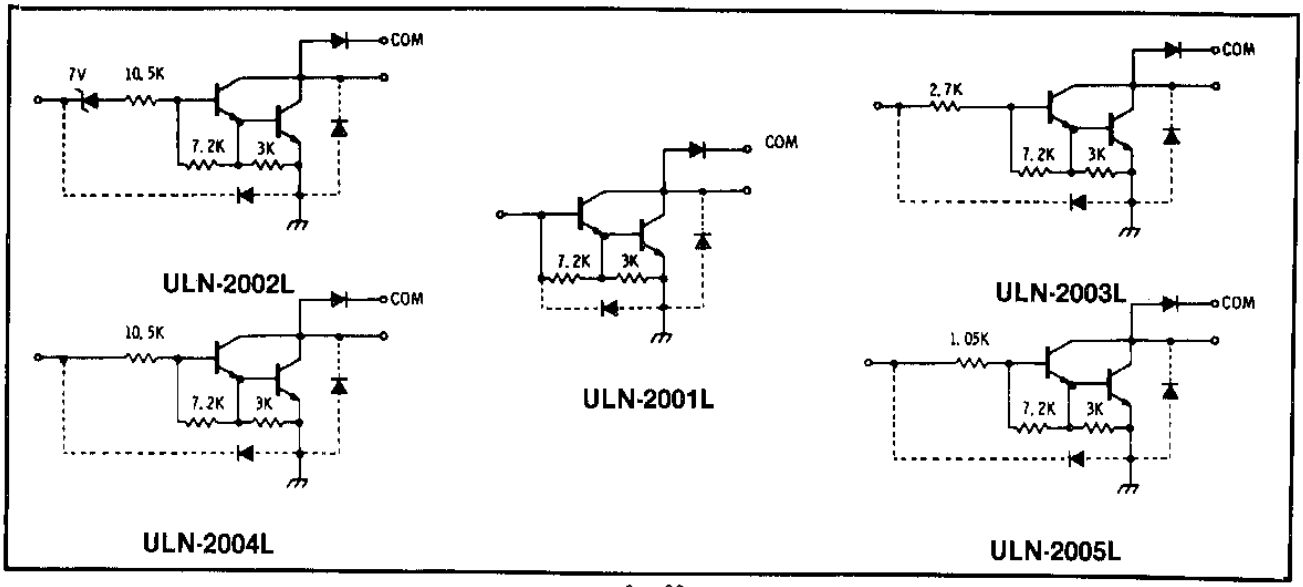
SOIC PACKAGE

The ULN-2004L has a 10.5 kΩ series input resistor that permits operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of Series ULN-2003L, while the required input voltage is less than that required by Series ULN-2002L.

The ULN-2005L is designed for use with standard TTL and Schottky TTL, with which higher output currents are required and loading of the logic output is not a concern. These devices will sink a minimum of 350 mA when driven from a "totem pole" logic output.

3

PARTIAL SCHEMATICS



ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature for any one Darlington pair (unless otherwise noted)

Output Voltage, V_{CE} . . . . . 50 V
Input Voltage,
V_{IN} (ULN-2002, 2003, 2004L) . . . . . 30 V
(ULN-2005L) . . . . . 15 V
Continuous Collector Current, I_C . . . . . 500 mA
Continuous Input Current, I_{IN} . . . . . 25 mA
Power Dissipation, P_D (total package) . . . . . 0.96 W*
Operating Ambient Temperature Range, T_A . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

*Derate at rate of 7.7 mW/°C above = 25°C.

Device Number Designation

$V_{CE(MAX)}$ / $I_{C(MAX)}$	50 V / 500 mA
Logic	Type Number
General Purpose PMOS, CMOS	ULN-2001L
14-25 V PMOS	ULN-2002L
5 V TTL, CMOS	ULN-2003L
6-15 V CMOS, PMOS	ULN-2004L
High-Output TTL	ULN-2005L

ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	µA
			V_{CE} = 50 V, T_A = 70°C	—	—	100	µA
		ULN-2002L	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	µA
		ULN-2004L	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	I_C = 100 mA, I_B = 250 µA	—	0.9	1.1	V
			I_C = 200 mA, I_B = 350µA	—	1.1	1.3	V
			I_C = 350 mA, I_B = 5 µA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	ULN-2002L	V_{IN} = 17 V	—	0.82	1.25	mA
		ULN-2003L	V_{IN} = 3.85 V	—	0.93	1.35	mA
		ULN-2004L	V_{IN} = 5.0 V	—	0.35	0.5	mA
			V_{IN} = 12 V	—	1.0	1.45	mA
		ULN-2005L	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	All	I_C = 500 µA, T_A = 70°C	50	65	—	µA
Input Voltage	$V_{IN(ON)}$	ULN-2002L	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
		ULN-2003L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
			V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
			V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
		ULN-2004L	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
		ULN-2004L	V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
			V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
			V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
		ULN-2005L	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
DC Forward Current Transfer Ratio	h_{FE}	ULN-2001L	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	—
Input Capacitance	C_{IN}	All		—	15	25	pF
Turn-On Delay	t_{PLH}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Turn-Off Delay	t_{PHL}	All	0.5 E_{IN} to 0.5 E_{OUT}	—	0.25	1.0	µs
Clamp Diode Leakage Current	I_R	All	V_R = 50 V, T_A = 25°C	—	—	50	µA
			V_R = 50 V, T_A = 70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	All	I_F = 350 mA	—	1.7	2.0	V

UDN-2522A QUAD BUS TRANSCEIVER

—Data and Direct Inductive Load Control

FEATURES

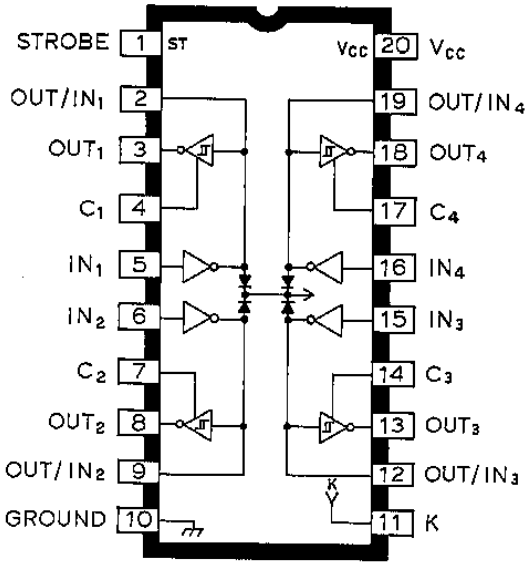
- Driver Output Current to 300 mA
- Driver Output Sustaining Voltage of 50 V
- Pulse-Width Discriminating Receivers
- Internal Receiver Hysteresis
- Compatible with TTL and MOS Logic
- Driver Output Clamp Diodes

Designed for bidirectional flow of data over unbalanced lines, the UDN-2522A quad bus transmitter/receivers feature a unique driver/receiver combination. A 300 mA output current, 50 V sustaining voltage rating, and internal clamp and blocking diodes allow these transmitter/receivers to directly control loads such as relays and solenoids, as well as the usual line receivers.

The driver stages include a common STROBE input pin for extended control flexibility. The STROBE turns off all four drivers but does not affect receiver operation. Because of the high driver output current, a large number of transmitter/receivers can be connected to a single data bus.

Each receiver's input is internally connected to its companion driver output. The receivers include a pulse-width discriminator and hysteresis for pulse reconstruction and improved noise immunity. The minimum detectable pulse width is determined by the user's choice of capacitor on the "C" pin for each of the four channels.

The UDN-2522A is rated for operation over the temperature range of −20°C to +85°C. It is packaged in a 20-pin dual in-line plastic package with copper leadframe for enhanced power dissipation. The drivers are capable of simultaneously sinking maximum rated current over the full operating temperature range.



Dwg. No. A-14,178

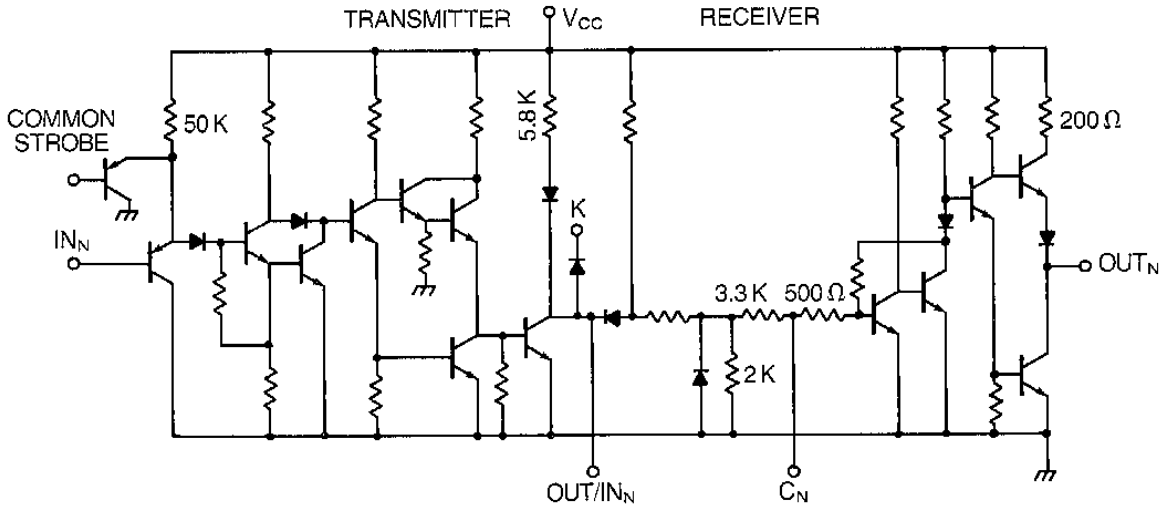
ABSOLUTE MAXIMUM RATINGS AT T_A = +25°C

Driver Output Voltage, V_{CE}	70 V
Driver Output Sustaining Voltage, $V_{CE(sus)}$	50 V
Driver Continuous Output Current, I_{OUT}	300 mA
Driver Input Voltage, V_{IN}	5.5 V
Receiver Output Current, I_{OUT}	50 mA
Receiver Input Voltage, V_{IN}	70 V
Supply Voltage, V_{CC}	7.0 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

3

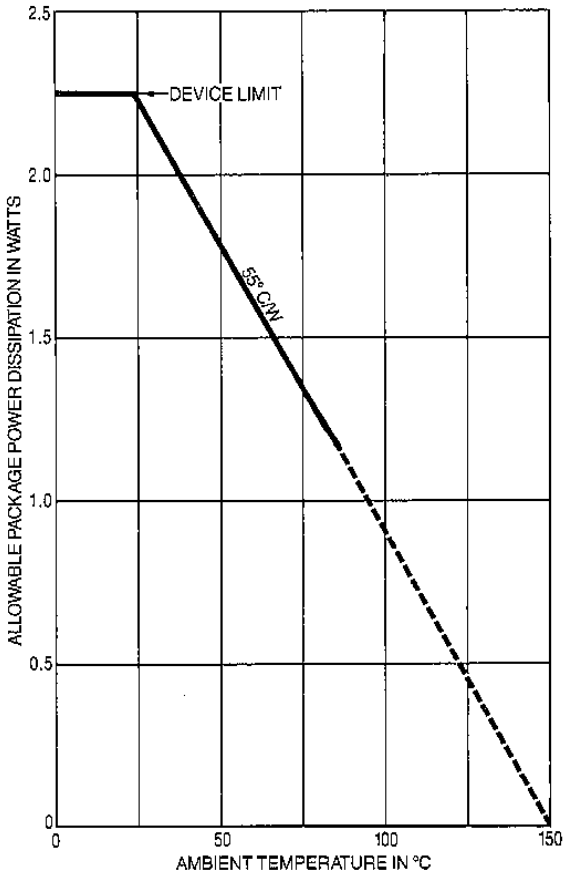
PARTIAL SCHEMATIC

(1 of 4 Channels)



Dwg. No. W-147

ALLOWABLE AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-10,379B

ELECTRICAL CHARACTERISTICS at T_A = +25°C, Figure 1 and 2, 3, 4, or 5 as specified.

Characteristic	Test Conditions						Limits			
	Vcc	Input	Strobe	Out/In	C	Output	Min.	Typ.	Max.	Units
DRIVERS										
Output Leakage Current	4.5V	Open	0.8V	70V†	Open	Open	—	—	70	µA
Output Saturation Voltage	4.5V	2.0V	2.0V	210mA	Open	Open	—	0.2	0.4	V
	4.5V	2.0V	2.0V	300mA	Open	Open	—	0.4	0.6	V
Output Sat. Voltage Matching	4.5V	2.0V	2.0V	210mA	Open	Open	—	±20	±50	mV
Output Sustaining Voltage*	5.0V	3⌊0V	2.0V	Fig. 2	Open	Open	50	—	—	V
Output Voltage	4.5V	0.8V	2.0V	−160µA	Open	Open	2.25	—	—	V
Logic Input Voltage	4.5V	—	—	Open	Open	Open	2.0	—	—	V
	4.5V	—	—	Open	Open	Open	—	—	0.8	V
Logic Input Current	5.5V	5.5V	2.0V	Open	Open	Open	—	—	20	µA
	5.5V	0.1V	2.0V	Open	Open	Open	−1.0	—	−20	µA
Strobe Input Current	5.5V	2.0V	5.5V	Open	Open	Open	—	—	50	µA
	5.5V	2.0V	0.1V	Open	Open	Open	—	—	−50	µA
Input Clamp Voltage	Open	−12mA	Open	Open	Open	Open	0	—	−1.6	V
Propagation Delay Time	5.5V	3⌊0V	2.0V	Fig. 3	Open	Open	—	—	750	ns
	5.5V	2.0V	3⌊0V	Fig. 3	Open	Open	—	—	750	ns
	5.5V	3⌊0V	2.0V	Fig. 4	Open	Open	—	—	1.4	µs
	5.5V	2.0V	3⌊0V	Fig. 4	Open	Open	—	—	1.4	µs
	4.5V	0⌈3V	2.0V	Fig. 3	Open	Open	—	—	600	ns
	4.5V	2.0V	0⌈3V	Fig. 3	Open	Open	—	—	600	ns
	4.5V	0⌈3V	2.0V	Fig. 4	Open	Open	—	—	600	ns
	4.5V	2.0V	0⌈3V	Fig. 4	Open	Open	—	—	600	ns
Output Rise Time	4.5V	3⌊0V	2.0V	Fig. 3	Open	Open	—	—	175	ns
Ouput Fall Time	5.5V	0⌈3V	2.0V	Fig. 3	Open	Open	—	—	175	ns
Clamp Diode Leakage Current	V_R = 70V			0.0V	Open	Open	—	—	70	µA
Clamp Diode Forward Voltage	I_F = 300mA				Open	Open	—	1.6	1.8	V
Supply Current (All Drivers)	5.5V	0.0V	0.8V	—	Open	Open	—	—	20	mA
	5.5V	2.0V	2.0V	—	Open	Open	—	—	50	mA
RECEIVERS										
Output Voltage	4.5V	0.8V	2.0V	Open	2.0V	4.0mA	—	—	0.5	V
	4.5V	2.0V	2.0V	Open	0.0V	−400µA	2.4	—	—	V
Short-Circuit Output Current	5.5V	2.0V	2.0V	Open	Open	0.0V	−2.0	—	−50	mA
Input Current	5.5V	Open	0.0V	4.0V	Open	Open	−250	—	—	µA
	4.5V	Open	0.0V	0.1V	Open	Open	—	—	−500	µA
Input Voltage	4.5V	Open	0.0V	—	Open	Low	2.0	—	—	V
	4.5V	Open	0.0V	—	Open	High	—	—	0.8	V
Input Voltage Hysteresis	4.5V	Open	0.0V	0⌈3⌊0V	Open		250	—	775	mV
Propagation Delay Time	4.5V	Open	0.0V	0⌈3V	Open	Fig. 5	—	—	375	ns
	5.5V	Open	0.0V	3⌊0V	Open	Fig. 5	—	—	375	ns
Output Fall Time	5.5V	Open	0.0V	0⌈3V	Open	Fig. 5	—	—	75	ns
Output Rise Time	5.5V	Open	0.0V	3⌊0V	Open	Fig. 5	—	—	75	ns
Noise Immunity	5.5V	Open	0.0V	0⌈2V	0.1µF	Open	400	—	—	µs
	4.5V	Open	0.0V	0⌈2V	0.1µF	Open	—	—	1400	µs

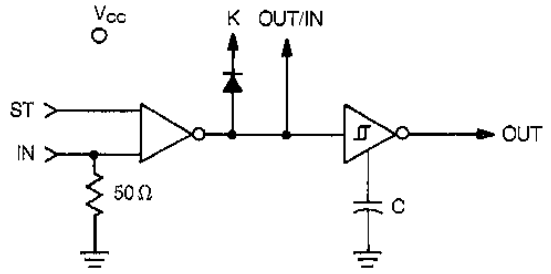
Note: Negative current is defined as coming out of (sourcing) the specified device pin.

**$V_{OUT(sus)}$ is measured with a 5 ms ON pulse, 12 ms after turn-OFF.*

†Output clamp diode reverse-biased with V_K = 71 V.

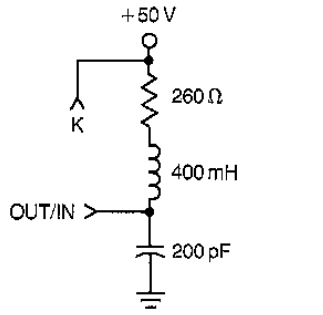
3

TEST FIGURES



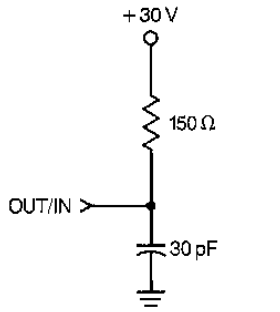
Dwg. No. W-148

Figure 1



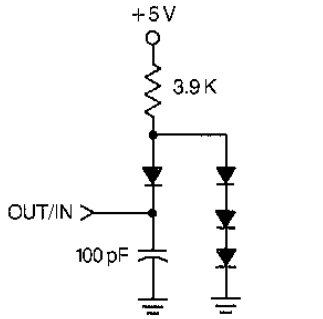
Dwg. No. W-149

Figure 2



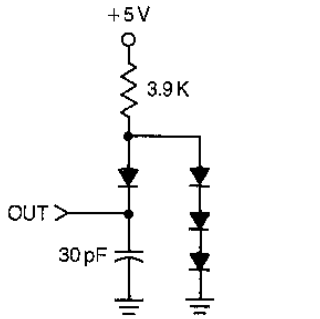
Dwg. No. W-151

Figure 3



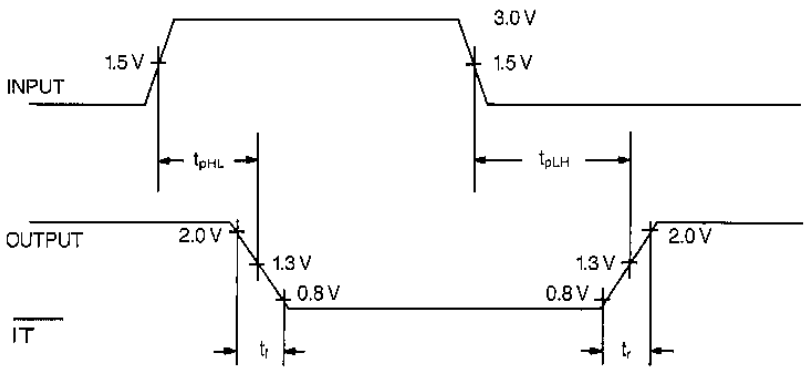
Dwg. No. W-150

Figure 4



Dwg. No. W-152

Figure 5



Dwg. No. W-153

TIMING WAVESHAPES
(Figures 4 and 5)

APPLICATIONS INFORMATION

Systems designers are often concerned with interfacing subsystems and transmitting data a considerable distance. Whether it is to a nearby circuit board or to another unit in a large spread-out system, the quality of the signal reproduced in the receiving unit is dependent on:

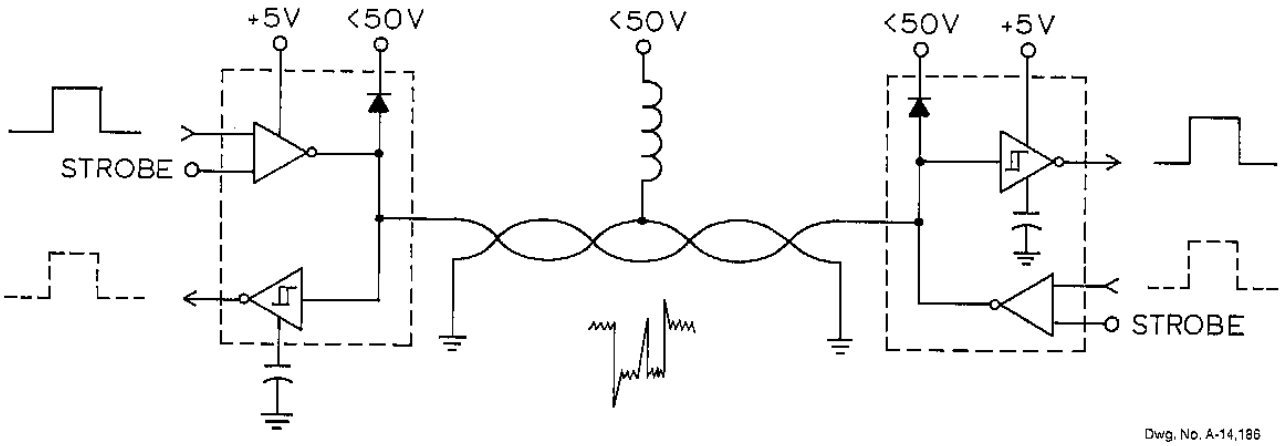
Driver characteristics
Transmission line characteristics
Line length
General layout and noise environment
Receiver characteristics
Data transmission rate

Unbalanced (common-mode) data transmission is often preferred, since the cabling requires only a single wire plus ground and the circuits are generally lower in cost. However, the data transmission is susceptible to common-mode noise, such as ground IR noise and crosstalk. For noise immunity, the receiver should include pulse-width discrimination and hysteresis. A bus should not extend out of its subsystem's electronic enclosure without special care. Cables should be in the form of twisted pair or flat cable where the signal wires are alternated with ground wires.

If power loads are not being driven, a high output current drive capability allows party-line operation with a low line impedance. The line can be terminated at both ends and still give considerable noise margin at the receiver.

3

TYPICAL APPLICATION

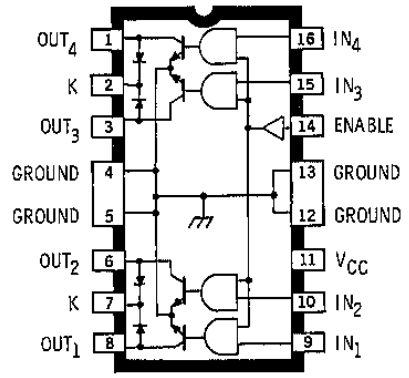


Dwg. No. A-14,186

UDN-2543B QUAD NAND-GATE POWER DRIVER —For Incandescent or Inductive Loads

FEATURES

- 1.0 A Output Current
- Output Voltage to 60 V
- Low Output-Saturation Voltage
- Integral Output-Suppression Diodes
- Efficient Input/Output Pin Structure
- TTL, CMOS, PMOS, NMOS Compatible
- Over-Current Protected



Dwg. No. A-11,561

Providing interface between low-level signal processing circuits and power loads to 240 W, the UDN-2543B quad power driver combines NAND logic gates and high-current bipolar outputs. Each of the four independent outputs can sink up to 1 A in the ON state. The outputs have a minimum breakdown voltage of 60 V and a sustaining voltage of 35 V. Inputs are compatible with most TTL, DTL, LSTTL, and 5 V CMOS and PMOS logic systems.

Over-current protection has been designed into the UDN-2543B and typically occurs at 1 A. It protects the device from output short-circuits with supply voltages of up to 25 V. When the maximum driver output current is reached, that output stage is driven linearly. If the over-current condition continues, that output driver's thermal limiting will operate, limiting the driver's power dissipation and junction temperature. The outputs also include transient suppression diodes for use with inductive loads such as relays, solenoids, and dc stepping motors. In display applications, the diodes can be used for the lamp-test function.

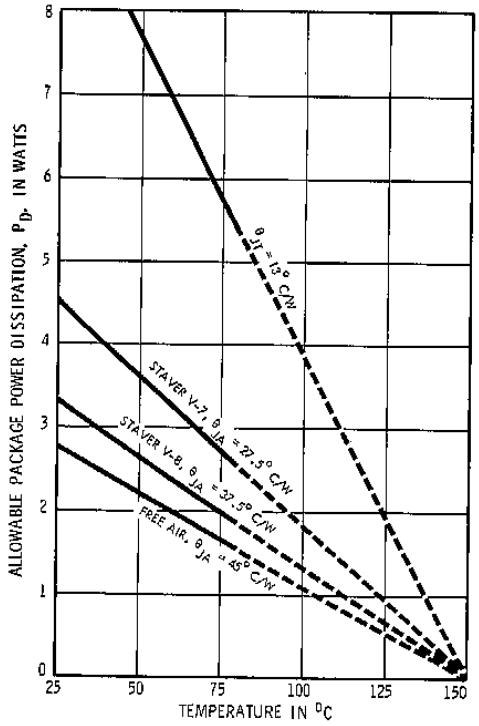
The UDN-2543B is supplied in a 16-pin dual in-line plastic package with heat-sink contact tabs. The lead configuration allows easy attachment of an inexpensive heat-sink and fits a standard integrated circuit socket or a printed wiring board layout.

ABSOLUTE MAXIMUM RATINGS
at $T_A = +25°C$

Output Voltage, V_{CE}	60 V
Over-Current Protected Output Voltage, V_{CE}	25 V
Min. Output Sustaining Voltage, $V_{CE(SUS)}$	35 V
Output Current, I_{OUT}	1.0 A*
Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{IN}	18 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

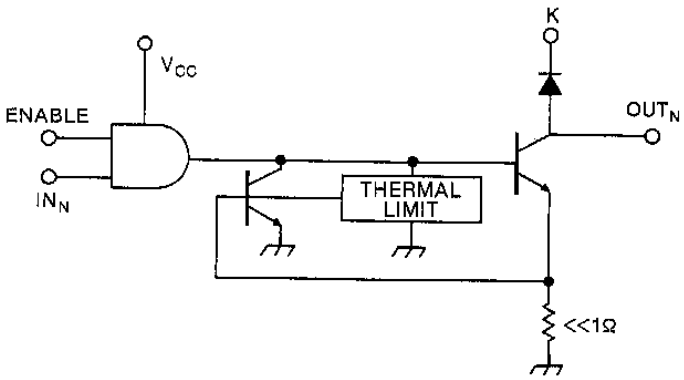
*Outputs are current limited at approximately 1.0 A per driver and junction temperature limited if current in excess of 1.0 A is attempted. See Circuit Description and Applications Section for further information.

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-11,793A

FUNCTIONAL BLOCK DIAGRAM
(1 of 4 Channels)



Dwg. No. D-1005

3

ELECTRICAL CHARACTERISTICS AT T_A = +25°C, V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 60 V, V_{IN} = 0.8 V, V_{ENABLE} = 2.0 V	–	100	µA
		V_{OUT} = 60 V, V_{IN} = 2.0 V, V_{ENABLE} = 0.8 V	–	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 100 mA, V_{IN} = V_{ENABLE} = 0.8 V	35	–	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100 mA, V_{IN} = V_{ENABLE} = 2.0 V	–	200	mV
		I_{OUT} = 400 mA, V_{IN} = V_{ENABLE} = 2.0 V	–	400	mV
		I_{OUT} = 700 mA, V_{IN} = V_{ENABLE} = 2.0 V	–	600	mV
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$	2.0	–	V
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$	–	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$ = 2.0 V	–	10	µA
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$ = 0.8 V	–	-10	µA
Total Supply Current	I_{CC}	I_{OUT} = 700 mA, V_{IN}* = V_{ENABLE} = 2.0 V	–	65	mA
		Outputs Open, V_{IN}* = 0.8 V, V_{ENABLE} = 2.0 V	–	15	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	–	1.6	V
		I_F = 1.5 A	–	2.0	V
Clamp Diode Leakage Current	I_R	V_R = 60 V, V_{IN} = V_{ENABLE} = 2.0 V, $D_1 + D_2$ or $D_3 + D_4$	–	50	µA

**All inputs simultaneously, all other tests are performed with each input tested separately.*

CIRCUIT DESCRIPTION AND APPLICATION

INCANDESCENT LAMP DRIVER

High incandescent lamp turn-on/in-rush current can destroy semiconductor lamp drivers and contributes to poor lamp reliability. However, lamps with steady-state current ratings up to 700 mA can be driven with the UDN-2543A without the need for warming or current limiting resistors.

When an incandescent lamp is initially turned ON, the cold lamp filament is at minimum resistance and would normally allow a 10× to 12× in-rush current. With the UDN-2543A, during turn-on, the high in-rush current is sensed by the internal low-value sense resistor, drive current to the output stage is diverted by the shunting transistor, and the load current is limited to approximately 1 A. During this short transition period, the output driver is driven in a linear fashion. During lamp warm-up, the filament resistance increases to its maximum value, the output driver goes into saturation and applies full supply voltage to the lamp.

The internal diodes can be used to perform the lamp-test function.

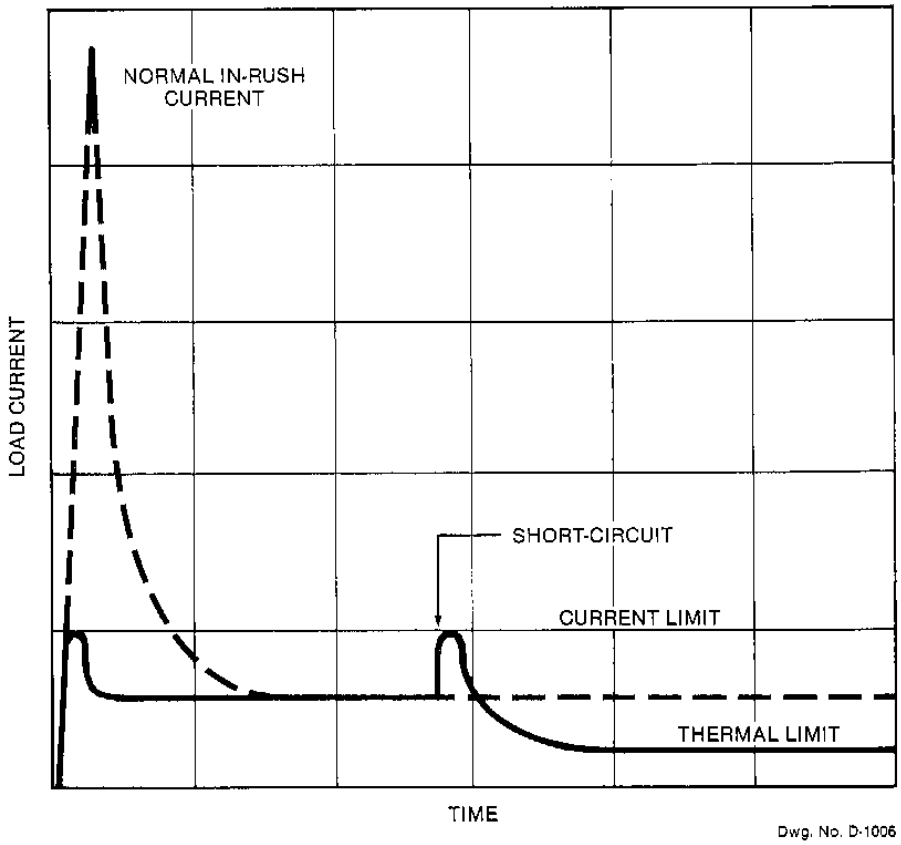
INDUCTIVE LOAD DRIVER

Bifilar (unipolar) stepper motors can be driven directly. The internal flyback diodes prevent damage to the output transistors by suppressing the high-voltage spikes which occur when turning OFF an inductive load.

FAULT CONDITIONS

(Shorted Load or Stalled Motor)

In the event of a shorted load, shorted winding, or stalled motor, the load current will attempt to increase. As described above, the drive current to the output stage is diverted (limiting the load current to about 1 A), causing the output stage to go linear. As the junction temperature of the output stage increases, the thermal limit circuit will become operational, further decreasing the drive current. The load current (junction temperature) is then a function of ambient temperature, state of remaining drivers, supply voltage, and load resistance. If the fault condition is corrected, the output driver will return to its normal saturated condition.



Dwg. No. D-1006

SERIES UDN-2580A
8-CHANNEL SOURCE DRIVERS

FEATURES

- TTL, CMOS, PMOS, NMOS Compatible
- High Output Current Ratings
- Internal Transient Suppression
- Efficient Input/Output Pin Structure

THIS versatile family of integrated circuits, originally designed to link NMOS logic with high-current inductive loads, will work with many combinations of logic- and load-voltage levels, meeting interface requirements beyond the capabilities of standard logic buffers.

Series UDN-2580A source drivers can drive incandescent, LED, or vacuum fluorescent displays. Internal transient-suppression diodes permit the drivers to be used with inductive loads.

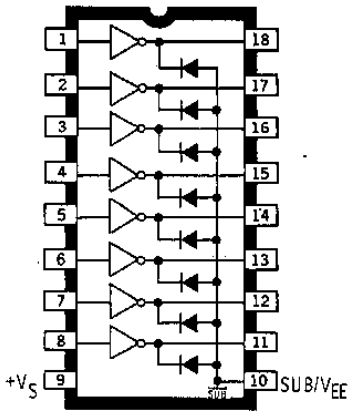
Type UDN-2580A is a high-current source driver used to switch the ground ends of loads that are directly connected to a negative supply. Typical loads are telephone relays, PIN diodes, and LEDs.

Type UDN-2585A is a driver designed for applications requiring low output saturation voltages. Typical loads are low-voltage LEDs and incandescent displays. The eight non-Darlington outputs will simultaneously sustain continuous load currents of -120 mA at ambient temperatures to $+70°C$.

Type UDN-2588A, a high-current source driver similar to Type UDN-2580A, has separate logic and driver supply lines. Its eight drivers can serve as an interface between positive logic (TTL, CMOS, PMOS) or negative logic (NMOS) and either negative or split-load supplies.

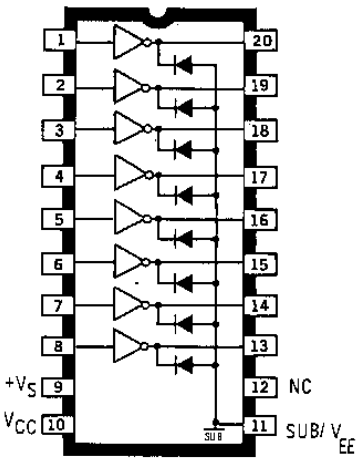
Types UDN-2580A and UDN-2588A are rated for operation with output voltages of up to 50 V. Selected devices, carrying the suffix "-1" on the Sprague part number, have maximum ratings of 80 V.

Types UDN-2580A and UDN-2585A are furnished in 18-pin dual in-line plastic packages; Type UDN-2588A is supplied in a 20-pin dual in-line plastic package. All input connections are on one side of the packages, output pins on the other, to simplify printed wiring board layout.



DWG.NO. A-11,359

UDN-2580A
UDN-2585A



DWG.NO. A-11,357

UDN-2588A

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature for Any One Driver (unless otherwise noted)

	UDN-2580A	UDN-2580A-1	UDN-2585A	UDN-2588A	UDN-2588A-1
Output Voltage, V_{CE}	50 V	80 V	25 V	50 V	80 V
Supply Voltage, V_S (ref. sub.)	50 V	80 V	25 V	50 V	80 V
Supply Voltage, V_{CC} (ref. sub.)	—	—	—	50 V	80 V
Input Voltage, V_{IN} (ref. V_S)	−30 V	−30 V	−20 V	−30 V	−30 V
Total Current, $I_{CC} + I_S$	−500 mA	−500 mA	−250 mA	−500 mA	−500 mA
Substrate Current, I_{SUB}	3.0 A	3.0 A	2.0 A	3.0 A	3.0 A

Allowable Power Dissipation, P_D (single output) ..... 1.0 W
(total package) ..... 2.2 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +150°C

*Derate at the rate of 18 mW/°C above 25°C

For simplification, these devices are characterized on the following pages with specific voltages for inputs, logic supply (V_S), load supply (V_{EE}), and collector supply (V_{CC}). Typical use of the UDN-2580A and UDN-2580A-1 is with negative referenced logic. The more common application of the UDN-2585A, UDN-2588A, and UDN-2588A-1 is with positive referenced logic supplies. In application, the devices are capable of operation over a wide range of logic and supply voltage levels:

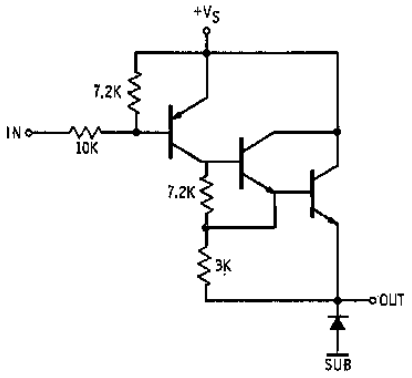
TYPICAL OPERATING VOLTAGES

V_S	$V_{IN(ON)}$	$V_{IN(OFF)}$	V_{CC}	$V_{EE(MAX)}$	Device Type
0 V	−15 V to −3.6 V	−0.5 V to 0 V	NA	−25 V	UDN-2585A
				−50 V	UDN-2580A
				−80 V	UDN-2580A-1
+5 V	0 V to +1.4 V	+4.5 V to +5 V	NA	−20 V	UDN-2585A
				−45 V	UDN-2580A
				−75 V	UDN-2580A-1
			≤5 V	−45 V	UDN-2588A
				−75 V	UDN-2588A-1
+12 V	0 V to +8.4 V	+11.5 V to +12 V	NA	−13 V	UDN-2585A
				−38 V	UDN-2580A
				−68 V	UDN-2580A-1
			≤12 V	−38 V	UDN-2588A
				−68 V	UDN-2588A-1
+15 V	0 V to +11.4 V	+14.5 V to +15 V	NA	−10 V	UDN-2585A
				−35 V	UDN-2580A
				−65 V	UDN-2580A-1
			≤15 V	−35 V	UDN2588A
				−65 V	UDN-2588A-1

NOTE: The substrate must be tied to the most negative point in the external circuit to maintain isolation between drivers and to provide for normal circuit operation.

UDN-2580A
UDN-2580A-1

PARTIAL SCHEMATIC



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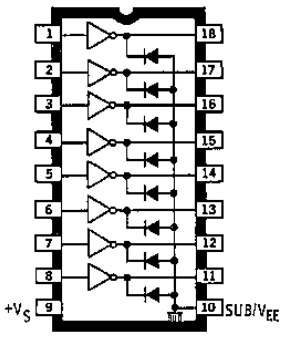


DWG.NU. A-11,359

3

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 0 V, V_{EE} = −45 V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UDN-2580A	V_{IN} = −0.5 V, V_{OUT} = V_{EE} = −50 V	—	50	μA
			V_{IN} = −0.4 V, V_{OUT} = V_{EE} = −50 V, T_A = 70°C	—	100	μA
		UDN-2580A-1	V_{IN} = −0.5 V, V_{OUT} = V_{EE} = −80 V	—	50	μA
			V_{IN} = −0.4 V, V_{OUT} = V_{EE} = −80 V, T_A = 70°C	—	100	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	UDN-2580A	V_{IN} = −0.4 V, I_{OUT} = −25 mA, Note 1	35	—	V
		UDN-2580A-1	V_{IN} = −0.4 V, V_{EE} = −75 V, I_{OUT} = −25 mA, Note 1	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Both	V_{IN} = −2.4 V, I_{OUT} = −100 mA	—	1.8	V
			V_{IN} = −3.0 V, I_{OUT} = −225 mA	—	1.9	V
			V_{IN} = −3.6 V, I_{OUT} = −350 mA	—	2.0	V
Input Current	$I_{IN(ON)}$	Both	V_{IN} = −3.6 V, I_{OUT} = −350 mA	—	−500	μA
			V_{IN} = −15 V, I_{OUT} = −350 mA	—	−2.1	mA
	$I_{IN(OFF)}$	Both	I_{OUT} = −500 μA, T_A = 70°C, Note 3	−50	—	μA
Input Voltage	$V_{IN(ON)}$	Both	I_{OUT} = −100 mA, V_{CE} ≤1.8 V, Note 4	—	−2.4	V
			I_{OUT} = −225 mA, V_{CE} ≤1.9 V, Note 4	—	−3.0	V
			I_{OUT} = −350 mA, V_{CE} ≤2.0 V, Note 4	—	−3.6	V
	$V_{IN(OFF)}$	Both	I_{OUT} = −500 μA, T_A = 70°C	−0.2	—	V
Clamp Diode Leakage Current	I_R	UDN-2580A	V_R = 50 V, T_A = 70°C	—	50	μA
		UDN-2580A-1	V_R = 80 V, T_A = 70°C	—	50	μA
Clamp Diode Forward Voltage	V_F	Both	I_F = 350 mA	—	2.0	V
Input Capacitance	C_{IN}	Both		—	25	pF
Turn-On Delay	t_{PHL}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs
Turn-Off Delay	t_{PLH}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs

NOTES: 1. Pulsed test, t_p ≤300 μs, duty cycle ≤2%.
2. Negative current is defined as coming out of the specified device pin.
3. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
4. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
5. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.

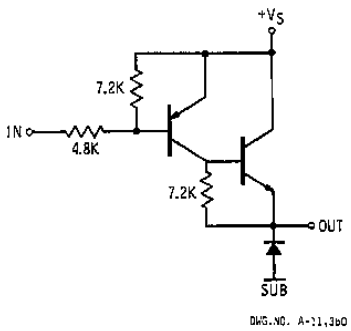
UDN-2585A

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 0 V, V_{EE} = −20 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{IN} = −0.5 V, V_{OUT} = V_{EE} = −25 V	—	50	μA
		V_{IN} = −0.4 V, V_{OUT} = V_{EE} = −25 V, T_A = 70°C	—	100	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	V_{IN} = −0.4 V, I_{OUT} = −25 mA, Note 1	15	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	V_{IN} = −4.6 V, I_{OUT} = −60 mA	—	1.1	V
		V_{IN} = −4.6 V, I_{OUT} = −120 mA	—	1.2	V
Input Current	$I_{IN(ON)}$	V_{IN} = −4.6 V, I_{OUT} = −120 mA	—	−1.6	mA
		V_{IN} = −14.6 V, I_{OUT} = −120 mA	—	−5.0	mA
Input Voltage	$V_{IN(ON)}$	I_{OUT} = −120 mA, V_{CE} ≤1.2 V, Note 3	—	−4.6	V
	$V_{IN(OFF)}$	I_{OUT} = −100 μA, T_A = 70°C	−0.4	—	V
Clamp Diode Leakage Current	I_R	V_R = 25 V, T_A = 70°C	—	50	μA
Clamp Diode Forward Voltage	V_F	I_F = 120 mA	—	2.0	V
Input Capacitance	C_{IN}		—	25	pF
Turn-On Delay	t_{PHL}	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs
Turn-Off Delay	t_{PLH}	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs

NOTES: 1. Pulsed test, t_p ≤300 μs, duty cycle ≤2%.
2. Negative current is defined as coming out of the specified device pin.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
4. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.

PARTIAL SCHEMATIC



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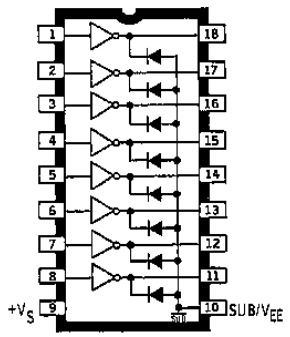
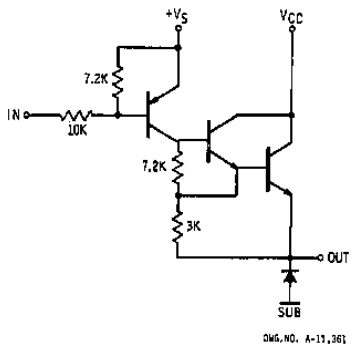


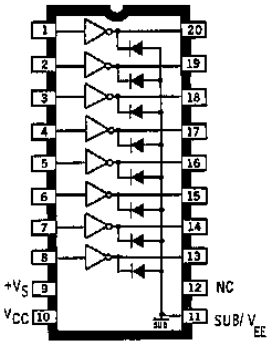
DWG.NO. A-11,359

UDN-2588A
UDN-2588A-1

PARTIAL SCHEMATIC



DWG. NO. A-11,361



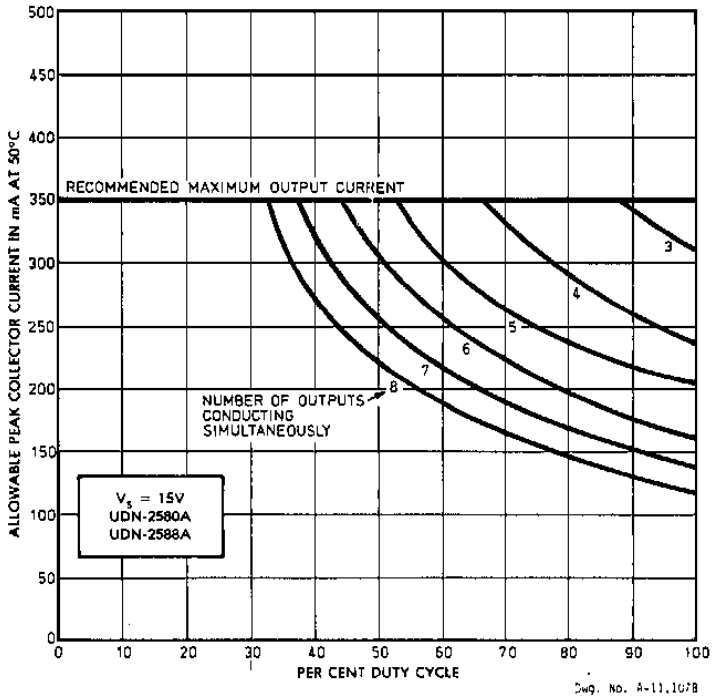
DWG. NO. A-11,357

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = 5.0 V, V_{CC} = 5.0 V, V_{EE} = −40 V (unless otherwise noted)

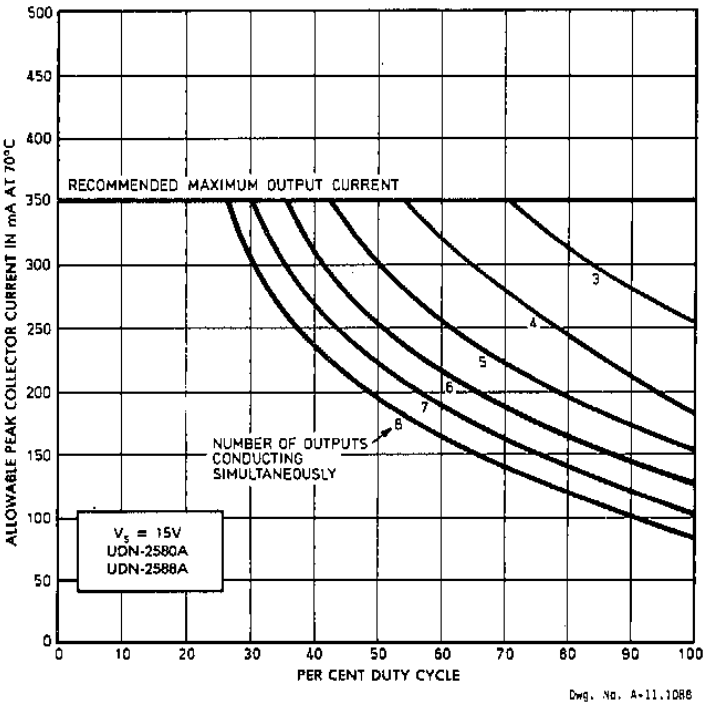
Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UDN-2588A	V_{IN} ≥4.5 V, V_{OUT} = V_{EE} = −45 V	—	50	μA
			V_{IN} ≥4.6 V, V_{OUT} = V_{EE} = −45 V, T_A = 70°C	—	100	μA
		UDN-2588A-1	V_{IN} ≥4.5 V, V_{OUT} = V_{EE} = −75 V	—	50	μA
			V_{IN} ≥4.6 V, V_{OUT} = V_{EE} = −75 V, T_A = 70°C	—	100	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	UDN-2588A	V_{IN} ≥4.6 V, I_{OUT} = −25 mA, Note 1	35	—	V
		UDN-2588A-1	V_{IN} ≥4.6 V, V_{EE} = −70 V, I_{OUT} = −25 mA, Note 1	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Both	V_{IN} = 2.6 V, I_{OUT} = −100 mA, Ref. V_{CC}	—	1.8	V
			V_{IN} = 2.0 V, I_{OUT} = −225 mA, Ref. V_{CC}	—	1.9	V
			V_{IN} = 1.4 V, I_{OUT} = −350 mA, Ref. V_{CC}	—	2.0	V
Input Current	$I_{IN(ON)}$	Both	V_{IN} = 1.4 V, I_{OUT} = −350 mA	—	−500	μA
			V_S = 15 V, V_{EE} = −30 V, V_{IN} = 0 V, I_{OUT} = −350 mA	—	−2.1	mA
	$I_{IN(OFF)}$	Both	I_{OUT} = −500 A, T_A = 70°C, Note 3	−50	—	μA
Input Voltage	$V_{IN(ON)}$	Both	I_{OUT} = −100 mA, V_{CE} ≤1.8 V, Note 4	—	2.6	V
			I_{OUT} = −225 mA, V_{CE} ≤1.9 V, Note 4	—	2.0	V
			I_{OUT} = −350 mA, V_{CE} ≤2.0 V, Note 4	—	1.4	V
	$V_{IN(OFF)}$	Both	I_{OUT} = −500 μA, T_A = 70°C	4.8	—	V
Clamp Diode Leakage Current	I_R	UDN-2588A	V_R = 50 V, T_A = 70°C	—	50	μA
		UDN-2588A-1	V_R = 80 V, T_A = 70°C	—	50	μA
Clamp Diode Forward Voltage	V_F	Both	I_F = 350 mA	—	2.0	V
Input Capacitance	C_{IN}	Both		—	25	pF
Turn-On Delay	t_{PHL}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs
Turn-Off Delay	t_{PLH}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs

NOTES: 1. Pulsed test, t_p ≤300 μs, duty cycle ≤2%.
2. Negative current is defined as coming out of the specified device pin.
3. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
4. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
5. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.
6. V_{CC} must never be more positive than V_S.

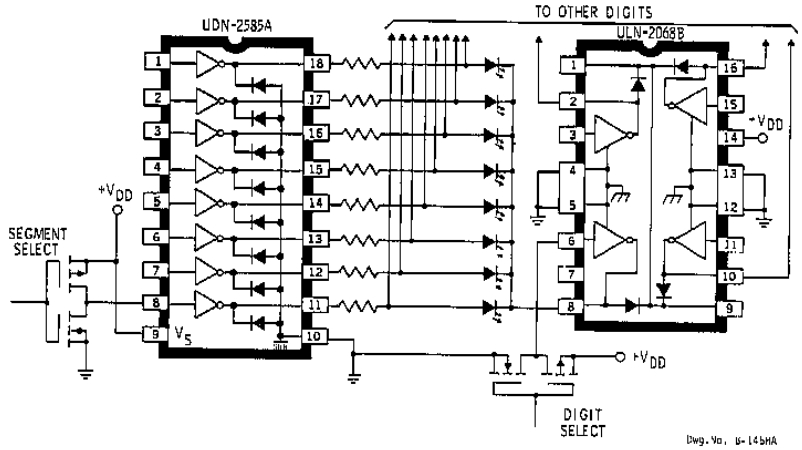
ALLOWABLE PEAK COLLECTOR CURRENT AT 50°C AS A FUNCTION OF DUTY CYCLE



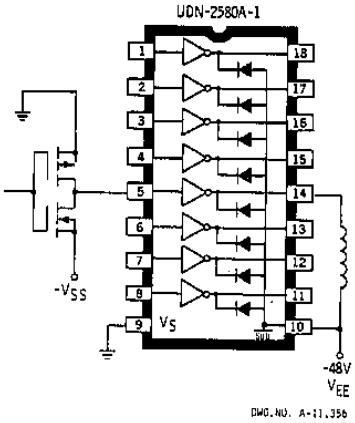
ALLOWABLE PEAK COLLECTOR CURRENT AT 70°C AS A FUNCTION OF DUTY CYCLE



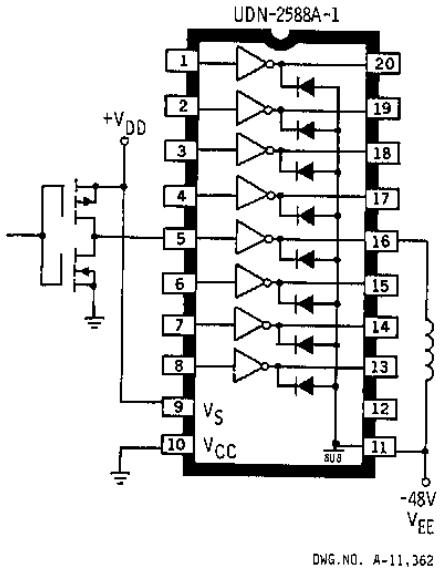
TYPICAL APPLICATIONS



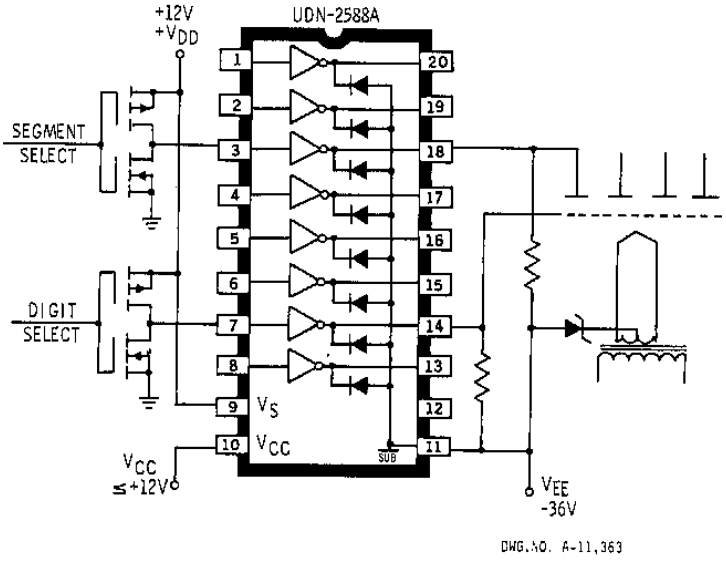
COMMON-CATHODE LED DRIVER



TELECOMMUNICATIONS RELAY DRIVER (Negative Logic)



TELECOMMUNICATIONS RELAY DRIVER (Positive Logic)

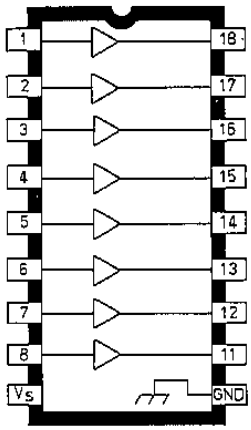


VACUUM FLUORESCENT DISPLAY DRIVER (Split Supply)

UDN-2595A
8-CHANNEL CURRENT-SINK DRIVER

FEATURES

- 200 mA Current Rating
- Low Saturation Voltage
- TTL, CMOS, NMOS Compatible
- Efficient Input/Output Pin Format
- 18-Pin Dual In-Line Plastic Package



Dwg. No. A-11,407

DEVELOPED for use with low-voltage LED and incandescent displays requiring low output saturation voltage, Type UDN-2595A meets many other interface needs, including those exceeding the capabilities of standard logic buffers.

The eight non-Darlington outputs of this driver can simultaneously sink load currents of 100 mA at ambient temperatures of up to +85°C.

The eight-channel driver's active low inputs can be linked directly to TTL, Schottky TTL, DTL, 5 to 16 V CMOS, and NMOS logic. All input connections are on one side of the package, output connections on the other, for simplified layout of printed wiring boards.

Type UDN-2595A is supplied in an 18-pin dual-in-line plastic package with a copper lead frame that maximizes the driver's power-handling capabilities. A hermetically sealed version of Type UDN-2595A, with reduced package power dissipation ratings, is available on special order.

This device complements Sprague Type UDN-2585A, an eight-channel source driver.

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature

for any one driver
(unless otherwise noted)

Output Voltage, V_{CE} ..... 20 V
Supply Voltage, V_S ..... 20 V
Input Voltage, V_{IN} ..... 20 V
Output Collector Current, I_C ..... 200 mA
Ground Terminal Current, I_{GND} ..... 1.6 A
Allowable Power Dissipation, P_D
(single output) ..... 1.0 W
(total package) ..... 2.2 W*
Operating Temperature Range, T_A ..... −20°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +150°C

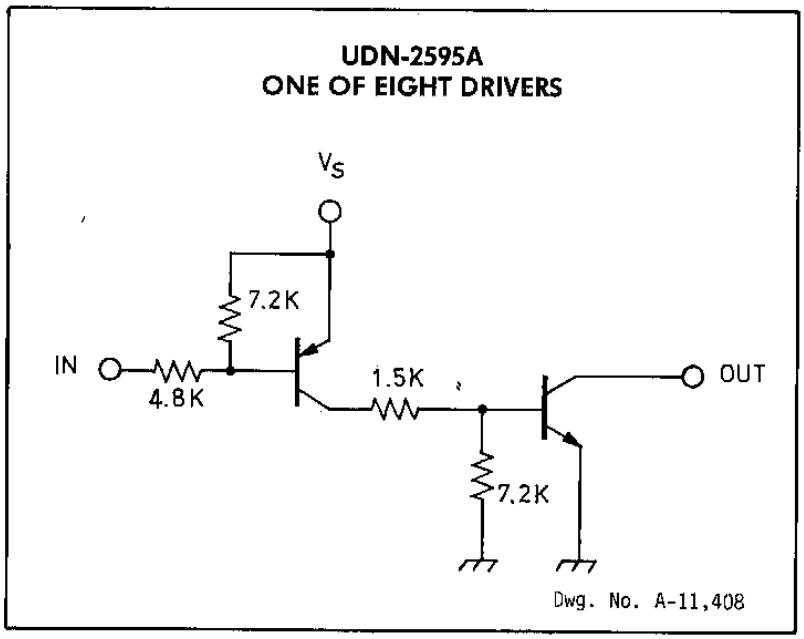
*Derate at the rate of 18 mW/°C above +25°C.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_S = 5.0$ V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{IN} \geq 4.5$ V, $V_{OUT} = 20$ V, $T_A = 25°C$	—	50	μA
		$V_{IN} \geq 4.6$ V, $V_{OUT} = 20$ V, $T_A = 70°C$	—	100	μA
Output Saturation Voltage	$V_{CE(SAT)}$	$V_{IN} = 0.4$ V, $I_{OUT} = 50$ mA	—	0.5	V
		$V_{IN} = 0.4$ V, $I_{OUT} = 100$ mA	—	0.6	V
Input Current	$I_{IN(ON)}$	$V_{IN} = 0.4$ V, $I_{OUT} = 100$ mA	—	−1.6	mA
		$V_{IN} = 0.4$ V, $I_{OUT} = 100$ mA, $V_S = 15$ V	—	−5.0	mA
Input Voltage	$V_{IN(ON)}$	$I_{OUT} = 100$ mA, $V_{OUT} \leq 0.6$ V, $V_S = 5$ V	—	0.4	V
	$V_{IN(OFF)}$	$I_{OUT} = 100$ μA, $T_A = 70°C$	4.6	—	V
Input Capacitance	C_{IN}		—	25	pF
Supply Current	I_{SS}	$V_{IN} = 0.4$ V, $I_{OUT} = 100$ mA	—	6.0	mA
		$V_{IN} = 0.4$ V, $I_{OUT} = 100$ mA, $V_S = 15$ V	—	20	mA

NOTES:
1. Negative current is defined as coming out of the specified device pin.
2. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified conditions.
3. I_{SS} is measured with any one of eight drivers turned ON.

3



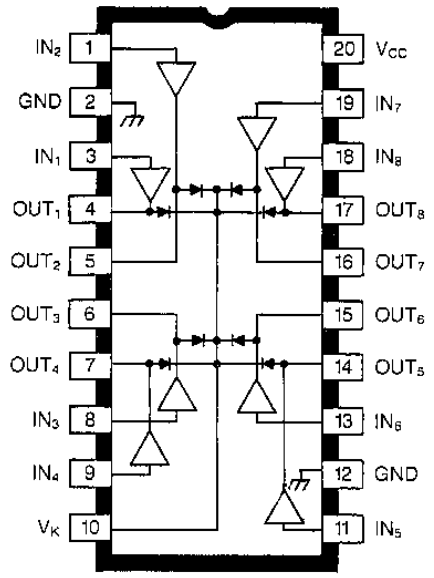
UDN-2596A THROUGH UDN-2599A
8-CHANNEL SATURATED SINK DRIVERS

FEATURES

- Low Output ON Voltages
- Up to 1.0A Sink Capability
- 50V Min. Output Breakdown
- Output Transient-Suppression Diodes
- Output Pull-Down for Fast Turn-Off
- TTL, CMOS Compatible Inputs

Low output saturation voltages at high load currents are provided by UDN-2596A through UDN-2599A sink driver ICs. These devices can be used as interface buffers between standard low-power digital logic (particularly MOS) and high-power loads such as relays, solenoids, stepping motors, and LED or incandescent displays. The eight saturated sink drivers in each device feature high-voltage, high-current open-collector outputs. Transient suppression clamp diodes and a minimum 35V output sustaining voltage allow their use with many inductive loads.

The saturated (non-Darlington) NPN outputs provide low collector-emitter voltage drops as well as improved turn-off times due to an active pull-down function within the output predrive section. The UDN-2596A and UDN-2598A are for use with output loads to 500mA while the UDN-2597A and UDN-2599A are for use with loads to 1A. Adjacent outputs may be paralleled for higher load currents.

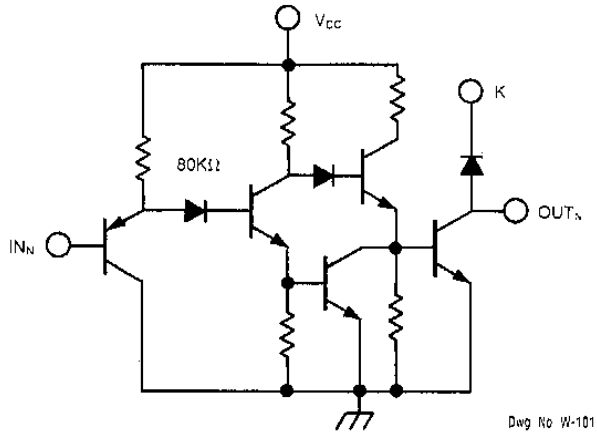


Dwg. No. W-100

Inputs require very low input current and are activated by a low logic level consistent with the much greater sinking capability associated with NMOS, CMOS, and TTL logic. The UDN-2596A and UDN-2597A are rated for use with 5V logic levels while the UDN-2598A and UDN-2599A are for use with 10V to 12V logic levels.

All devices are furnished in 20-pin DIP packages with copper leadframes for improved thermal characteristics.

ONE OF EIGHT DRIVERS



Dwg No W-101

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Output Voltage, V_{CE} 50V
Output Current, I_{OUT}
(UDN-2596/98A) 500mA
(UDN-2597/99A) 1.0A
Supply Voltage, V_{CC}
(UDN-2596/97A) 7.0V
(UDN-2598/99A) 15V
Input Voltage, V_{IN}
(UDN-2596/97A) 7.0V
(UDN-2598/99A) 15V
Package Power Dissipation, P_D 2.27W*
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −65°C to +150°C

*Derate at the rate of 18.2mW/°C above T_A = 25°C.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 5.0V$ (UDN-2596/97A) or 12V (UDN-2598/99A)

Characteristics	Symbol	Applicable Devices*	Test Conditions	Limits		
				Min.	Max.	Units
Output Leakage Current	I_{CEX}	All	$V_{OUT} = 50V$, $V_{IN} = 2.4V$	—	10	µA
Output Sustaining Voltage	$V_{CE(sus)}$	2596/98	$I_{OUT} = 300mA$, L = 2mH	35	—	V
		2597/99	$I_{OUT} = 750mA$, L = 2mH	35	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	2596/98	$I_{OUT} = 300mA$	—	0.5	V
		2597/99	$I_{OUT} = 750mA$	—	1.0	V
Clamp Diode Leakage Current	I_R	All	$V_R = 50V$	—	10	µA
Clamp Diode Forward Voltage	V_F	2596/98	$I_F = 300mA$	—	1.8	V
		2597/99	$I_F = 750mA$	—	1.8	V
Logic Input Current	$I_{IN(0)}$	2596/97	$V_{IN} = 0.8V$	—	−15	µA
		2598/99	$V_{IN} = 0.8V$	—	−50	µA
	$I_{IN(1)}$	2596/97	$V_{IN} = 2.4V$	—	10	µA
		2598/99	$V_{IN} = 12V$	—	10	µA
Supply Current (per driver)	$I_{CC(ON)}$	2596/98	$V_{IN} = 0.8V$	—	6.0	mA
		2597/99	$V_{IN} = 0.8V$	—	22	mA
	$I_{CC(OFF)}$	2596/97	$V_{IN} = 2.4V$	—	1.3	mA
		2598/99	$V_{IN} = 2.4V$	—	2.0	mA
Turn-On Delay	t_{pd0}	All	$0.5E_{IN}$ to $0.5E_{OUT}$	—	3.0	µs
Turn-Off Delay	t_{pd1}	All	$0.5E_{IN}$ to $0.5E_{OUT}$	—	2.0	µs

*Complete part number includes prefix UDN- and suffix A, e.g. UDN-2596A.

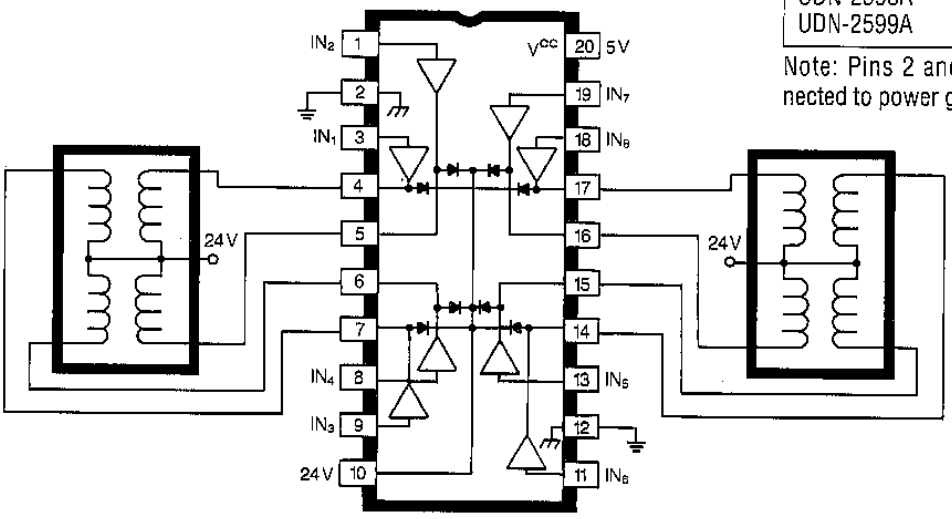
3

RECOMMENDED OPERATING CONDITIONS

Type Number	Logic	I_{OUT}
UDN-2596A	5.0V	300mA
UDN-2597A	5.0V	750mA
UDN-2598A	10-12V	300mA
UDN-2599A	10-12V	750mA

Note: Pins 2 and 12 must both be connected to power ground.

TYPICAL APPLICATION
DUAL STEPPER MOTOR DRIVE



Dwg. No. W-102A

SERIES ULN-2800A
HIGH-VOLTAGE, HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAYS

IDEALLY SUITED for interfacing between low-level digital logic circuitry and high-power peripheral loads, the Series ULN-2800A high-voltage, high-current Darlington transistor arrays feature peak load current ratings of 600 mA (Series ULN-2800A and ULN-2820A) or 750 mA (Series ULN-2810A) for each of the eight drivers in each device. Under the proper conditions, high-power loads of up to 4 A at 50V (200 W at 23% duty cycle) or 3.2 A at 95 V (304 W at 33% duty cycle) can be controlled. Typical loads include relays, solenoids, stepping motors, multiplexed LED and incandescent displays, and heaters. All devices feature open collector outputs and integral diodes for inductive load transient suppression.

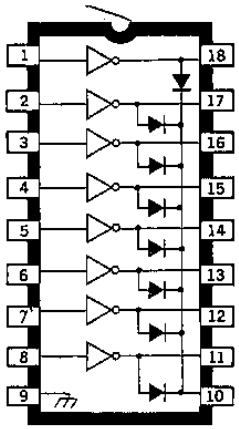
The Series ULN-2801A devices are general purpose arrays which may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate ease of circuit board layout and are priced to compete directly with discrete transistor alternatives.

The Series ULN-2802A was specifically designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also means excellent noise immunity for these devices.

The Series ULN-2803A has a 2.7 kΩ series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs – particularly those beyond the capabilities of standard logic buffers.

The Series ULN-2804A features a 10.5 kΩ series input resistor to permit their operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of the Series ULN-2803A while the required input voltage is less than that required by the Series ULN-2802A.

The Series ULN-2805A is especially designed for use with standard and Schottky TTL where higher output currents are required and loading of the logic output is not a concern. These devices will sink a minimum of 350 mA when driven from a "totem pole" logic output.



DWG. NO. A-10,322

The Series ULN-2800A is the standard high-voltage, high-current Darlington array. The output transistors are capable of sinking 500mA and will withstand at least 50 V in the OFF state. Outputs may be paralleled for higher load current capability. The Series ULN-2810A devices are similar except that they will sink 600mA. The Series ULN-2820A will withstand 95 V in the OFF state.

All Series ULN-2800A Darlington arrays are furnished in an 18-pin dual in-line plastic package.

Device Type Number Designation

$V_{CE(MAX)}$ = $I_{C(MAX)}$ =	50 V 500 mA	50 V 600 mA	95 V 500 mA
	Type Number		
General Purpose PMOS, CMOS	ULN-2801A	ULN-2811A	ULN-2821A
14 - 25 V PMOS	ULN-2802A	ULN-2812A	ULN-2822A
5 V TTL, CMOS	ULN-2803A	ULN-2813A	ULN-2823A
6 - 15 V CMOS, PMOS	ULN-2804A	ULN-2814A	ULN-2824A
High Output TTL	ULN-2805A	ULN-2815A	ULN-2825A

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature for any one Darlington pair (unless otherwise noted)

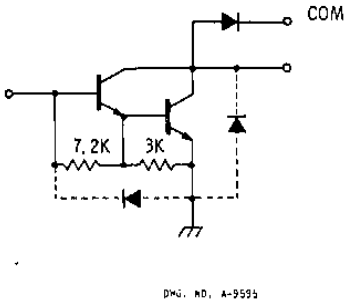
Output Voltage, V_{CE} (Series ULN-2800, 2810A)	50 V
(Series ULN-2820A)	95 V
Input Voltage, V_{IN} (Series ULN-2802, 2803, 2804A)	30 V
(Series ULN-2805A)	15 V
Continuous Collector Current, I_C (Series ULN-2800, 2820A)	500 mA
(Series ULN-2810A)	600 mA
Continuous Base Current, I_B	25 mA
Power Dissipation, P_D (one Darlington pair)	1.0 W
(total package)	2.25 W*
Operating Ambient Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 18.18mW/°C above 25°C.

Under normal operating conditions, these devices will sustain 350 mA per output with $V_{CE(SAT)}$ = 1.6 V at 50°C with a pulse width of 20 ms and a duty cycle of 40%.

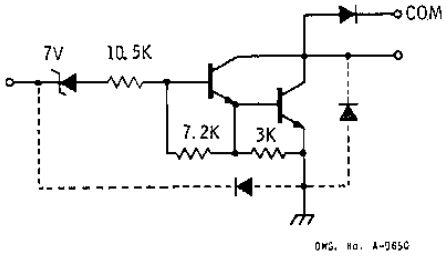
3

PARTIAL SCHEMATICS



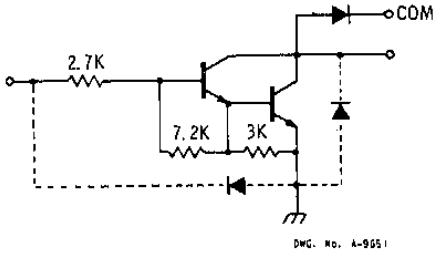
DWG. NO. A-9595

Series ULN-2801A
(each driver)



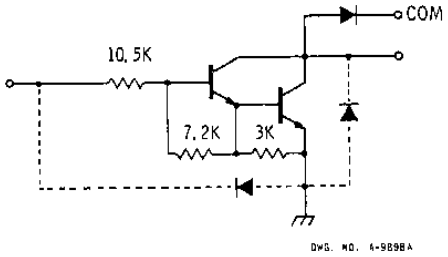
DWG. NO. A-9650

Series ULN-2802A
(each driver)



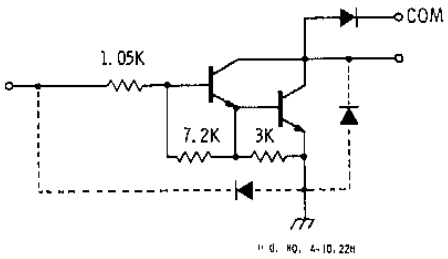
DWG. NO. A-9651

Series ULN-2803A
(each driver)



DWG. NO. A-9898A

Series ULN-2804A
(each driver)



DWG. NO. A-10,228

Series ULN-2805A
(each driver)

SERIES ULN-2800A

ELECTRICAL CHARACTERISTICS at 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 50 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2802A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2804A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 μA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2802A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2803A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2804A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2805A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2802A	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
			ULN-2803A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN-2804A	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
			ULN-2805A	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2801A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
Input Capacitance	C_{IN}	–	All		—	15	25	pF
Turn-On Delay	t_{ON}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{OFF}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	μA
				V_R = 50 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

SERIES ULN-2810A

ELECTRICAL CHARACTERISTICS at 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 50 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2812A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2814A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
				I_C = 500 mA, I_B = 600 μA	—	1.7	1.9	V
Input Current	$I_{IN(ON)}$	3	ULN-2812A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2813A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2814A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2815A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2812A	V_{CE} = 2.0 V, I_C = 500 mA	—	-	17	V
			ULN-2813A	V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	—	—	3.5	V
			ULN-2814A	V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	—	—	9.5	V
			ULN-2815A	V_{CE} = 2.0 V, I_C = 500 mA	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2811A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
				V_{CE} = 2.0 V, I_C = 500 mA	900	—	—	
Input Capacitance	C_{IN}	-	All		—	15	25	pF
Turn-On Delay	t_{ON}	-	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{OFF}	-	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	μA
				V_R = 50 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V
				I_F = 500 mA	—	2.1	2.5	V

3

SERIES ULN-2820A

ELECTRICAL CHARACTERISTICS at 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			Units
					Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 95 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 95 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2822A	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2824A	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 μA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2822A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2823A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2824A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2825A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2822A	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
			ULN-2823A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN-2824A	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
			ULN-2825A	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2821A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
Input Capacitance	C_{IN}		All		—	15	25	pF
Turn-On Delay	t_{ON}		All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{OFF}		All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 95 V, T_A = 25°C	—	—	50	μA
				V_R = 95 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

TEST FIGURES

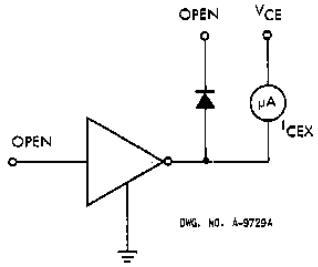


FIGURE 1A

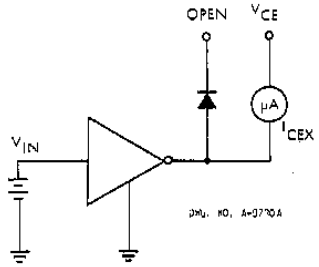


FIGURE 1B

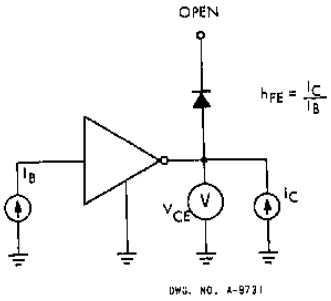


FIGURE 2

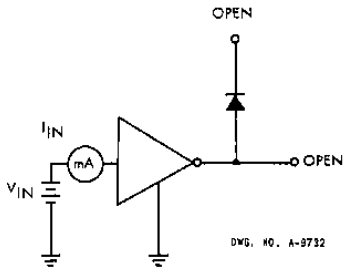


FIGURE 3

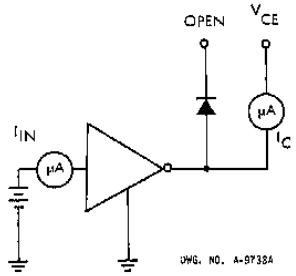


FIGURE 4

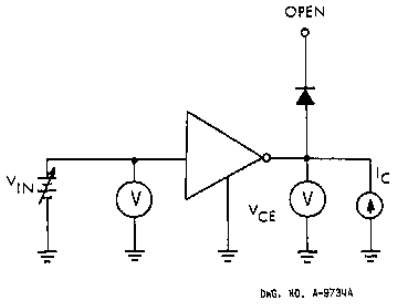


FIGURE 5

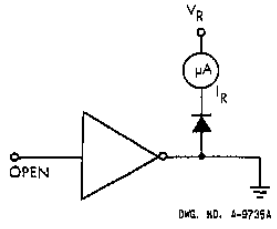


FIGURE 6

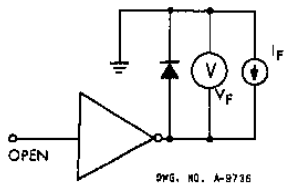
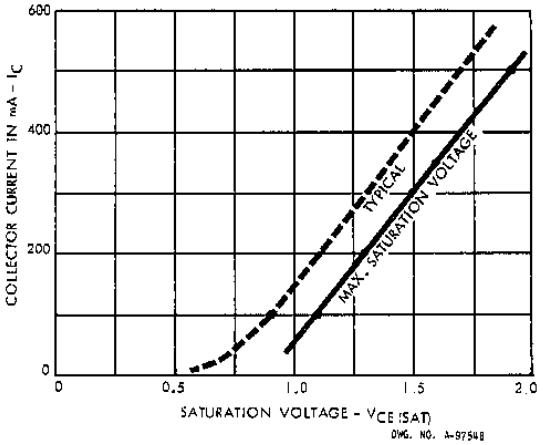
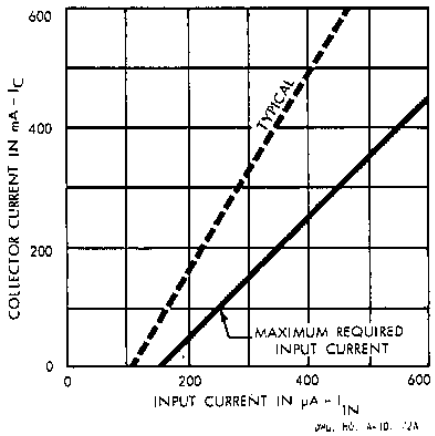


FIGURE 7

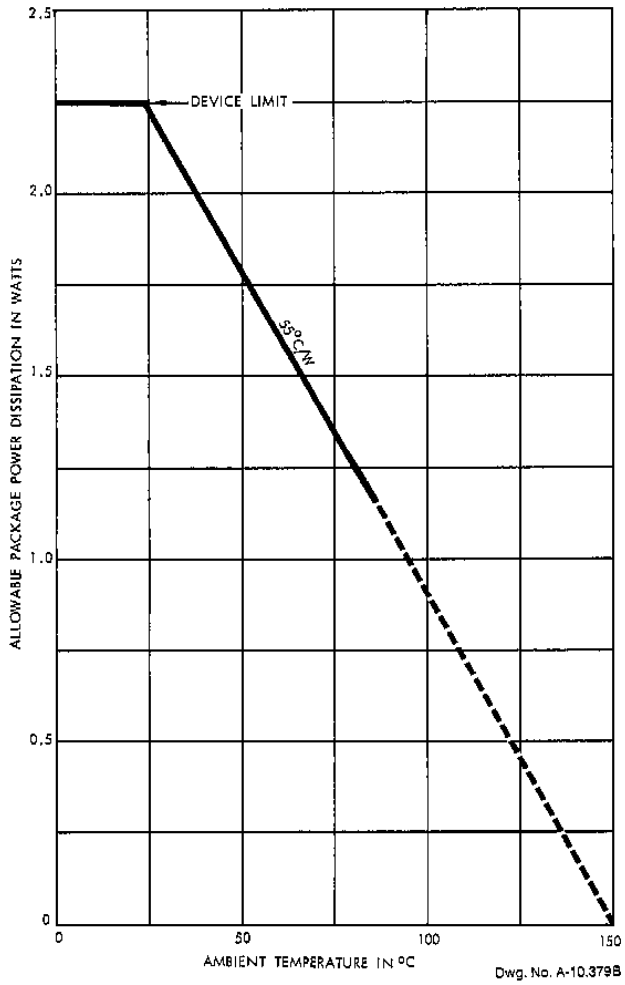
COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



ALLOWABLE AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



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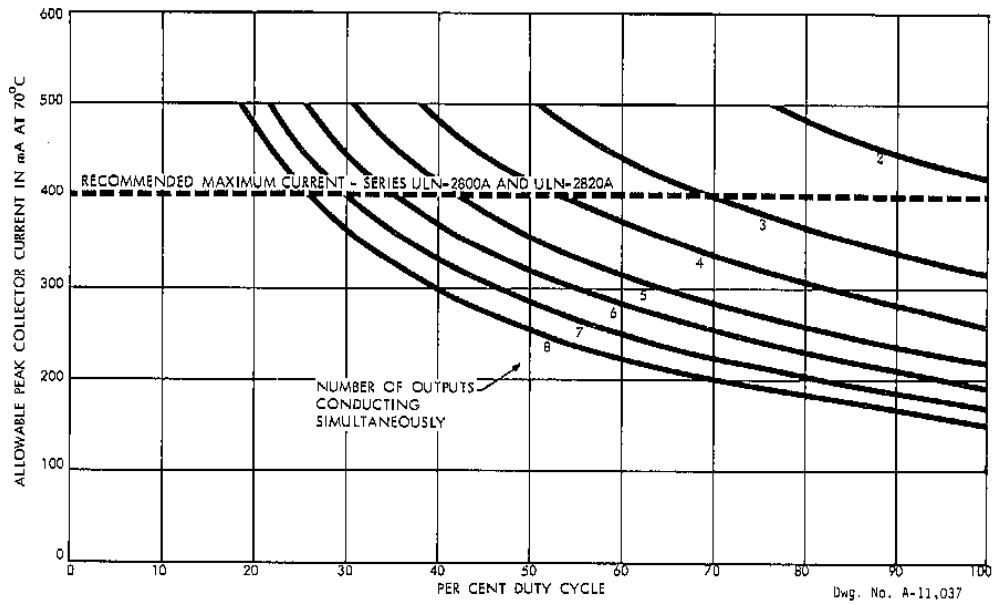
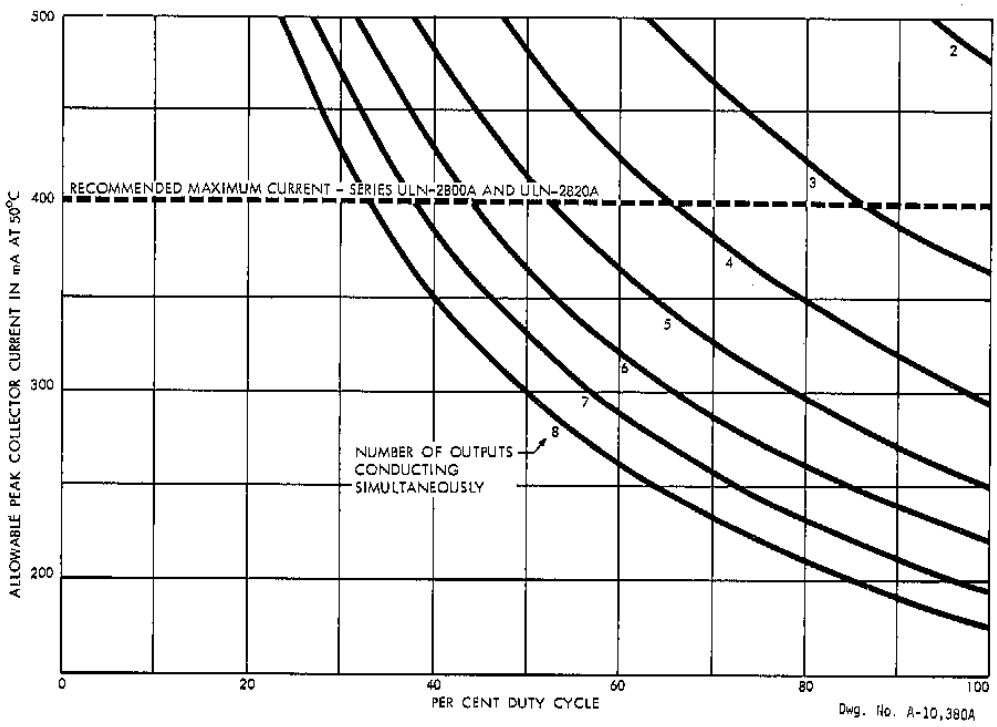
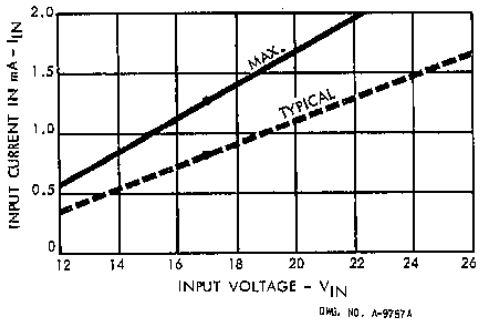
PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

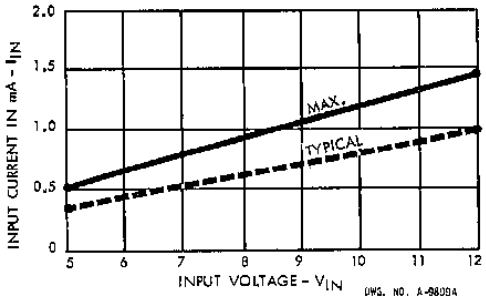




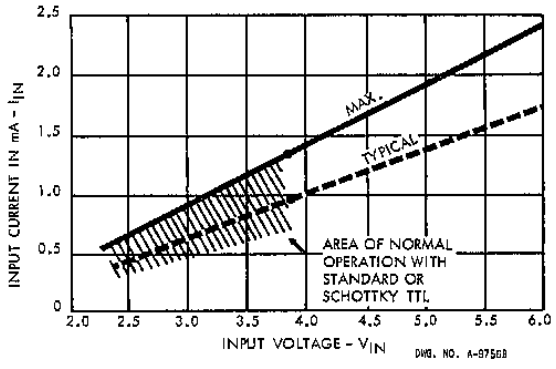
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



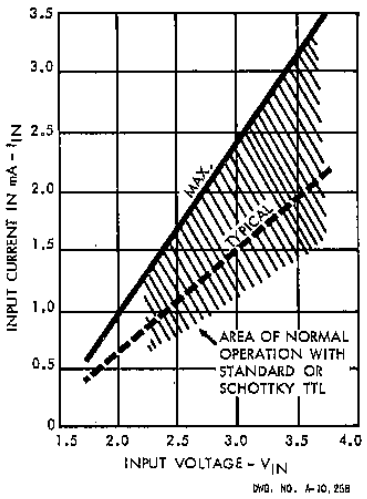
SERIES ULN-2802A



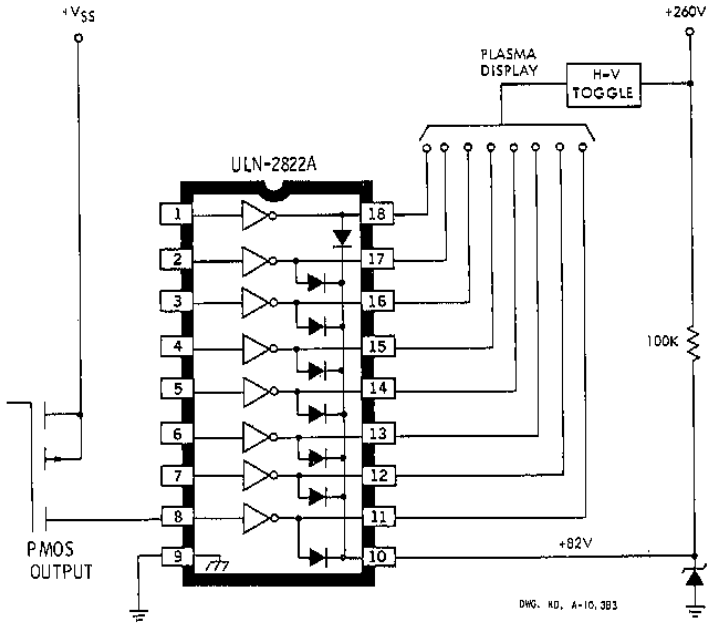
SERIES ULN-2804A



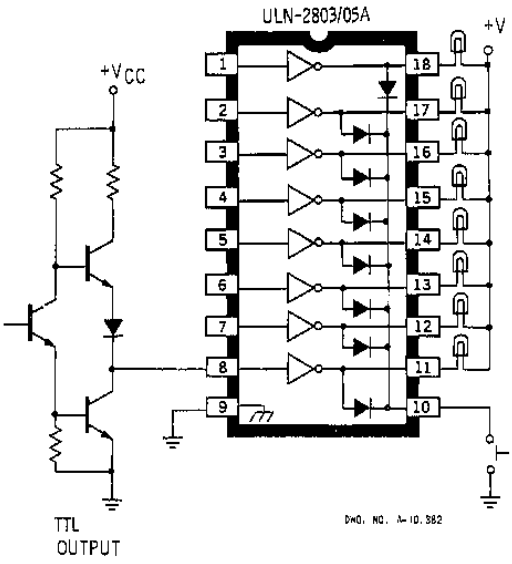
SERIES ULN-2803A



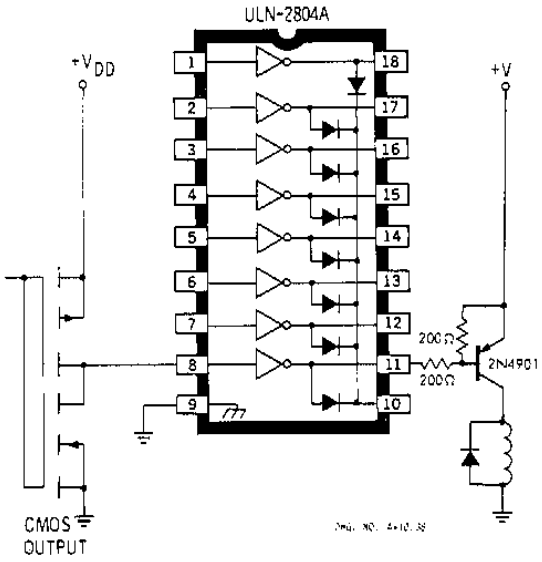
SERIES ULN-2805A



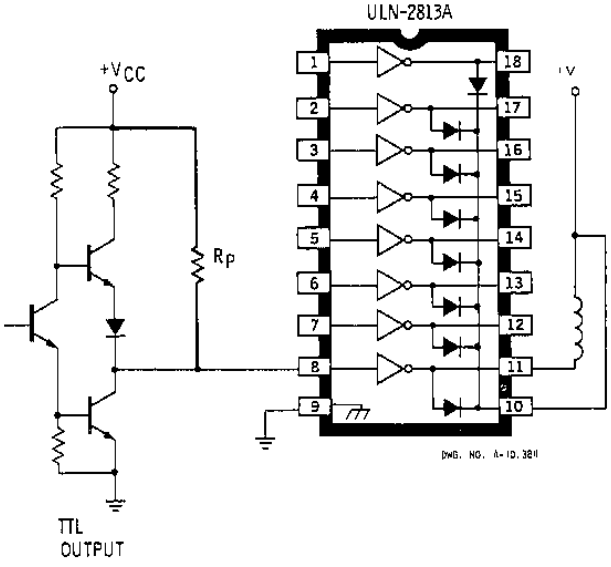
OFF VOLTAGE BIAS FOR HIGH-VOLTAGE LOADS



TTL TO LOAD

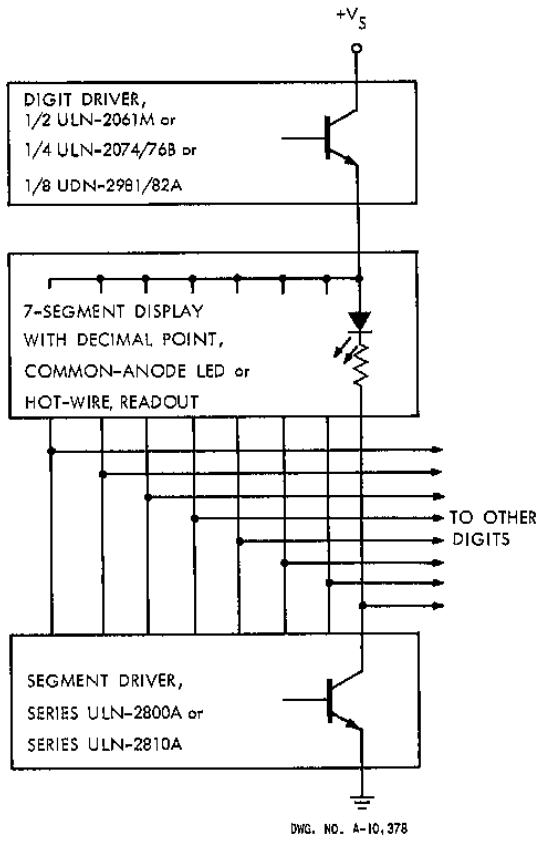


BUFFER FOR HIGHER CURRENT LOADS



USE OF PULL-UP RESISTORS TO INCREASE DRIVE CURRENT

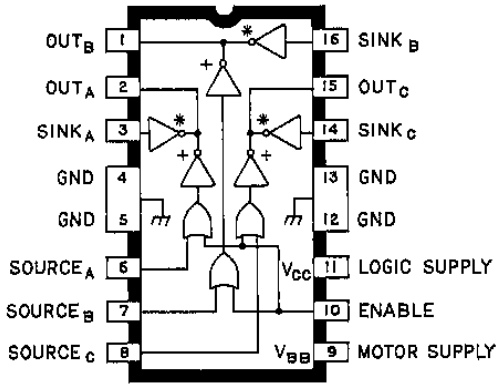
TYPICAL DISPLAY INTERFACE



UDN-2933B AND UDN-2934B
3-CHANNEL HALF-BRIDGE MOTOR DRIVERS

FEATURES

- Output Currents to 1 A
- Output Voltages to 30 V
- Low Output-Saturation Voltage
- Transient-Protected Outputs
- Tri-State Outputs
- TTL or CMOS Compatible Inputs
- Reliable Monolithic Construction



Dwg. No. A-12,356

DEVELOPED for use in 3-phase brushless d-c motor applications, Types UDN-2933B and UDN-2934B provide drive capabilities to 1 A and 30 V. Saturated drivers provide for low output voltage drops at maximum rated current.

The 1 A half-bridge drivers differ only in input circuitry: Type UDN-2933B is compatible with TTL and 5 V CMOS; Type UDN-2934B is used with 12 V CMOS.

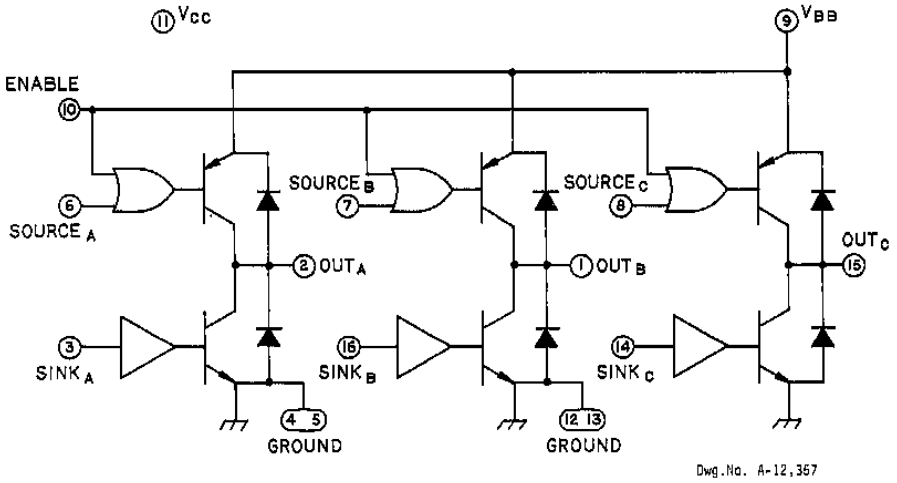
Monolithic construction and a 16-pin dual in-line package with centered heat-sink contact tabs enable cost-effective and reliable systems designs supported by excellent power dissipation ratings, minimum size, and ease of installation. The package configuration allows easy attachment of an inexpensive heat sink. It fits a standard IC socket or printed wiring board layout.

Half-bridge drivers with Darlington outputs (Type UDN-2935Z and UDN-2950Z) are supplied in TO-220 power-tab packages for operation with load currents of up to 3.5 A.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Motor Supply Voltage, V_{BB} . . . . . 30 V
Logic Supply Voltage Range, V_{CC}
(UDN-2933B) . . . . . 4.5 V to 7.0 V
(UDN-2934B) . . . . . 10 V to 15 V
Logic Input Voltage, V_{IN} . . . . . V_{CC}
Output Current, I_{OUT} . . . . . ±1.0 A
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

FUNCTIONAL BLOCK DIAGRAM

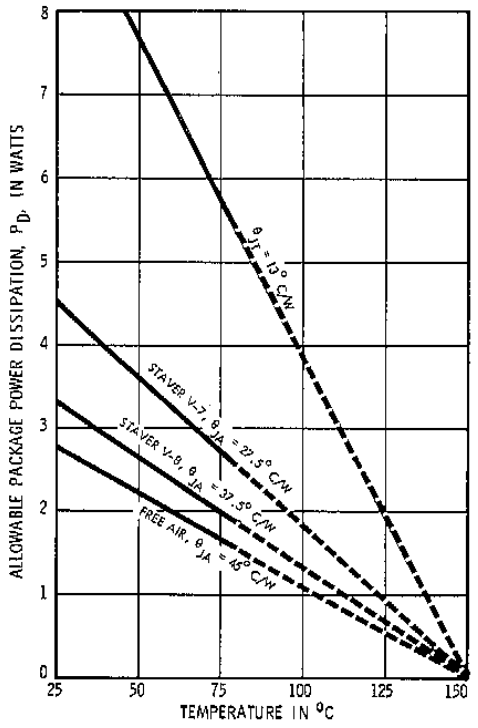


Dwg.No. A-12,367

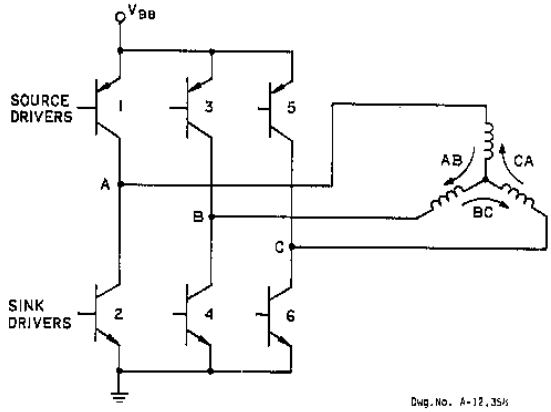
TRUTH TABLE

Sink Driver Input	Source Driver Input	Enable Input	Output
Low	Low	Low	High
Low	High	Low	Open
High	Low	Low	Disallowed
High	High	Low	Low
High	Any	High	Low
Low	Any	High	Open

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-11,793A



Dwg.No. A-12,354

TYPICAL COMMUTATION SEQUENCE

Drivers ON*	Motor Current	Elec. Degrees
1+4	AB	0
1+6	−CA	60
3+6	BC	120
3+2	−AB	180
5+2	CA	240
5+4	−BC	300

*Enable input must be low; Source drivers are turned ON with a logic low, sink drivers are turned ON with a logic high.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 30$ V, $V_{CC} = 5$ V (UDN-2933B) or $V_{CC} = 12$ V (UDN-2934B), $T_{TAB} \leq +70°C$

Characteristic	Symbol	Applicable Devices	Test Condtions	Limits			
				Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	Both	All Drivers OFF, $V_{OUT} = 0$ V	—	−5.0	−100	μA
			All Drivers OFF, $V_{OUT} = 30$ V	—	5.0	100	μA
Output Saturation Voltage	$V_{CE(SAT)}$	Both	$I_{OUT} = -100$ mA	—	0.80	1.1	V
			$I_{OUT} = 100$ mA	—	0.08	0.2	V
			$I_{OUT} = -250$ mA	—	0.90	1.2	V
			$I_{OUT} = 250$ mA	—	0.13	0.3	V
			$I_{OUT} = -500$ mA	—	1.1	1.5	V
			$I_{OUT} = 500$ mA	—	0.25	0.6	V
			$I_{OUT} = -800$ mA	—	1.3	1.8	V
			$I_{OUT} = 800$ mA	—	0.45	0.8	V
Output Sustaining Voltage	$V_{CE(SUS)}$	Both	$I_{OUT} = \pm 800$ mA, L = 3 mH	30	—	—	V
Motor Supply Current	I_{BB}	Both	All Drivers OFF	—	50	200	μA
			1 Source + 1 Sink ON, No Loads	—	1.0	1.3	mA
Clamp Diode Forward Voltage	V_F	Both	$I_F = 500$ mA	—	1.3	2.0	V
			$I_F = 800$ mA	—	1.3	2.0	V
Logic Input Voltage	$V_{IN(1)}$	UDN-2933B		2.4	—	—	V
		UDN-2934B		8.0	—	—	V
	$V_{IN(0)}$	UDN-2933B		—	—	0.8	V
		UDN-2934B		—	—	4.0	V
Logic Input Current	$I_{IN(1)}$	UDN-2933B	$V_{IN} = 2.4$ V	—	<1.0	10	μA
		UDN-2934B	$V_{IN} = 8.0$ V	—	<1.0	10	μA
	$I_{IN(0)}$	Both	$V_{IN} = 0.8$ V	—	−50	−300	μA
Logic Supply Current	I_{CC}	Both	All Drivers OFF	—	1.7	3.0	mA
			1 Source + 1 Sink ON	—	30	40	mA
Output Rise Time	t_r	Both	$I_{OUT} = -500$ mA, $V_{BB} = 20$ V	—	250	—	ns
			$I_{OUT} = 500$ mA, $V_{BB} = 20$ V	—	30	—	ns
Output Fall Time	t_f	Both	$I_{OUT} = -500$ mA, $V_{BB} = 20$ V	—	500	—	ns
			$I_{OUT} = 500$ mA, $V_{BB} = 20$ V	—	50	—	ns

NOTES: 1. Each driver is tested separately.
2. Positive (negative) current is defined as going into (coming out of) the specified device pin.

UDN-2956A AND UDN-2957A
HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

FEATURES

- 500 mA Output Source Current
- 50 V Output Sustaining Voltage
- Output Transient Protection
- 6-16 V PMOS,CMOS Input—UDN-2956A
- TTL, DTL, 5 V CMOS Input—UDN-2957A
- Plastic or Cer-DIP Package

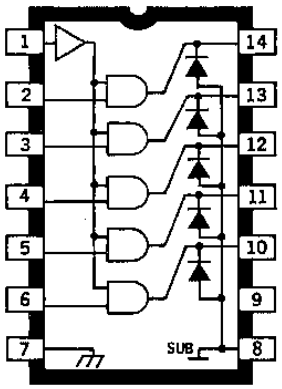
COMPRISED of five common-collector NPN Darlington output stages, associated common-base PNP input stages, and a common ENABLE stage, the UDN-2956A and UDN-2957A high-voltage, high-current source drivers are used to switch the ground end of loads that are directly connected to a negative supply. Typical loads include telephone relays, PIN diodes, and LEDs.

Both devices will sustain output OFF voltages of −80 V and will source currents to −500 mA per driver. Under normal operating conditions, these units will sustain load currents of −200 mA on each of the five drivers simultaneously at ambient temperatures up to +70°C.

The UDN-2956A driver is intended for use with MOS (PMOS or CMOS) logic input levels operating with supply voltages from 6 V to 16 V. The UDN-2957A driver has appropriate input-current limiting resistors for operation from TTL, Schottky TTL, DTL, and 5 V CMOS. With either device, the input and ENABLE levels must both be biased towards the positive supply to activate the output load.

Integral transient-suppression diodes allow these devices to be used with inductive loads without adding discrete diodes. In order to maintain isolation between drivers, the substrate should be connected to the most negative supply.

Input connections are on one side of the dual in-line package, output connections on the other side to simplify printed wiring board layout.



Dwg. No. A-10,229A

The UDN-2956A and UDN-2957A high-voltage, high-current drivers are supplied in 14-lead dual in-line packages conforming to JEDEC outline TO-116 (MO-001AA). These devices can also be ordered in ceramic/glass (cer-DIP) hermetic packages by changing the last character of the part number from 'A' to 'R.' Except for slightly reduced package power dissipation capability, devices in cer-DIP hermetic packages have electrical ratings identical to those in plastic packages and are pin compatible with them.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
(Reference Pin 7)

Supply Voltage, V_{EE}	−80 V
Input Voltage, V_{IN} (UDN-2956A)	+20 V
(UDN-2957A)	+10 V
Output Current, I_{OUT}	−500 mA
Power Dissipation, P_D (any one driver)	1.0 W
(total package)	2.0 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

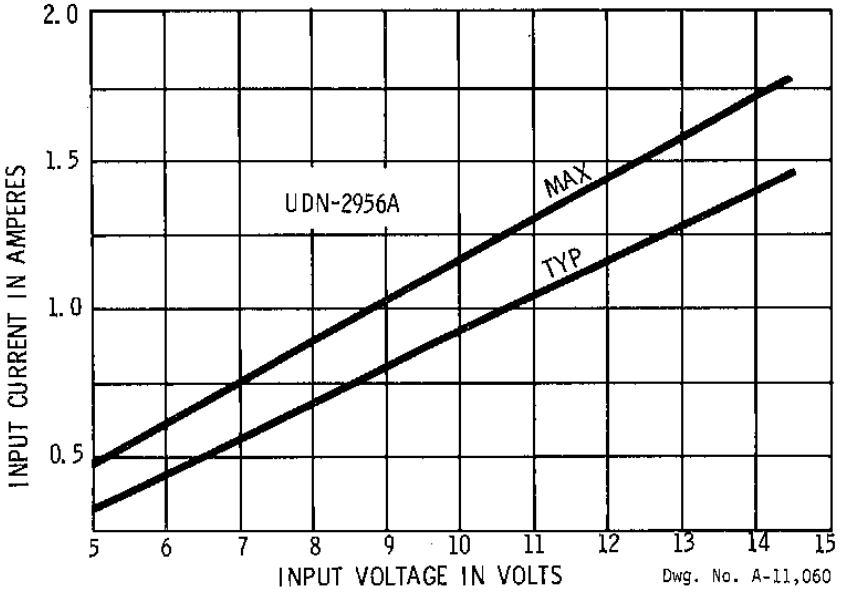
*Derate at the rate of 16.67 mW/°C above 25°C.

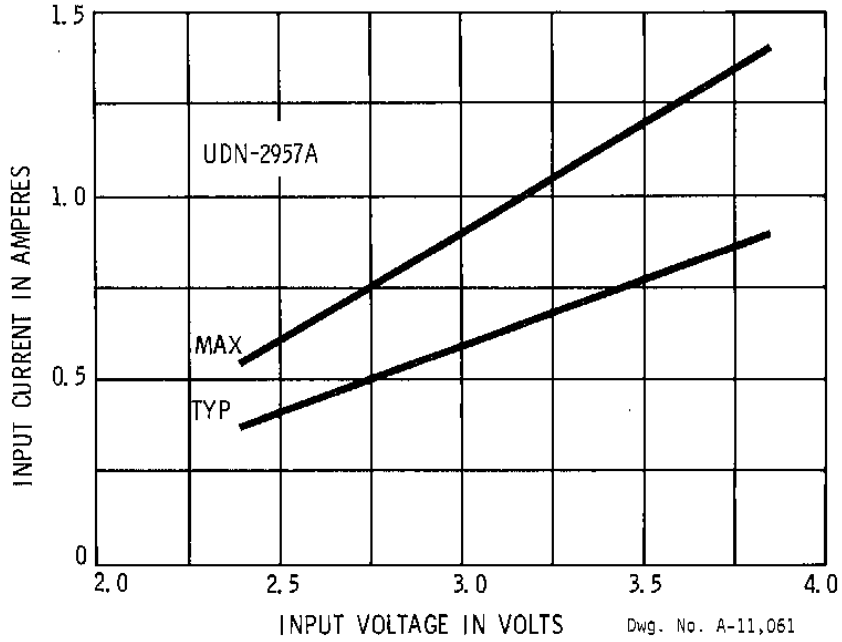
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{ENABLE} = V_{IN}$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limit
Output Leakage Current	I_{CEX}	UDN-2956A	$V_{IN} = V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
			$V_{IN} = 0.4$ V, $V_{ENABLE} = 15$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
			$V_{IN} = 15$ V, $V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
		UDN-2957A	$V_{IN} = V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
			$V_{IN} = 0.4$ V, $V_{ENABLE} = 3.85$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
			$V_{IN} = 3.85$ V, $V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = 70°C$	−200 μA Max.
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	UDN-2956A	$V_{IN} = 6.0$ V, $I_{OUT} = -100$ mA	− 1.20 V Max.
			$V_{IN} = 7.0$ V, $I_{OUT} = -175$ mA	− 1.35 V Max.
			$V_{IN} = 10$ V, $I_{OUT} = -350$ mA	− 1.70 V Max.
		UDN-2957A	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	− 1.20 V Max.
			$V_{IN} = 2.7$ V, $I_{OUT} = -175$ mA	− 1.35 V Max.
			$V_{IN} = 3.9$ V, $I_{OUT} = -350$ mA	− 1.70 V Max.
Input Current	$I_{IN(ON)}$	UDN-2956A	$V_{IN} = 6.0$ V, $V_{OUT} = -2.0$ V	650 μA Max.
			$V_{IN} = 15$ V, $V_{OUT} = -2.0$ V	1.85 mA Max.
		UDN-2957A	$V_{IN} = 2.4$ V, $V_{OUT} = -2.0$ V	675 μA Max.
			$V_{IN} = 3.85$ V, $V_{OUT} = -2.0$ V	1.40 mA Max.
	$I_{IN(OFF)}$	ALL	$I_{OUT} = -500$ μA, $T_A = +70°C$	50 μA Min.
Output Source Current	I_{OUT}	UDN-2956A	$V_{IN} = 5.0$ V, $V_{OUT} = -2.0$ V	−125 mA Min.
			$V_{IN} = 6.0$ V, $V_{OUT} = -2.0$ V	−200 mA Min.
			$V_{IN} = 7.0$ V, $V_{OUT} = -2.0$ V	−250 mA Min.
			$V_{IN} = 8.0$ V, $V_{OUT} = -2.0$ V	−300 mA Min.
			$V_{IN} = 9.0$ V, $V_{OUT} = -2.0$ V	−350 mA Min.
		UDN-2957A	$V_{IN} = 2.4$ V, $V_{OUT} = -2.0$ V	−125 mA Min.
			$V_{IN} = 2.7$ V, $V_{OUT} = -2.0$ V	−200 mA Min.
			$V_{IN} = 3.0$ V, $V_{OUT} = -2.0$ V	−250 mA Min.
			$V_{IN} = 3.3$ V, $V_{OUT} = -2.0$ V	−300 mA Min.
			$V_{IN} = 3.6$ V, $V_{OUT} = -2.0$ V	−350 mA Min.
Output Sustaining Voltage	$V_{CE(SUS)}$	UDN-2956A	$V_{IN} = 0.4$ V, $I_{OUT} = -25$ mA	50 V Min.
		UDN-2957A	$V_{IN} = 0.4$ V, $I_{OUT} = -25$ mA	50 V Min.
Clamp Diode Leakage Current	I_R	ALL	$V_R = 80$ V	50 μA Max.
Clamp Diode Forward Voltage	V_F	ALL	$I_F = 350$ mA	2.0 V Max.
Turn-On Delay	t_{ON}	ALL	0.5 E_{in} to 0.5 E_{out}, $R_L = 400\ \Omega$ $C_T = 25$ pF	4.0 μs Max.
Turn-Off Delay	t_{OFF}	ALL	0.5 E_{in} to 0.5 E_{out}, $R_L = 400\ \Omega$ $C_T = 25$ pF	10 μs Max.

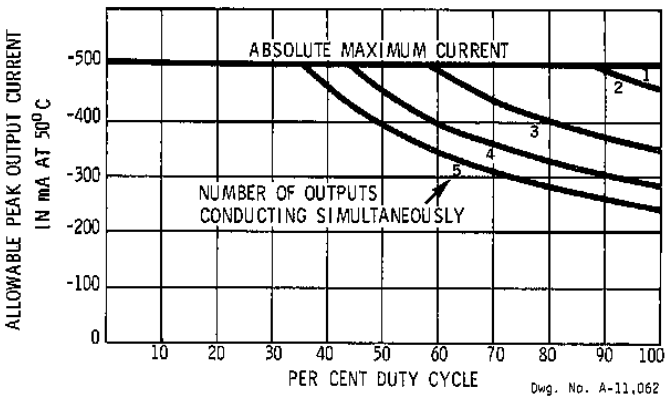
3

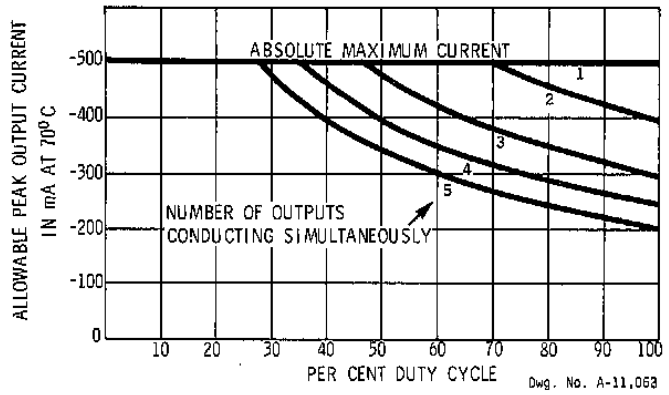
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

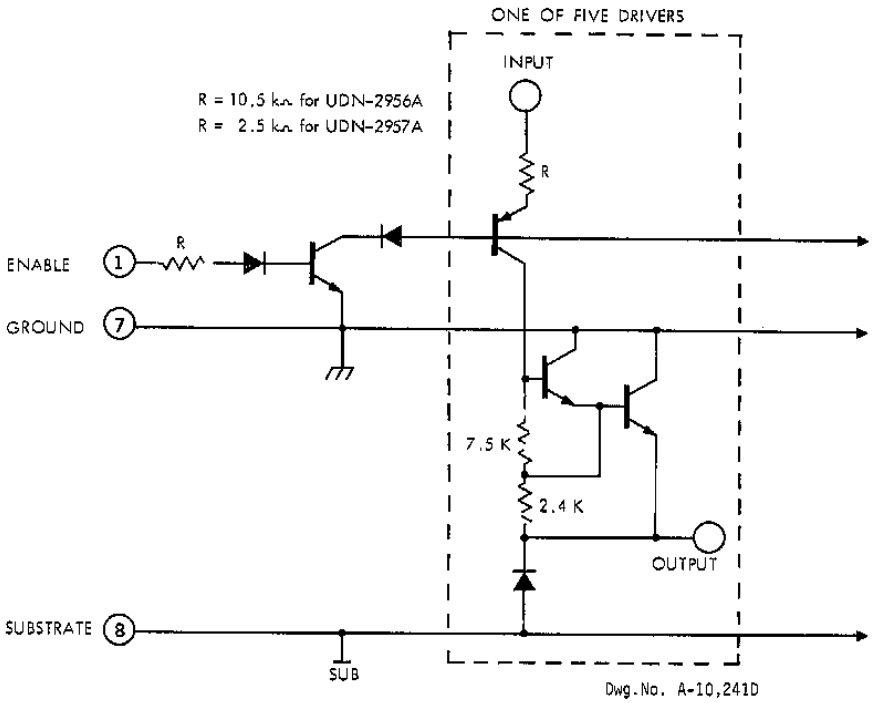




ALLOWABLE PEAK OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE



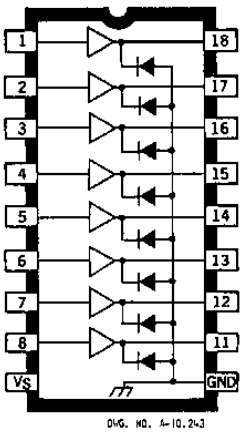




SERIES UDN-2980A
HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 500 mA Output Source Current Capability
- Transient-Protected Outputs
- Output Breakdown Voltage to 80 V



DWG. NO. A-10,243

RECOMMENDED for applications requiring separate logic and load grounds, load supply voltage to +80 V, and load currents to 500 mA, Series UDN-2980A source drivers are used as interfaces between standard low-power digital logic and relays, solenoids, stepping motors, and LEDs.

Under normal operating conditions, these devices will sustain 120 mA continuously for each of the eight outputs at an ambient temperature of +50°C and a supply of +15 V. All devices in this series incorporate input current limiting resistors and output transient suppression diodes.

Type UDN-2981A and UDN-2983A drivers are for use with +5 V logic systems — TTL, Schottky TTL, DTL, and 5 V CMOS. Type UDN-2982A and UDN-2984A drivers are intended for MOS interface (PMOS and CMOS) operating from supply voltages of 6 to 16 V. Types UDN-2981A and UDN-2982A will withstand a maximum output OFF voltage of +50 V, while Types UDN-2983A and UDN-2984A will withstand an output voltage of +80 V. In all cases, the output is switched ON by an active high input level.

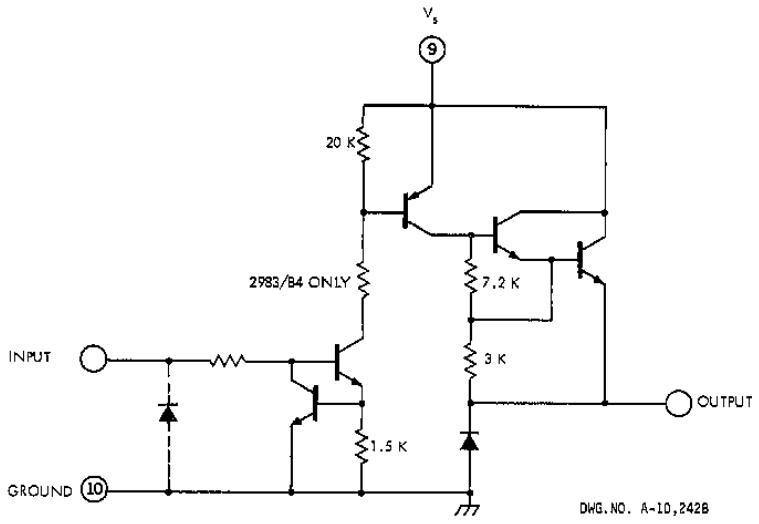
Series UDN-2980A high-voltage, high-current source drivers are supplied in 18-lead dual in-line packages. On special order, hermetically-sealed versions of these devices (with reduced package power dissipation capability) can also be furnished.

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature

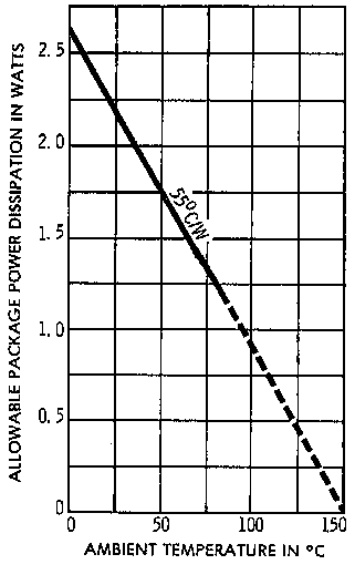
Output Voltage Range, V_{CE} (UDN-2981A & UDN-2982A)	+5 V to +50 V
(UDN-2983A & UDN-2984A)	+35 V to +80 V
Input Voltage, V_{IN} (UDN-2981A & UDN-2983A)	+15 V
(UDN-2982A & UDN-2984A)	+30 V
Output Current, I_{OUT}	−500 mA
Power Dissipation, P_D (any one driver)	1.1 W
(total package)	2.2 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 18 mW/°C above +25°C.

ONE OF EIGHT DRIVERS



POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-11,112A

3

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Test Fig.	Limit Min.	Limit Typ.	Limit Max.	Units
Output Leakage Current	I_{CEX}	UDN-2981/82A	V_{IN} = 0.4 V*, V_S = 50 V, T_A = +70°C	1	—	—	200	μA
		UDN-2983/84A	V_{IN} = 0.4 V*, V_S = 80 V, T_A = +70°C	1	—	—	200	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	V_{IN} = 2.4 V, I_{OUT} = −100 mA	2	—	1.6	1.8	V
			V_{IN} = 2.4 V, I_{OUT} = −225 mA	2	—	1.7	1.9	V
			V_{IN} = 2.4 V, I_{OUT} = −350 mA	2	—	1.8	2.0	V
Input Current	$I_{IN(ON)}$	UDN-2981/83A	V_{IN} = 2.4 V	3	—	140	200	μA
			V_{IN} = 3.85 V	3	—	310	450	μA
		UDN-2982/84A	V_{IN} = 2.4 V	3	—	140	200	μA
			V_{IN} = 12 V	3	—	1.25	1.93	mA
Output Source Current	I_{OUT}	UDN-2981/83A	V_{IN} = 2.4 V, V_{CE} = 2.0 V	2	−350	—	—	mA
		UDN-2982/84A	V_{IN} = 2.4 V, V_{CE} = 2.0 V	2	−350	—	—	mA
Supply Current (Outputs Open)	I_S	UDN-2981/82A	V_{IN} = 2.4 V*, V_S = 50 V	4	—	—	10	mA
		UDN-2983/84A	V_{IN} = 2.4 V*, V_S = 80 V	4	—	—	10	mA
Clamp Diode Leakage Current	I_R	UDN-2981/82A	V_R = 50 V, V_{IN} = 0.4 V*	5	—	—	50	μA
		UDN-2983/84A	V_R = 80 V, V_{IN} = 0.4 V*	5	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All	I_F = 350 mA	6	—	1.5	2.0	V
Turn-On Delay	t_{ON}	All	0.5 E_{IN} to 0.5 E_{OUT}, R_L = 100Ω, V_S = 35 V	—	—	1.0	2.0	μs
Turn-Off Delay	t_{OFF}	All	0.5 E_{IN} to 0.5 E_{OUT}, R_L = 100Ω, V_S = 35 V	—	—	5.0	10	μs

*All Inputs Simultaneously

TEST FIGURES

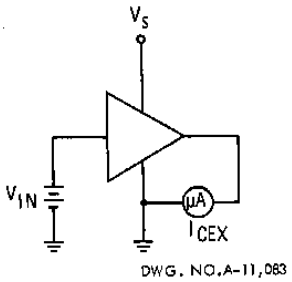


Figure 1

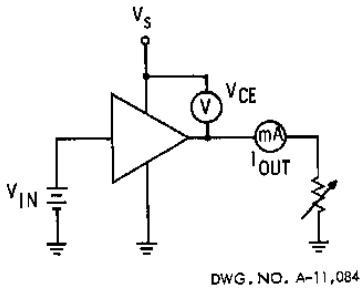


Figure 2

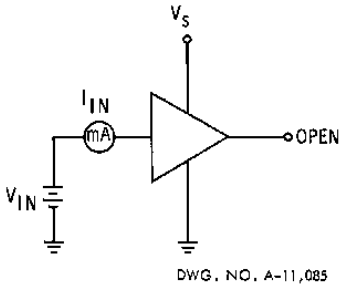


Figure 3

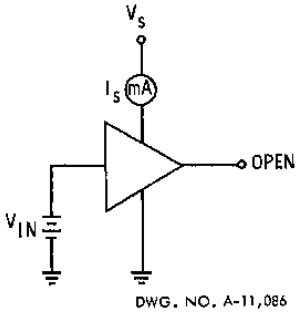


Figure 4

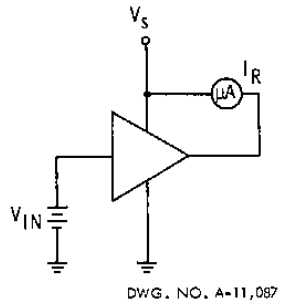


Figure 5

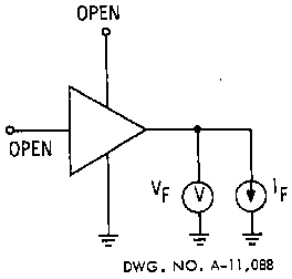
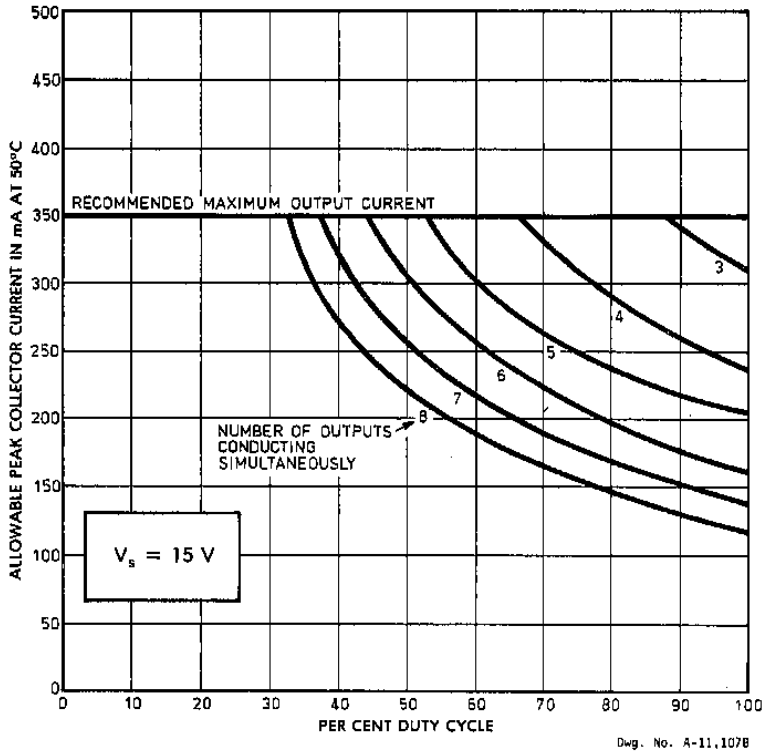
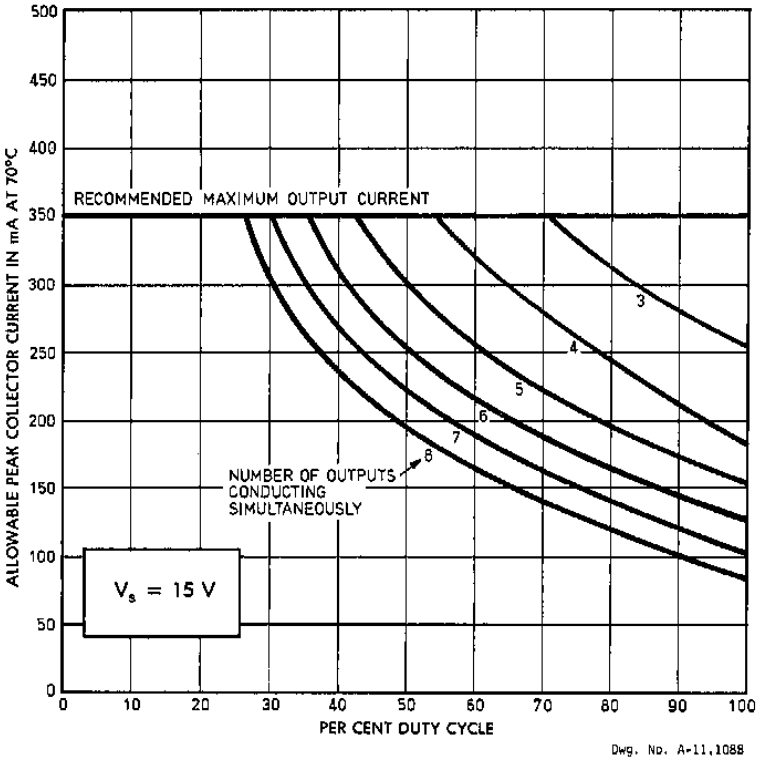


Figure 6

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE TYPE UDN-2981A/82A

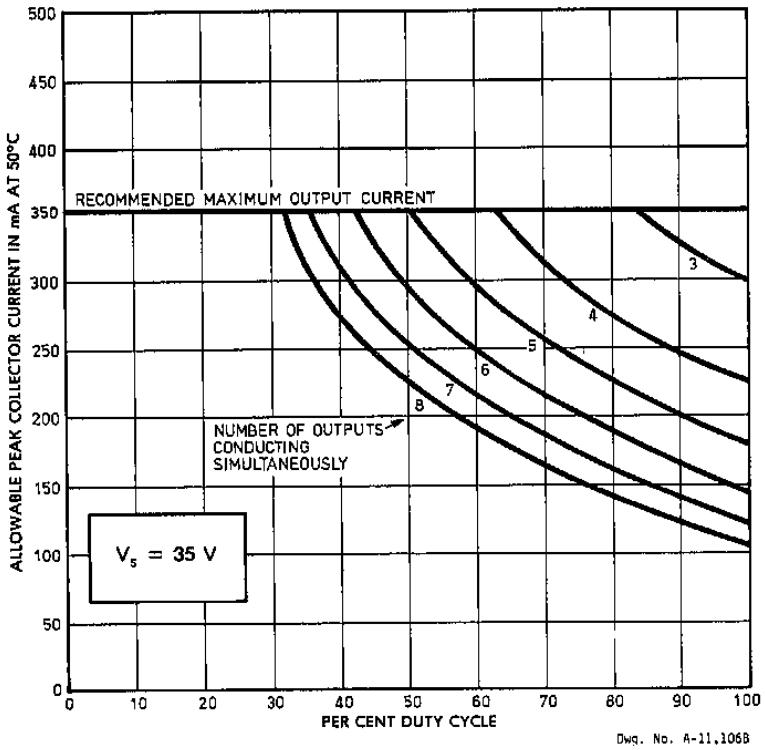


Dwg. No. A-11,1078

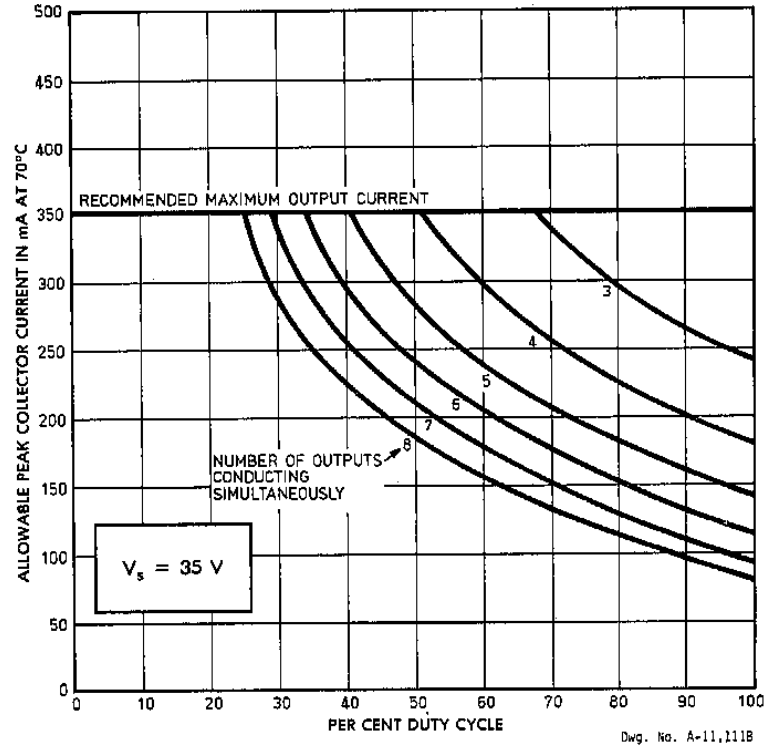


Dwg. No. A-11,1088

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE SERIES UDN-2980A

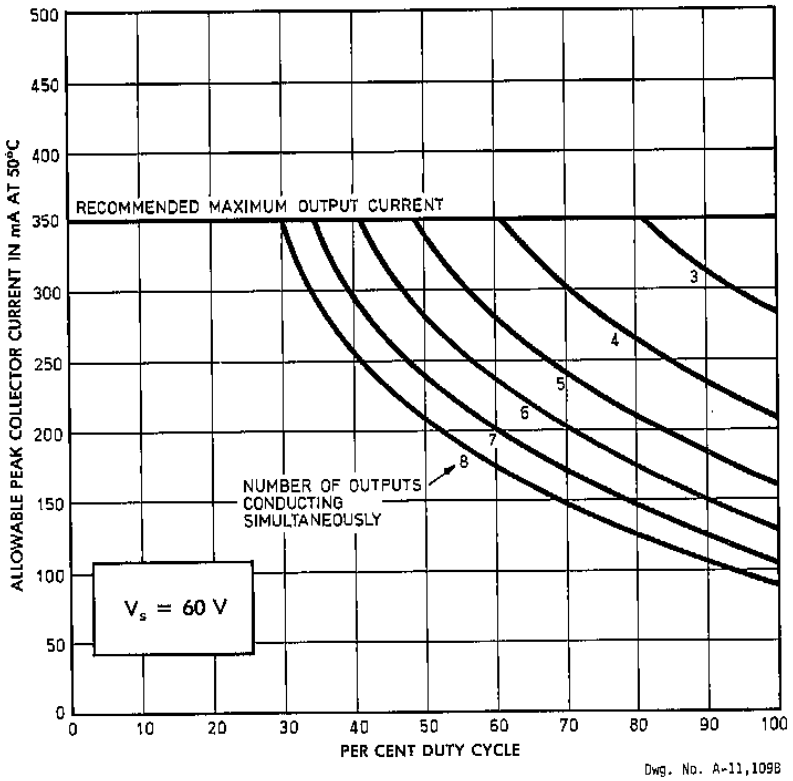


Dwg. No. A-11,106B

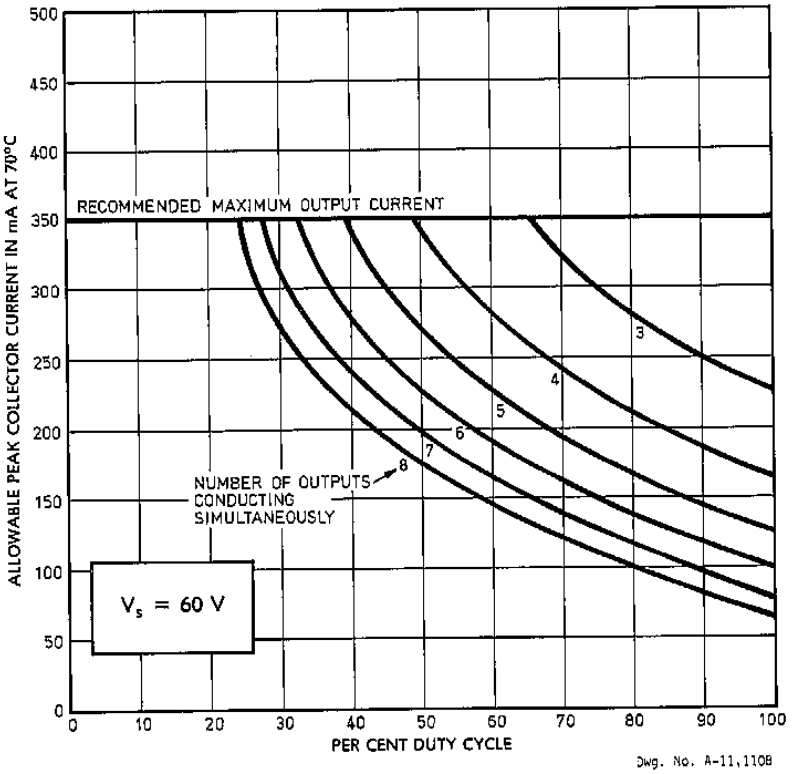


Dwg. No. A-11,111B

ALLOWABLE PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE TYPES UDN-2983A/84A

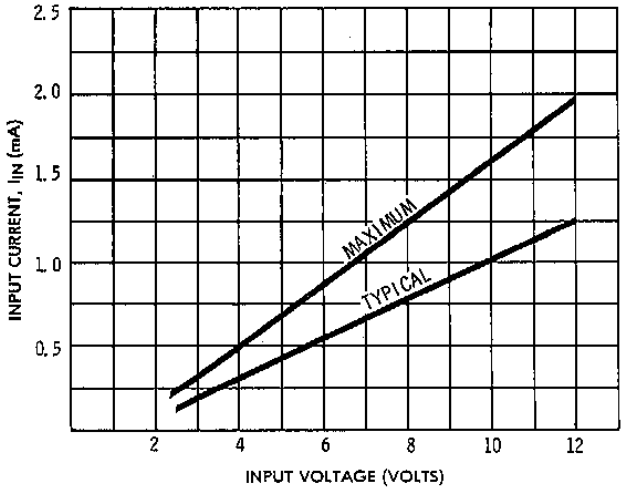


Dwg. No. A-11,109B



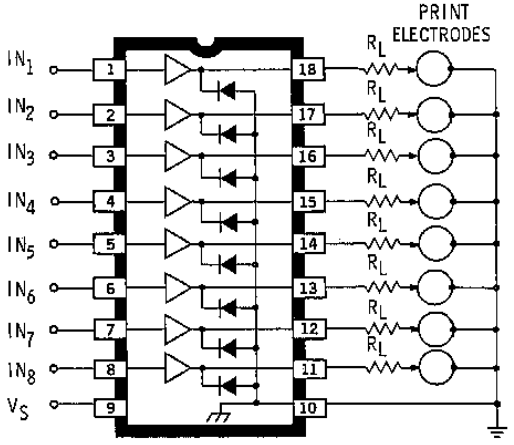
Dwg. No. A-11,110B

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



Dwg. No. A-11,115B

TYPICAL ELECTROSENSITIVE PRINTER APPLICATION



Dwg. No. A-11,113A

TYPICAL VALUES: V_S = 50 V
I_{OUT} = 200-300 mA

UDN-2985A AND UDN-2986A
8-CHANNEL SOURCE DRIVERS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 250 mA Output Source Current Capability
- Output Transient-Suppression Diodes
- 30 V Minimum Output Breakdown Voltage
- Low Output-Saturation Voltage

Recommended for applications requiring separate logic and load grounds, load supply voltages to 30 V, and load currents to 250 mA, the UDN-2985A and UDN-2986A source drivers are used as interface between standard low-power digital logic and LEDs, relays and solenoids. The outputs feature saturated transistors for low collector-emitter saturation voltages.

The UDN-2985A driver is for use with 5 V logic systems—TTL, Schottky TTL, DTL, and CMOS. The UDN-2986A is intended for MOS interface (PMOS and CMOS) operating from supply voltages of 6 to 16 V. Both devices have a minimum output breakdown rating of 30 V with a minimum output sustaining voltage of 15 V. In all cases, the output is switched ON by an active high input level.

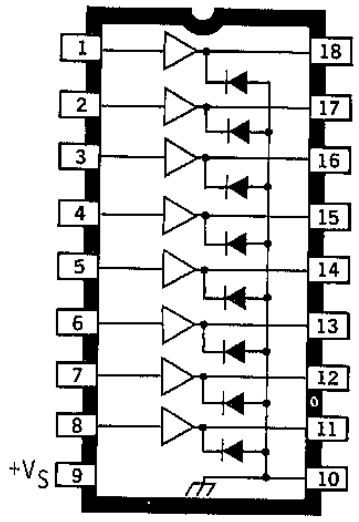
Under normal operating conditions, these devices can source up to 120 mA for each of the eight outputs at an ambient temperature of 75°C and a supply voltage of 15 V. Both devices incorporate input current-limiting resistors and output transient suppression diodes.

The UDN-2985A and UDN-2986A source drivers are supplied in 18-lead dual in-line packages. All inputs are on one side of the package, output pins on the other, to simplify printed wiring board layout.

ABSOLUTE MAXIMUM RATINGS
at $T_A = 25°C$

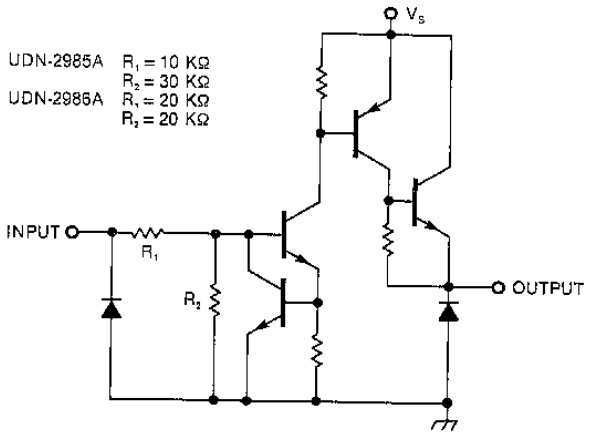
Driver Supply Voltage, V_S . . . . . 30 V
Continuous Output Current, I_{OUT} . . . . . −250 mA
Input Voltage, V_{IN} . . . . . 20 V
Package Power Dissipation, P_D . . . . . 2.2 W*
Operating Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

*Derate at the rate of 18 mW/°C above $T_A = 25°C$



Dwg. No. A-10, 243

PARTIAL SCHEMATIC DIAGRAM
1 of 8 Drivers



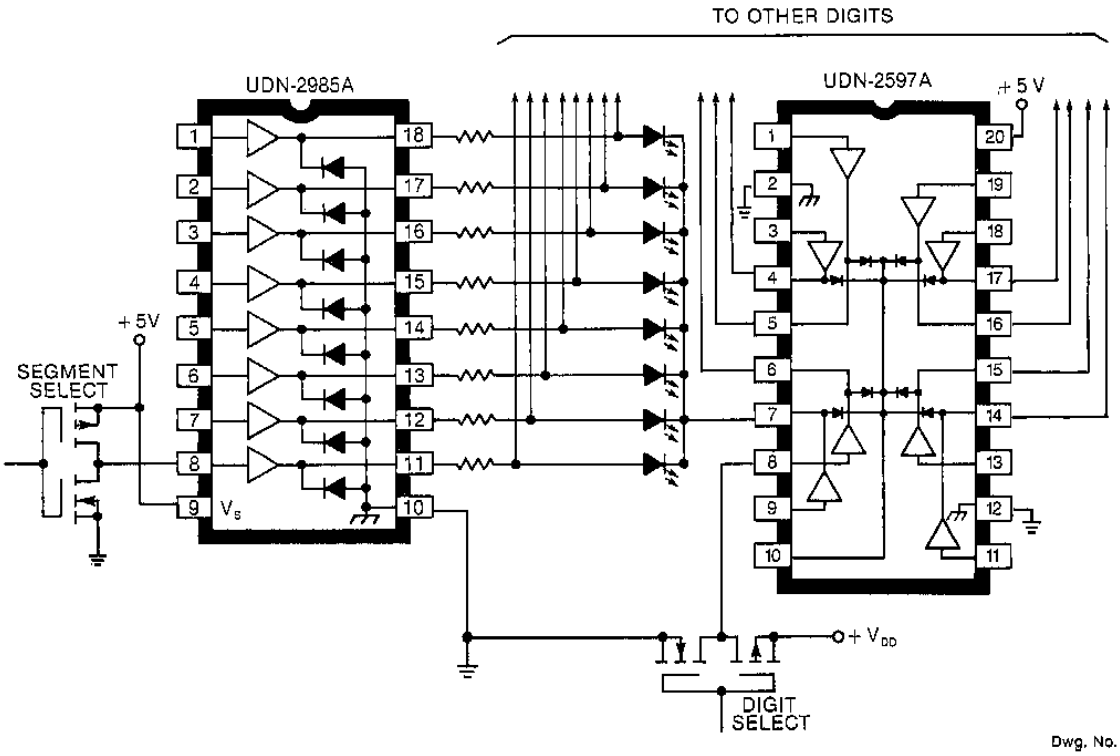
Dwg. No. DS-1013

ELECTRICAL CHARACTERISTICS AT $T_A = 25°C$, $V_S = 30V$ (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	Both	$V_{IN} = 0.4$ V, $V_{OUT} = 0$ V	–	<–1.0	–100	µA
Output Sustaining Voltage	$V_{CE(sus)}$	Both	$I_{OUT} = -120$ mA, L = 3 mH	15	–	–	V
Output Saturation Voltage	$V_{CE(SAT)}$	UDN-2985A	$V_{IN} = 2.4$ V, $I_{OUT} = -60$ mA	–	0.8	1.1	V
			$V_{IN} = 2.4$ V, $I_{OUT} = -120$ mA	–	0.9	1.2	V
		UDN-2986A	$V_{IN} = 4.0$ V, $I_{OUT} = -60$ mA	–	0.8	1.1	V
			$V_{IN} = 4.0$ V, $I_{OUT} = -120$ mA	–	0.9	1.2	V
Input Current	$I_{IN(ON)}$	UDN-2985A	$V_{IN} = 2.4$ V	–	90	225	µA
			$V_{IN} = 5.0$ V	–	280	650	µA
		UDN-2986A	$V_{IN} = 4.0$ V	–	90	250	µA
			$V_{IN} = 15$ V	–	450	1150	µA
	$I_{IN(OFF)}$	Both	$V_{IN} = 0.4$ V	–	10	15	µA
Supply Current (outputs open)	I_S	Both	$V_S = 30$ V, $V_{IN} = 2.4$ V	–	10	15	mA
Clamp Diode Leakage Current	I_R	Both	$V_R = 30$ V, $T_A = 70°C$	–	<1.0	50	µA
Clamp Diode Forward Voltage	V_F	Both	$I_F = 120$ mA	–	1.1	2.0	V
Turn-On Delay	t_{ON}	Both		–	0.5	1.0	µs
Turn-Off Delay	t_{OFF}	Both		–	5.0	10	µs

NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.

COMMON-CATHODE LED DRIVER

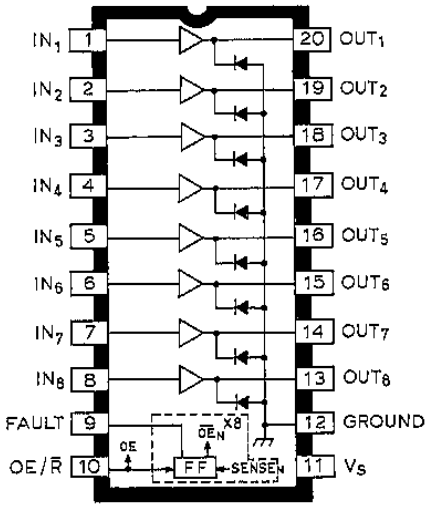


Dwg. No. DS-1014A

UDN-2987A
8-CHANNEL SOURCE DRIVER
With Over-Current Protection

FEATURES

- 350 mA Output Source Current
- Over-Current Protected
- Internal Ground Clamp Diodes
- Output Breakdown Voltage 35 V, Minimum
- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Internal Thermal Shutdown



Dwg. No. A-13,285

Providing over-current protection for each of its eight sourcing outputs, the UDN-2987A driver is used as an interface between standard low-level logic and relays, motors, solenoids, LEDs and incandescent lamps. The device includes thermal shutdown and output transient protection/clamp diodes for use with sustaining voltages to 35 V.

In this driver, each channel includes a latch to turn OFF that channel if the maximum channel current is exceeded. All channels are disabled if the thermal shutdown is activated. A common FAULT output is used to indicate either chip thermal shutdown or any over-current condition. All outputs are enabled by pulling the common OE/R input high. When OE/R is low, all outputs are inhibited and the eight latches are reset. The UDN-2987A is supplied in a 20-lead dual in-line plastic package.

Under normal operating conditions each of eight outputs will source in excess of 100 mA continuously at an ambient temperature of 25°C and a supply of 35 V. The over-current fault circuit will protect the device from short-circuits to ground with supply voltages of up to 35 V.

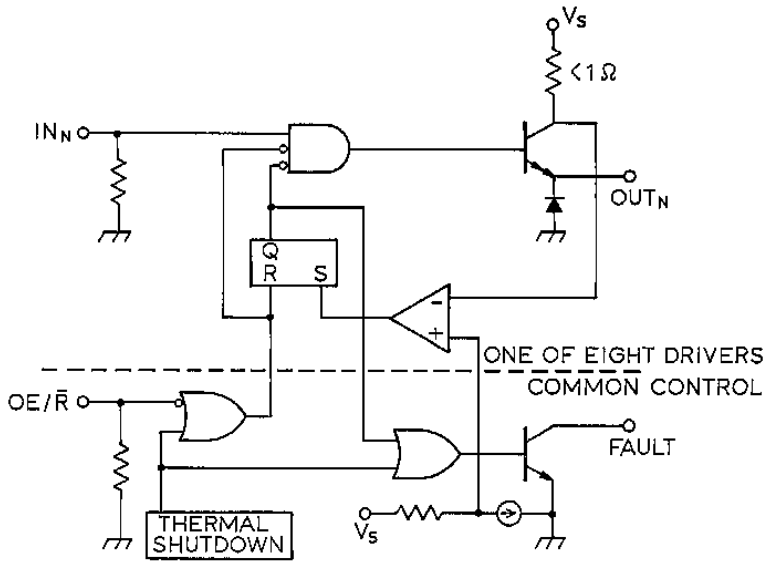
The inputs are compatible with 5 V and 12 V logic systems—TTL, Schottky TTL, DTL, PMOS, and CMOS. In all cases, the output is switched ON by an active high input level.

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Driver Supply Voltage, V_S	35 V
Output Sustaining Voltage, $V_{CE(SUS)}$	35 V
Continuous Output Current, I_{OUT}	−500 mA*
FAULT Output Voltage, V_{CE}	50 V
FAULT Output Current, I_C	30 mA
Input Voltage, V_{IN}	15 V
Package Power Dissipation, P_D	See Graph
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

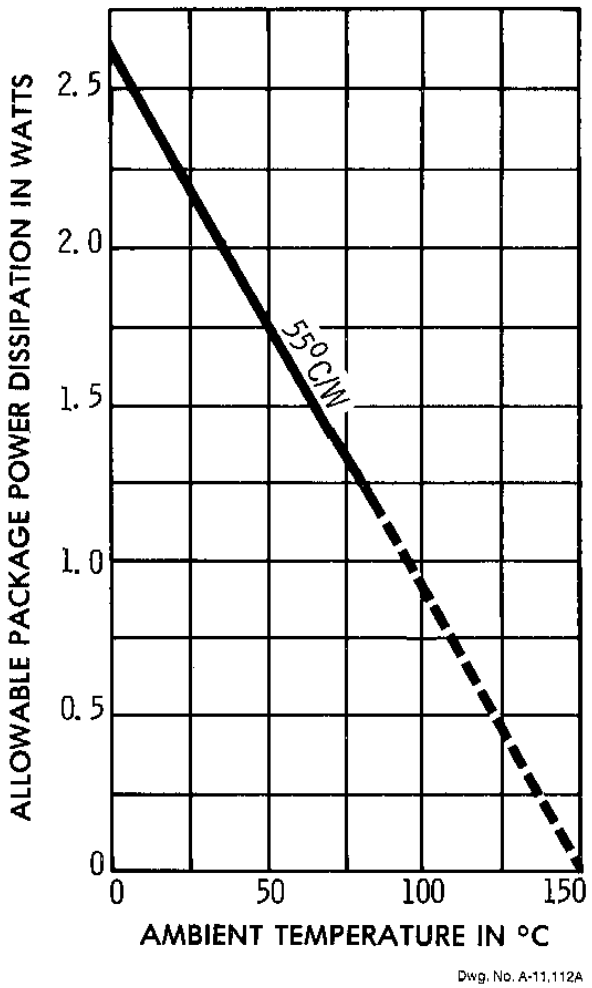
*Outputs are disabled at approximately −500 mA per driver.

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-13,286

ALLOWABLE POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-11,112A

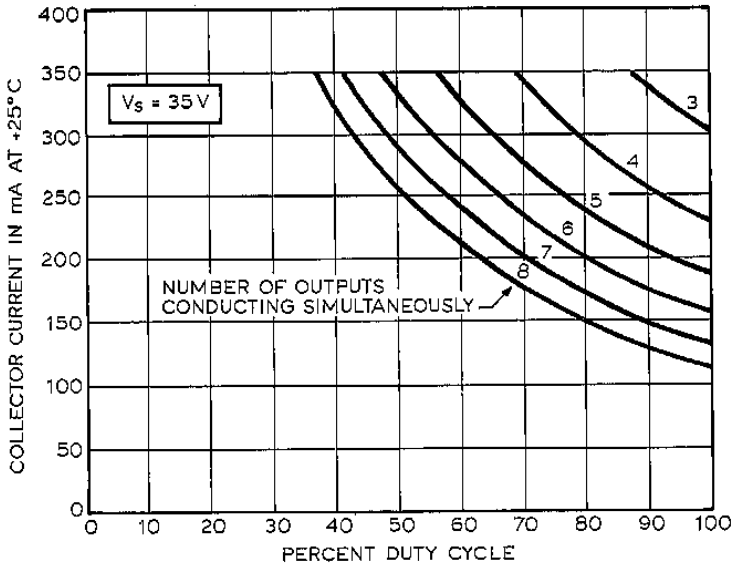
ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{OE} = 2.4 V, V_S = 35 V unless otherwise noted.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Functional Supply Range	V_S		7.0	—	35	V
Output Leakage Current	I_{CEX}	V_{IN} = 0.4 V*	—	< −5	−200	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = −350 mA, L = 2.0 mH	35	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	V_{IN} = 2.4 V, I_{OUT} = −100 mA	—	1.6	1.8	V
		V_{IN} = 2.4 V, I_{OUT} = −225 mA	—	1.7	1.9	V
		V_{IN} = 2.4 V, I_{OUT} = −350 mA	—	1.8	2.0	V
Channel Shutdown Threshold	I_M	V_{IN} = 2.4 V	−400	−500	—	mA
FAULT Leakage Current	I_{CEX}	V_{CC} = 35 V	—	<1.0	100	µA
FAULT Saturation Voltage	$V_{CE(SAT)}$	I_C = 30 mA	—	0.3	0.8	V
Input Voltage	$V_{IN(ON)}$		2.4	—	—	V
	$V_{IN(OFF)}$		—	—	0.4	V
Input Current	$I_{IN(ON)}$	V_{IN} = 2.4 V	—	125	170	µA
		V_{IN} = 5.0 V	—	840	1020	µA
		V_{IN} = 12 V	—	1500	1800	µA
	$I_{IN(OFF)}$	V_{IN} = 0.4 V	—	—	15	µA
Clamp Diode Leakage Current	I_R	V_R = 35 V, T_A = 70°C	—	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.5	1.8	V
Supply Current	$I_{S(ON)}$	V_{IN} = 2.4 V*, Outputs Open	—	13	18	mA
	$I_{S(OFF)}$	V_{IN} = 0.4 V*	—	8.0	12	mA
Thermal Shutdown	T_J		—	165	—	°C
Thermal Hysteresis	T_J		—	15	—	°C
Propagation Delay Time	t_{PLH}	R_L = 100Ω	—	0.3	0.6	µs
	t_{PHL}	R_L = 100Ω	—	2.0	4.0	µs
Dead Time	t_d		—	1.0	—	µs

*All inputs simultaneously.

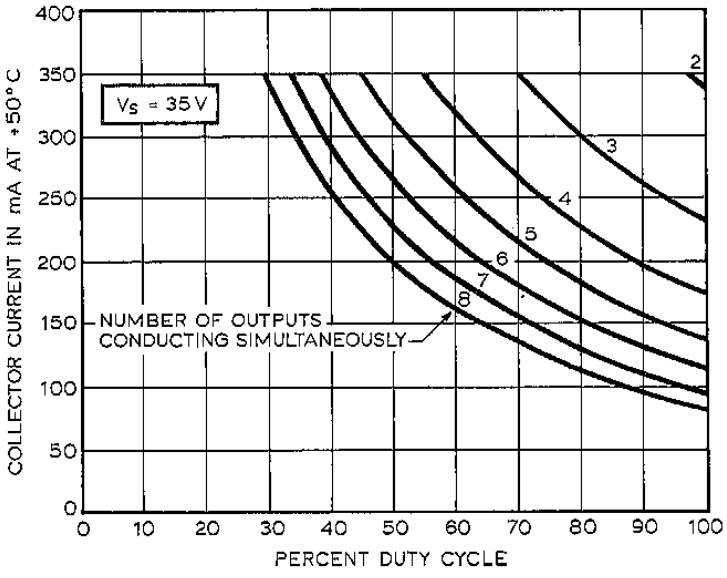
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

AT +25°C



Dwg. No. A-13,288

AT +50°C



Dwg. No. A-13,289

APPLICATIONS INFORMATION AND CIRCUIT DESCRIPTION

As with all power integrated circuits, the UDN-2987A has a maximum allowable output current rating. The 500 mA rating does not imply that operation at that value is permitted or even obtainable. The channel output current trip point is specified as −400 mA, minimum; therefore, attempted operation at current levels greater than −400 mA may cause a fault indication and channel shutdown. The device is tested at a maximum of −350 mA and that is the recommended maximum output current per driver. It provides protection for current overloads or shorted loads up to 35 V.

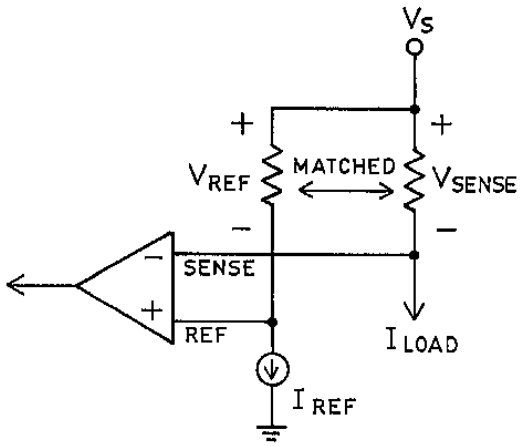
All outputs are enabled by pulling the OE/R input high. When OE/R is low or allowed to float (internal pull-down), all outputs are inhibited and the latches are reset. The latches are also reset during power-up, regardless of the state of the OE/R input.

The load current causes a small voltage drop across the internal low-value sense resistor. This voltage is compared to the voltage drop across a reference resistor with a constant current. The two resistors are matched to eliminate errors due to manufacturing tolerances or temperature effects. Each channel includes a comparator and its own latch. An over-current fault ($V_{SENSE_j} > V_{REF}$) will set the affected latch and shut down only that channel. All other channels will continue to operate normally. The latch includes a 1 μs delay (t_d) to prevent unwanted triggering due to crossover currents generated when switching inductive loads. For an abrupt short circuit, the delay and output switching times will allow a brief, permissable current in excess of the trip current before the output driver is turned OFF.

A common thermal shutdown disables all outputs if the chip temperature exceeds +165°C. At thermal shutdown, all latches are reset. The outputs are disabled until the chip cools down to about +150°C (thermal hysteresis).

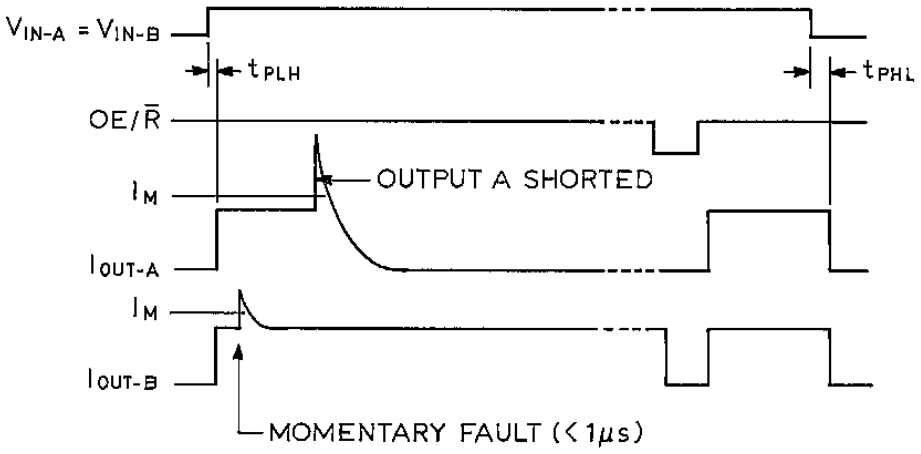
A common open-collector FAULT output is used to indicate any channel over-current condition or chip thermal shutdown.

OVER-CURRENT FAULT SENSE



Dwg. No. A-13,292

OUTPUT CURRENT WAVESHAPES

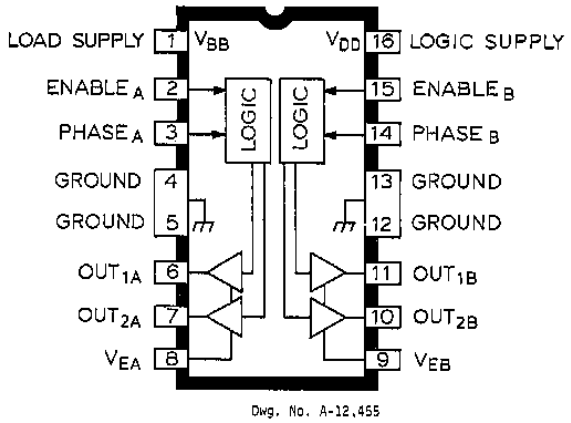


Dwg. No. A-13,293

UDN-2993B
DUAL H-BRIDGE MOTOR DRIVER

FEATURES

- ±600 mA Output Current
- Output Voltage to 40 V
- Crossover Current Protection
- TTL/NMOS/CMOS Compatible Inputs
- Low Input Current
- Internal Clamp Diodes
- Plastic DIP With Heat-Sink Tabs (Machine Insertable)



Dwg. No. A-12,455

BRUSHLESS D-C or bipolar stepper motors to 40 V and 500 mA per phase are economically driven with the Type UDN-2993B dual H-bridge driver. Each of the pair of full-bridge drivers has separate input level shifting, internal logic, source and sink drivers in an H-bridge configuration, and internal clamp diodes.

The device provides an internally-generated deadtime to prevent crossover currents during changes in load-current phase. Monolithic, space-saving construction offers reliability unobtainable with discrete components.

Except for supply voltages, the two H-bridges are independent. The ENABLE function is provided for each bridge to allow pulse-width (chopper) modulation with the use of external comparators. The chopper-drive mode is characterized by low power-dissipation levels and maximum efficiency.

A PHASE input to each bridge determines load-current direction. In addition, the emitters from each bridge are externally available to allow the addition of current-sensing circuitry.

The Type UDN-2993B integrated circuit is supplied in a 16-pin dual in-line plastic package with a copper lead frame for optimum power dissipation without a heat sink. The lead configuration allows automatic insertion, fits a standard integrated circuit socket or printed wiring board layout, and enables easy attachment of a heat sink for maximum power-handling capability. The heat-sink tabs are at ground potential and require no insulation.

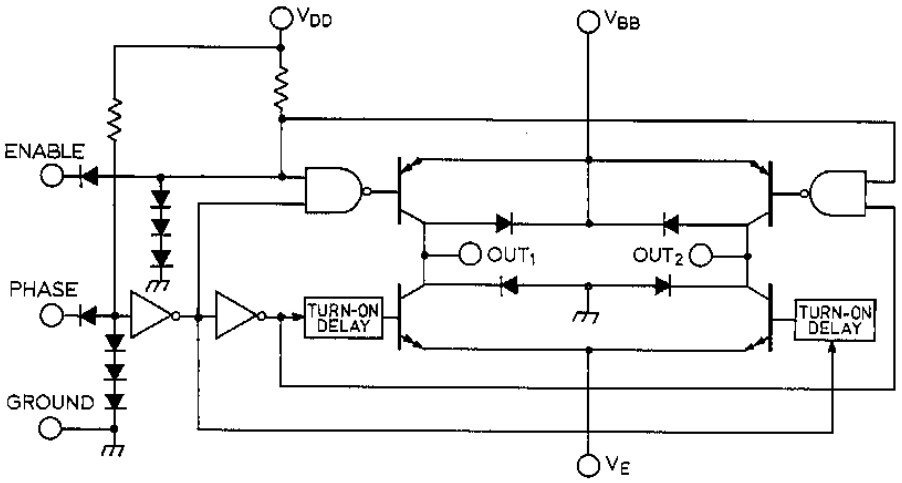
A full-bridge bipolar driver with a current rating of ±3.5 A is supplied as Type UDN-2952B. It is described in Sprague Engineering Bulletin 29319.

ABSOLUTE MAXIMUM RATINGS
at $T_{TAB} \leq +70°C$

Load Supply Voltage, V_{BB} . . . . . 40 V
Logic Supply Voltage, V_{DD} . . . . . 7.0 V
Logic Input Voltage Range,
V_{PHASE} or V_{ENABLE} . . . . . -0.3 V to $V_{DD} + 0.3$ V
Output Current, I_{OUT} . . . . . ±600 mA
Sink Driver Emitter Voltage, V_E . . . . . 1.5 V
Package Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . . $-55°C$ to $+150°C$

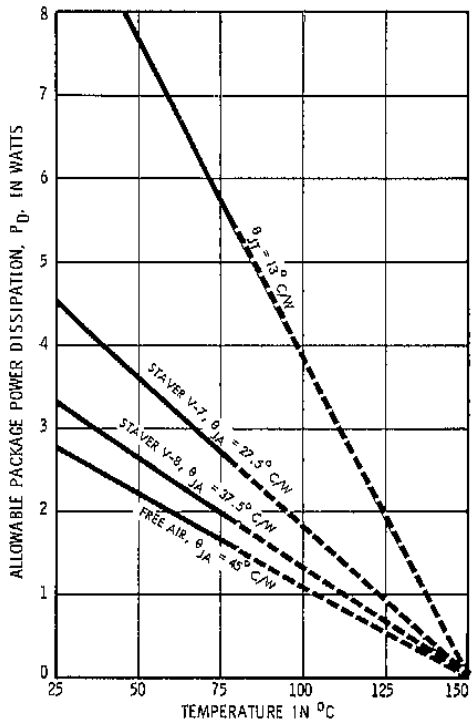
NOTE: Output current rating may be limited by chopping frequency, ambient temperature, air flow, and heat sinking. Under any set of conditions, do not exceed the specified maximum current and a junction temperature of +150°C.

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)



Dwg. No. A-12,447

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-11,793A

To maintain isolation between integrated circuit components and to provide for normal transistor operation, the ground tab must be connected to the most negative point in the external circuit.

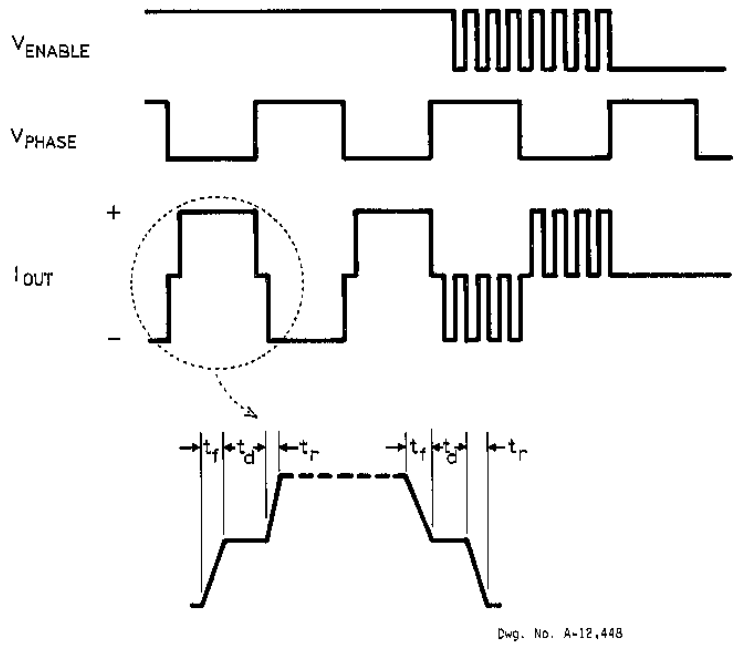
TRUTH TABLE

Enable Input	Phase Input	Output 1	Output 2
High	High	Low	High
High	Low	High	Low
Low	High	Low	Open
Low	Low	Open	Low

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 40\ V$, $V_{DD} = 5\ V$, $V_E = 0\ V$, $T_{TAB} \leq +70°C$ Figure 1 (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Drivers						
Operating Voltage Range	V_{BB}		10	—	40	V
Output Leakage Current	I_{CEX}	$V_{ENABLE} = 0.8\ V$, $V_{OUT} = V_{BB}$, Note 2	—	<1.0	10	µA
		$V_{ENABLE} = 0.8\ V$, $V_{OUT} = 0\ V$, Note 2	—	<−1.0	−10	µA
Output Saturation Voltage	$V_{CE(SAT)}$	$V_{ENABLE} = 2.4\ V$, $I_{OUT} = 500\ mA$	—	1.6	1.8	V
		$V_{ENABLE} = 2.4\ V$, $I_{OUT} = -500\ mA$	—	1.6	2.0	V
Output Sustaining Voltage	$V_{CE(SUS)}$	$I_{OUT} = \pm 500\ mA$, Figure 2, Note 2	40	50	—	V
Motor Supply Current	$I_{BB(ON)}$	$V_{ENABLE} = 2.4\ V$, Outputs Open, Note 2	—	1.0	3.0	mA
	$I_{BB(OFF)}$	$V_{ENABLE} = 0.8\ V$, Outputs Open, Note 2	—	<1.0	10	µA
Source Driver Rise Time	t_r	$I_{OUT} = -500\ mA$, $V_{BB} = 30\ V$	—	75	—	ns
Source Driver Fall Time	t_f	$I_{OUT} = -500\ mA$, $V_{BB} = 30\ V$	—	280	—	ns
Deadtime	t_d	$I_{OUT} = \pm 500\ mA$, $V_{BB} = 30\ V$	—	1.5	—	µs
Clamp Diode Forward Voltage	V_F	$I_F = 500\ mA$	—	1.6	1.8	V
Control Logic (PHASE or ENABLE)						
Logic Input Current	$I_{IN(1)}$	V_{PHASE} or $V_{ENABLE} = 2.4\ V$	—	<1.0	10	µA
	$I_{IN(0)}$	V_{PHASE} or $V_{ENABLE} = 0.8\ V$	—	−200	−300	µA
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Supply Current	I_{DD}		—	14	20	mA
Turn-On Delay Time	t_{pd0}	ENABLE Input to Source Drivers	—	250	—	ns
Turn-Off Delay Time	t_{pd1}	ENABLE Input to Source Drivers	—	500	—	ns

NOTES: 1. Each driver is tested separately.
2. Test is performed with $V_{PHASE} = 0.8\ V$ and then repeated for $V_{PHASE} = 2.4\ V$.
3. Negative current is defined as coming out of (sourcing) the specified device pin.



Dwg. No. A-12,448

TEST FIGURES

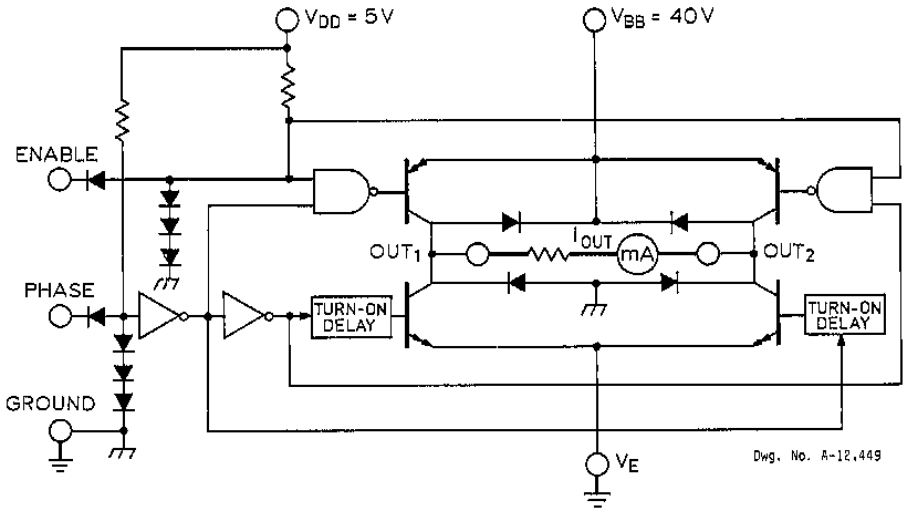


FIGURE 1

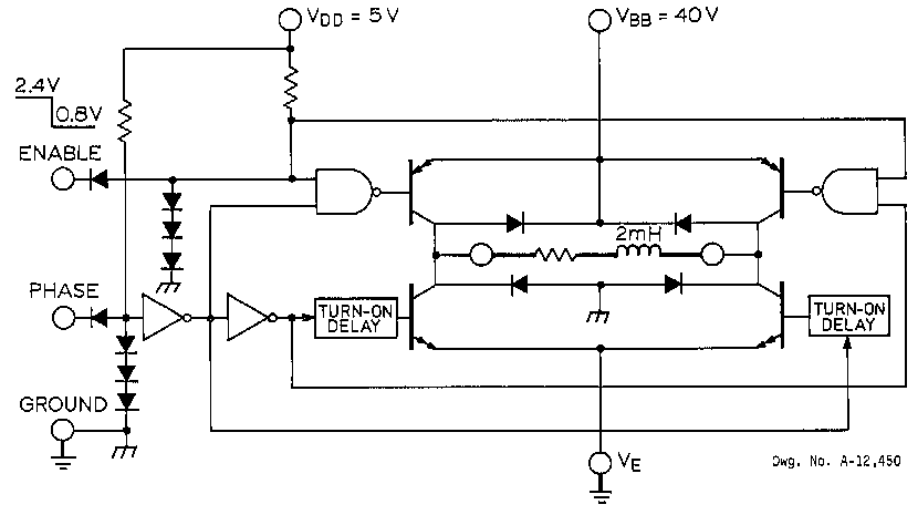
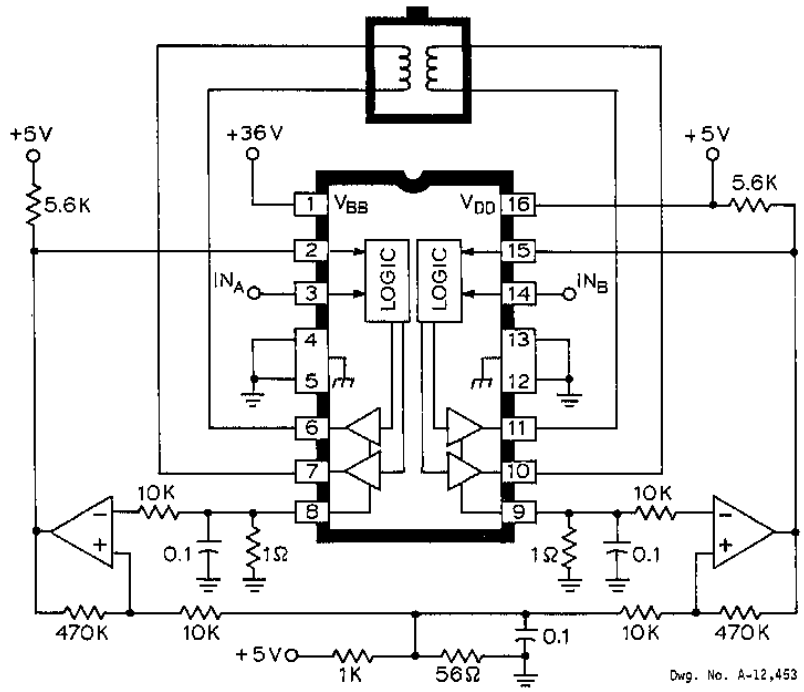
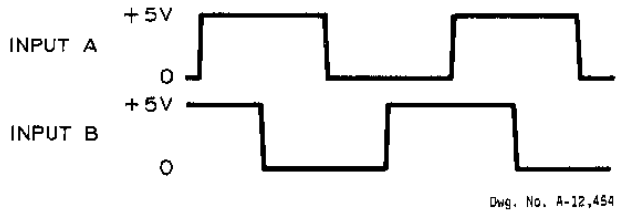


FIGURE 2

TYPICAL APPLICATION

2-PHASE BIPOLAR STEPPER MOTOR DRIVE
(Chopper Mode)





SERIES UDN-3610M
DUAL 2-INPUT PERIPHERAL/POWER DRIVERS

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Standoff Voltage of 80 V
- Pin-for-Pin Replacement for Series LM3600N
- Pin-for-Pin Replacement for SN75451BP through SN75454BP and 75461 through 75464

Description

THESE MINI-DIP dual 2-input peripheral power drivers are bipolar monolithic integrated circuits with AND, NAND, OR, or NOR logic gates and high-current switching transistors on the same chip. The two output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will withstand at least 80 V.

Applications

Series UDN-3600M dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, heaters, and other non-inductive loads of up to 600 mA (both drivers in parallel).

With appropriate external-diode transient-suppression, Series UDN-3600M drivers can also be used with inductive loads such as relays, solenoids, and stepping motors.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{IN}	30 V
Output Off-State Voltage, V_{OFF}	80 V
Output On-State Sink Current, I_{ON}	600 mA
Power Dissipation, P_D	1.5 W
Each Driver	0.8 W
Derating Factor Above T_A = 25°C	12.5 mW/°C or 80°C/W
Operating Free-Air Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into any output (ON state)			300	mA

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

3

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current	$I_{in(0)}$		MAX	0.4 V	30 V			−50	−100	μA	2
"1" Input Current	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS at V_{CC} = 5.0 V, T_A = 25°C

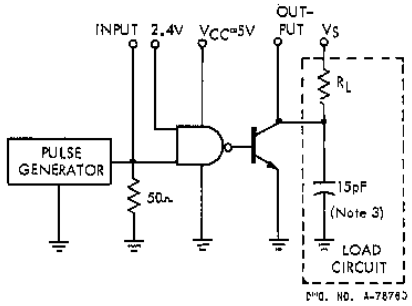
Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		300	750	ns	3

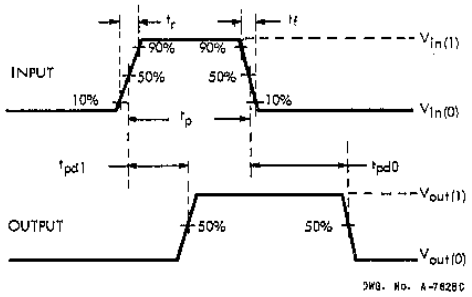
NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

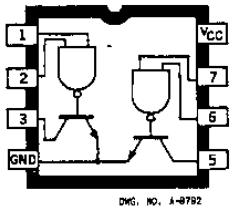
Type UDN-3611M Dual AND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	100 mA		0.25	0.4	V	
			MIN	0.8 V	V_{CC}	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			35	49	mA	1, 2



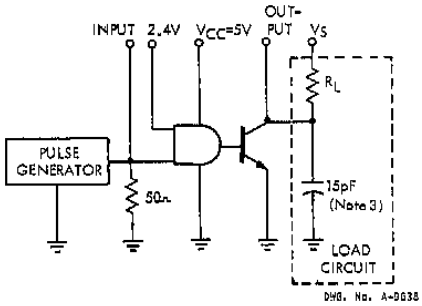


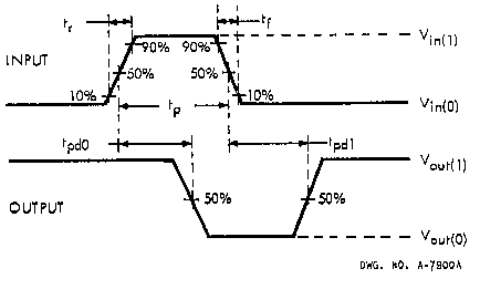


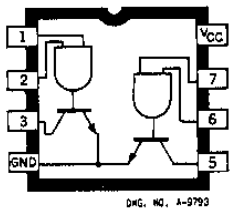
Type UDN-3612M Dual NAND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	100 mA		0.25	0.4	V	
			MIN	2.0 V	2.0 V	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	14	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	53	mA	1, 2





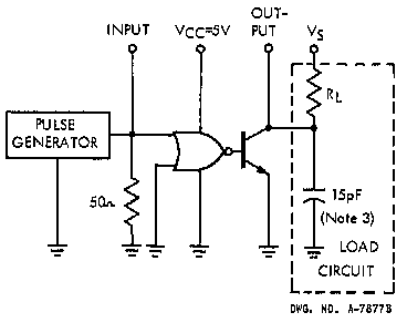


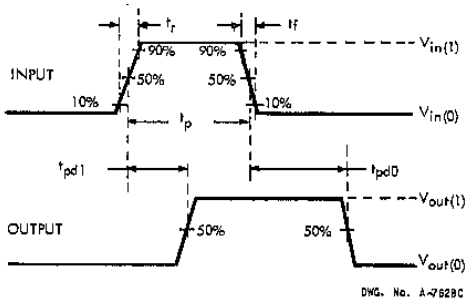
NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

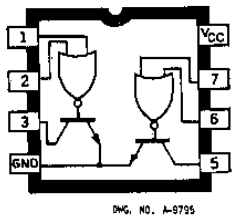
Type UDN-3613M Dual OR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	100 mA		0.25	0.4	V	
			MIN	0.8 V	0.8 V	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			36	50	mA	1, 2



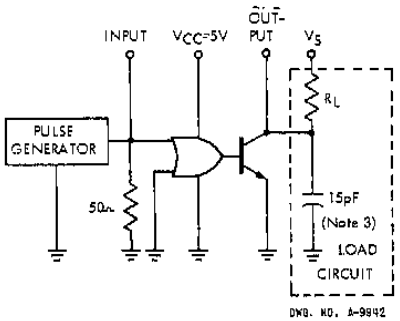


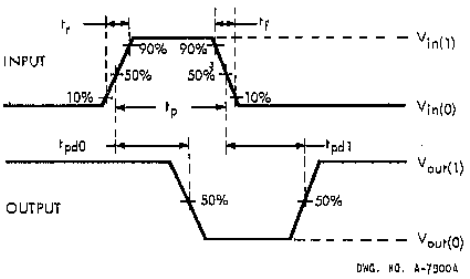


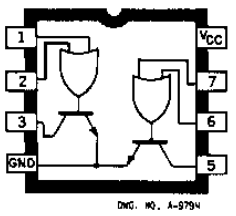
Type UDN-3614M Dual NOR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	100 mA		0.25	0.4	V	
			MIN	2.0 V	0 V	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	50	mA	1, 2







NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

SERIES UDN-5700A
QUAD 2-INPUT PERIPHERAL/POWER DRIVERS
—Transient-Protected Outputs

FEATURES:

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Standoff Voltage of 80 V

Description

THESE 16-LEAD QUAD 2-input peripheral and power drivers are bipolar monolithic integrated circuits containing AND, NAND, OR, or NOR logic gates, high-current switching transistors, and transient-suppression diodes on the same chip. The four output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will withstand at least 80 V.

Applications

Series UDN-5700A quad drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

The integral transient-suppression diodes allow their use with inductive loads such as relays, solenoids, or stepping motors without the need of discrete diodes. For non-inductive loads, the diode-common bus can be used for a convenient lamp test.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{IN}	30 V
Output Off-State Voltage, V_{OFF}	80 V
Output On-State Sink Current, I_{ON}	600 mA
Suppression Diode Off-State Voltage, V_{OFF}	80 V
Suppression Diode On-State Current, I_{ON}	600 mA
Power Dissipation, P_D	2.0 W
Each Driver	0.8 W
Derating Factor Above 25°C	16.7 mW/°C or 60°C/W
Operating Free-Air Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC}):	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into any output (ON state)			300	mA

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

3

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current	$I_{in(0)}$		MAX	0.4 V	30 V			−50	−100	μA	2
"1" Input Current	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS at V_{CC} = 5.0 V, T_A = 25°C

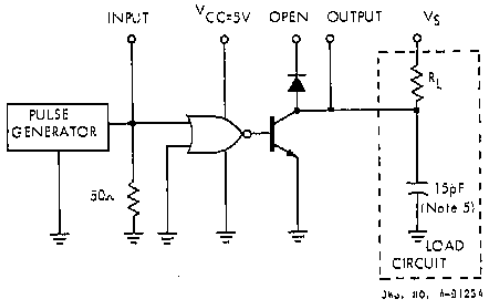
Characteristic	Symbol	Test Conditions	Limits			Units	Notes
			Min.	Typ.	Max.		
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		300	750	ns	3

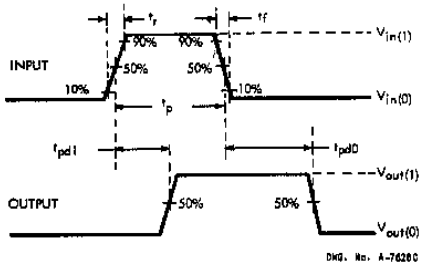
NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

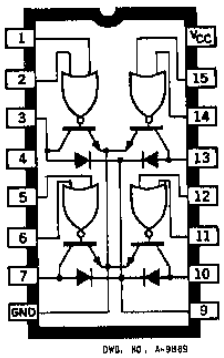
Type UDN-5703A Quad OR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA		0.35	0.5	V	
			MIN	0.8 V	0.8 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			16	25	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			72	100	mA	1, 2



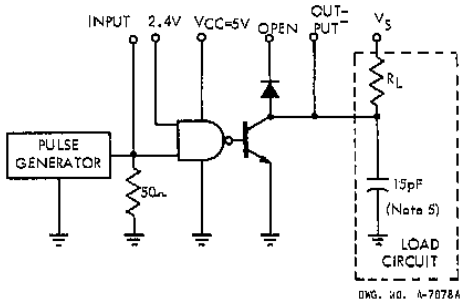


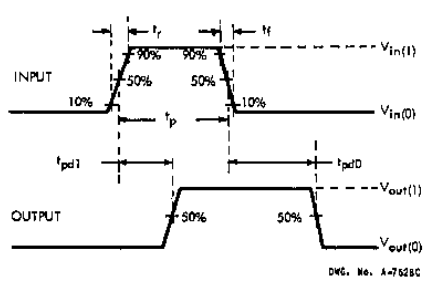


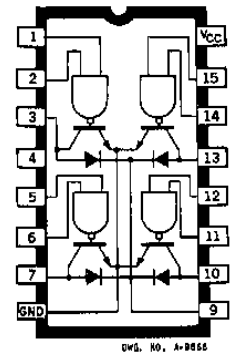
Type UDN-5706A Quad AND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.35	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			16	24	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			70	98	mA	1, 2





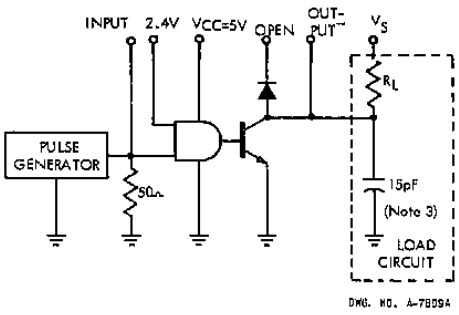


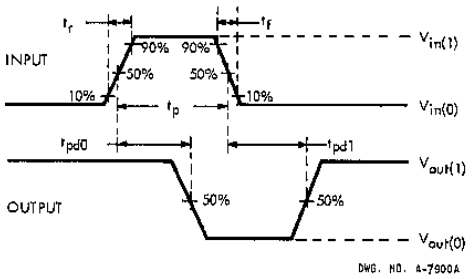
NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

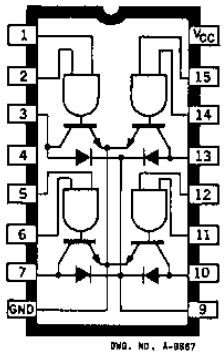
Type UDN-5707A Quad NAND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			80	106	mA	1, 2



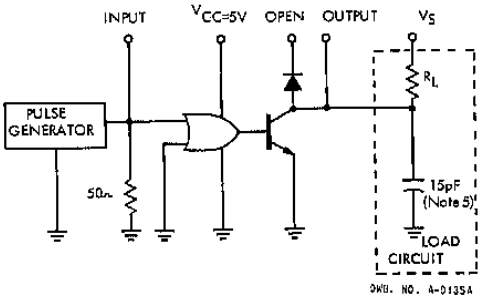


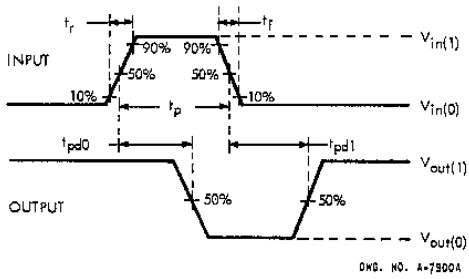


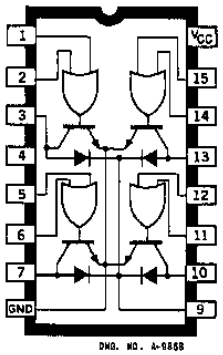
Type UDN-5733A Quad NOR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			80	100	mA	1, 2







NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

SERIES UDN-5710M
DUAL PERIPHERAL/POWER DRIVERS
—Transient Protected Outputs

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Standoff Voltage of 80 V

Description

THESE MINI-DIP dual peripheral and power drivers are bipolar monolithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, high-current switching transistors, and transient-suppression diodes on the same chip. The two output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will withstand at least 80 V.

Applications

Series UDN-5700M dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters with a load current of up to 600 mA.

The integral transientsuppression diodes allow the use of these drivers with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. When not required for transient suppression, the diode-common bus can be used for the "lamp test" function.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . . 7.0 V
Input Voltage, V_{IN} . . . . . 30 V
Output Off-State Voltage, V_{OFF} . . . . . 80 V
Output On-State Sink Current, I_{ON} . . . . . 600 mA
Suppression Diode Off-State Voltage, V_{OFF} . . . . . 80 V
Suppression Diode On-State Current, I_{ON} . . . . . 600 mA
Power Dissipation at T_A = +25°C, P_D . . . . . 1.5 W
  Each Driver . . . . . 0.8 W
  Derating Factor . . . . . 12.5 mW/°C or 80°C/W
Operating Free-Air Temperature Range, T_A . . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC}):	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into any output (ON state)			300	mA

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current at all Inputs except Strobe	$I_{in(0)}$		MAX	0.4 V	30 V			−50	−100	μA	2
"0" Input Current at Strobe	$I_{in(0)}$		MAX	0.4 V	30 V			−100	−200	μA	
"1" Input Current at all Inputs except Strobe	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
"1" Input Current at Strobe	$I_{in(1)}$		MAX	30 V	0 V				20	μA	
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS at V_{CC} = 5.0 V, T_A = 25°C

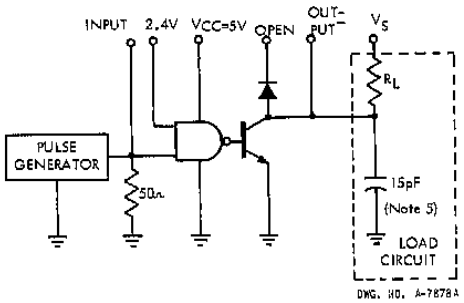
Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		300	750	ns	3

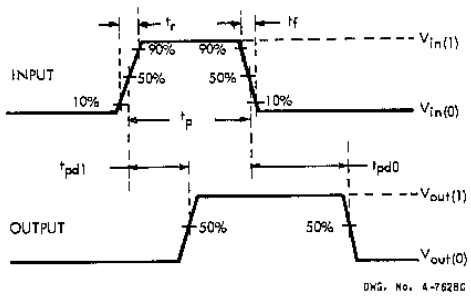
NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

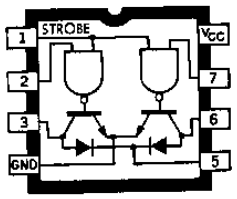
Type UDN-5711M Dual AND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.35	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			35	49	mA	1, 2



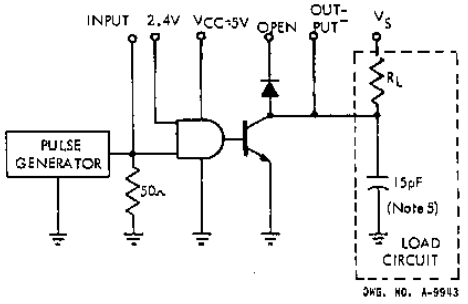


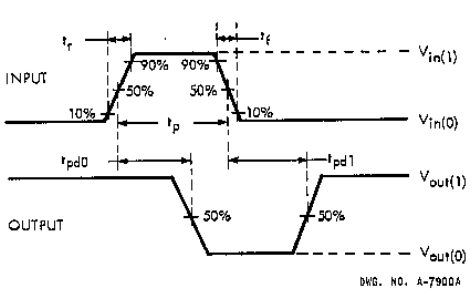


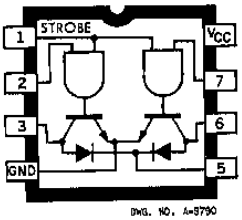
Type UDN-5712M Dual NAND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	53	mA	1, 2





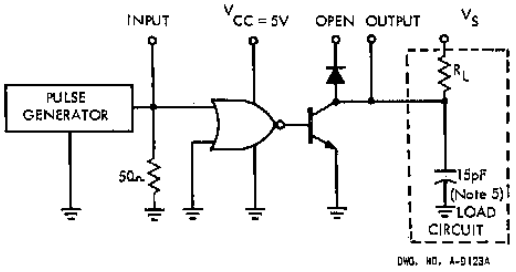


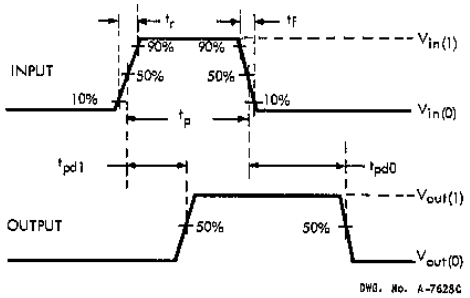
NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA
5. Capacitance values specified include probe and test fixture capacitance.

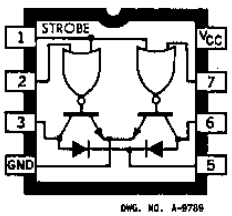
Type UDN-5713M Dual OR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA		0.35	0.5	V	
			MIN	0.8 V	0.8 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			36	50	mA	1, 2





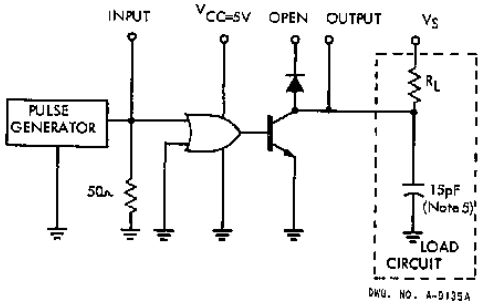


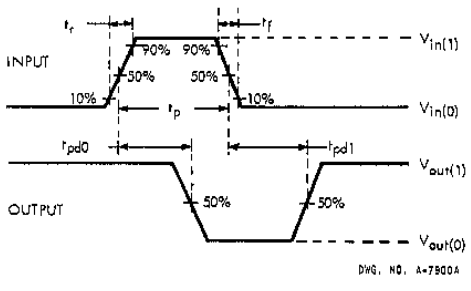
3

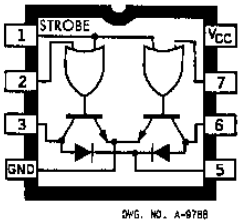
Type UDN-5714M Dual NOR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	50	mA	1, 2





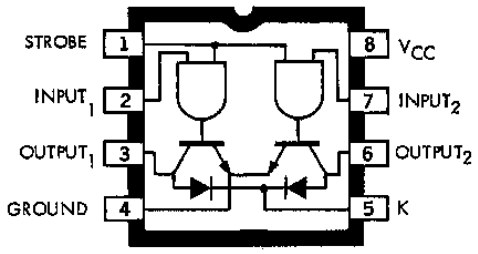


NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

SERIES UDN-5720M, UDN-5740M, UDN-5750M
DUAL PERIPHERAL/POWER DRIVERS
—Transient-Protected Outputs

FEATURES

- DTL/TTL/PMOS/CMOS Compatible
- Low Input Current
- Continuous Output Current to 700 mA
- 70 V Output Standoff Voltage
- Low Supply-Current Requirement



Dwg. No. A-9790B

UDN-5722/42/52M

PERIPHERAL AND POWER DRIVERS combining dual logic gates, high-current saturated output transistors, and transient-supression diodes are the Series UDN-5720/40/50M. These monolithic dual drivers surpass the interface requirements normally associated with standard logic buffers and are ideally suited for interface between low-level logic and high-current inductive loads. Internal transient-suppression diodes allow their use with loads such as stepping motors, relays, or solenoids. Additional (non-inductive) applications include driving peripheral loads such as light-emitting diodes, memories, heaters, and incandescent lamps with peak load currents of up to 700 mA. When not required for transient suppression, the diode common bus can be used to perform the "lamp test" function.

The Series UDN-5720M output transistors are capable of simultaneously sinking 350 mA continuously over the rated operating temperature range. The Series UDN-5740M is capable of sinking 600 mA continuously for a single output (57% duty cycle for both outputs). The series UDN-5750M will sink 500 mA continuously for a single output (86% duty cycle for both outputs). The outputs may be paralleled for higher load-current capability. In the OFF state, the drivers will withstand at least 70 V.

All devices in this series are supplied in a miniature 8-pin dual-in-line plastic package with a copper lead frame for superior package power dissipation ratings.

ABSOLUTE MAXIMUM RATINGS

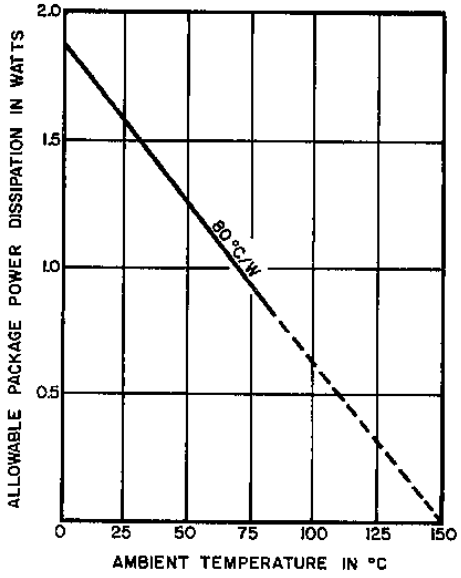
Supply Voltage, V_{CC} (UDN-5740/50M)	7.0 V
(UDN-5720M)	15 V
Input Voltage, V_{IN}	30 V
Output Off-State Voltage, V_{OFF}	70 V
Output On-State Sink Current, I_{ON} (UDN-5720/50M)	600 mA
(UDN-5740M)	700 mA
Suppression Diode Off-State Voltage, V_{OFF}	70 V
Suppression Diode On-State Current, I_{ON} (UDN-5720/50M)	600 mA
(UDN-5740M)	700 mA
Allowable Package Power Dissipation, P_D	1.5 W*
Operating Free-Air Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 12.5 mW/°C above T_A = +25°C

RECOMMENDED OPERATING CONDITIONS

Operating Condition	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC} (UDN-5720M)	4.75	—	12.6	V
(UDN-5740/50M	4.75	5.00	5.25	V
Output Current, I_{ON} (UDN-5720M)	—	—	350	mA
(UDN-5740M)	—	—	600	mA
(UDN-5750M)	—	—	500	mA
Operating Temperature Range	0	+25	+85	°C

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



Dwg. No. A-13,220

SWITCHING CHARACTERISTICS at T_A = +25°C, V_{CC} = 5.0 V

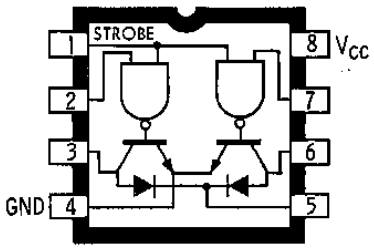
Characteristic	Symbol	Test Conditions	Limits			Notes
			Min.	Max.	Units	
Turn-On Delay Time	$t_{pd\,0}$	V_S = 30 V, R_L = 100 (10 W), C_L = 15 pF	—	500	ns	1, 2
Turn-Off Delay Time	$t_{pd\,1}$	V_S = 30 V, R_L = 100 (10 W), C_L = 15 pF	—	750	ns	1, 2

Notes: 1. Capacitance value specified includes probe and test fixture capacitance.
2. Voltage values shown in test circuit waveforms are with respect to network ground.

Input-Pulse Characteristics

$V_{IN(0)}$ = 0 V	$t_f \leq 7$ ns	t_p = 1 µs
$V_{IN(1)}$ = 3.5 V	$t_r \leq 14$ ns	PRR = 500kHz

UDN-5721M, UDN-5741M, UDN-5751M

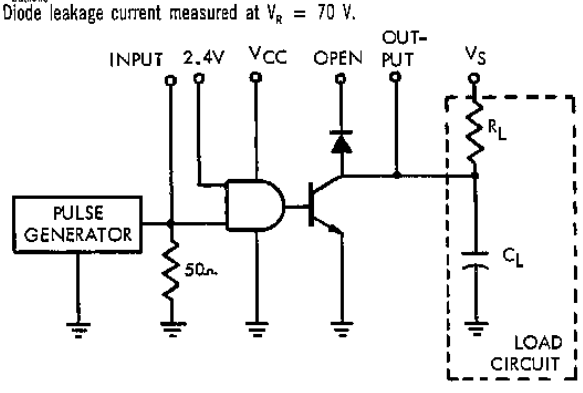


Dwg. No. A-9791A

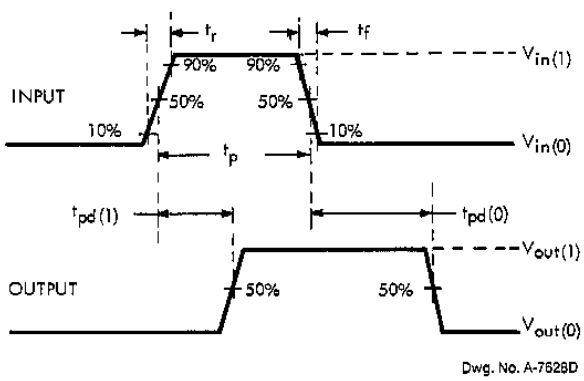
ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices*	Test Conditions				Limits				Notes
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max	Units	
Output Reverse Current	I_{CEX}	—	All	4.75	2.0 V	2.0 V	70 V	—	—	100	µA	—
				Open	2.0 V	2.0 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	5721	4.75	0.8 V	4.75 V	200 mA	—	0.4	0.6	V	—
			5741/51	4.75	0.8 V	4.75 V	300 mA	—	0.3	0.6	V	—
			5721	4.75	0.8 V	4.75 V	350 mA	—	0.6	0.8	V	—
			5751	4.75	0.8 V	4.75 V	500 mA	—	0.5	0.8	V	—
			5741	4.75	2.0 V	4.75 V	600 mA	—	0.7	1.0	V	—
Input Voltage	$V_{IN(1)}$	—	All	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	All	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(1)}$	—	All	Max.	0.4 V	30 V	—	—	−5.0	−10	µA	1, 2
	$I_{IN(1)}$	—	All	Max.	30 V	0 V	—	—	5.0	10	µA	1, 2
Strobe Input Current	$I_{IN(1)}$	—	All	Max.	0.4 V	30 V	—	—	−10	−20	µA	2
	$I_{IN(1)}$	—	All	Max.	30 V	0 V	—	—	10	20	µA	2
Input Clamp Volt.	V_{CLAMP}	—	All	4.75	−12 mA	—	—	—	—	−1.5	V	—
Diode Leakage Current	I_R	+25°C	All	5.0	0 V	0 V	Open	—	—	100	µA	3
Diode Forward Voltage	V_F	+25°C	5721	5.0	5.0 V	5.0 V	300 mA	—	1.5	1.75	V	—
			5751	5.0	5.0 V	5.0 V	500 mA	—	1.5	2.0	V	—
			5741	5.0	5.0 V	5.0 V	600 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5721	5.25	5.0 V	5.0 V	—	—	1.0	2.0	mA	—
				12.6	5.0 V	5.0 V	—	—	2.6	4.0	mA	—
			5741/51	5.25	5.0 V	5.0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5721	5.25	0 V	0 V	—	—	13	16	mA	—
				12.6	0 V	0 V	—	—	38	45	mA	—
			5741/51	5.25	0 V	0 V	—	—	20	25	mA	—

Notes:
* Complete part number includes the prefix UDN- and the package suffix M, e.g. UDN-5721M.
1. Except STROBE input, each input tested separately.
2. $V_{CC(MAX)}$ is 12.6 V for Series UDN-5720M and 5.25 V for Series UDN-5740M and UDN-5750M.
3. Diode leakage current measured at V_R = 70 V.

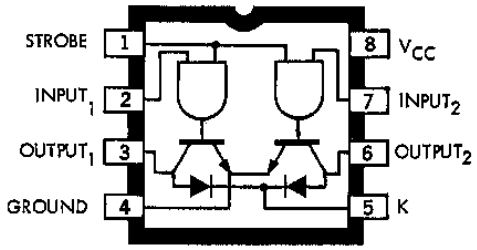


Dwg. No. A-11,746A



Dwg. No. A-7628D

UDN-5722M, UDN-5742M, UDN-5752M

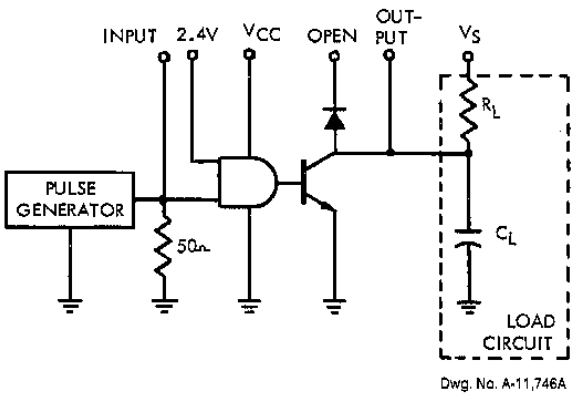


Dwg. No. A-9790B

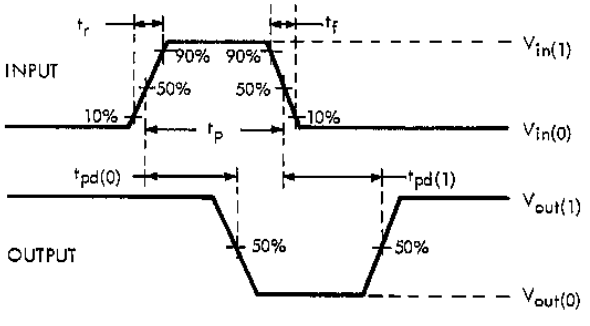
ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices*	Test Conditions				Limits				Notes
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max	Units	
Output Reverse Current	I_{CEX}	—	All	4.75	0.8 V	4.75 V	70 V	—	—	100	µA	—
				Open	0.8 V	4.75 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	5722	4.75	2.0 V	2.0 V	200 mA	—	0.4	0.6	V	—
			5742/52	4.75	2.0 V	2.0 V	300 mA	—	0.3	0.6	V	—
			5722	4.75	2.0 V	2.0 V	350 mA	—	0.6	0.8	V	—
			5752	4.75	2.0 V	2.0 V	500 mA	—	0.5	0.8	V	—
			5742	4.75	2.0 V	2.0 V	600 mA	—	0.7	1.0	V	—
Input Voltage	$V_{IN(1)}$	—	All	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	All	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	30 V	—	—	−5.0	−10	µA	1, 2
	$I_{IN(1)}$	—	All	Max.	30 V	0 V	—	—	5.0	10	µA	1, 2
Strobe Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	30 V	—	—	−10	−20	µA	2
	$I_{IN(1)}$	—	All	Max.	30 V	0 V	—	—	10	20	µA	2
Input Clamp Volt.	V_{CLAMP}	—	All	4.75	−12 mA	—	—	—	—	−1.5	V	—
Diode Leakage Current	I_R	+25°C	All	5.0	5.0 V	5.0 V	Open	—	—	100	µA	3
Diode Forward Voltage	V_F	+25°C	5722	5.0	0 V	0 V	300 mA	—	1.5	1.75	V	—
			5752	5.0	0 V	0 V	500 mA	—	1.5	2.0	V	—
			5742	5.0	0 V	0 V	600 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5722	5.25	0 V	0 V	—	—	1.0	2.0	mA	—
				12.6	0 V	0 V	—	—	2.6	4.0	mA	—
			5742/52	5.25	0 V	0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5722	5.25	5.0 V	5.0 V	—	—	13	16	mA	—
				12.6	5.0 V	5.0 V	—	—	38	46	mA	—
			5742/52	5.25	5.0 V	5.0 V	—	—	20	25	mA	—

Notes:
* Complete part number includes the prefix UDN- and the package suffix M, e.g. UDN-5722M.
1. Except STROBE input, each input tested separately.
2. $V_{CC(MAX)}$ is 12.6 V for Series UDN-5720M and 5.25 V for Series UDN-5740M and UDN-5750M.
3. Diode leakage current measured at V_R = 70 V.



Dwg. No. A-11,746A



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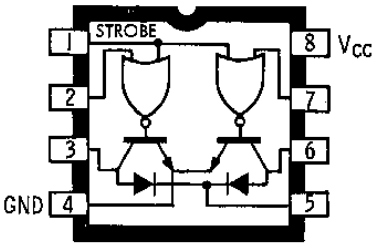
UDN-5723M, UDN-5743M, UDN-5753M

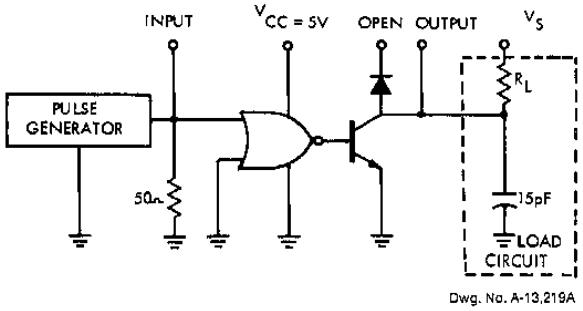


Dwg. No. A-9789A

ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices*	Test Conditions				Limits				Notes
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max	Units	
Output Reverse Current	I_{OEX}	—	All	4.75	2.0 V	0 V	70 V	—	—	100	µA	—
				Open	2.0 V	0 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	5723	4.75	0.8 V	0.8 V	200 mA	—	0.4	0.6	V	—
			5743/53	4.75	0.8 V	0.8 V	300 mA	—	0.3	0.6	V	—
			5723	4.75	0.8 V	0.8 V	350 mA	—	0.6	0.8	V	—
			5753	4.75	0.8 V	0.8 V	500 mA	—	0.5	0.8	V	—
			5743	4.75	0.8 V	0.8 V	600 mA	—	0.7	1.0	V	—
Input Voltage	$V_{IN(1)}$	—	All	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	All	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	30 V	—	—	−5.0	−10	µA	1, 2
	$I_{IN(1)}$	—	All	Max.	30 V	0 V	—	—	5.0	10	µA	1, 2
Strobe Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	30 V	—	—	−10	−20	µA	2
	$I_{IN(1)}$	—	All	Max.	30 V	0 V	—	—	10	20	µA	2
Input Clamp Volt.	V_{CLAMP}	—	All	4.75	−12 mA	—	—	—	—	−1.5	V	—
Diode Leakage Current	I_R	+25°C	All	0	0 V	0 V	Open	—	—	100	µA	3
Diode Forward Voltage	V_F	+25°C	5723	5.0	5.0 V	5.0 V	300 mA	—	1.5	1.75	V	—
			5753	5.0	5.0 V	5.0 V	500 mA	—	1.5	2.0	V	—
			5743	5.0	5.0 V	5.0 V	600 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5723	5.25	5.0 V	5.0 V	—	—	1.0	2.0	mA	—
				12.6	5.0 V	5.0 V	—	—	2.6	4.0	mA	—
			5743/53	5.25	5.0 V	5.0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5723	5.25	0 V	0 V	—	—	13	16	mA	—
				12.6	0 V	0 V	—	—	38	45	mA	—
			5743/53	5.25	0 V	0 V	—	—	20	25	mA	—

Notes:
* Complete part number includes the prefix UDN- and the package suffix M, e.g. UDN-5723M.
1. Except STROBE input, each input tested separately.
2. $V_{CC(MAX)}$ is 12.6 V for Series UDN-5720M and 5.25 V for Series UDN-5740M and UDN-5750M.
3. Diode leakage current measured at V_R = 70 V.



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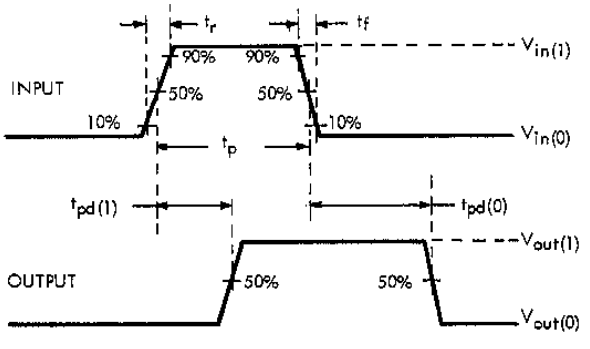
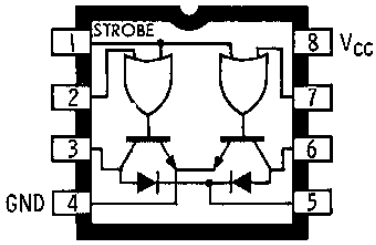


Dwg. No. A-7628D

UDN-5724M, UDN-5744M, UDN-5754M

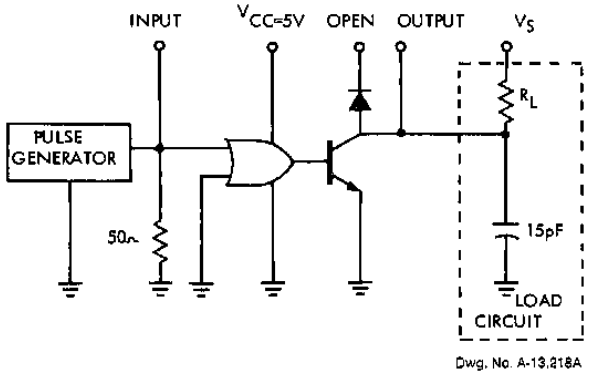


Dwg. No. A-9788A

ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	Applicable Devices*	Test Conditions				Limits				Notes
				V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max	Units	
Output Reverse Current	I_{CEX}	—	All	4.75	0.8 V	0.8 V	70 V	—	—	100	µA	—
				Open	0.8 V	0.8 V	70 V	—	—	100	µA	—
Output Voltage	$V_{CE(SAT)}$	—	5724	4.75	2.0 V	0 V	200 mA	—	0.4	0.6	V	—
			5744/54	4.75	2.0 V	0 V	300 mA	—	0.3	0.6	V	—
			5724	4.75	2.0 V	0 V	350 mA	—	0.6	0.8	V	—
			5754	4.75	2.0 V	0 V	500 mA	—	0.5	0.8	V	—
			5744	4.75	2.0 V	0 V	600 mA	—	0.7	1.0	V	—
Input Voltage	$V_{IN(1)}$	—	All	4.75	—	—	—	2.0	—	—	V	—
	$V_{IN(0)}$	—	All	4.75	—	—	—	—	—	0.8	V	—
Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	0 V	—	—	−5.0	−10	µA	1, 2
	$I_{IN(1)}$	—	All	Max.	30 V	30 V	—	—	5.0	10	µA	1, 2
Strobe Input Current	$I_{IN(0)}$	—	All	Max.	0.4 V	0 V	—	—	−10	−20	µA	2
	$I_{IN(1)}$	—	All	Max.	30 V	30 V	—	—	10	20	µA	2
Input Clamp Volt.	V_{CLAMP}	—	All	4.75	−12 mA	—	—	—	—	−1.5	V	—
Diode Leakage Current	I_R	+25°C	All	5.0	5.0 V	5.0 V	Open	—	—	100	µA	3
Diode Forward Voltage	V_F	+25°C	5724	5.0	0 V	0 V	300 mA	—	1.5	1.75	V	—
			5754	5.0	0 V	0 V	500 mA	—	1.5	2.0	V	—
			5744	5.0	0 V	0 V	600 mA	—	1.5	2.0	V	—
Supply Current (Total Package)	$I_{CC(1)}$	+25°C	5724	5.25	0 V	0 V	—	—	1.0	2.0	mA	—
				12.6	0 V	0 V	—	—	2.6	4.0	mA	—
			5744/54	5.25	0 V	0 V	—	—	1.0	3.0	mA	—
	$I_{CC(0)}$	+25°C	5724	5.25	5.0 V	5.0 V	—	—	13	16	mA	—
				12.6	5.0 V	5.0 V	—	—	38	45	mA	—
			5744/54	5.25	5.0 V	5.0 V	—	—	20	25	mA	—

Notes:
* Complete part number includes the prefix UDN- and the package suffix M, e.g. UDN-5724M.
1. Except STROBE input, each input tested separately.
2. $V_{CC(MAX)}$ is 12.6 V for Series UDN-5720M and 5.25 V for Series UDN-5740M and UDN-5750M.
3. Diode leakage current measured at V_R = 70 V.



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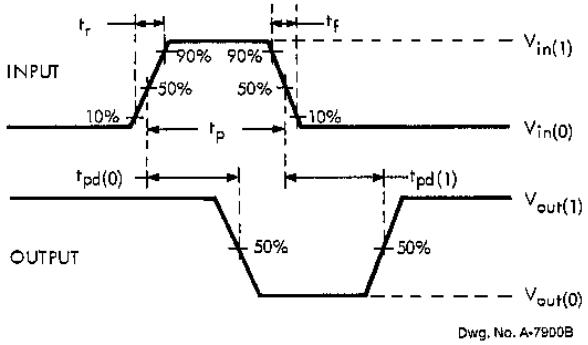


Dwg. No. A-7900B

SERIES ULN-2000A DARLINGTON TRANSISTOR ARRAYS*

—Description and Application

Introduction

The increased use of electronic circuits in systems formerly built with mechanical, electro-mechanical, or hydraulic components has resulted in systems becoming more precise, more reliable, generally less expensive, smaller, more efficient, and faster. Although the drive capabilities of monolithic integrated logic circuits are adequate for most information processing applications, there now exists a large and rapidly growing number of system applications where the current-carrying and/or voltage-sustaining capability of the integrated circuit logic is inadequate. Typically, these deficiencies arise when the logic must control such peripheral components as relays, solenoids, punches, stepping motors, and a variety of indicators (incandescent, LED, or gas discharge lamps and displays).

A very common solution to this output interface inadequacy has been the addition of discrete power transistors (or SCRs) and associated passive components to the logic output in order to obtain the necessary current and/or voltage capability. Although this provides a very satisfactory electrical solution, the large number of discrete components often required, high assembly labor costs, and space (packaging) limitations often mean additional problems and cost. A simple, and less expensive solution is the use of monolithic integrated circuits.

The Series ULN-2000A is comprised of four different high-voltage/high-current interface circuits. They are capable of controlling resistive, inductive, or tungsten filament loads of up to 125 watts and are compatible with all standard digital logic families (DTL, TTL, PMOS, and CMOS) without the need for additional discrete components.

High-Voltage and High-Current Capability

A large number of interface problems have been simplified by the Series ULN-2000A high-voltage, high-current Darlington transistor arrays. These devices are suitable for voltage, current, and gain levels beyond the limits of other monolithic buffers and arrays.

The four devices in the ULN-2000A series are all comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for use with inductive loads.

All devices have an output sink current capability of 500 mA although peak inrush currents to 600 mA are permissible, making them ideal for use with tungsten filament lamps. All of the outputs will sustain "OFF" voltages of at least 50 volts. Each individual Darlington circuit may therefore switch up to 25 watts (50 V at 500 mA).

A definite asset of monolithic device technology is the very fine match between adjacent outputs when used in parallel. Applications requiring a sink current beyond the capability of a single output can be accommodated by parallel outputs. Continuous operation of all outputs at the maximum rated current is not allowed because of power dissipation limitations imposed by the package. However, as illustrated in Figure 1, under certain conditions, the Series ULN-2000A Darlington arrays are capable of switching loads totaling more than 125 watts at an ambient temperature of +70°C.

*Examples and data in this application note apply equally to Series ULN-2800A Darlington arrays.

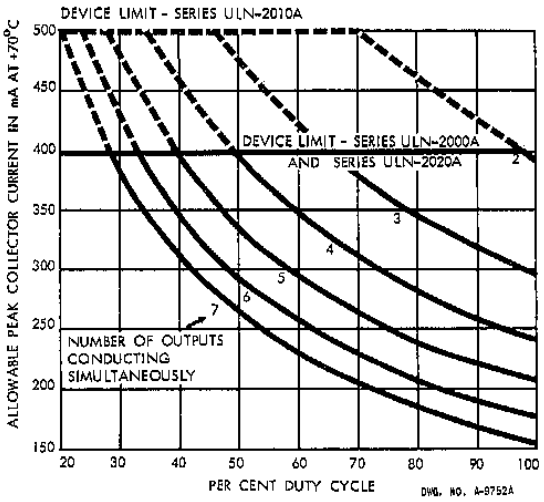


Figure 1

COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS

3

High-Power Capability

A primary limitation of many interface circuits is the power dissipation of the device package. Until recently, very little concern was expressed for monolithic integrated circuit power dissipation. Improvements in silicon device technology have brought about a growing number of monolithic circuits capable of power considerably in excess of present package technology.

The Series ULN-2000A is supplied in a 16-pin dual in-line plastic package with a copper lead frame. Shown in Figure 2 is a comparison of the allowable package power dissipation for the industry standard iron-nickel alloy (Kovar) lead frame and the Sprague copper lead frame used on these devices. As shown, at an ambient temperature of +70°C, the Kovar lead frame allows only 0.64 watts while the copper lead frame allows 1.33 watts. At +25°C the copper lead frame permits a package power dissipation of 2.0 watts!

Actual power dissipation in any application for the Series ULN-2000A devices is the sum of the individual driver power dissipations. In turn, the individual driver dissipation is the product of the collector-emitter saturation voltage, the collector current, and the duty cycle. The collector-emitter saturation voltage is dependent on the collector current and, to a lesser extent, operating temperature.

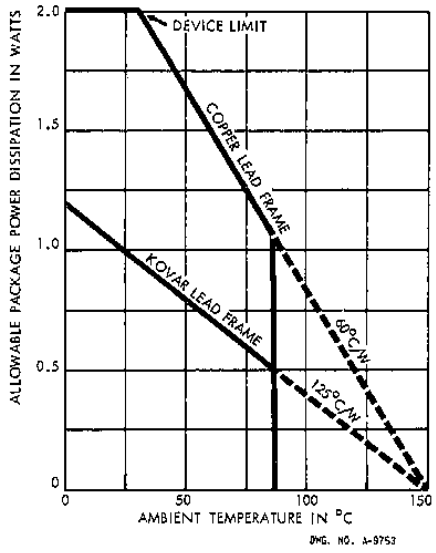


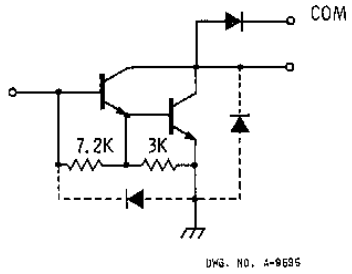
Figure 2

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

The Basic Darlington Array

The first, and basic array, in this series, is the Type ULN-2001A. This is a general-purpose version with input current limiting normally accomplished via the use of an appropriate discrete resistor connected in series with each input. It is also possible to utilize the intrinsic current limiting of many MOS outputs as shown in Figure 4; a typical P-channel characteristic.

The use of TTL in such a manner is not recommended due to the higher currents and resultant high level of package power dissipation. Outputs of most PMOS and CMOS circuits will not normally source currents of any significance due to their high source impedance.



(each driver)

Figure 3

TYPE ULN-2001A SCHEMATIC

14 to 25 Volts PMOS Applications

The Type ULN-2002A Darlington array was specifically designed for use with 14 to 25 volt PMOS devices. Each input has a 7 V Zener diode and a 10,500 ohm resistor (nominal values) to limit the input current to within the capability of most PMOS of the type specified. The basic circuit diagram is shown in Figure 5 with a typical application. Note that there are *no* pull-down resistors or other external discrete components necessary. The incorporation of the Zener diode also results in excellent noise immunity for this array.

TTL and CMOS INTERFACE

The ULN-2001A and ULN-2002A allow only a limited number of input options. Shown in Figure 6 is the basic circuit diagram of the Type ULN-2003A. This device has a series base input resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS logic operating at a supply voltage of 5 V (or 12 V CMOS using FET characteristics).

A guarantee of 200 mA output sink current capability (saturated) is provided with the worse case TTL logic *1* level of 2.4 volts. Low-power Schottky-clamped TTL logic is generally specified to have a minimum V_{OUT} of 2.7 volts. The ULN-2003A is guaranteed to sink 250 mA under this input condition. With the more typical input of 3 volts, the ULN-2003A Darlington pair will sink at least 300 mA in the "ON" state.

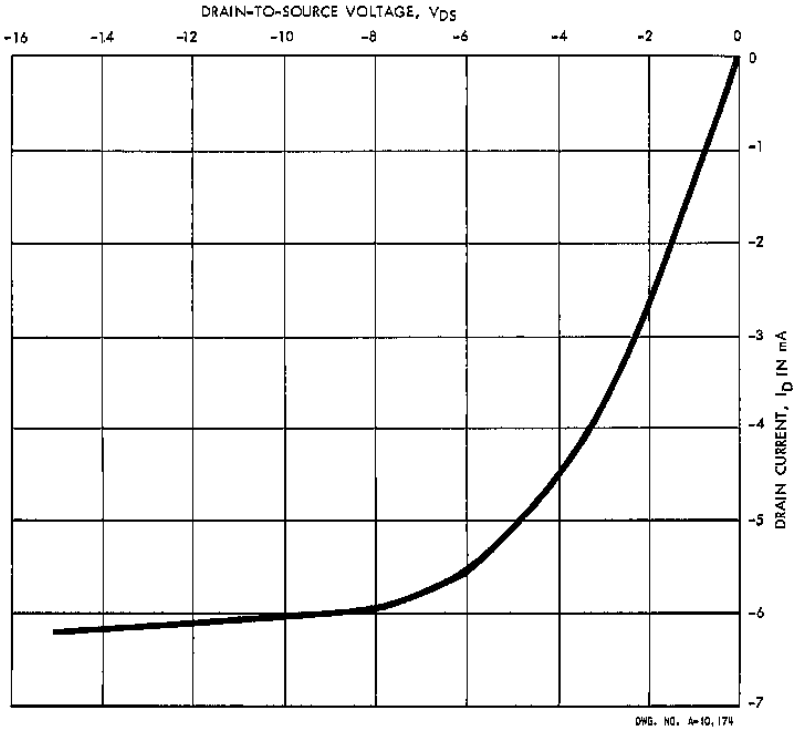


Figure 4

TYPICAL P-CHANNEL DRAIN CHARACTERISTIC

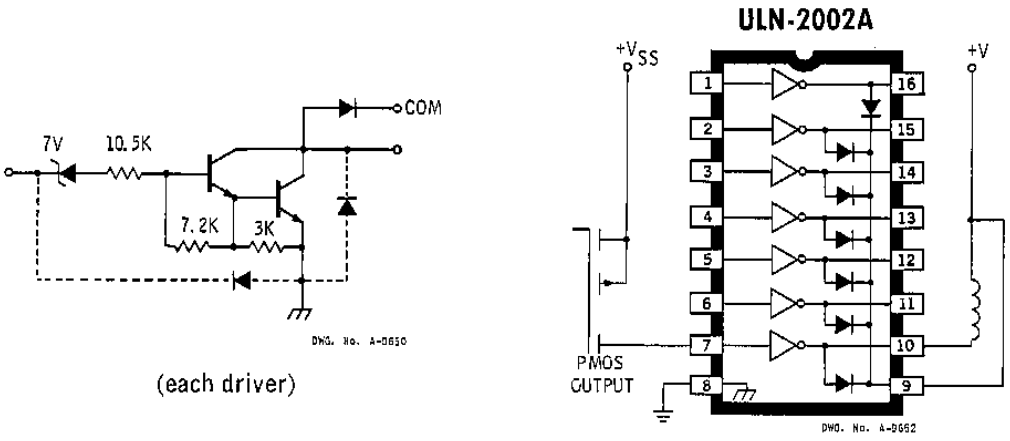


Figure 5
TYPE ULN-2002A SCHEMATIC AND APPLICATION

3

TTL totem pole outputs are not specified between the 400 μA logic *1* fanout condition and the maximum output short-circuit current (20 to 55 mA for the 7400 series). Between these rather wide limits lies the required ULN-2003A input current. The maximum Type ULN-2003A input current level is specified at 1.35 mA at the extrapolated TTL maximum logic *1* level of 3.85 V.

The ULN-2003A Darlington array will handle a great many interface needs – particularly those beyond the capabilities of TTL buffers. Also shown in Figure 6, is a typical application of the ULN-2003A Darlington array. Of particular interest in this application is an unusual use of the transient-suppression diodes for a non-inductive load. The lamp test feature can of course be used with any of the devices in this series.

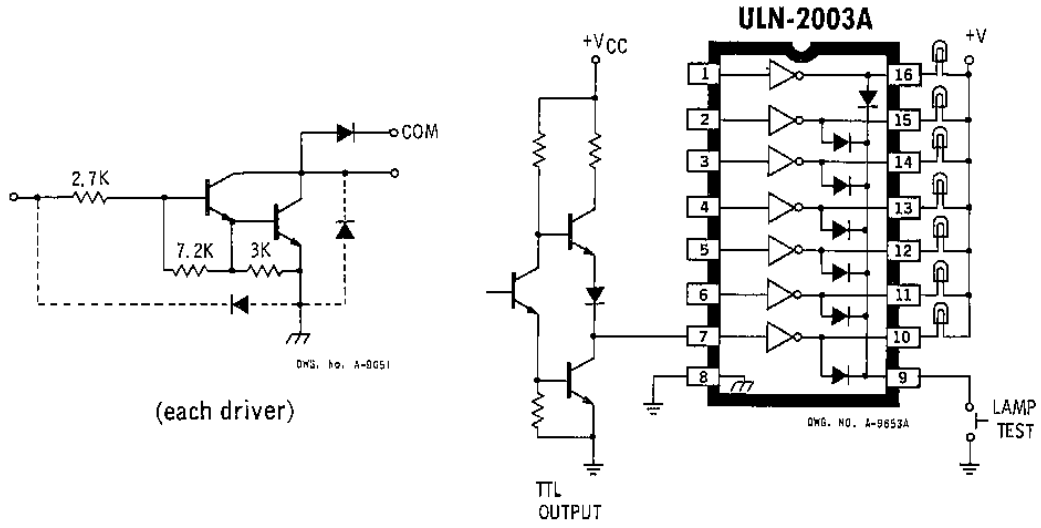


Figure 6
TYPE ULN-2003A SCHEMATIC AND APPLICATION

The diodes are designed to handle the same current and voltages as the output transistors. Switching can be accomplished through an ordinary switch or an appropriate power transistor. With the standard +70°C ambient and the most widely used lamps (No. 327 or No. 387 lamps) there is no problem with continuous operation.

6 to 15 Volt CMOS or PMOS Applications

The Type ULN-2004A Darlington array has an appropriate series input resistor (nominally 10.5 kΩ) to allow its operation directly from CMOS or PMOS logic outputs utilizing supply voltages of between 6 and 15 V.

Shown in Figure 7 is a typical application of this array. Although the discrete output buffer could be used to increase the output capability of any of the devices in this series, this is most often done by paralleling outputs as was described earlier.

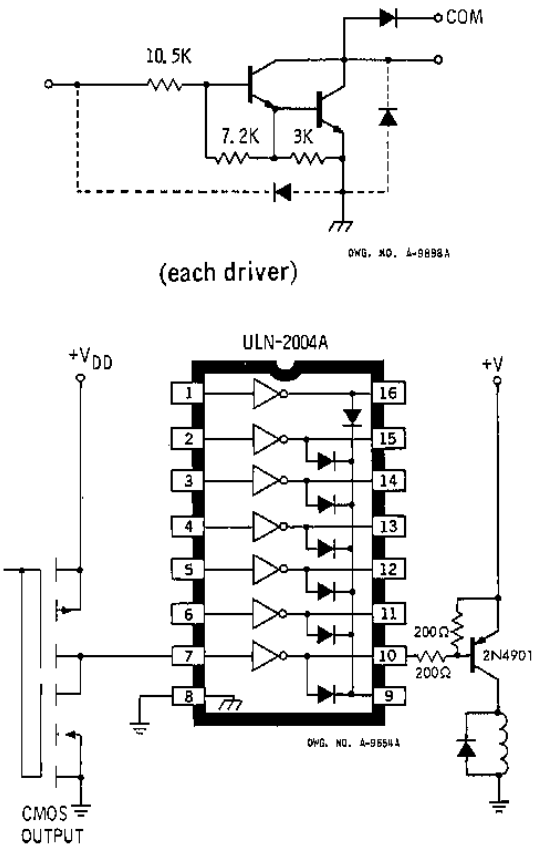


Figure 7
Type ULN-2004A SCHEMATIC AND APPLICATION

Input Current

The Darlington collector current (output in saturation) at an ambient temperature of +25°C, for any input current is the same for all four devices in this series and is shown in the graph of Figure 8. More accurately, the maximum input current for any collector current is described by the equation:

$$I_{IN(\mu A)} = I_{C(mA)} + 140\ \mu A$$

where I_{IN} is the input current in microamperes, I_C is the collector current in milliamperes, and the figure 140 represents the maximum shunt current through the emitter-base resistors. The typical input current can be described as:

$$I_{IN(\mu A)} = 0.58\ I_{C(mA)} + 110\ \mu A$$

where the figure 0.58 is an adjustment for the typical Darlington current gain and the figure 110 represents the typical shunt current.

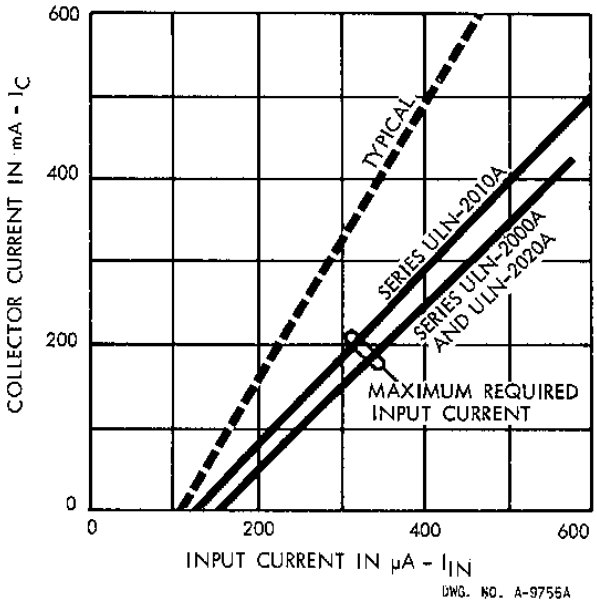


Figure 8
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT

The input current as a function of input voltage is shown in Figure 9 for the ULN-2002A, ULN-2003A, and the ULN-2004A. The Type ULN-2001A Darlington array is not shown since input current is more a function of the external circuitry. Systems utilizing either CMOS or PMOS logic should be evaluated for intrinsic current limiting as was shown in Figure 4.

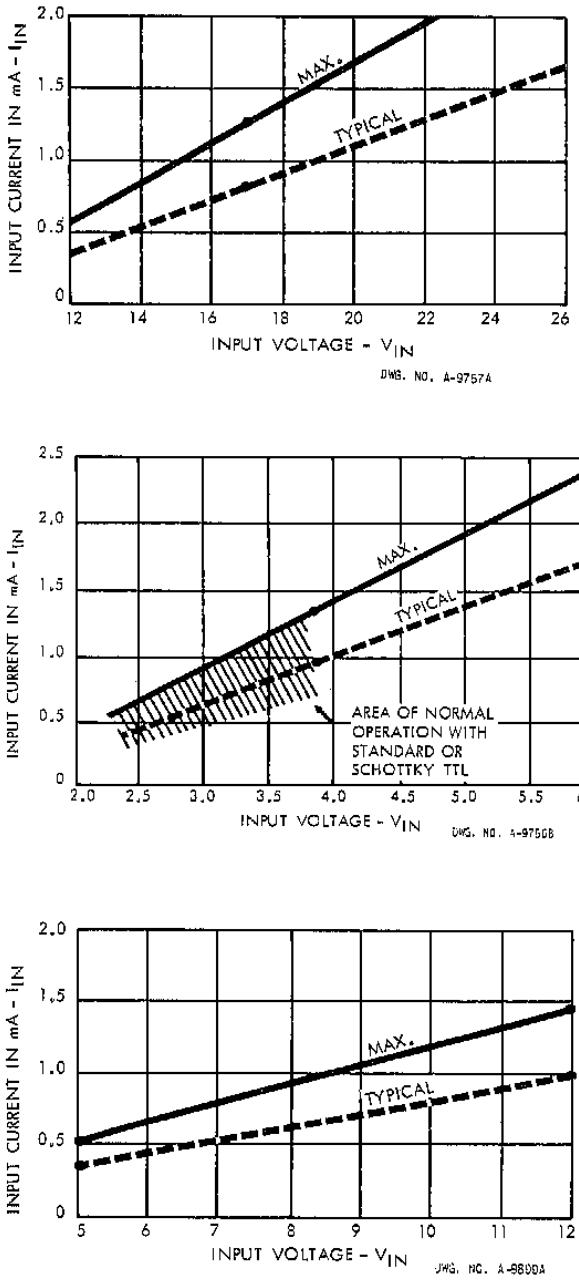


Figure 9

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

Low Available Drive Current Operation

Occasionally, applications featuring minimum available input drive current and a high output load current have shown the Type ULN-2003A and ULN-2004A Darlington arrays to be inadequate for the particular requirement under worst case conditions. This usually results from the restricted drive current available from a TTL or CMOS gate operating from a nominal supply of 5 volts.

Under worst case conditions with a low logic *1* voltage (2.4 V), and a high input resistor value (3.51 kΩ), the available load current is reduced to only 145 mA. Compounding this problem would be the effect that a high drive current requirement would have on the logic output voltage since that is normally specified at only 400 μA. If the gate output is connected to additional logic elements, a minimum logic *1* voltage of 2.0 V must be maintained and at that level the worst case Darlington load current would be reduced to only 31 mA!

A simple solution to this problem is through the use of inexpensive pull-up resistors as shown in Figure 10. The minimum resistor value is determined by the maximum allowable sink current (16 mA for TTL, 360μ A for CMOS), the minimum logic *0* output voltage, and the maximum supply voltage as per the following equation:

$$R_P \geq \frac{V_S - V_{OUT(0)}}{I_{OUT}}$$

For standard TTL, the minimum value for R_P is about 316 Ω with values between 3000 Ω and 5000 Ω being used customarily. Multiple pull-up resistors in a single in-line package are shown in Sprague Engineering Bulletin No. 7041; resistors in a dual in-line package are shown in Bulletin No. 7042.

Conclusion

Since the Series ULN-2000A high-voltage, high-current Darlington transistor arrays are quite conservatively designed, the basic product is fully capable of being ordered to higher voltages and/or higher currents than the standard specifications. Presently, parts are available to withstand up to 95 volts on the output. Parts with this higher voltage rating would create a potential for switching loads far in excess of 125 watts! Aside from the higher power handling capability, the higher voltage rating is required for driving plasma or gas-discharge displays.

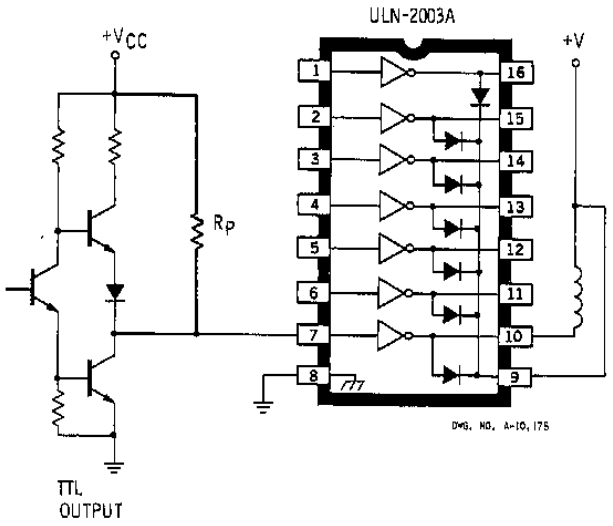


Figure 10
USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT

Although not intended for high power applications, there is also available a Series ULS-2000H with hermetic sealing and an operating temperature range to +125°C. These parts are recommended for military and aerospace applications as well as commercial and industrial control applications where severe environments may be encountered.

Cer-DIP, industrial-grade hermetic devices, Series ULQ-2000R, are rated for use over the temperature range of −40°C to +85°C, permitting their use in commercial and industrial applications requiring a moderate package power dissipation (1 W at T_A = +85°C).

All of these Darlington transistor arrays offer a common solution to a great many interface needs. The minimal component count and straightforward printed wiring board layout offer benefits in cost reduction, simplicity of board layout, and savings in space. Other benefits are a reduction in insertion costs, and lower handling and inventory costs than other alternatives. Cost benefits from some of these factors are not very tangible. However, fewer components, less complex boards, etc. usually result in lower system manufacturing costs.

EXPANDING THE FRONTIERS OF IC INTERFACE FOR ELECTRONIC DISPLAYS

INTRODUCTION

The original monolithic high-voltage/high-current power drivers from Sprague were capable of sustaining 100 V and sinking load currents of 250 mA on each of four outputs. That 1970 peripheral driver capability has since been expanded and improved on to solve many of the most difficult display interfaces. Our newest devices are rated for operation to 130 V, sourcing or sinking to 1.5 A, and as many as eight drivers per package (not all together) with inputs for TTL, Schottky TTL, DTL, CMOS, and PMOS.

LAMP (INCANDESCENT) INTERFACE

Utilizing marketing inputs that related to existing hybrid interface circuits, a group at Sprague designed and manufactured monolithic ICs which initially were largely used for aircraft indicator lamp interface. Although not widely known, these quad driver units were developed quite independently (and simultaneously) to the ubiquitous TI 75451 series of high-speed, low-voltage peripheral drivers. A concentration upon circuit design factors, improvements in DIP packaging (copper alloy lead frames), and tighter, tougher control of diffusion-related parameters has allowed the manufacture of quad power drivers rather than the dual mini-DIPs offered by TI.

An increased awareness for improvements in reliability and space and power reductions provided a rather successful military market for Sprague lamp and relay interface; early success was evident in military aircraft indicator lamp interface, a tough application for TTL type ICs due to severe inrush currents resulting in secondary breakdown during "turn on". The increased current sinking capability of the Sprague ICs offers a solution to lamp interface that usually obviates the need for "warming" resistors (across the output) which slightly warm the lamp filament and thus minimize problems associated with cold lamp filaments.

The relay driver types of Sprague IC drivers (and other similar transient-protected ICs) are somewhat more useful than the so-called general purpose types, since the diode common terminal may be switched for a system lamp test. As shown in Figure 1, only a single connection to each DIP is required.

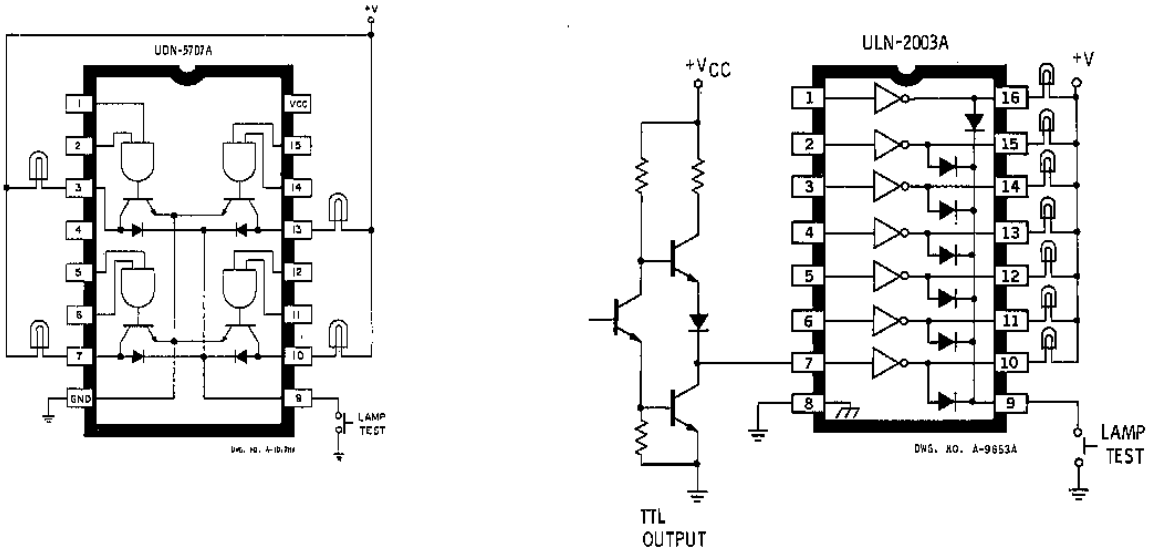


Figure 1

The high current-sinking capability of the Sprague ICs allow such loads as the #327 or #387 lamps to be driven without difficulty of secondary breakdown. The device beta will usually not allow sinking of the 10 to 13 times (nominal value) inrush current of cold lamps; but the lamp rapidly reaches a current level within the device output limitations (Figure 2 shows current as a function of time for a single #327 lamp). Sustaining this instantaneous inrush current and its peak power has been a key element in the success of many lamp interface circuits.

GAS DISCHARGE DISPLAY ICs

Early in 1972, Sprague successfully produced its first high-voltage IC designed for gas discharge displays—a five channel, 130 V unit for cathode (segment) interface. Subsequently, other circuits, both cathode and anode drivers, were produced; most of which were used in calculator applications with the Burroughs Panaplex® II. In Figure 3 is shown a display interface system utilizing the UHP-481 and UHP-491 display drivers, associated thick-film networks, and discretes. This was a step forward, but still required external discrete components.

Through a collaborative effort begun late in 1973 between Sprague Electric and Burroughs Corp. a newer, more efficient interface scheme evolved. Featured in "Electronic Displays '75," this series of monolithic IC interface devices for the high-voltage gas discharge panels has been one of the trailblazers in the world of display interface ICs. Intended for use in multiplexed display systems, these ICs present one of the easiest and least expensive solutions to a difficult interface problem. A combination of high-voltage bipolar techniques with thin-film resistor technology (circuit resistors sputtered over the IC dielectric) has provided both digit (anode) and segment (cathode) interface.

To facilitate a minimum component interface, a split supply (± 100 V) is employed to allow d-c level-shifting (rather than capacitors or >200 V transistors) and both digit and segment drivers incorporate all pull-up, pull-down, current limiting, off-bias reference, etc. which were formerly required in discrete and/or hybrid systems. With the combination of the digit and segment drivers (each capable of withstanding 120 V), the split power supply approach affords PN diode IC technology suitable for driving a display usually requiring a 180 V minimum ionization voltage (equivalent to ±90 V in the split system).

The use of the Series UDN-6100/7100A gas discharge display drivers shows the need for only two monolithic ICs for displays of up to eight digits and eight segments as shown in Figure 4. Systems requiring digit or segment counts greater than eight employ additional driver ICs, and with the exception of the Type UDN-7180A segment driver, the segment ICs all have outputs with internal current-limiting resistors for the display segments. The UDN-7180A device, for reasons of package power dissipation and/or dissimilar segment currents (certain 14 or 16 segment alphanumeric panels) can also be used, but must have external, discrete current-limiting resistors.

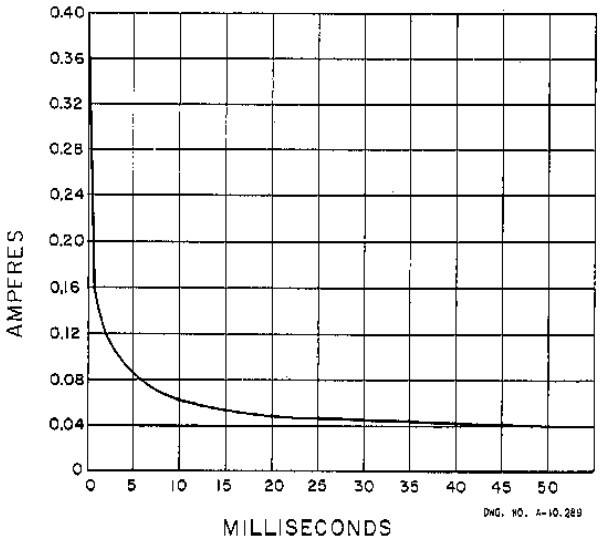


Figure 2

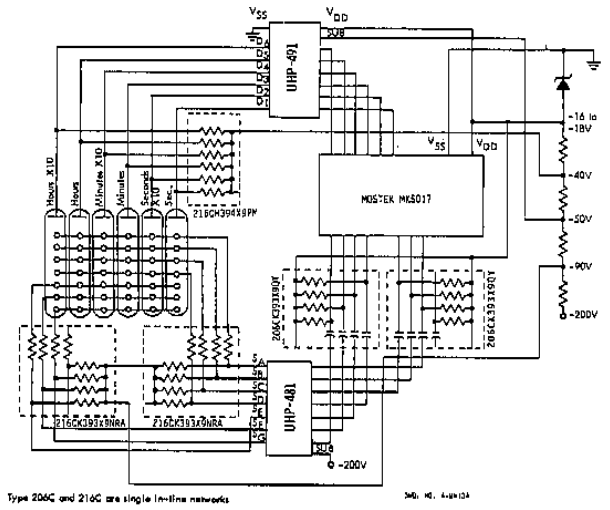


Figure 3

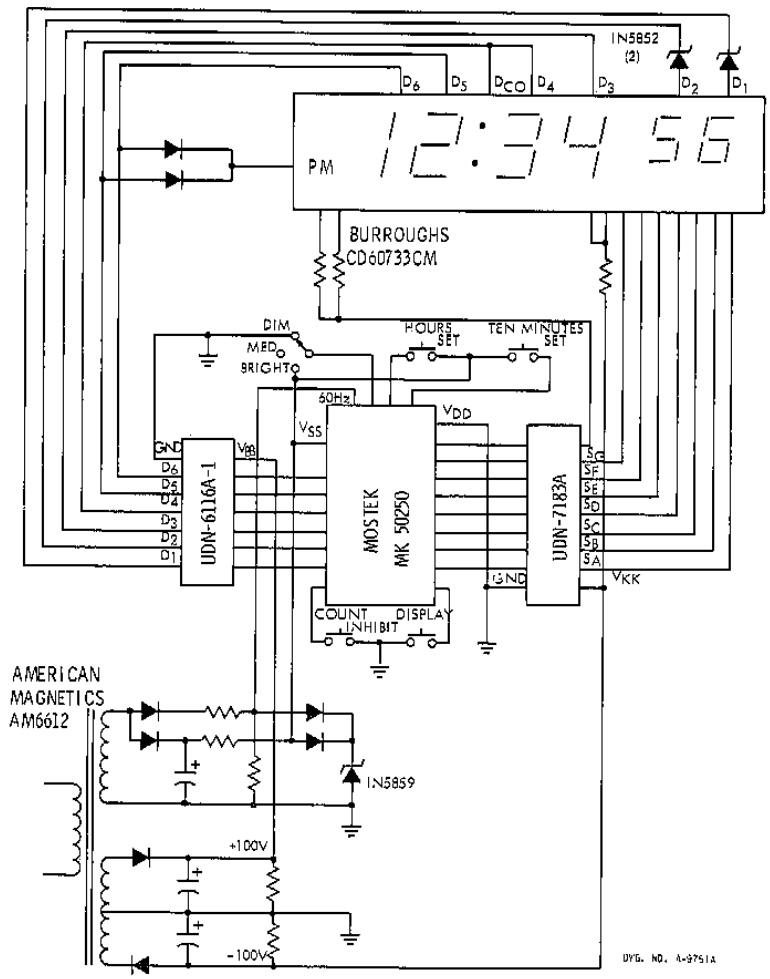


Figure 4

Higher current applications are difficult for both programmable current and switching type display drivers. Segment currents beyond 2.5 or 3 mA present package power dissipation limitations to most dual in-line packages. By using external resistors, the Type UDN-7180A driver allows segment currents of up to 14 mA.

The transistor switch with current-limiting resistor scheme used in Sprague gas discharge display drivers also minimizes problems associated with gas panel arcing which can destroy programmable current circuits. Some of the gas display manufacturers recommend the use of series resistors in each segment line to prevent destruction to the semiconductor interface circuit should such a panel arc occur. Without these series resistors (internal thin-film resistors in Sprague devices) the IC can be destroyed by the high voltage and resulting high current should the panel voltage drop to a very-low level during an arc.

LED INTERFACE

With the obvious abundance and variety of LED interface integrated circuits it would seem unlikely that there are still systems in search of an IC hardware solution to further minimize cost, component count, space, etc.; but this is definitely the case. The deficiencies are chiefly related to the limited number of current-sourcing circuits and/or high-current drivers.

The efficiency of LED displays has improved, but with the larger digits (up to 1" presently) most of the IC drivers are unable to switch the higher currents required in multiplexed systems. The rule-of-thumb generally applied uses the suggested d-c current - multiplied by the number of digits in the display. For example, a multiplexed display of 160 mA peak current will give approximately the same light intensity output as a steady 20 mA in each of eight digits. Of particular difficulty is the switching of currents associated with the lower efficiency yellow and green LEDs. Sprague has provided monolithic integrated circuit solutions to applications requiring segment currents of 350 mA and digit currents of up to 1.5 amperes!

Many of the Sprague ICs used in high-current LED applications were originally designed for use with electro-mechanical loads (relays, solenoids, motors, etc.) although the high-voltage ratings of the drivers are obviously not a concern. A combination of high-current, high-voltage Darlington drivers is shown in Figure 5.

The ULN-2074B source driver is utilized as a modified emitter-follower. Through the use of discrete diodes in the common collector line, allowing the base to be switched to a potential higher than the collector, it is then possible to obtain a saturated output. This prevents the usual emitter-follower problems associated with gain, the MOS output impedance, and power. It is also possible to now better define the voltage at the emitter output and to then provide suitable segment current-limiting resistors for the LEDs.

The ULN-2002A sink driver is a high-current Darlington array with the capability of switching multiplexed LEDs with an available limit of 155 mA for each of the seven drivers when used at a 100% duty cycle. Even the more inefficient yellow or green LEDs can be driven with higher output currents at lower duty cycles (400 mA at a 28% duty cycle).

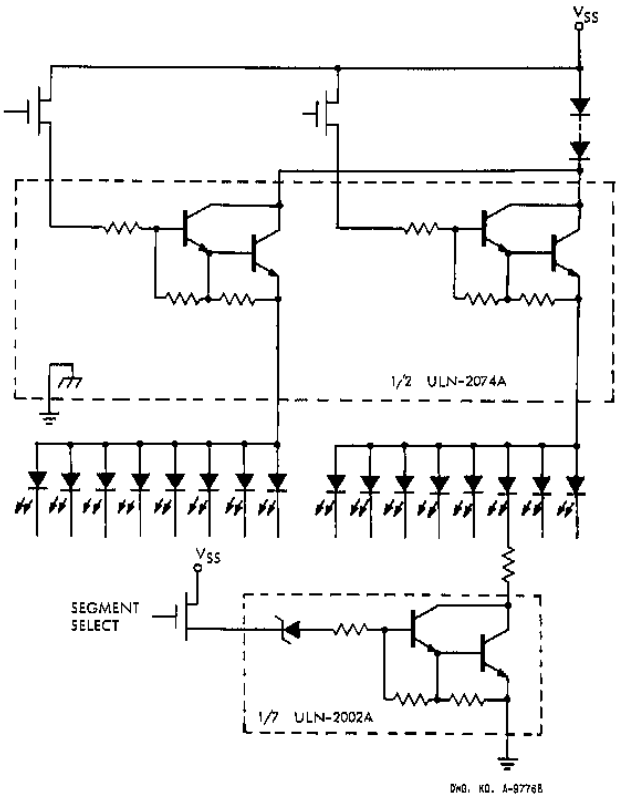


Figure 5

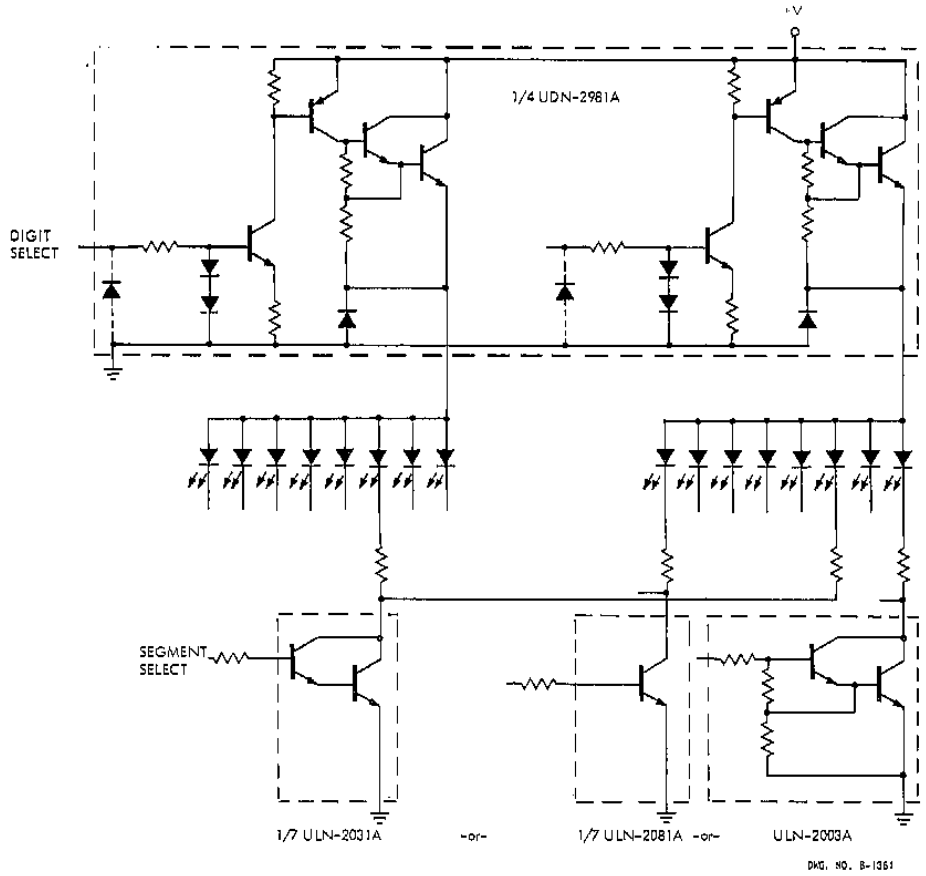


Figure 6

A new eight-channel source driver is shown as a digit switch for common anode LEDs in Figure 6. The Series UDN-2980A drivers will handle output currents to a maximum of 500 mA. Two basic versions of the driver will allow interface from TTL, Schottky TTL, DTL, PMOS, and CMOS levels. Other versions of the ULN-2003A driver are also available for use with the various logic levels.

Of the three sink drivers shown, the ULN-2003A is probably the better choice from a standpoint of both pinout and component count. It also has straightforward in-out pinning. The ULN-2031A and ULN-2081A devices offer lower cost. They are also interchangeable from a pinning aspect although the output ON voltage will be dissimilar.

A common-cathode LED configuration is shown in Figure 7 for currents of up to 1.5 A per digit! A series UDN-2980A source driver is used to switch the segment side, the ULN-2064B or ULN-2074B to switch the digit side. As has been shown with Figure 5, the IC package power dissipation must be considered with high-current applications.

The three examples that have been shown for LED interface represent only a very-small portion of the total applications area. The high-current capabilities and high gain of the Sprague drivers represent potential solutions to many difficult LED display systems - alphanumeric, seven-segment, or matrix; common-cathode or common-anode; continuous or multiplexed.

A-C PLASMA DISPLAY INTERFACE

Plasma displays, such as those manufactured by National Electronics/NCR (USA) and NEC or Fujitsu (Japan), all have one common element with their gas discharge cousin - both types use a neon gas mixture. The plasma panels emit an orange glow when switched at rather high frequencies, and light output intensity is a function of frequency. The a-c term for the plasma display is something of a misnomer since these panels actually operate from a toggled d-c supply (usually in the area of 20 kHz).

The panel is basically a neon-filled capacitor, and has plates (electrodes) which are covered with the dielectric - between which is the neon mixture. Switching this capacitive load presents a problem

with high peak currents in addition to the older problem of the high voltages which are associated with gas displays. Drive circuits use supply voltages of 150 to 260 V (depending on unipolar or bipolar drive), and the semiconductors used must switch instantaneous currents in the order of several hundred milliamperes for the larger displays.

Several high-voltage, high-current arrays made at Sprague Electric can provide an answer to one side of the a-c plasma display interface. The Series ULN-2020A Darlingtons are rated at 95 V while the Series UHP-500 power drivers are rated at 100 V. They are both able to handle the application shown in Figure 8 (a basic d-c, non-multiplexed clock interface rather than a more complex multiplexed system). The ULN-2022A is specifically designed for 14 to 25 V PMOS logic levels while the UHP-506 is intended for use with TTL.

The high-current diodes that are internal to the Sprague arrays are utilized in the unipolar drive scheme connected to a suitable OFF reference. In one POS application, a set of 14 ULN-2023A Darlington drivers replaced more than 400 discrete components. The cost and space savings in such a machine are considerable, and a very complex printed wiring board was greatly simplified.

Further improvements in interface and plasma displays will no doubt evolve, and thus benefit all concerned - display and interface vendor along with the end user. Plasma displays are well-suited to custom panels (particularly those with various sizes of characters) and with improvements in IC breakdown voltages some further simplification of interface should evolve.

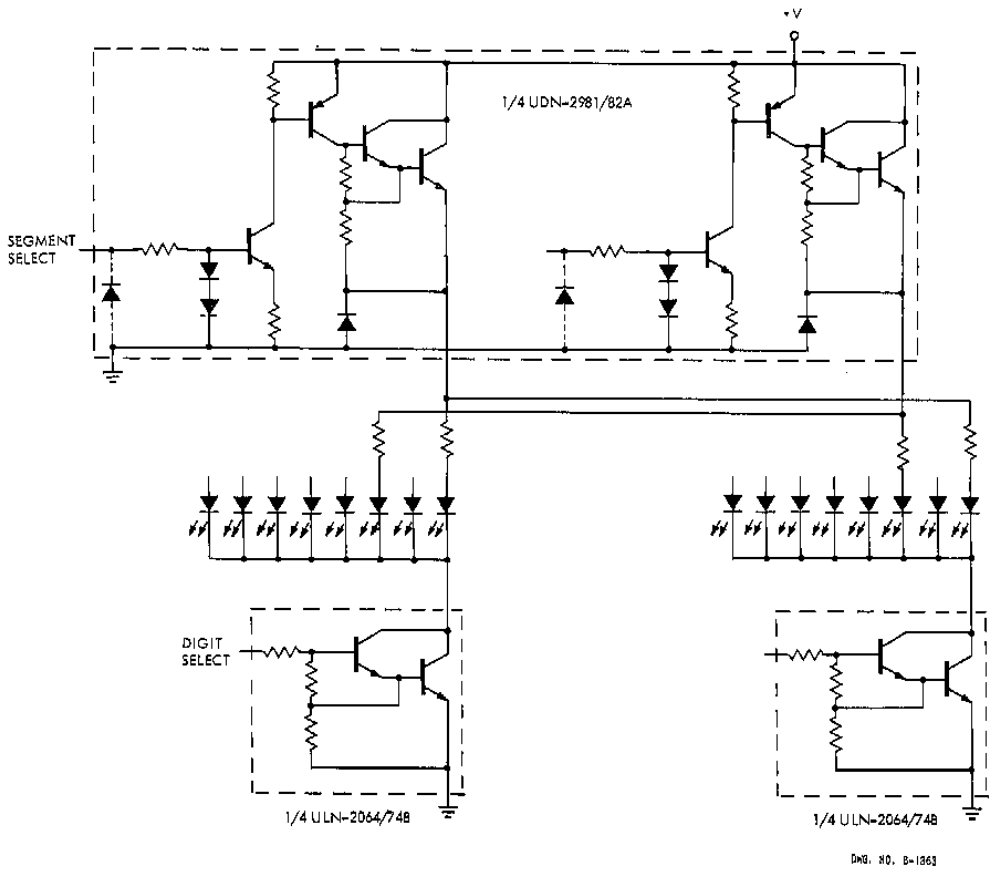


Figure 7

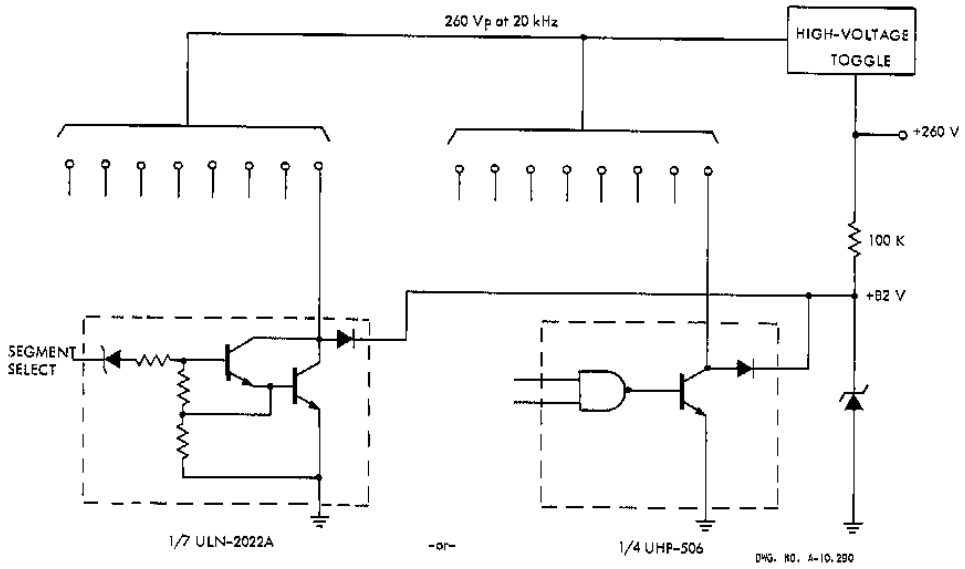


Figure 8

FLUORESCENT DISPLAY INTERFACE

Although the vast majority of fluorescent displays are directly driven from MOS logic (handheld and low-cost desk calculators), there is an emerging need for interface integrated circuits for use with the larger characters (higher currents) and the higher voltages coming into use. These blue-green display panels originated in Japan, and the manufacturers are quite aggressively pursuing markets such as POS systems, clocks, cash registers, appliances, automotive displays, etc. Larger and/or more complex styles are being made, including displays with alphanumeric capability (a starburst 14 or 16-segment pattern).

Modest voltage capability (60 or 70 volts) is all that is required of a semiconductor device to drive these panels, and the currents are in 20 to 30 mA region. These electrical requirements are well within the capability of many gas discharge digit drivers.

The UDN-6118/28A devices are designed specifically for use with fluorescent displays and include internal pull-down resistors so that up to eight segments and eight digits will require only two packages and a greatly simplified power supply. The Type UDN-6118A driver is compatible with TTL, Schottky TTL, DTL, and 5 volt CMOS. The Type UDN-6128A driver is for use with 6 to 15 volt PMOS or CMOS logic.

The future of fluorescent displays look rather strong, particularly if competition further reduces prices. For the moment at least, these displays will not seriously tax the capability of IC interface except, perhaps, from a price/cost standpoint.

HOT WIRE READOUTS

Although hot wire readouts could easily be placed in the incandescent category, their application in multidigit, multiplexed display systems more closely resembles LED circuit operation. Since hot wire displays will conduct current in either direction, isolation diodes are required to prevent sneak paths from partially turning ON unaddressed segments. Compare the typical hot wire display of Figure 10 with LED display of Figure 6. The availability of a suitable, inexpensive diode array would be of considerable asset in multiplexed hot wire systems.

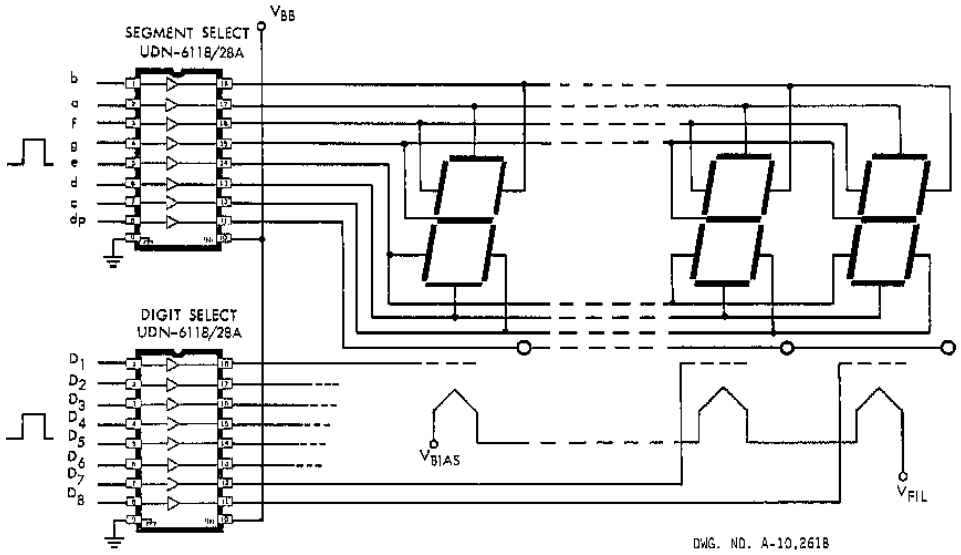


Figure 9

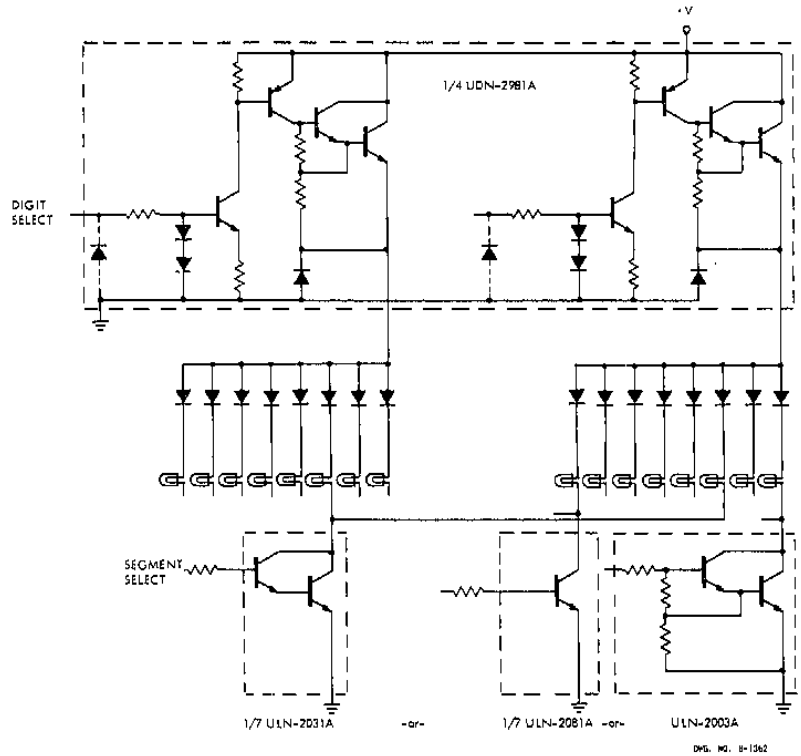


Figure 10

The hot wire readouts are available in both seven-segment and alphanumeric (16-segment) versions and are quite well-suited to high ambient light applications. They do not wash out in sunlight, although their reliability diminishes with the higher currents required in brightly lighted applications. As described, multiplexed schemes can be cumbersome because of the great number of discrete diodes required. One avionics system using a 16-character, 16-segment alphanumeric panel required 256 discrete diodes.

INTEGRATED CIRCUITS FOR CURRENT-SOURCING APPLICATIONS

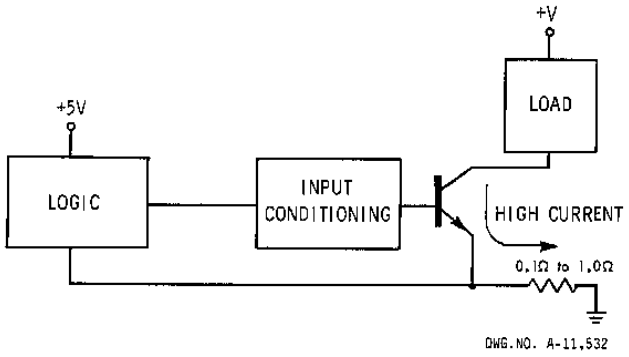
DURING RECENT YEARS, the appearance of many new low-power monolithic devices (LSI and microprocessors) has created an increased need of peripheral power driver integrated circuits. Interface drivers are typically categorized in terms of their output-drive functions. When current flows out of the driver output terminal and into the load, the device is said to "source" current. Conversely, current flows from a load into a "sink" driver.

Sprague integrated source drivers usually consist of high-voltage PNP devices and high-power NPN Darlington outputs (which provide PNP-type action), with input-level shifting. These power ICs are useful for interfacing low-level logic (TTL, CMOS, NMOS, PMOS) and high-current or high-voltage relays, solenoids, lamps (incandescent, LED, neon), motors, and displays (gas-discharge, LED, vacuum-fluorescent). They can also be used to provide multi-channel buffers for discrete power semiconductors.

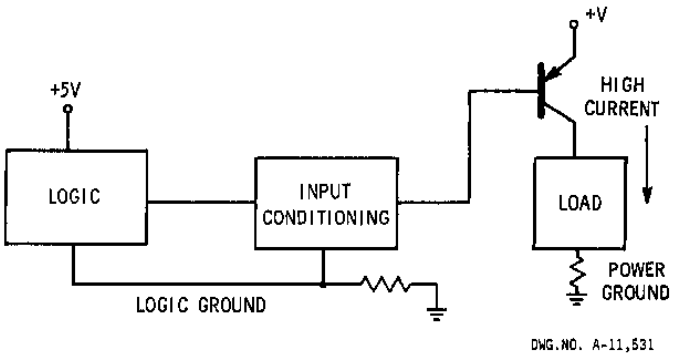
The advantages of source drivers for display interface are quite evident. The X-Y addressing of most readouts requires both source and sink functions to minimize pin count, interconnections, and package count.

A more subtle advantage of source drivers is related to their use with inductive loads or incandescent lamps. Both types of load generate troublesome transients and noise currents on common logic/load ground lines. In addition, high ground currents can shift the ground rail, affecting logic input levels, thresholds, and noise immunity. The use of source drivers can minimize many of these concerns by separating the logic and power returns.

FLOATING LOGIC-GROUND LEVEL
(Sink Driver)



SEPARATE GROUND RETURNS
(Source Driver)



RELAY-DRIVER APPLICATIONS

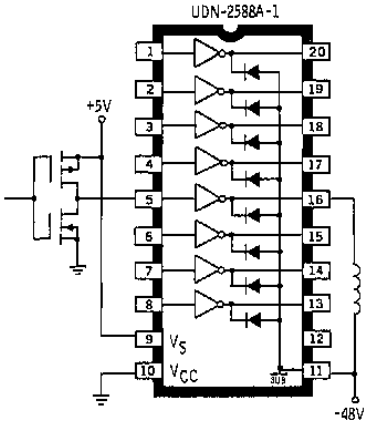
SERIES UDN-2580A, eight-channel source drivers, and Types UDN-2956A and UDN-2957A, five-channel source drivers, provide current/voltage translation from TTL, positive CMOS, or negative CMOS logic to −48 V telecommunication relays requiring less than 350 mA. All devices have internal inductive-load transient-suppression diodes.

Type UDN-2580A-1 is best driven from negative-reference CMOS or NMOS logic (−5 V or −12 V swing) in order to provide a −48 V swing at the output. The active-low input Type UDN-2588A-1 can be driven from positive logic TTL (+5 V swing) or CMOS (+12 V swing) levels. The active-high input Type UDN-2956A is similar to Type UDN-2588A-1, but it also has a chip-enable function that requires a minimum number of drive lines to control outputs from several packages in a simple multiplex scheme.

RECOMMENDED MAX. OPERATING CONDITIONS

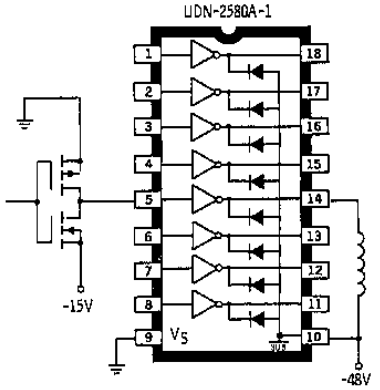
Supply Voltage, V_{EE} ..... −50 V
Continuous Output Current, I_{OUT} (per output) ..... −350 mA

TELECOMMUNICATIONS RELAY DRIVER (Positive Logic)



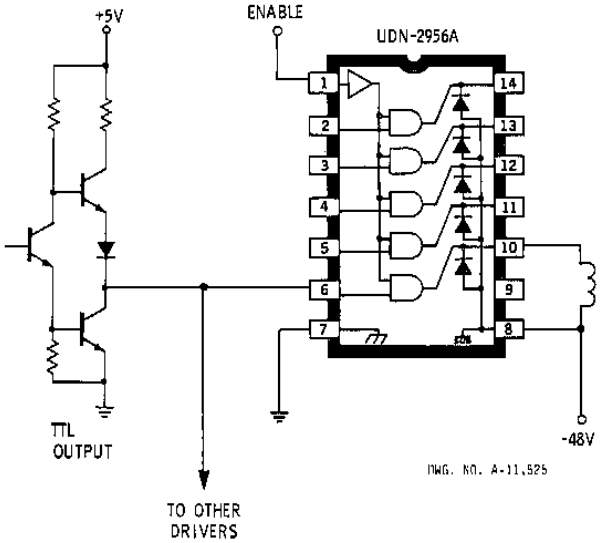
DWG. NO. A-11,524

TELECOMMUNICATIONS RELAY DRIVER (Negative Logic)



DWG.NO. A-11,538

MULTIPLEXED RELAY DRIVER



DWG. NO. A-11,525

PRINTER APPLICATIONS

SPRAGUE SOURCE DRIVERS have been used extensively in electrosensitive, thermal, and impact printer applications. Multi-channel devices in the Series UDN-2580A and UDN-2980A reduce parts count and provide up to 350 mA per output at voltages up to 75 V (resistive load). Copper lead frames make these devices capable of simultaneously delivering up to 125 mA continuously from all eight channels at an ambient temperature of +50°C.

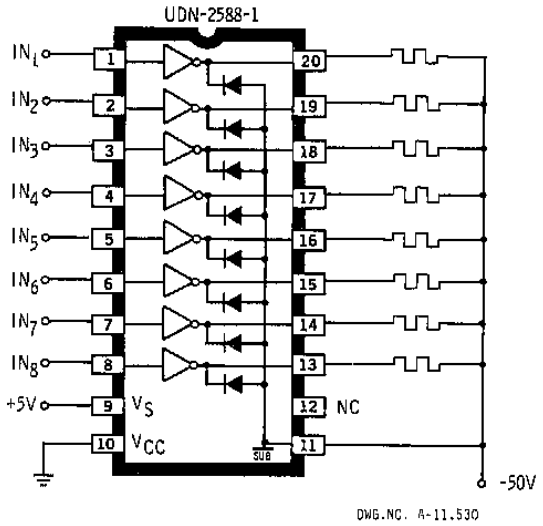
RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage Range, V_S
- UDN-2588A-I . . . . . to 75 V
- UDN-2981A and UDN-2982A . . . . . 5 V to 45 V
- UDN-2983A and UDN-2984A . . . . . 35 V to 75 V

Logic Voltage, V_{IN} . . . . . 12 V
Continuous Output Current, I_{OUT} (per output) . . . . . −350 mA
Peak Output Current, I_{OP} . . . . . −500 mA

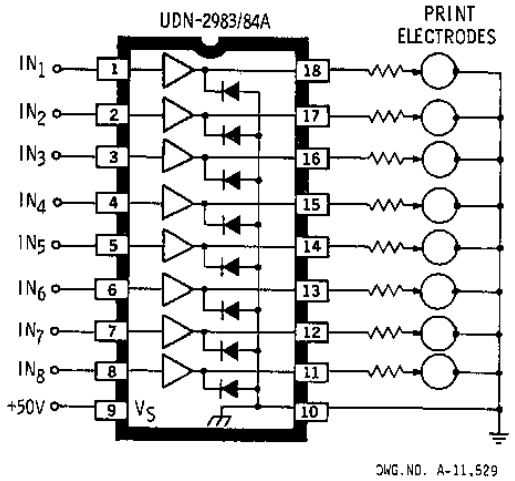
3

THERMAL PRINTER APPLICATION



DWG.NO. A-11,530

ELECTROSENSITIVE PRINTER APPLICATION



DWG.NO. A-11,529

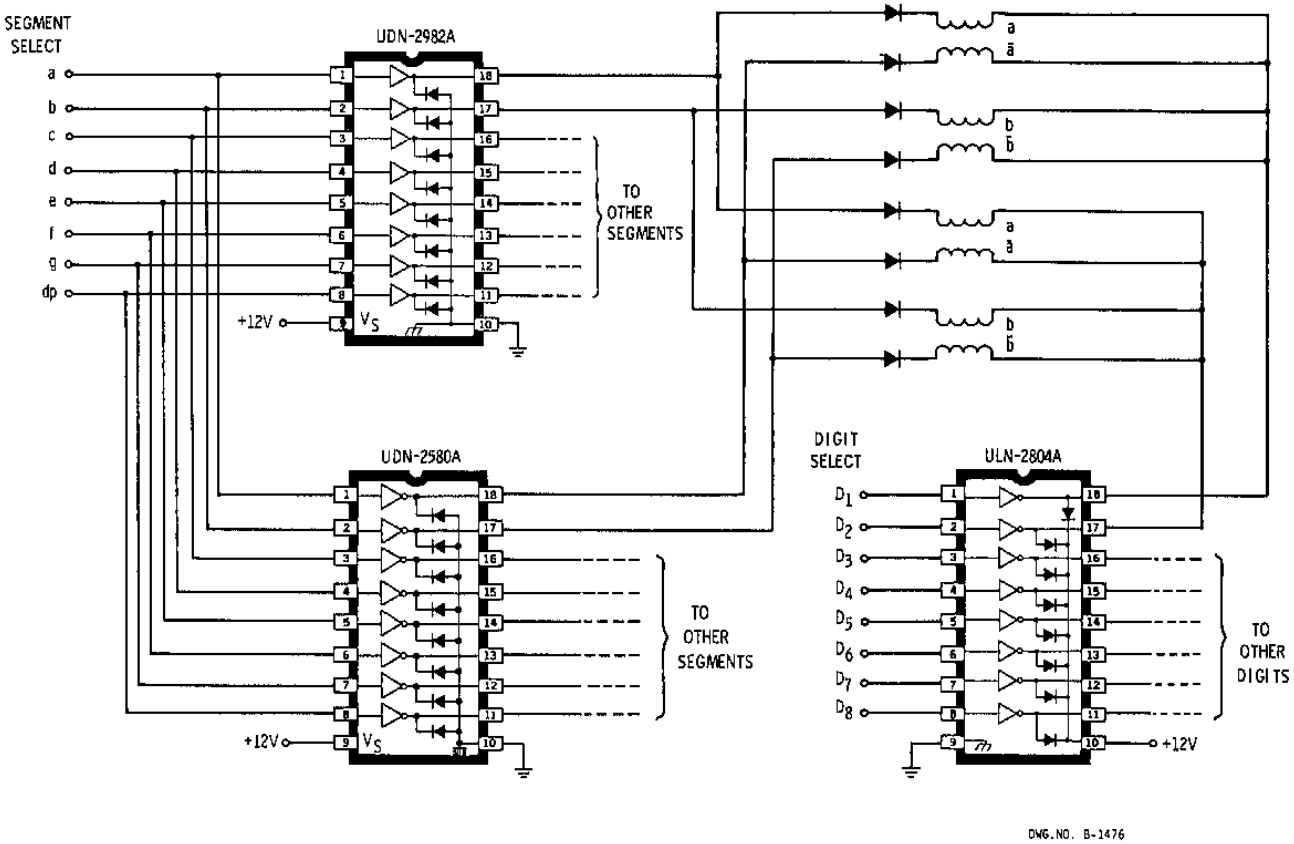
ELECTRO-MECHANICAL DISPLAY APPLICATIONS

SOURCE DRIVERS in the Series UDN-2580A and UDN-2980A, when combined with the Type ULN-2804A sink driver, provide a simple interface between 12 V CMOS logic and a multiplexed electro-mechanical display. As shown, the need for additional inverter packages is eliminated since Type UDN-2580A is activated by a low input level and Type UDN-2982A is turned ON by a high input level. All drivers have internal inductive-load transient-suppression diodes and copper lead frames for improved package power dissipation capability.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage, V_S ..... 35 V
Continuous Output Current, I_{OUT} (per output) ..... −350 mA

MULTIPLEXED ELECTRO-MECHANICAL DISPLAY DRIVERS



VACUUM-FLUORESCENT/GAS-DISCHARGE DISPLAY APPLICATIONS

SPRAGUE SERIES UDN-6100A and UDN-2580A source drivers provide solutions to problems encountered in driving higher-voltage vacuum-fluorescent and planar gas-discharge displays. Both series of parts provide TTL, CMOS, and NMOS input-logic compatibility. Series UDN-6100A devices are active high (non-inverting) drivers. Series UDN-2580A drivers are active low (inverting) devices.

At minimum cost, Series UDN-6100A-2 devices offer 60 V output breakdowns for vacuum-fluorescent displays typically utilizing less than 32 characters. Featuring a minimum 80 V output breakdown voltage, standard Series UDN-6100A drivers (no additional suffix) guarantee 25 mA per output. Suffix -1 devices provide for a 110 V breakdown, recommending them for 40 to 80-digit or dot-matrix V-F applications or gas-discharge anode-drive applications requiring the higher output voltage. All of these drivers include internal pull-down resistors and provide operation from single-ended positive supplies.

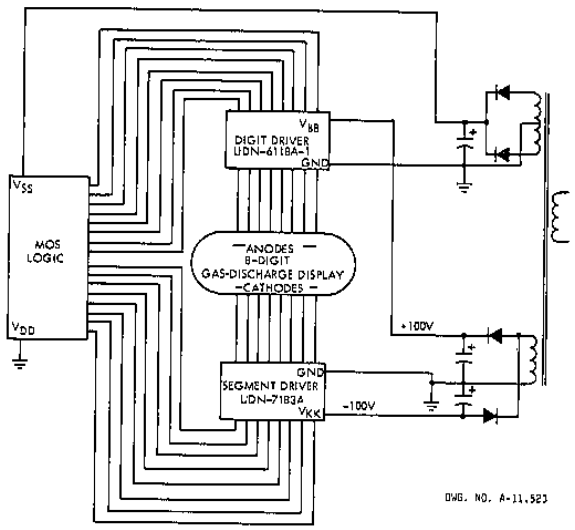
Operation from a split-supply allows the user to bias the V-F filament at ground potential or to utilize a system-supply voltage above ground (±40 V instead of +80 V). Either Type UDN-6138A or Type UDN-6148A source drivers are recommended.

For vacuum-fluorescent display applications requiring a higher current capability (operating several displays with common drive circuitry), Type UDN-2588A can be used with appropriate external output pull-down resistors to provide up to 350 mA per output.

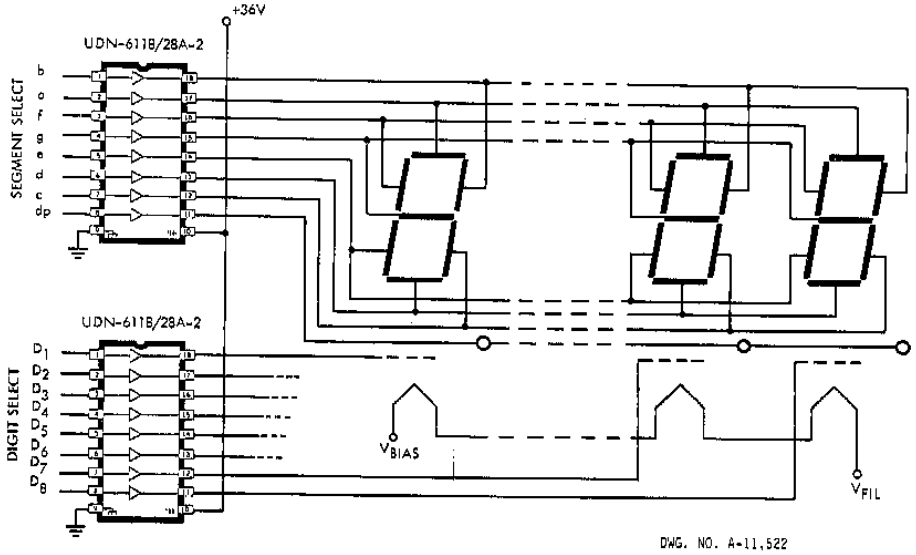
MAXIMUM OPERATING VOLTAGES

V_S V_{BB}	$V_{IN(ON)}$	$V_{IN(OFF)}$	V_{CC}	$V_{EE(MAX)}$	Device Type
+5	<1.4	>4.5	0	−45	UDN-2588A
				−75	UDN-2588A-1
+12	<8.4	>11.5	0	−45	UDN-2588A
				−75	UDN-2588A-1
+30	2.4	<0.4	NA	−30	UDN-6138A-2
	4.0	<0.4	NA	−30	UDN-6148A-2
+40	2.4	<0.4	NA	−40	UDN-6138A
	4.0	<0.4	NA	−40	UDN-6148A
+60	TTL or CMOS		NA	0	Series UDN-6100A-2
+80	TTL or CMOS		NA	0	Series UDN-6100A
+110	TTL or CMOS		NA	0	Series UDN-6100A-1

GAS-DISCHARGE DISPLAY DRIVERS

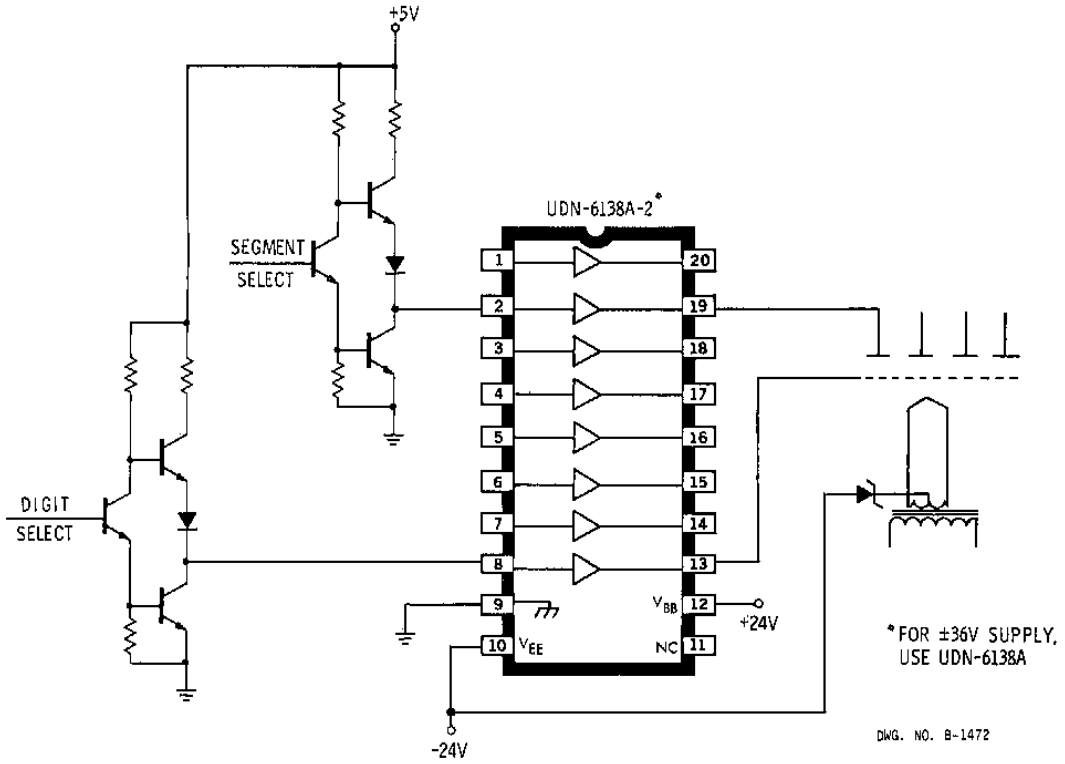


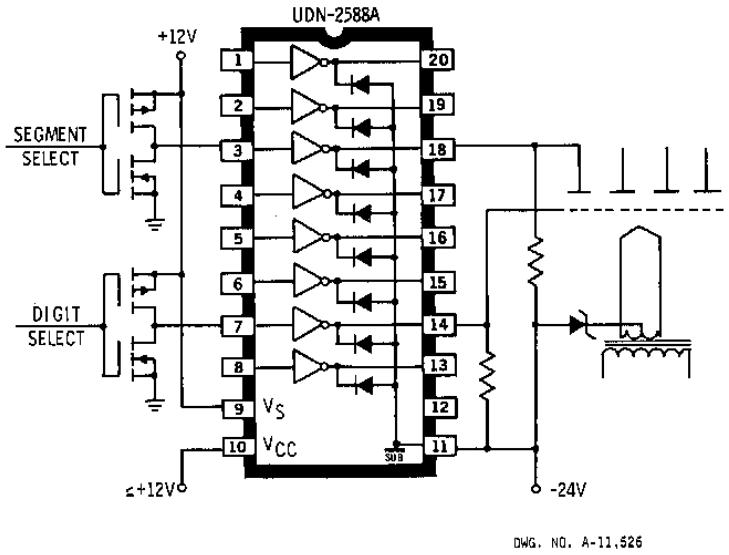
MULTIPLEXED VACUUM-FLUORESCENT DISPLAY DRIVERS



VACUUM-FLUORESCENT/GAS-DISCHARGE DISPLAY APPLICATIONS (Continued)

VACUUM-FLUORESCENT DISPLAY DRIVERS (Split Supply)





INCANDESCENT LAMP DRIVER APPLICATIONS

DRIVING MULTIPLEXED incandescent lamps at voltages up to 75 V with peak currents approaching 500 mA per segment, Series UDN-2980A eight-channel source drivers, when combined with Type ULN-2069B sink drivers, provide for a very cost-effective approach. Multiplexed lamps must typically be operated at a voltage $\sqrt{N}$ (N = the number of digits) times the nominal d-c voltage, to obtain sufficient brightness. For example, a four-digit, 28 V display requires 56 V to operate satisfactorily. In addition, care must be taken to select a proper driver to withstand the substantial inrush currents created by cold filaments. Peak currents of up to ten times the nominal operating currents have been observed. Multiplexed lamps must also incorporate diodes to prevent series/parallel paths to unaddressed elements.

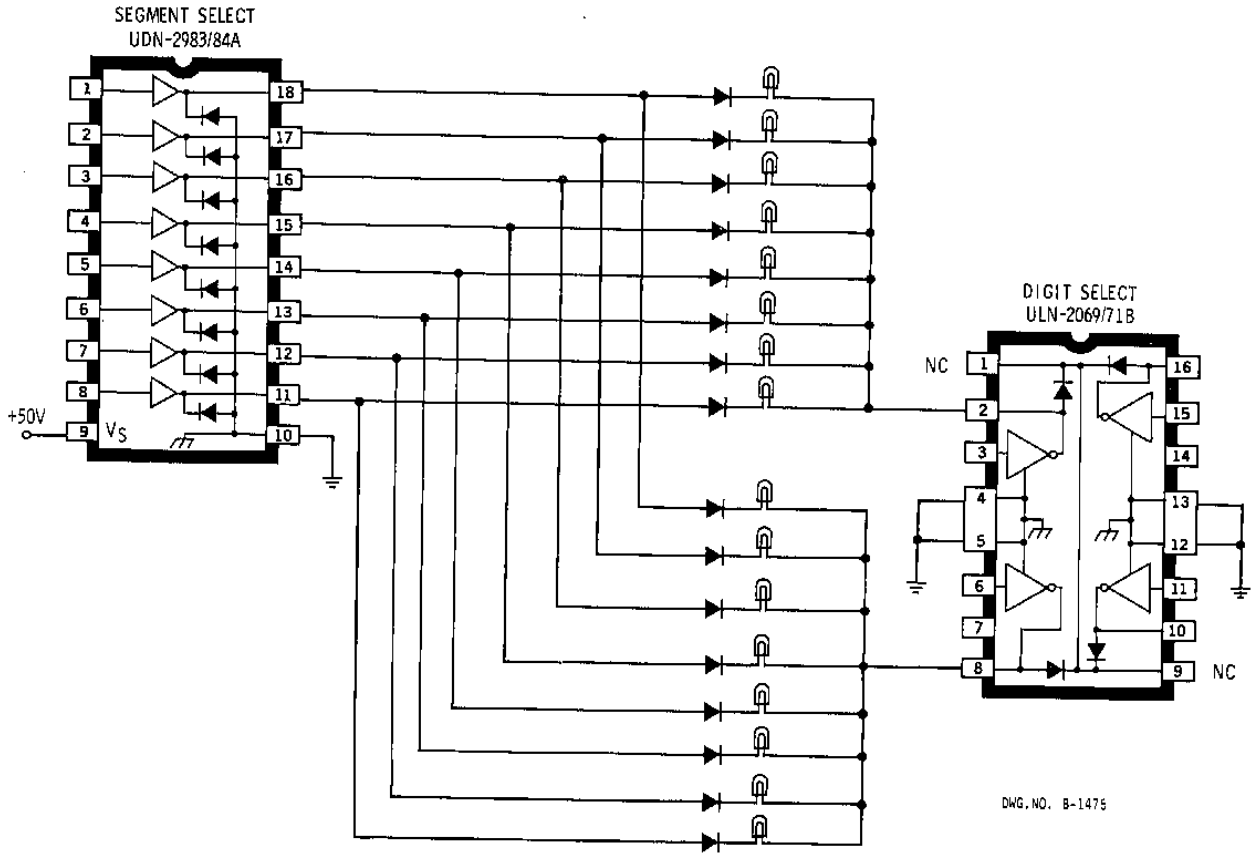
RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage Range, V_S
- UDN-2981A and UDN-2982A . . . . . 5 V to 45 V
- UDN-2983A and UDN-2984A . . . . . 35 V to 75 V

Continuous Output Current, I_{OUT} (per output) . . . . . −350 mA
Peak Output Current, I_{OP} . . . . . −500 mA

3

MULTIPLEXED LAMP DRIVER, TTL- OR MOS-COMPATIBLE



LIGHT-EMITTING DIODE APPLICATIONS

SERIES UDN-2580A and Series UDN-2980A 8-channel source drivers provide monolithic solutions to problems associated with driving multiplexed LED displays in common-cathode or common-anode configurations.

Type UDN-2585A is a non-Darlington inverting (input low = output high) source driver that is frequently used as a segment or dot driver in a common-cathode LED display where multiplexed segment or dot currents do not exceed 120 mA. This device features input logic-level compatibility with open-collector TTL, standard TTL, CMOS, and NMOS, as well as low output saturation voltages.

For common-cathode applications requiring higher segment currents, or for common-anode digit drive applications, Series UDN-2980A is recommended. This non-inverting (input high = output high) series features 350 mA per output continuous current ratings with peak currents reaching 500 mA per output. Outputs may be paralleled for higher current capability. Type UDN-2982A is logic-compatible with 2.4 V output levels of TTL and CMOS. Similar high output current ratings, for use in inverting applications, are offered by the Type UDN-2580A driver.

Combining Sprague source drivers with multi-channel, high-current sink drivers (such as Type ULN-2068B, UDN-2595A, or ULN-2814A) provides simple, compact, and economical solutions to driving high-current multiplexed LED displays.

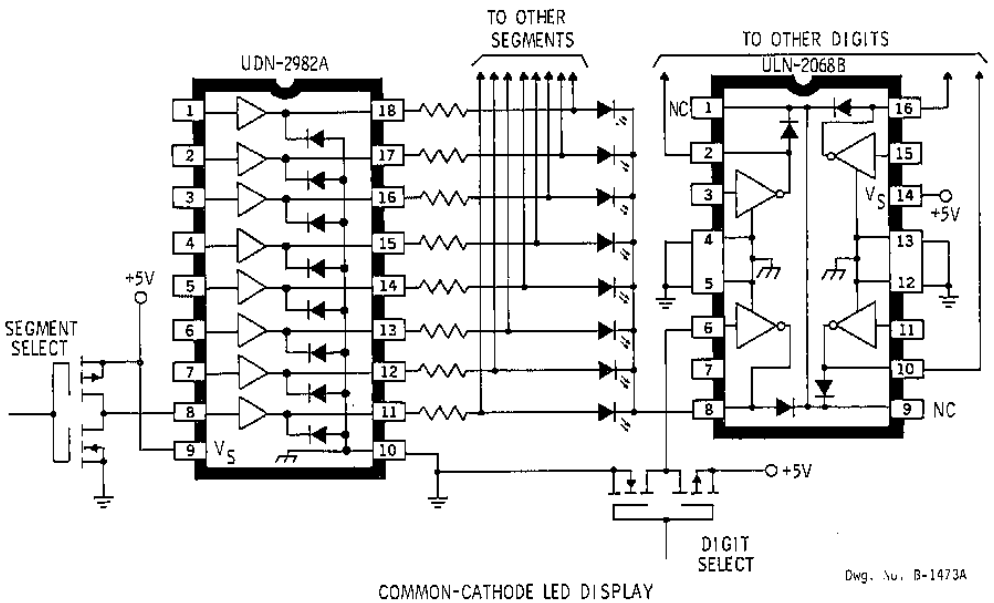
RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage, V_S
- UDN-2585A ..... 15 V
- UDN-2982A ..... 45 V

Continuous Output Current, I_{OUT} (per output)
- UDN-2585A ..... −120 mA
- UDN-2982A ..... −350 mA

Input Voltage, V_{IN} ..... 15 V

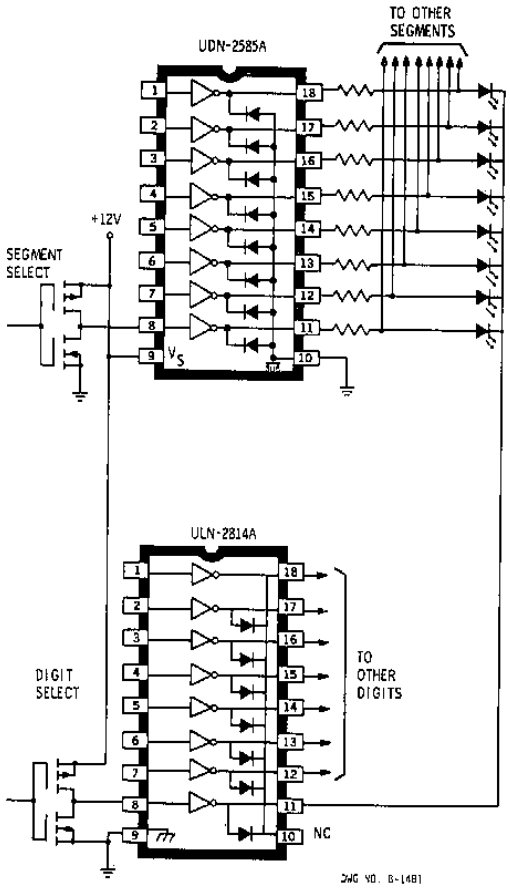
COMMON-CATHODE LED DISPLAY



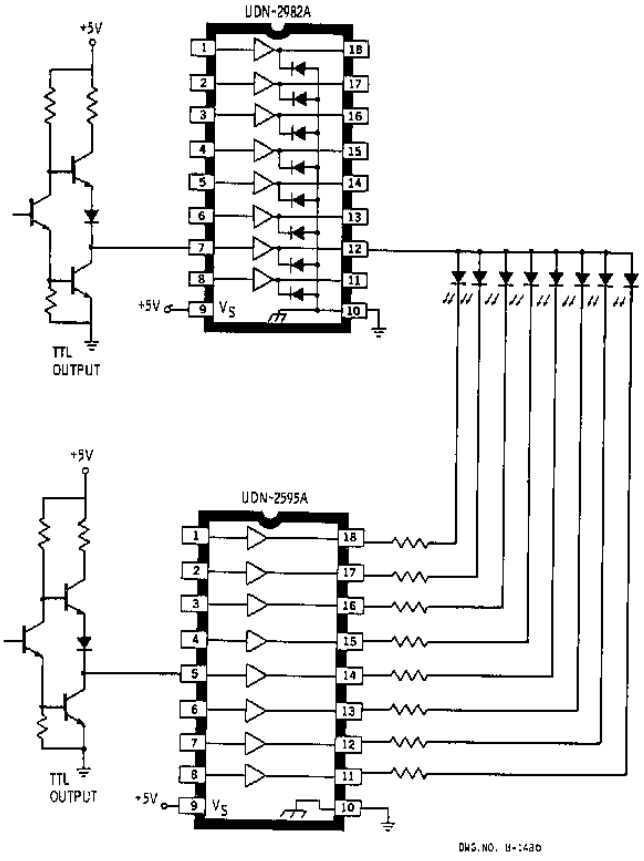
COMMON-CATHODE LED DISPLAY

LIGHT-EMITTING DIODE APPLICATIONS
(Continued)

COMMON-CATHODE LED DISPLAY



COMMON-ANODE LED DISPLAY

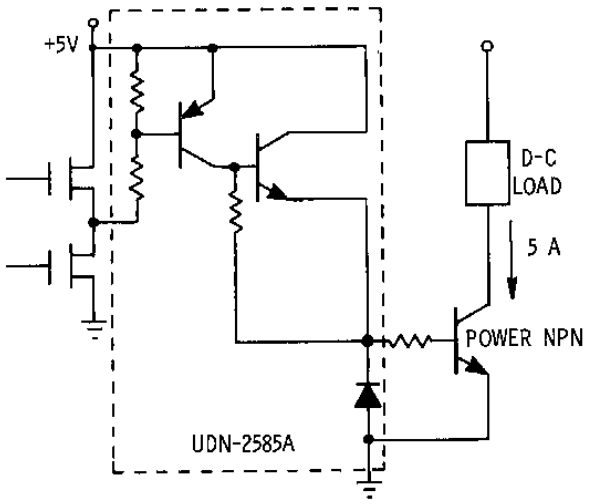


MULTI-CHANNEL INTERFACE TO HIGH-POWER LOADS

SPRAGUE SOURCE DRIVERS can be employed as multi-channel pre-drivers for discrete high-current or high-voltage semiconductors, thus reducing the need for many discrete components. For instance, a UDN-2580A 8-channel source driver can provide up to 350 mA of pre-drive current into the base of power NPN devices, making 5 A load currents readily available. Higher load currents can be obtained by using power NPN Darlington devices.

For a-c loads, it is possible to use any of the Sprague source drivers to provide gate current (with appropriate current-limiting) to a power SCR or triac. This scheme can provide an economical solution to many applications such as driving incandescent lamps or a-c motors at up to 20 A.

DRIVER FOR HIGH-POWER DISCRETE DEVICES



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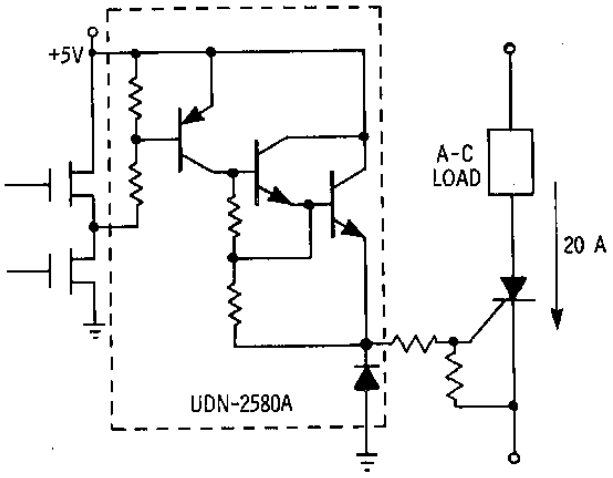

DWG.NO. A-11,534

RELIABILITY OF SERIES ULN-2000A AND ULN-2800A HIGH-CURRENT DARLINGTON DRIVERS

THIS REPORT SUMMARIZES accelerated-life tests that have been performed on Series ULN-2000A and ULN-2800A integrated circuits and provides information that can be used to calculate the failure rate at normal junction operating temperatures.

INTRODUCTION

Product-reliability improvement is a continuous and evolving process at Sprague Electric Company. Ongoing life tests, environmental tests, and stress tests are performed to establish failure rates and monitor established process-control procedures. Failures are analyzed to determine design changes or process improvements that can be implemented to improve device reliability.

The reliability of integrated circuits can be measured by qualification tests, accelerated tests, and burn-in:

1) Qualification testing is performed at an ambient temperature of +125°C for 1000 hours with an LTPD = 5 in accordance with MIL-STD-883B. This testing is normally conducted in response to a specific customer request or requirement. Qualification testing highlights design problems or gross processing problems, but does not provide sufficient data to generate accurate failure rates in a reasonable period of time.
2) Accelerated testing is performed at junction temperatures above +125°C and is used to generate failure-rate data.
3) Burn-in is intended to remove infant-mortality rejects and is conducted at +150°C for 96 hours or at +125°C for 168 hours. An analysis of test results from Sprague Electric's Double-Deuce™ burn-in program found 1.27% failures in more than 325,000 pieces tested in a recent time period. Most failures were due to slight parametric shifts. Catastrophic failures, which would cause user-equipment failure, were less than 0.1%.

ACCELERATED-LIFE TESTS

Sprague Electric performs accelerated-life tests on integrated circuits at junction temperatures of +150°C or +175°C at the recommended operating voltages. The internal power dissipation on some high-power circuits requires the ambient temperature to be lower than +150°C to keep the junction temperature between +150°C and +175°C.

In these tests, failures are produced so that the statistical life distribution may be established. The distribution cannot be established without failures. High-temperature accelerated-life testing is necessary to accumulate data in reasonable time periods. It has been established that the failure mechanisms at all temperatures in these tests are identical. Temperatures above +175°C are not generally used for the following reasons:

a) Industry-standard molding compounds degrade and release contaminants (halides) at approximately +200°C.
b) Life-test boards constructed with materials capable of withstanding exposure to temperatures greater than +175°C have been deemed to be cost prohibitive.
c) Increases in junction leakage currents may increase the power dissipation and device temperature to an indeterminant level.

Tables Ia and Ib contain data produced by life tests that were conducted at +150°C and +175°C. The data include the number of test samples, number of units in each sample, and the time periods during which failures occurred. The total time-on-test varies, with priority changes influencing alloca-

TABLE Ia
TEST RESULTS at T_J = +150°C

TEST NUMBER	QTY.	HOURS ON TEST 90	150	300	600	1200	1800	2400	3000	5000
		NUMBER OF FAILURES								
1	12	0	0	0	0	2	0	—	—	—
2	22	0	0	0	0	0	0	0	0	—
3	22	0	0	0	0	0	0	0	0	—
4	22	0	0	2	0	0	3	0	0	—
5	22	0	0	0	0	0	0	0	0	—
6	22	0	0	0	0	0	1	0	0	—
7	12	0	0	0	0	0	0	—	—	—
8	12	0	0	0	0	0	0	—	—	—
9	90	0	0	0	2	0	0	—	—	—
10	12	0	0	0	0	0	0	—	—	—
11	12	0	0	0	0	0	0	—	—	—
12	12	0	0	0	0	0	0	0	0	—
13	12	0	0	0	0	0	0	0	0	—
14	35	0	0	0	0	0	0	1	—	—
15	12	0	0	0	1	1	0	0	0	0
16	25	0	0	0	0	0	—	—	—	—
17	25	0	0	0	0	0	—	—	—	—
TOTAL ON TEST		381	381	381	379	376	323	173	138	10
TOTAL FAILURES		0	0	2	3	3	4	1	0	0
TOTAL GOOD		381	381	379	376	373	319	172	138	10
P_s		1.00	1.00	0.995	0.992	0.992	0.988	0.994	1.00	1.00
Cumulative P_s		1.00	1.00	0.995	0.987	0.979	0.967	0.961	0.961	0.961
$P_f = 1 - P_s$		0	0	0.005	0.013	0.021	0.033	0.039	0.039	0.039
Cumulative % Failures		0	0	0.5	1.3	2.1	3.3	3.9	3.9	3.9

tion of oven and board space, as new products are introduced. The time intervals between test readings were chosen for ease of plotting on log-normal paper.

The acceleration factor calculated using the Arrhenius equation, and a 1 eV activation energy, is approximately 5× for each 25°C temperature rise in junction temperature and is multiplicative.[1] This allows the data to be compared to qualification life-test data by equating 40 hours at +175°C or 200 hours at +150°C to 1000 hours of qualification life test at +125°C.

The data at the bottom of Tables Ia and Ib were compiled by calculating the probability of success (P_s), the cumulative probability of success, the probabilityof failure (P_f) and the percentage of failed units in each time period.

The cumulative percent of failures is plotted on log-normal plotting paper in Figure 1. This paper has a logarithmic time-scale axis and a probability-scale axis. A log-normal distribution plots as a straight line. A line of best fit is drawn through the plotted points and extended to determine the median lifetime at the 50% failure point. The mediam life at a junction temperature of +150°C is 1.6×10^5 hours. At +175°C, the median lifetime is 3.0×10^4 hours.

The log-normal distribution is commonly used because most semiconductor device data fit such a distribution.[2] When the median life has been found at the elevated temperature, it can be converted to the lower temperature of the actual application. The Arrhenius equation, which relates the reaction rate to temperature, is used to make this conversion.[1] The Arrhenius equation is:

$$V_r = V_r^{\circ} e^{-\epsilon/kT}$$

where V_r° = a constant
ϵ = activation energy
k = Boltzmann's constant
T = absolute temperature in degrees Kelvin

An activation energy of 1.0 electron-volt was established by testing Series ULN-2000A, Series UDN-5710M, and Series UDN-2980A devices at

TABLE Ib
TEST RESULTS at T_j = +175°C

TEST NUMBER	QTY.	HOURS ON TEST: 90	150	300	600	1200	1800	2400	3000	5000
		NUMBER OF FAILURES								
1	25	0	0	0	7	—	—	—	—	—
2	25	0	0	0	0	0	0	0	—	—
3	25	0	0	1	2	1	0	0	—	—
4	24	0	1	0	1	0	0	0	0	—
5	19	0	0	0	0	0	0	—	—	—
6	19	0	0	0	0	0	0	—	—	—
7	12	0	0	2	3	2	—	—	—	—
8	12	0	0	0	0	0	—	—	—	—
9	12	0	0	0	0	0	0	—	—	—
10	18	0	0	0	0	0	—	—	—	—
11	12	0	0	0	0	0	2	0	0	2
12	12	0	0	0	0	0	0	—	—	—
13	12	1	0	0	0	0	0	0	—	—
14	18	0	0	1	2	0	7	—	—	—
15	12	1	0	0	0	0	0	—	—	—
16	12	0	0	0	0	0	—	—	—	—
17	24	0	0	0	0	0	0	—	—	—
18	12	0	1	0	1	0	0	0	0	—
19	24	0	0	0	0	0	—	—	—	—
TOTAL ON TEST		329	327	325	321	287	213	99	42	10
TOTAL FAILURES		2	2	4	16	3	9	0	0	2
TOTAL GOOD		327	325	321	305	284	204	99	42	8
P_s		0.994	0.994	0.988	0.950	0.990	0.958	1.00	1.00	0.800
Cumulative P_s		0.994	0.988	0.976	0.927	0.917	0.879	0.879	0.879	0.703
$P_f = 1 - P_s$		0.006	0.012	0.024	0.073	0.083	0.121	0.121	0.121	0.300
Cumulative % Failures		0.6	1.2	2.4	7.3	8.3	12.1	12.1	12.1	30.0

multiple temperatures. Failure analysis of devices rejected during this testing of Series ULN-2000A and ULN-2800A also supports this activation energy, as failures were mainly due to increased leakages, reduced beta, and surface inversion.[3]

The median life-point is drawn on Arrhenius graph paper in Figure 2. Arrhenius plotting paper gives a graphical solution, rather than a mathematical solution, to the problem of equivalent median lifetime at any junction temperature. A line drawn through +150°C and +175°C failure points has a slope corresponding to that of the 1.0 eV failure mechanism.

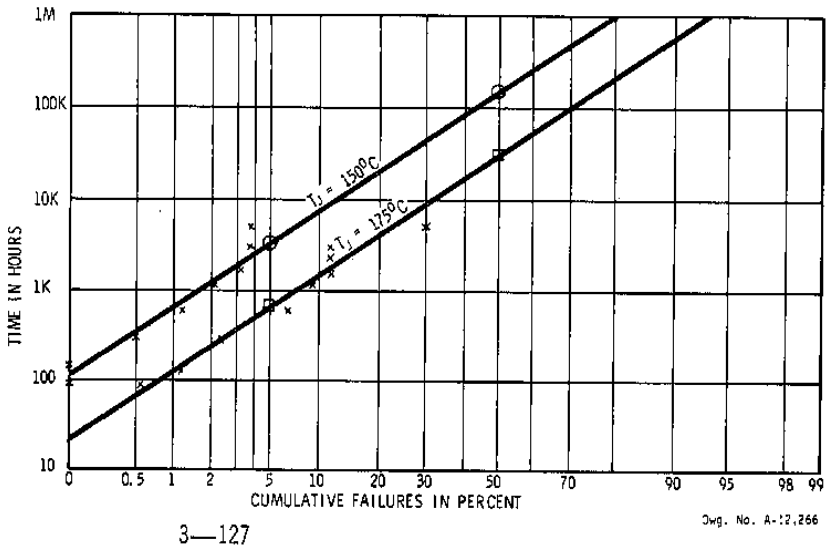

Figure 1
CUMULATIVE PERCENT OF FAILURES

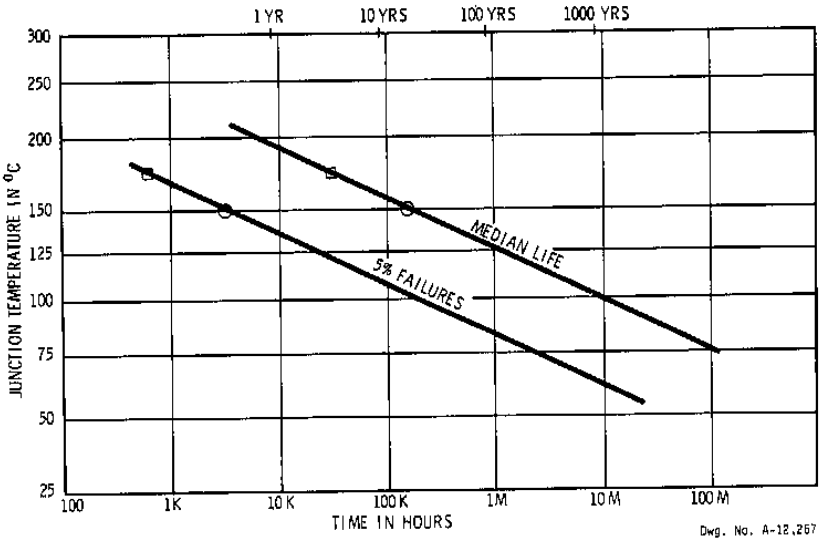

Figure 2
MEDIAN LIFE

Although not as statistically accurate as the median lifetime, the 5% failure point can be read from Figure 1. It is plotted in Figure 2.

The median life with lower junction temperatures can now be determined by using Figure 2. It must be emphasized that this is junction temperature and not ambient temperature. The temperature rise at the junction due to internal power dissipation must be taken into account using the formula:

$$T_J = P_D\theta_{JA} + T_A \text{ or } T_J = P_D\theta_{JC} + T_C$$

The median lifetime, or 50% failure point, as determined in Figure 2, is approximately 100 years at +125°C or 1,000 years at +100°C junction temperature.

The approximate failure rate (FR) can be determined from FR = 1/Median Life, where Median Life is taken from Figure 2 at the intersection of the junction-temperature line and median-life plot. The actual instantaneous failure rate may be calculated using a Goldwaite plot.[4] However, this approximation is very close. At +100°C the failure rate would be:

$$FR = 1/(8.8 \times 10^6 \text{ hours})$$
$$= 0.0011\%/1000 \text{ hours} = 11 \text{ FIT}$$

where *FIT* = failures per 10^9 unit-hours

TABLE II
SERIES ULN-2000A AND ULN-2800A FAILURE RATE

T_J (°C)	Median Life (h)	Failure Rate (%/100 h)	Failures In Time (No./10^9 unit-hours)
125	1.0×10^6	0.10	1000
100	8.8×10^6	0.011	110
75	1.0×10^8	0.0010	10
50	8.8×10^8	0.00011	1.1

CONCLUSION

The relationship between temperature and failure rate is well documented and is an important factor in all designs. Load currents, duty cycle, and ambient temperature must be considered by the design engineer to establish a junction-temperature limit that provides failure rates within design objectives.

Figure 2 shows that a design with a junction temperature of +100°C, calcualted from internal power dissipation and external ambient temperature, would not reach the 5% failure point in 10 years. Lowering the junction temperature to +70°C increases the time to the 5% failure point to 300 years.

A complete sequence of environmental tests on Series ULN-2000A and ULN-2800A, including temperature cycle, pressure cooker, and biased humidity tests are continuously monitored to ensure that assembly and package technology remain within established limits.

These environmental tests and accelerated-life tests establish a base line for comparisons of new processes and materials.

REFERENCES

1) Manchester, K. E., and Bird, D. W., "Thermal Resistance: A Reliability Consideration," *IEEE Transactions*, Vol. CHMT-3, No. 4, 1980, pp. 580-587 (Sprague Technical Paper TP 80-2).

2) Peck, D. S., and Trapp, O. D., *Accelerated Testing Handbook*, Technology Associates, 1978, pp. 2-1 through 2-6.

3) *ibid.*, p. 6-7.

4) Goldwaite, L. R., "Failure Rate Study for the Log-Normal Lifetime Model," *Proceedings of the 7th Symposium on Reliability and Quality Control*, 1961, pp. 208-213.

NOTES