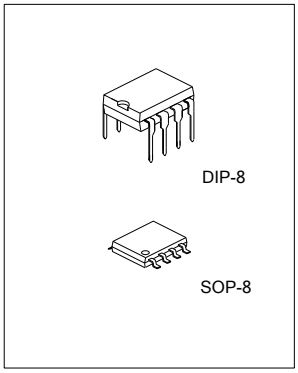
LOW NOISE J-FET DUAL OPERATIONAL AMPLIFIERS

LR072

DESCRIPTION

The LR072 is a high speed J-FET input dual operational amplifiers incorporating well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

The device features high slew rates, low input bias and offset currents , and low offset voltage temperature coefficient.



FEATURES

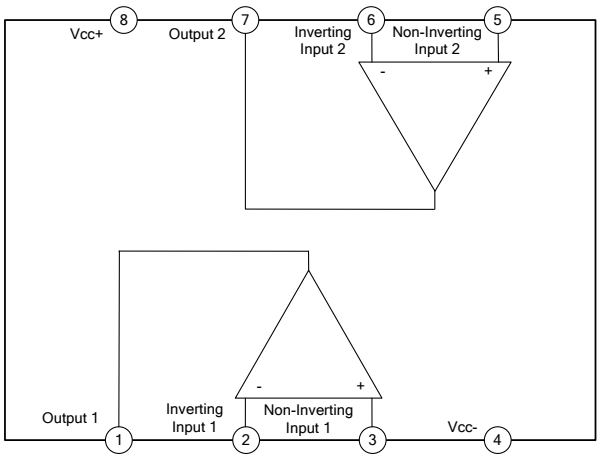
* Wide common-mode and differential voltage range
* Low input bias and offset current
* Low noise e_n=15nv/√Hz(typ)
* Output short-circuit protection
* High input impedance J-FET input stage
* Low harmonic distortion:0.01%(typ)
* Internal frequency compensation

ORDERING INFORMATION

Device	Package
LR072D	DIP-8-300-2.54
LR072E	SOP-8-225-1.27

* Latch up free operation
* High slew rate:16V/μs(typ)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage-note1	Vcc	±18	V
Input Voltage-note2	Vi	±15	V
Differential Input Voltage –note3	Vi(diff)	±30	V
Power Dissipation	Pd	680	mW
Output Short-Circuit Duration- note4		Infinite	
Operating Free-air Temperature	Topr	0 to +70	°C
Storage Temperature Range	Tstg	-65 to 150	°C

1. All voltage values,except differential voltage ,are with respect to zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between Vcc+ and Vcc-.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts,whichever is less .
3. Differential voltages are the non-inverting input terminal with respect to the inverting input interminal.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS

(Vcc=±15V,Ta=+25°C,unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Input Offset Voltage(Rs=50Ω)	V_{IO}	Ta=+25°C Tmin≤Ta≤Tmax		3	10 13	mV
Input Offset Voltage drift	DV_{IO}			10		μF/°C
Input Offset Current (Note 1）	I_{IO}	Ta=+25°C Tmin≤Ta≤Tmax		5	100 10	pA nA
Input Bias Current (Note 1)	I_{BIAS}	Ta=+25°C Tmin≤Ta≤Tmax		20	200 20	pA nA
Large Signal Voltage Gain (R_L=2KΩ,V_0=±10V)	GV	Ta=+25°C Tmin≤Ta≤Tmax	25 15	200		V/mV
Supply Voltage Rejection Ratio (Rs=50Ω)	SVR	Ta=+25°C Tmin≤Ta≤Tmax	70 70	86		dB
Supply Current,no load, per amplifier	Icc	Ta=+25°C Tmin<Ta<Tmax		1.4	2.5 2.5	mV
Input Common-mode Voltage Range	$VI_{(R)}$		±11	+15 -12		V
Common-mode rejection Ratio	CMRR	Ta=+25°C Tmin≤Ta≤Tmax	70 70	86		dB

(continued)

Output Shout-Circuit Current	Ios	Ta=+25°C Tmin≤Ta≤Tmax	10 10	40	60 60	mA
Output Voltage Swing	±Vopp	Ta=+25°C R_L=2KΩ R_L=10KΩ Tmin≤Ta≤Tmax R_L=2KΩ R_L=10KΩ	10 12 10 12	12 13.5		V
Slew Rate	SR	Ta=+25°C Vin=10V,R_L=2KΩ, C_L=100pF, unity again	8	16		V/μs
Rise Time	T_R	Ta=+25°C Vin=20mV,R_L=2KΩ, C_L=100pF, unity again		0.1		μs
Overshoot Factor	K_{OV}	Ta=+25°C Vin=20mV,R_L=2KΩ, C_L=100pF, unity again		10		%
Gain Bandwidth Product	GBP	Ta=+25°C Vin=10mV,R_L=2KΩ, C_L=100pF, f=100kHZ	2.5	4		MHZ
Input Resistance	Ri			10^{12}		Ω
Total Harmonic Distortion	THD	Ta=+25°C f=1kHZ ,R_L=2KΩ, C_L=100pF, Av=20dB,Vo=2Vpp		0.01		%
Equivalent Input Noise Voltage	E_N	Rs=100Ω,f=1KHz		15		$\frac{nv}{\sqrt{Hz}}$
Phase Margin	Φ_M			45		degree
Channel Separation	V_{o1}/V_{o2}	Av=100		120		dB

PARAMETER MEASUREMENT INFORMATION

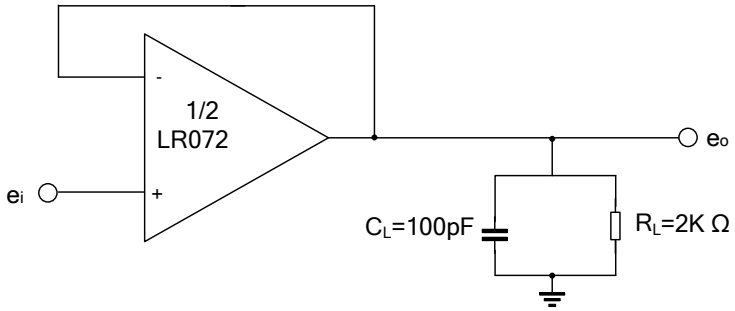


Figure 1: Voltage follower

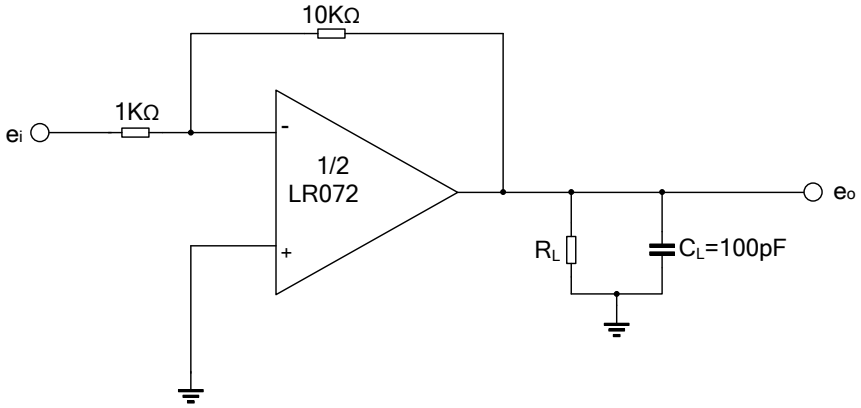
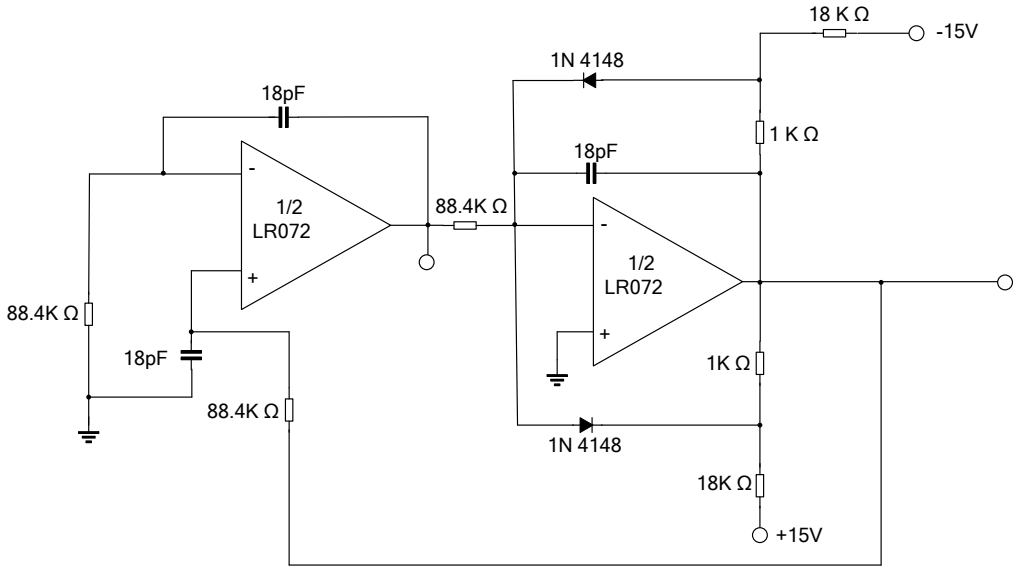


Figure 2: Gain-of-10 inverting amplifier

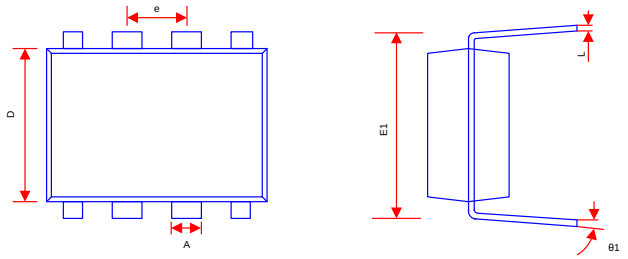
TYPICAL APPLICATIONS

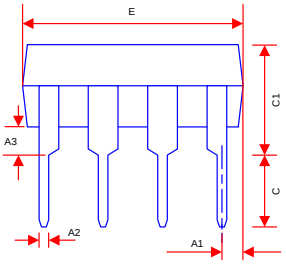
100KHZ QUADRUPLE OSCILLATOR



PACKAGE DIMENSIONS

DIP-8-300-2.54 UNIT: mm





Symbol	Min	Nom	Max
A	1.52	-	1.82
A1	0.59	0.89	1.24
A2	0.38	0.46	0.54
A3	0.5	-	-
D	6.10	6.35	6.6
E	9.10	9.40	9.80
E1	7.62	-	8.25
e	2.54BSC		
C	3.0	-	-
C1	-	-	4.36
θ1	-	15°	-
L	0.2	0.25	0.3

SOP-8-225-1.27 UNIT: mm

