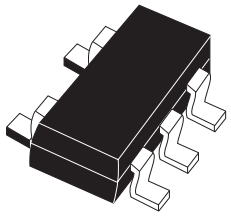
STM1831

Voltage detector with sense input and external delay capacitor

Features

- Voltage monitored on separate sense input V_{SEN}
- Factory-trimmed voltage thresholds in 100 mV increments from 1.6 V to 5.7 V
- ±2% voltage threshold accuracy
- Operating voltage 1.6 V to 6.0 V
- Open drain output
- Low supply current of 0.8 µA (typ.)
- Time delay programmable by external capacitor
- Power supply transient immunity
- Available in SOT23-5 package
- Operating temperature –40 to 85 °C



SOT23-5

Applications

- Microprocessor reset circuitry
- Charge voltage monitors
- Memory battery backup switch circuits
- Power failure detection circuits

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1 Description

The STM1831 is a voltage detector with very low current consumption. It monitors a voltage on a separate input pin (V_{SEN}), which is fully functional even if the monitored voltage goes down to 0 V. In addition, the delay of the output can be adjusted by an external capacitor.

Figure 1. Logic diagram

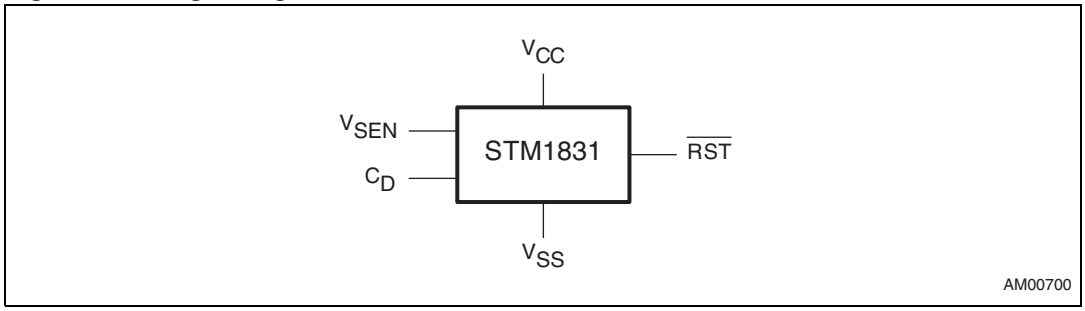
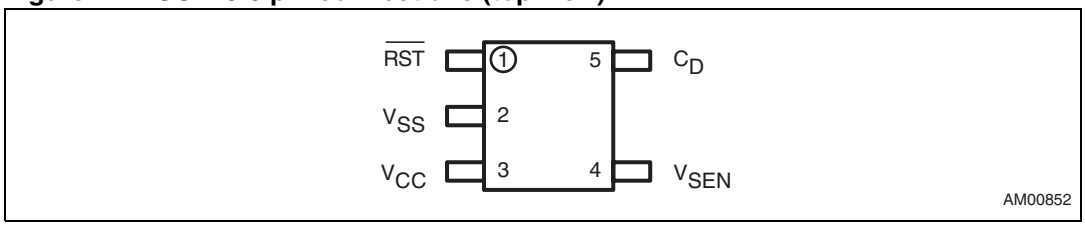


Table 1. Pin descriptions

Pin	Type	Name	Function
1	Output open drain	$\overline{RST}$	Active-low reset output
2	Power	V_{SS}	Ground
3	Power	V_{CC}	Supply voltage
4	Input	V_{SEN}	Sense voltage
5	I/O	C_D	Delay capacitor

Figure 2. SOT23-5 pin connections (top view)



1.1 Pin descriptions

See *Figure 1* and *Table 1* for a brief overview of the signals available on this device.

Power supply (V_{CC})

This pin is used to provide power to the device. A 0.1 µF decoupling ceramic capacitor is recommended to be connected between the V_{CC} and V_{SS} pins, as close to the STM1831 device as possible.

Sense voltage input (V_{SEN})

Input voltage on this pin is monitored. When it drops below the threshold (V_{DET}), reset output ($\overline{RST}$) is asserted. If V_{CC} is close to 0 V, internal logic disconnects the voltage divider from V_{SEN} input in order to minimize I_{SEN} current (see *Figure 3* and *Figure 20*).

Reset output ($\overline{RST}$)

Reset output is asserted when the voltage on the V_{SEN} input pin drops below the threshold (V_{DET}).

The STM1831 has an open drain, active-low output which sinks current when the output is asserted. Connect a pull-up resistor from $\overline{RST}$ to any supply voltage up to 6 V (see *Figure 4*). Select a resistor value large enough to register a logic low, and small enough to register a logic high, while all of the input current and leakage paths connected to the reset output line are being supplied. A 10 kΩ pull-up is sufficient in most applications.

The advantages of open drain output include the ability to connect more open drain outputs in parallel (wired OR connections) as well as connecting the output to a power supply voltage other than V_{CC}.

Delay capacitor (C_D)

Capacitor C_D determines the delay (t_{CD}) between reset deassertion and the moment when V_{SEN} voltage exceeds the V_{DET} threshold (see *Figure 5* with calculations for more details).

Any external leakage due to poor quality timing capacitors or excessive humidity may cause a significant leakage current which extends the t_{CD} timing. To minimize this effect, the PCB tracks between the C_D pin and its respective timing capacitor should be as short as possible, properly covered with solder mask and isolated from other tracks (especially V_{SS}) by as great a distance as possible. Low-leakage timing capacitors (ceramic or film capacitor) should be used.

Leave C_D pin open if unused (i.e. t_{CD} = 0 ms).

Figure 3. Block diagram

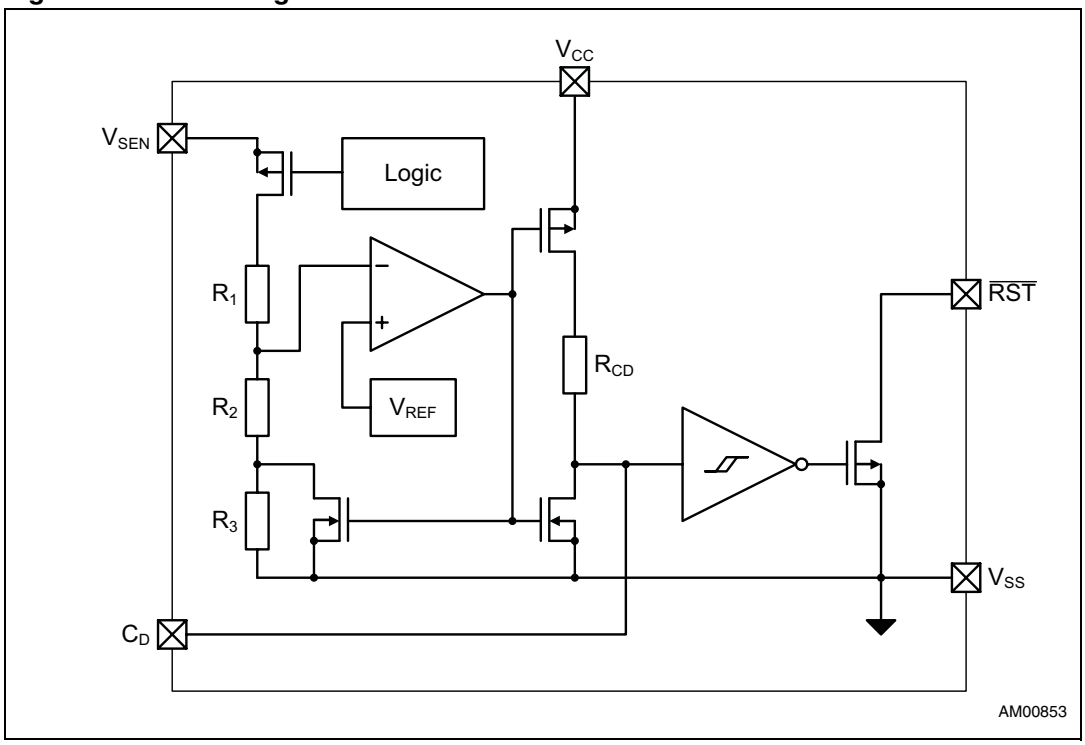
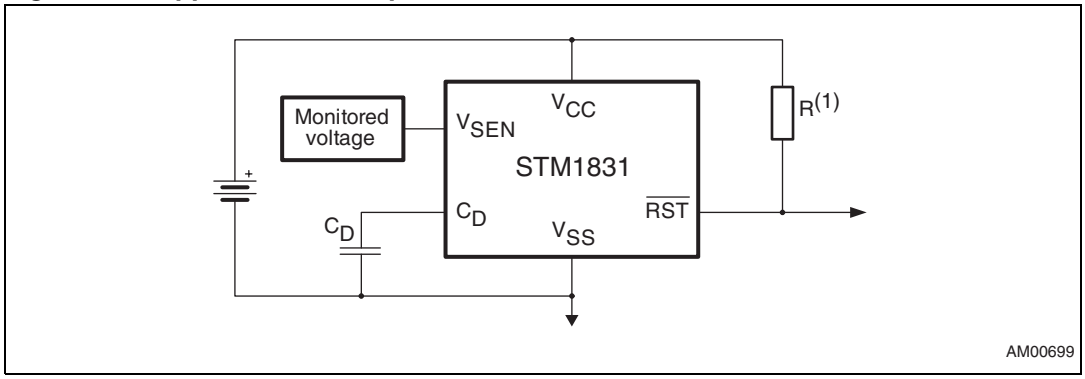


Figure 4. Application hookup



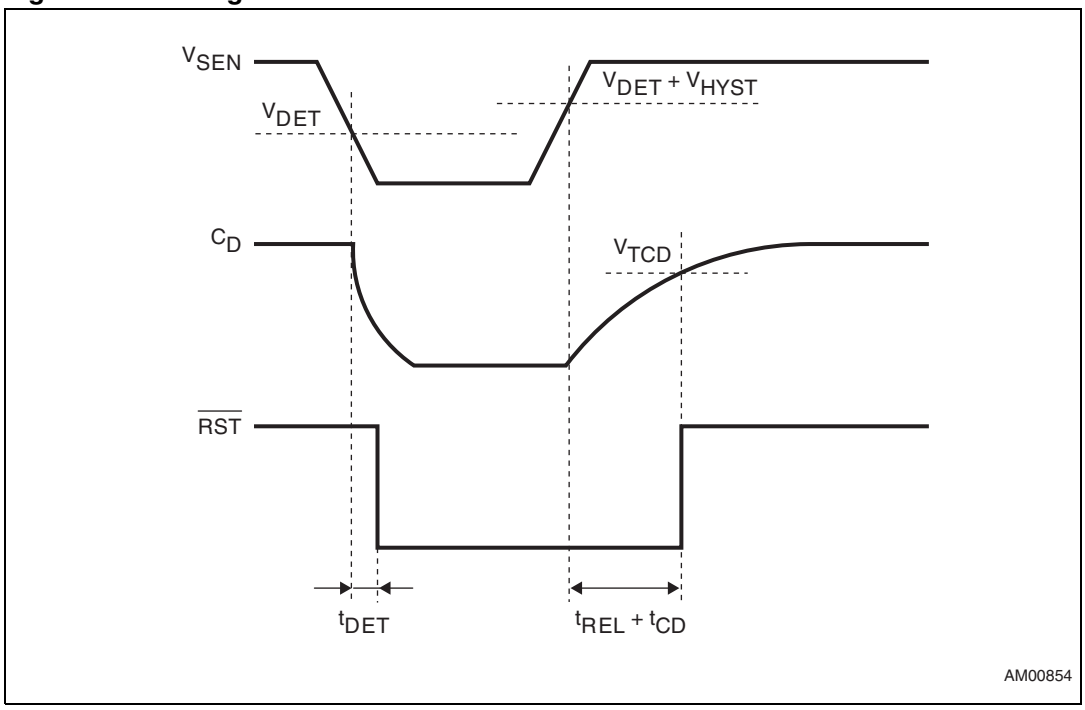
1. External pull-up resistor is needed for open drain $\overline{RST}$ output. A 10 kΩ is sufficient in most applications.

2 Operation

The STM1831 voltage detector monitors system voltages from 1.6 V to 5.7 V in 100 mV increments, has a voltage hysteresis (V_{HYS}) and an output delay programmable by external capacitor C_D.

The STM1831 asserts a reset output ($\overline{RST}$) whenever V_{CC} goes below the detect voltage (V_{DET}). The reset output stays asserted until V_{CC} goes above the detect voltage with hysteresis (V_{DET} + V_{HYS}). If the external capacitor is connected to the C_D pin, the reset output deassertion is adequately delayed (see *Figure 5* with calculations below for more details). Leave the C_D pin open if unused (i.e. t_{CD} = 0 ms).

Figure 5. Timing waveforms



t_{DET} detect delay time

t_{REL} release delay time (measured when external capacitor C_D is disconnected)

t_{CD} delay by external capacitor C_D.

The t_{CD} delay can be calculated based on *Equation 1*:

Equation 1

$$t_{CD} = -R_{CD} \times C_D \times \ln\left(1 - \frac{V_{TCD}}{V_{CC}}\right)$$

and considering R_{CD} = 2 MΩ (typ.) and V_{TCD} = 1.5 V (typ.) at V_{CC} = 3.0 V:

Equation 2

$$t_{CD} \cong 1.39 \times 10^6 \times C_D(s, F)$$

3 Typical operating characteristics

Figure 6. Supply current vs. sense voltage, V_{CC} = 3.0 V, V_{DET} = 2.0 V

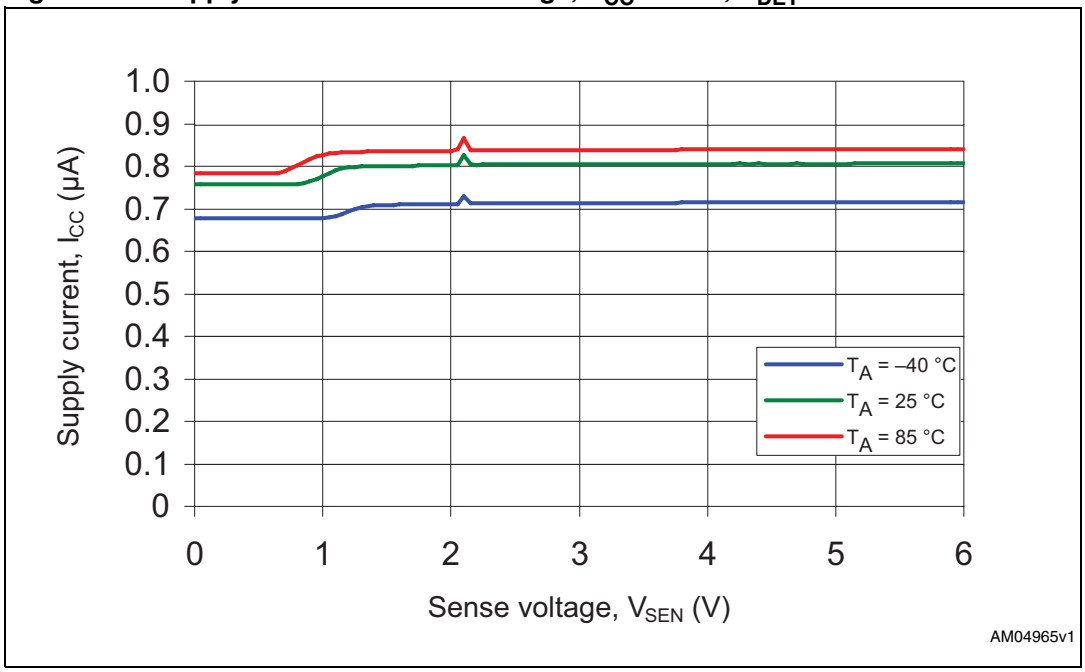


Figure 7. Supply current vs. input voltage, V_{SEN} = 1.9 V ($\overline{RST}$ asserted)

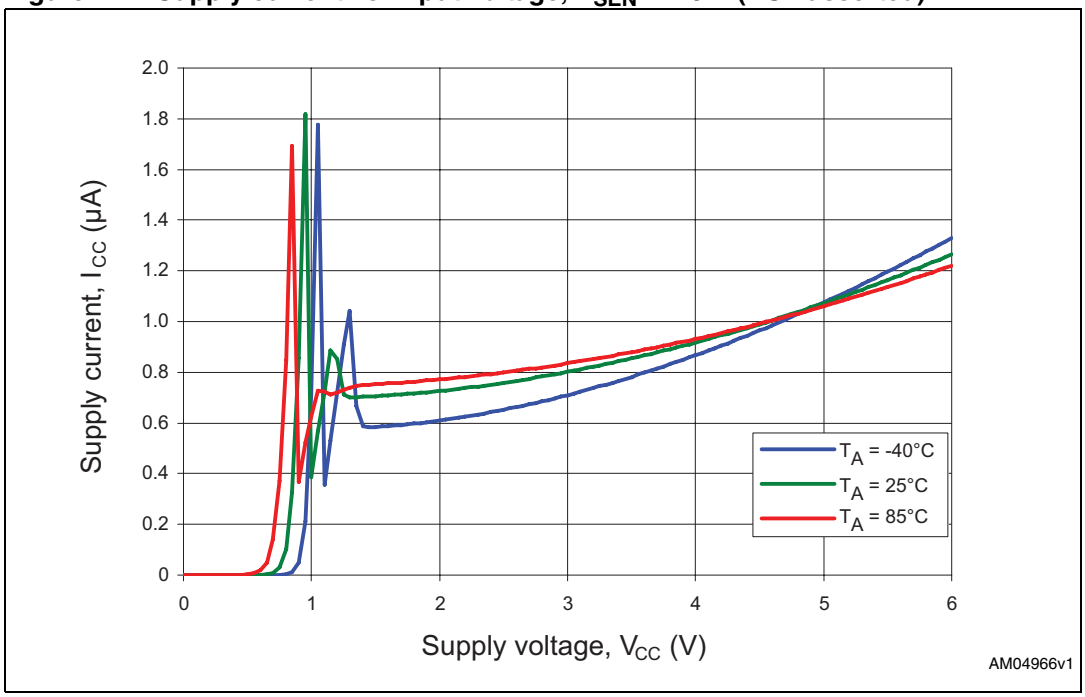


Figure 8. Detect voltage vs. ambient temperature, V_{DET} = 2.4 V

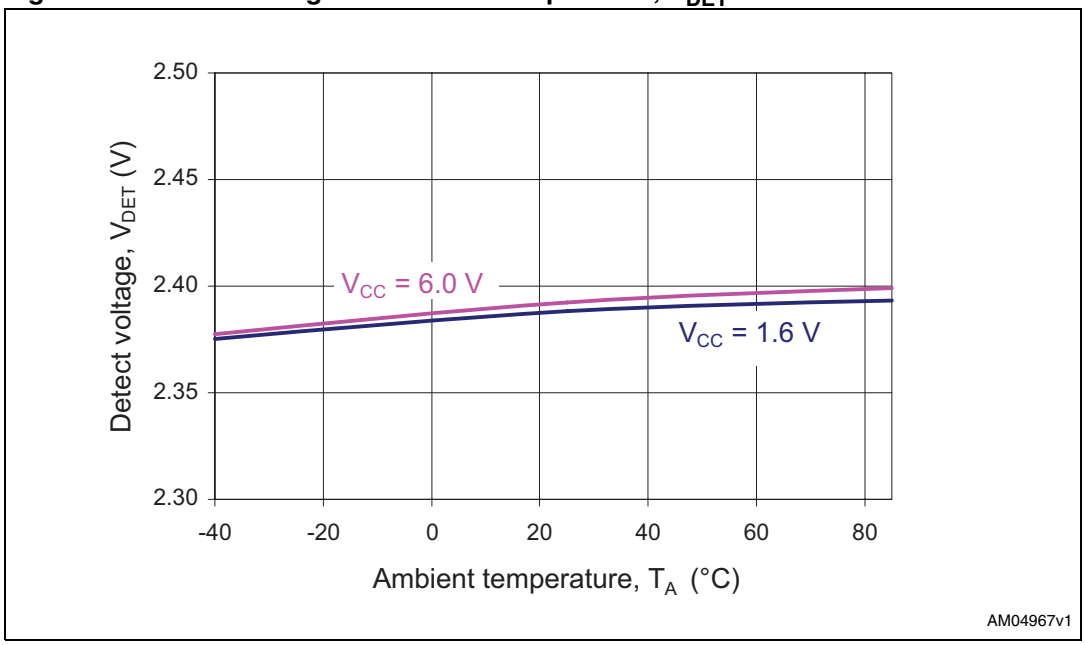


Figure 9. Detect voltage vs. supply voltage, V_{DET} = 2.4 V

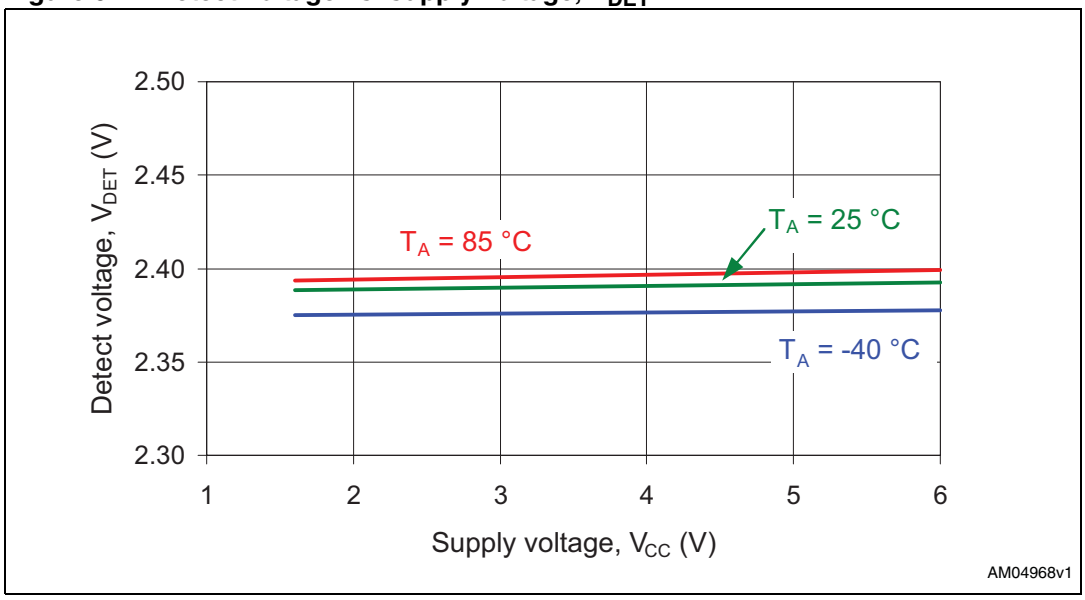


Figure 10. Hysteresis voltage vs. ambient temperature, V_{DET} = 2.4 V

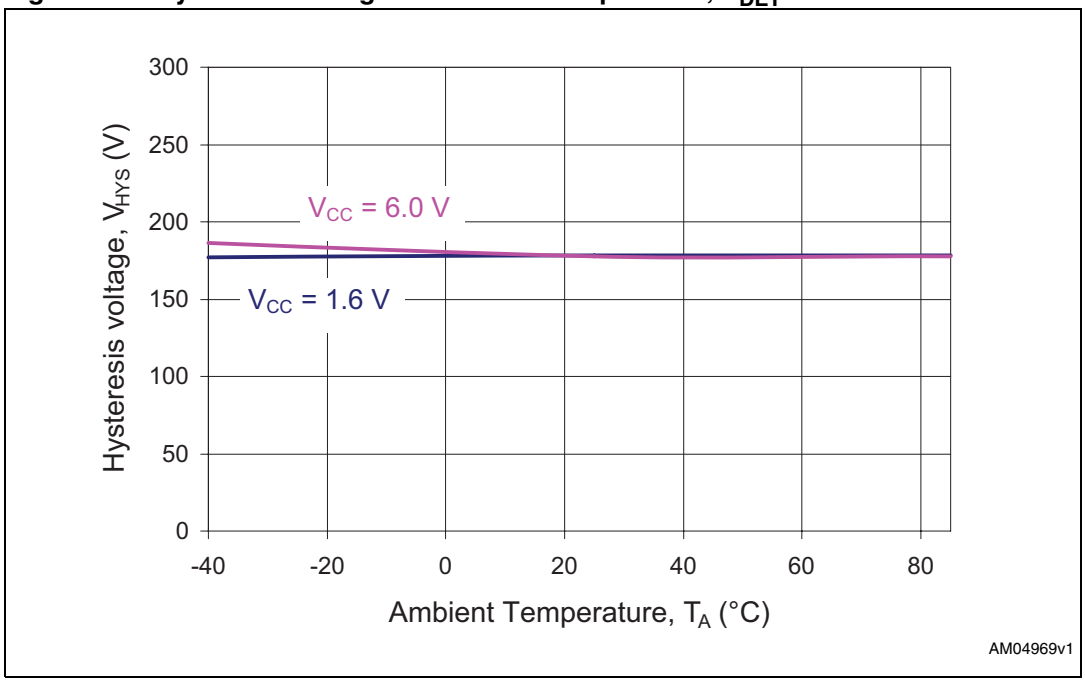


Figure 11. C_D pin sink current vs. supply voltage, V_{SEN} = 0 V, V_{CD} = 0.5 V

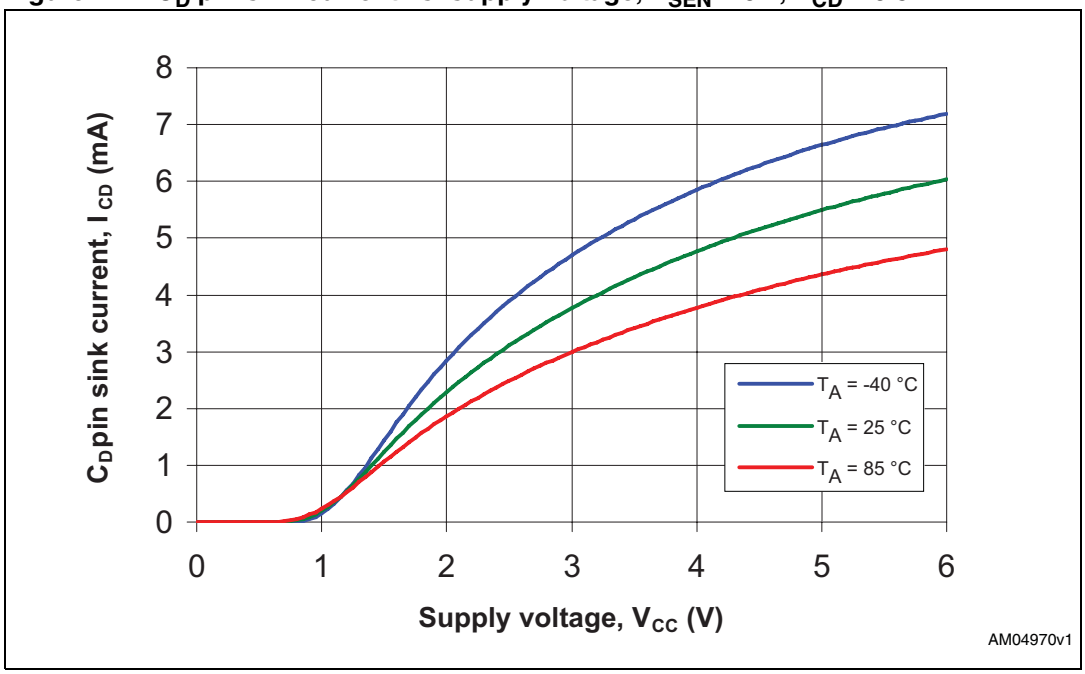


Figure 12. Output voltage vs. sense voltage, V_{DET} = 2.4 V, T_A = 25 °C, external pull-up resistor on $\overline{RST}$ is 100 kΩ, C_D pin open

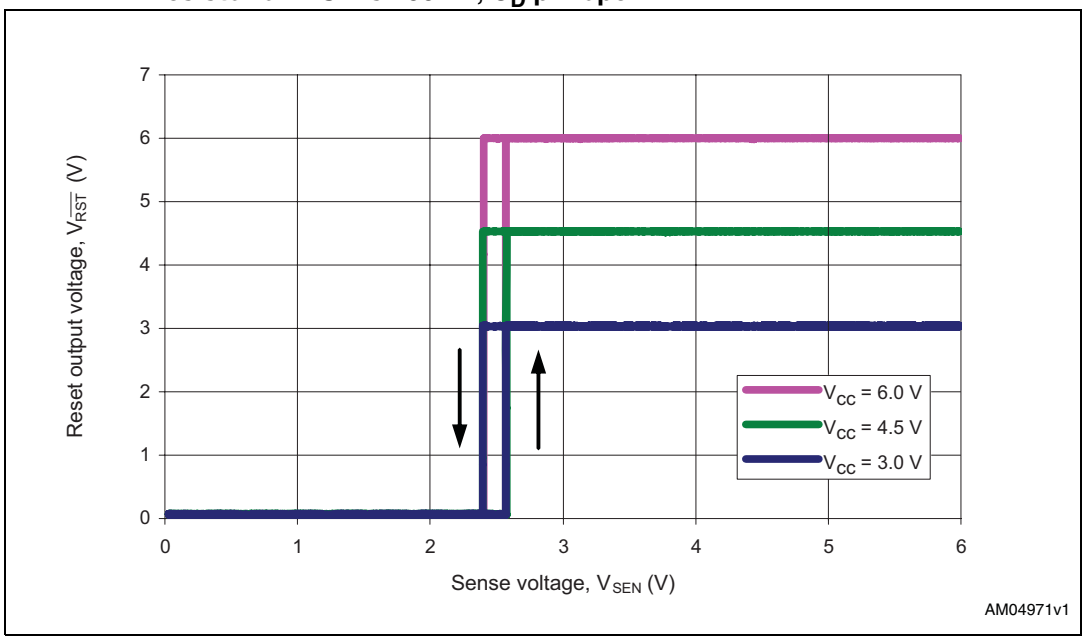


Figure 13. Output voltage vs. supply voltage, V_{SEN} = V_{CC}, external pull-up resistor on $\overline{RST}$ is 100 kΩ, C_D pin open

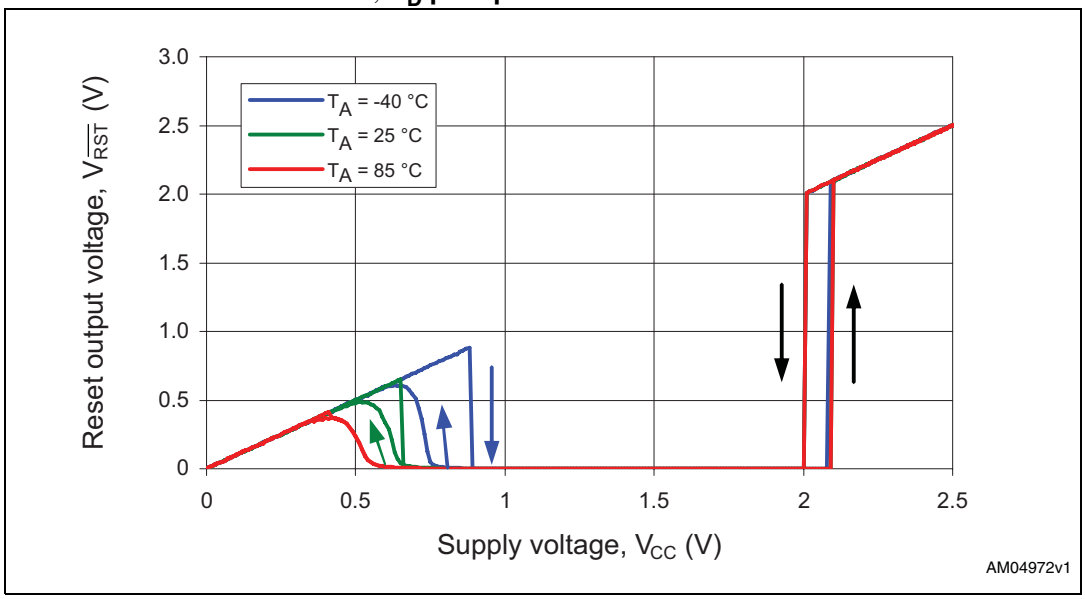


Figure 14. Output current vs. supply voltage, V_{SEN} = 0 V, $V_{\overline{RST}}$ = 0.5 V

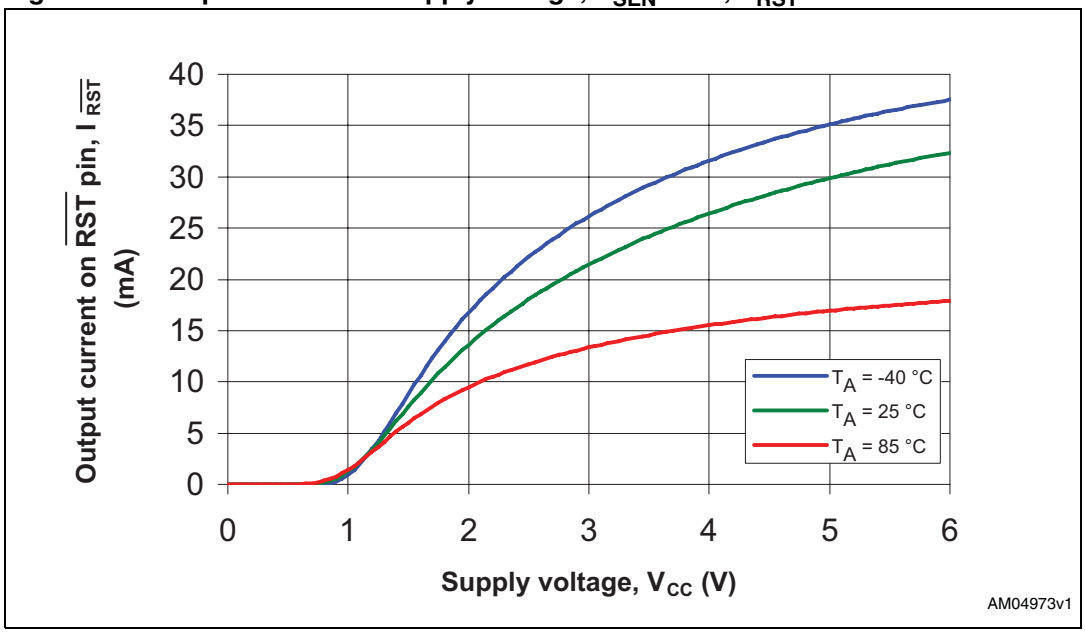


Figure 15. Relative delay resistance vs. ambient temperature, V_{CC} = 5 V, V_{SEN} = 6 V, V_{CD} = 0 V

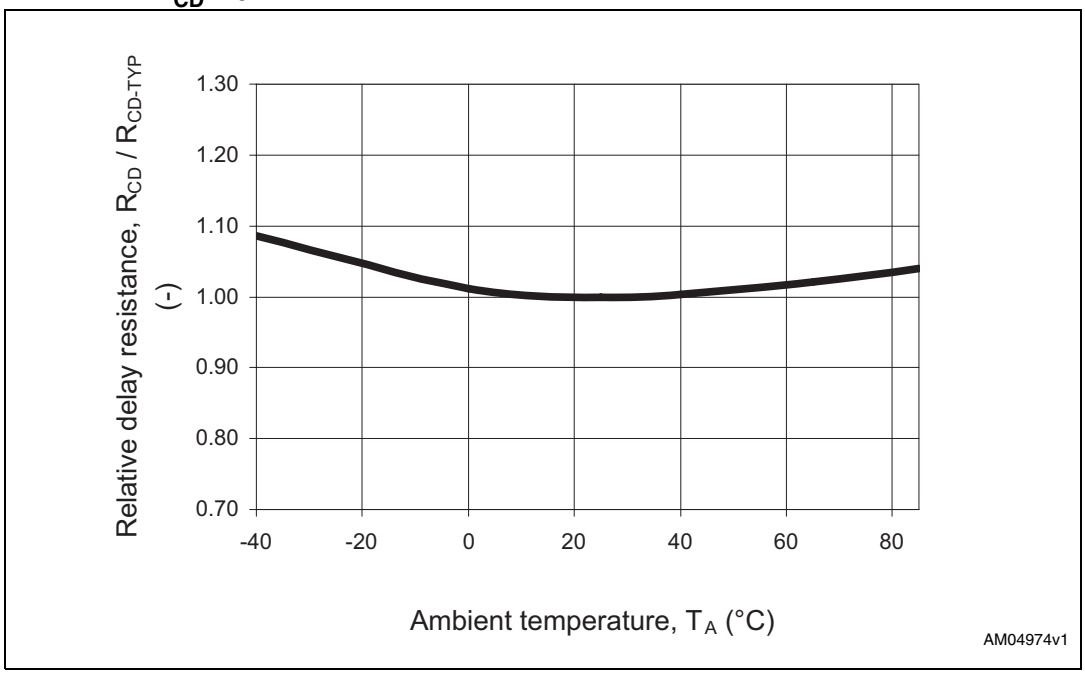


Figure 16. Release delay time vs. delay capacitance, T_A = 25 °C

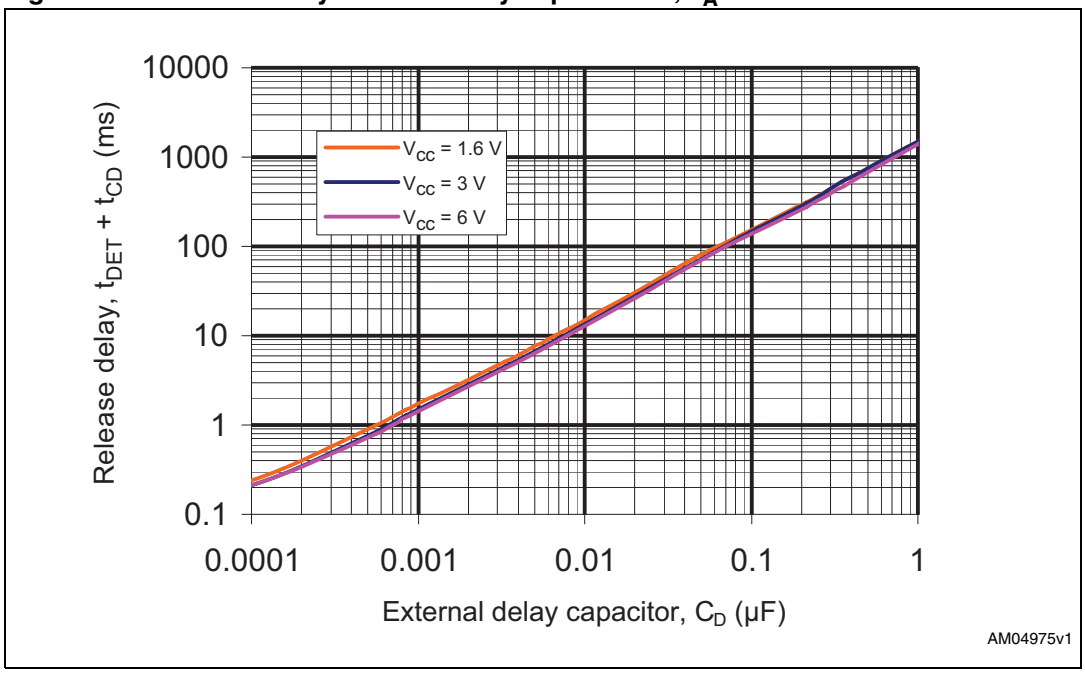


Figure 17. Detect delay time vs. delay capacitance, T_A = 25 °C

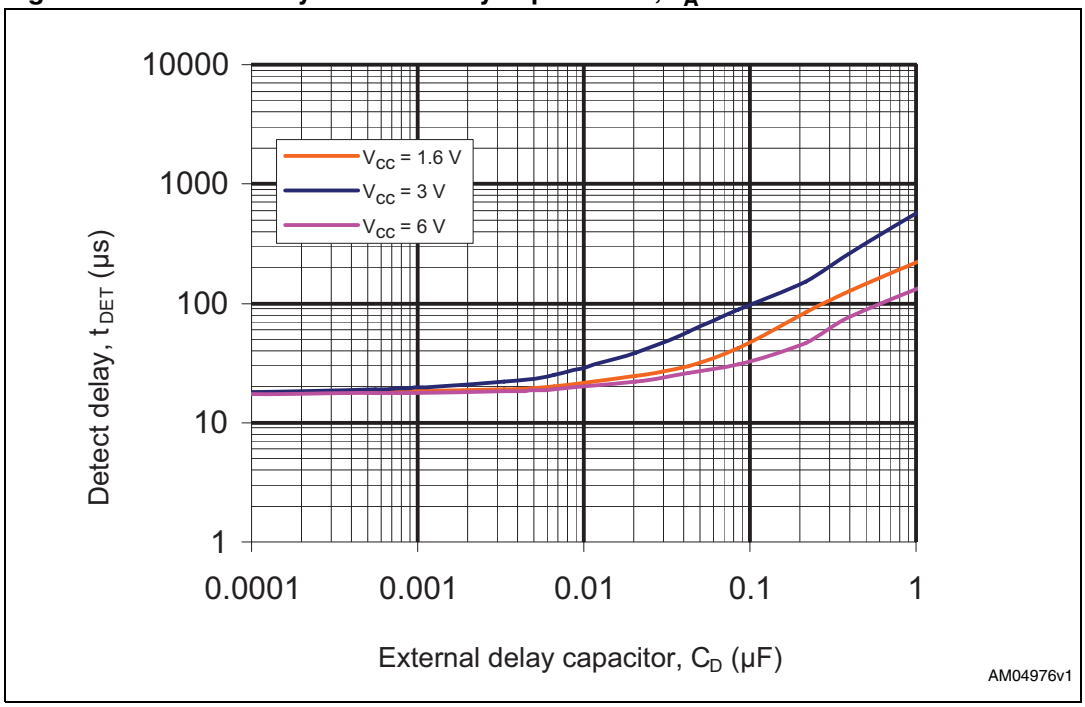


Figure 18. $\overline{RST}$ output leakage current vs. ambient temperature, $V_{CC} = V_{SEN} = V_{OUT} = 6.0$ V, C_D pin open

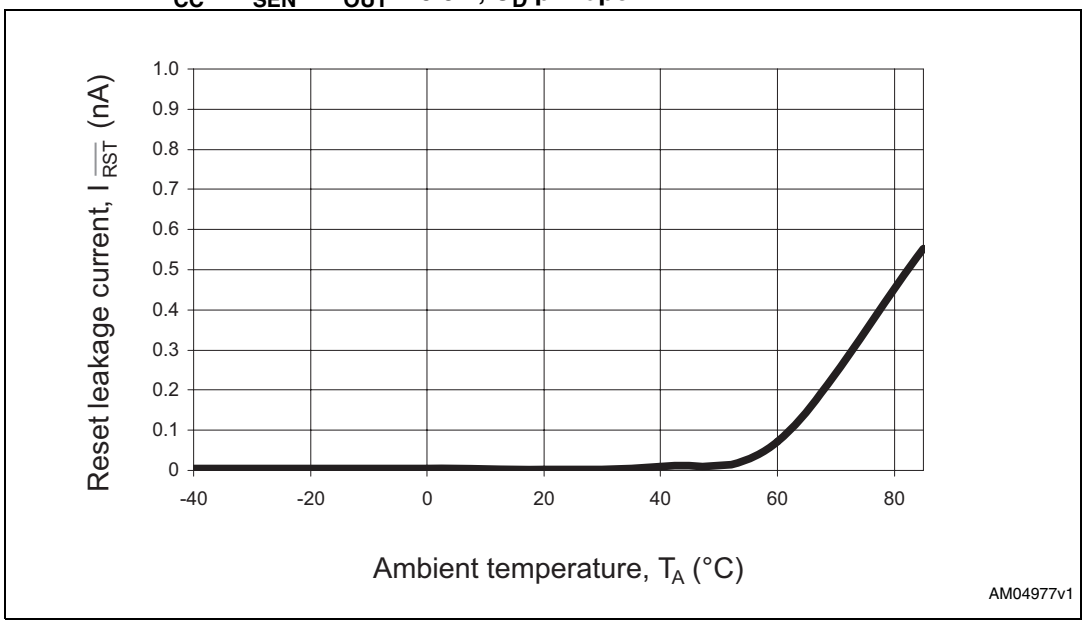


Figure 19. $\overline{RST}$ output leakage current vs. output voltage, $V_{CC} = V_{SEN} = 6.0$ V, $T_A = 85$ °C, C_D pin open

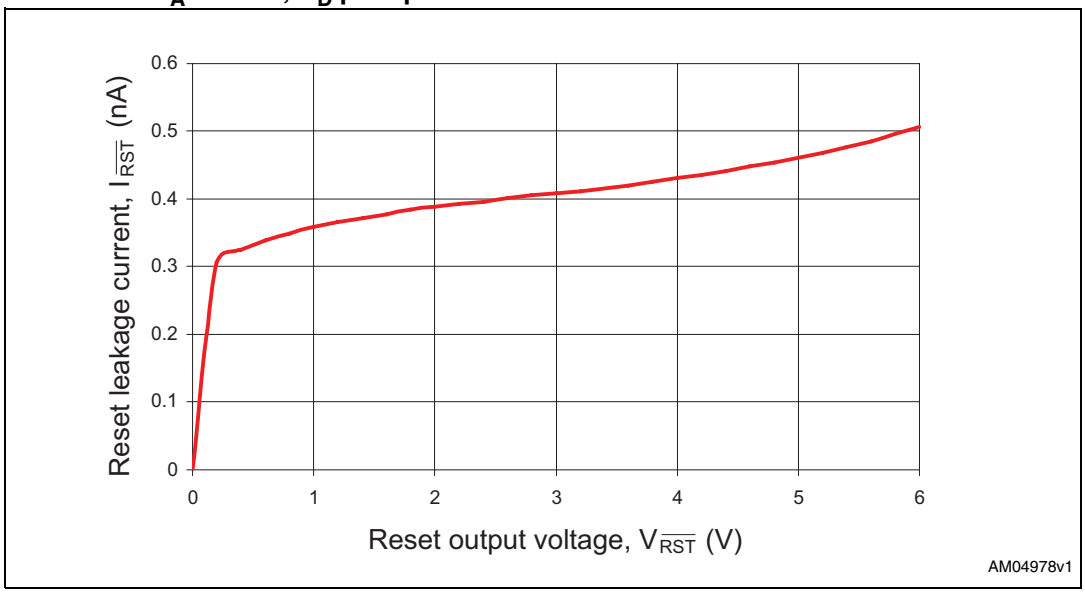


Figure 20. Sense current vs. supply voltage, V_{SEN} = 1.9 V

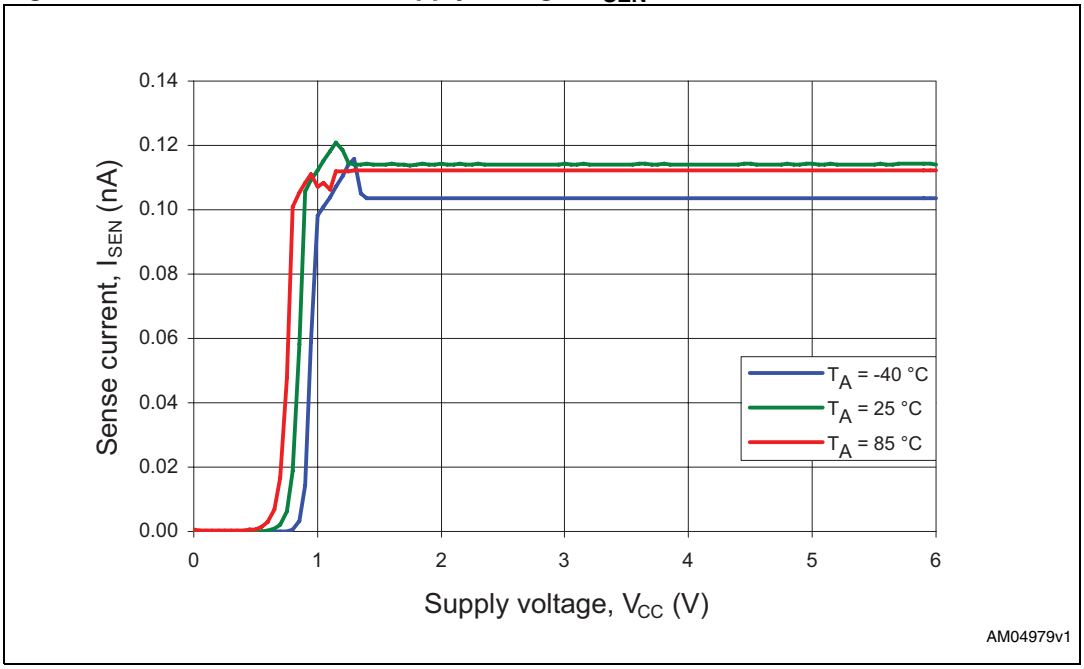
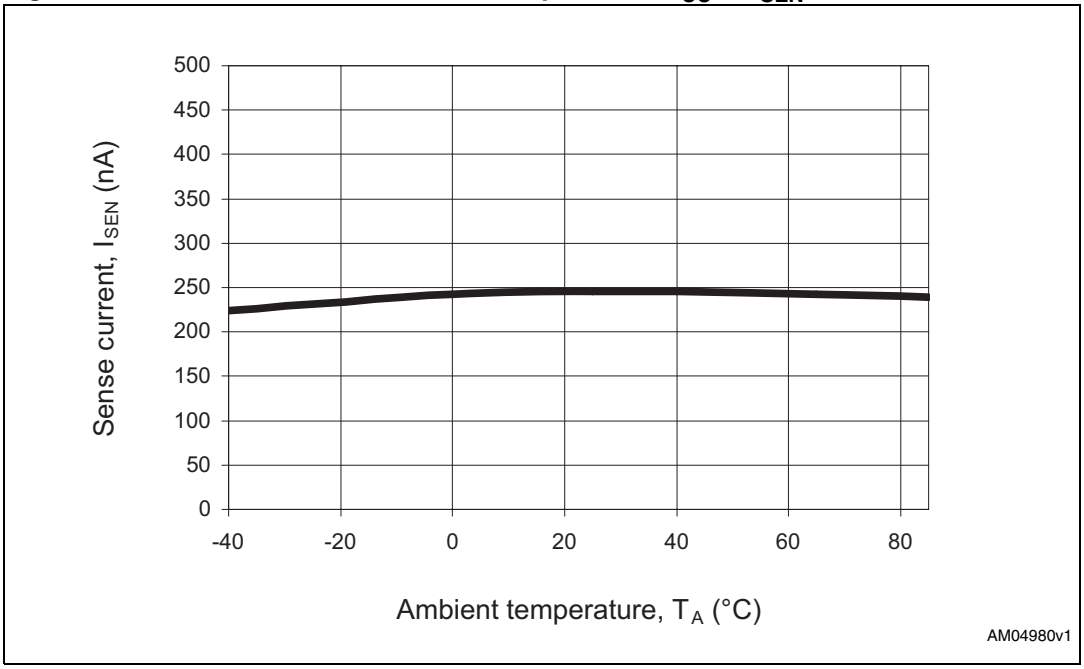


Figure 21. Sense current vs. ambient temperature, V_{CC} = V_{SEN} = 5 V



4 Maximum ratings

Stressing the device above the ratings listed in *Table 2* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{CC} off)	–55 to 150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds	260	°C
T_J	Maximum junction temperature	125	°C
V_{CC}	Supply voltage	–0.3 to 7.0	V
V_{CD}	Delay capacitor pin voltage	–0.3 to V_{CC} + 0.3	V
V_{RST}	Reset output voltage – N-channel open drain	 –0.3 to 7.0	V
V_{ESD}	ESD voltage – Human body model (MIL-STD-883, Method 3015) – Machine model	 2000 200	V

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

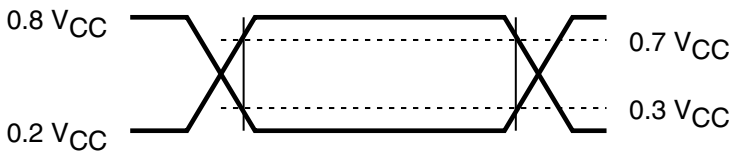
5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in *Table 4* that follow, are derived from tests performed under the measurement conditions summarized in *Table 3* and *Figure 5* with measurement conditions for t_{DET} and t_{REL}. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 3. Operating and AC measurement conditions

Parameter	Value	Unit
Supply voltage (V_{CC})	1.6 to 6.0	V
Ambient operating temperature (T_A)	–40 to 85	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8 V_{CC}	V
Input and output timing ref. voltages	0.3 to 0.7 V_{CC}	V

Figure 22. AC testing input/output waveforms



AI02568

Table 4. DC and AC characteristics

Symbol	Parameter	Conditions[1]		Min.	Typ.	Max.	Units
V_{CC}	Operating voltage	–40 °C < T_A < 85 °C		1.6	—	6.0	V
V_{DET}	Detect voltage[2]			V_{DET} –2%	V_{DET}	V_{DET} + 2%	V
V_{HYS}	Hysteresis voltage			0.02 V_{DET}	0.05 V_{DET}	0.08 V_{DET}	V
I_{CC}	Supply current		V_{CC} = 1.6 V	—	0.70	1.20	µA
			V_{CC} = 3.0 V	—	0.80	1.40	
			V_{CC} = 6.0 V	—	1.20	2.00	
$I_{\overline{RST}}$	Output current	V_{SEN} = 0 V, $V_{\overline{RST}}$ = 0.5 V	V_{CC} = 1.6 V	0.8	7.0	—	mA
			V_{CC} = 2.0 V	5.0	14.0	—	
			V_{CC} = 3.0 V	10.0	22.0	—	
			V_{CC} = 4.0 V	15.0	28.0	—	
			V_{CC} = 5.0 V	17.0	32.0	—	
			V_{CC} = 6.0 V	20.0	35.0	—	
I_{LEAK}	Output leakage current	V_{CC} = 6.0 V, V_{SEN} = 6.0 V, $V_{\overline{RST}}$ = 6.0 V, C_D: open		—	—	400	nA
ΔV_{DET} / (ΔT_A • V_{DET})	Temperature variation	–40 °C < T_A < 85 °C		—	±100	—	ppm/ °C
I_{SEN}	Sense current	V_{CC} = 0 V		—	10	—	nA
		V_{CC} > 1.6 V, V_{SEN} = 5.0 V		—	300	500	
R_{CD}	Delay resistance	V_{SEN} = 6.0 V, V_{CC} = 5.0 V, V_{CD} = 0 V		1.4	2.0	2.6	MΩ
I_{CD}	Delay capacitance pin sink current	V_{CD} = 0.5 V, V_{CC} = 1.6 V		0.2	1.4	—	mA
V_{TCD}	Delay capacitance pin threshold voltage	V_{SEN} = 6.0 V, V_{CC} = 1.6 V		0.70	0.85	1.00	V
		V_{SEN} = 6.0 V, V_{CC} = 3.0 V		1.25	1.50	1.70	
		V_{SEN} = 6.0 V, V_{CC} = 6.0 V		2.45	2.65	2.85	
t_{DET}	Detect delay time	V_{CC} = 6.0 V, V_{SEN} = 6.0 V→ 0 V, C_D: open		—	40	75	µs
t_{REL}	Release delay time	V_{CC} = 6.0 V, V_{SEN} = 0 V→ 6 V, C_D: open		—	55	170	µs

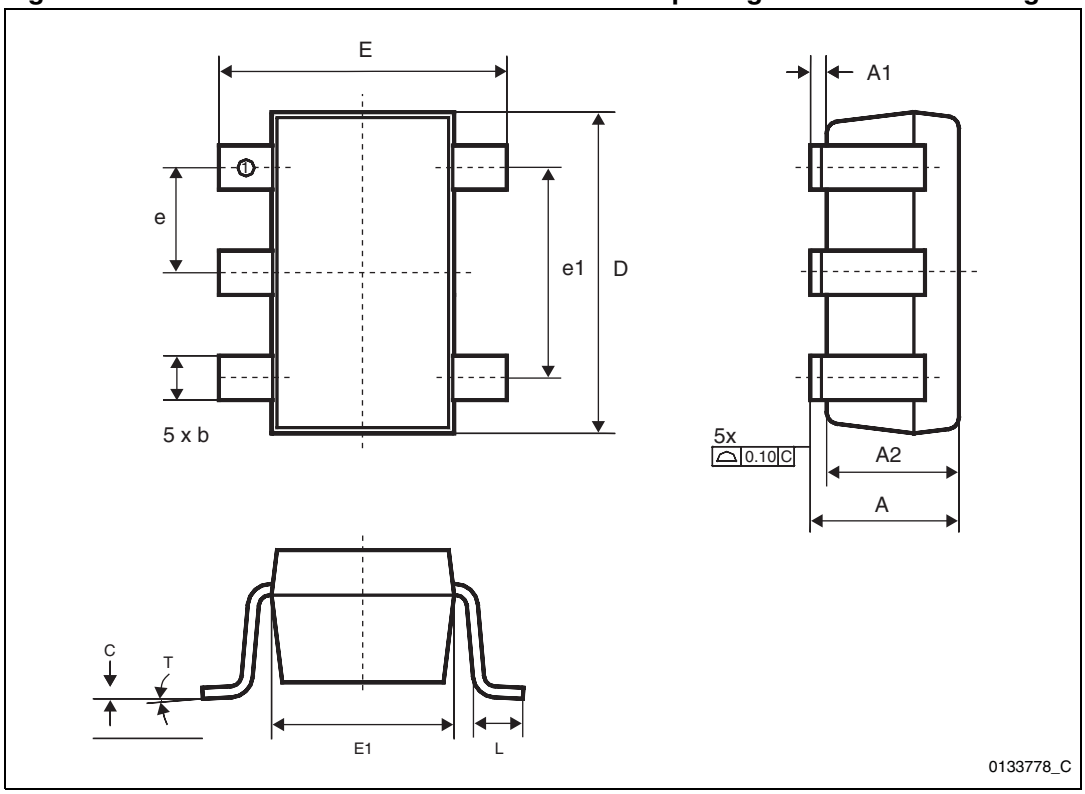
1. Valid for ambient operating temperature: T_A = 25 °C; V_{CC} = 1.6 V to 6.0 V (except where noted).
2. Factory-trimmed voltage thresholds in 100 mV increments from 1.6 V to 5.7 V.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 23. SOT23-5 - 5-lead small outline transistor package mechanical drawing



Note: Drawing is not to scale.

Table 5. SOT23-5 - 5-lead small outline transistor package mechanical data

Symbol	Millimeters			Inches			Note
	Typ.	Min.	Max.	Typ.	Min.	Max.	
A			1.45			0.057	
A1		0.00	0.15		0.00	0.006	
A2	1.15	0.90	1.30	0.045	0.035	0.051	
b		0.30	0.50		0.012	0.020	
c		0.08	0.22		0.003	0.009	
D	2.90			0.114			
E	2.80			0.110			
E1	1.60			0.063			
e	0.95			0.037			
e1	1.90			0.075			
L	0.45	0.30	0.60	0.018	0.012	0.024	
θ	4	0	8	4	0	8	Degrees
N	5			5			

7 Part numbering

Table 6. STM1831 ordering information scheme

Example: STM1831 L 24 WY 6 F

Device type

STM1831

Reset output polarity

L: active-low

Detector threshold(1)

24: 2.4 V typ.

(100 mV steps from 1.6 V to 5.7 V available)

Package

WY: SOT23-5

Temperature range

6: –40 °C to +85 °C

Shipping method

F: Lead-free ECOPACK® package, tape and reel

1. Other detector thresholds are offered. Minimum order quantities may apply. Contact local ST sales office for availability.

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
16-Nov-2010	1	Initial release.

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