SiT9003
Low Power Spread Spectrum Oscillator

The Smart Timing Choice™

Features

- Frequency range from 1 MHz to 110 MHz
- LVCMOS/LVTTL compatible output
- Standby current as low as 0.4 µA
- Fast resume time of 3 ms (Typ)
- <30 ps cycle-to-cycle jitter
- Spread options (contact SiTime for other spread options)
  - Center spread: ±0.50%, ±0.25%
  - Down spread: -1%, -0.5%
- Standby, output enable, or spread disable mode
- Industry-standard packages: 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm
- Outstanding mechanical robustness for portable applications
- All-silicon device with outstanding reliability of 2 FIT (10x improvement over quartz-based devices), enhancing system mean-time-to-failure (MTBF)
- Pb-free, RoHS and REACH compliant

Applications

- Printers
- Flat panel drivers
- PCI
- Microprocessors

DC Electrical Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	1	–	110	MHz	
Frequency Tolerance	F_tol	-50	–	+50	PPM	Inclusive of: Initial stability, operating temperature, rated power, supply voltage change, load change, shock and vibration Spread Off
		-100	–	+100	PPM	
Aging	Ag	-1	–	1	PPM	1st year at 25°C
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	1.71	1.8	1.89	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Current Consumption	Idd	–	3.7	4.1	mA	No load condition, f = 20 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	3.2	3.5	mA	No load condition, f = 20 MHz, Vdd = 1.8 V
Standby Current	I_std	–	2.4	4.3	µA	$\overline{ST}$ = GND, Vdd = 3.3 V, Output is Weakly Pulled Down
		–	1.2	2.2	µA	$\overline{ST}$ = GND, Vdd = 2.5 or 2.8 V, Output is Weakly Pulled Down
		–	0.4	0.8	µA	$\overline{ST}$ = GND, Vdd = 1.8 V, Output is Weakly Pulled Down
Duty Cycle	DC	45	–	55	%	All Vdds. f <= 70 MHz
		40	–	60	%	All Vdds. f >70 MHz
Rise/Fall Time	Tr, Tf	–	1	2	ns	20% - 80% Vdd=2.5 V, 2.8 V or 3.3 V, 15 pf load
		-	1.3	2.5	ns	20% - 80% Vdd=1.8 V, 15 pf load
Output Voltage High	VOH	90%	–	–	Vdd	IOH = -4 mA (Vdd = 3.3 V)
						IOH = -3 mA (Vdd = 2.8 V and 2.5 V)
						IOH = -2 mA (Vdd = 1.8 V)
Output Voltage Low	VOL	–	–	10	%Vdd	IOL = -4 mA (Vdd = 3.3 V)
						IOL = -3 mA (Vdd = 2.8 V and 2.5 V)
						IOL = -2 mA (Vdd = 1.8 V)
Output Load	Ld	–	–	15	pF	At maximum frequency and supply voltage. Contact SiTime for higher output load option
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$ or SD
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$ or SD
Startup Time	T_start	–	–	10	ms	Measured from the time Vdd reaches its rated minimum value
Resume Time	T_resume	–	3.0	3.8	ms	Measured from the time ST pin crosses 50% threshold
Cycle-to-Cycle Jitter	T_cyc	–	–	26	ps	f = 50 MHz, Spread = ON
		–	–	26	ps	f = 50 MHz, Spread = OFF

Spread Spectrum Modes[1]

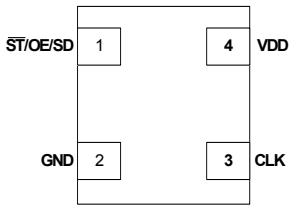
	Center Spread		Down Spread	
Code	B	D	O	Q
Percentage	±0.25%	±0.50%[2]	-0.5%	-1.0%[2]

Notes:
1. In both center spread and down spread modes, triangle modulation is employed with a frequency of ~32 kHz.
2. ±0.5% and -1.0% are available ONLY for <75 MHz in extended commercial temperature range.

Pin Configuration

Pin	Symbol	Functionality	
1	$\overline{ST}$/OE/SD	Standby (ST)	H or Open[3]: specified frequency output L: output is low (weak pull down). Oscillator stops
		Output Enable (OE)	H or Open[3]: specified frequency output L: output is high impedance.
		Spread Disable (SD)	H or Open: Spread = ON L: Spread =OFF
2	GND	Ground	Connect to Ground
3	CLK	Output	Clock Output
4	VDD	Power Supply	

Top View



Note:
3. In 1.8 V mode, a resistor of <10 kΩ between OE pin and VDD is recommended.

Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameters	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Number of Program Writes	–	1	NA
Program Retention over -40 to 125C, Process, VDD (0 to 3.65V)	–	1,000+	years

Thermal Considerations

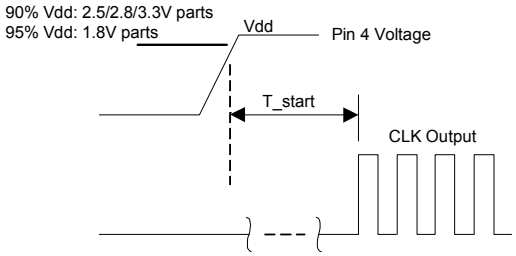
Package	Lead Count	Center Pad	Junction-to-Ambient Thermal Resistance (°C/W)		Junction-to-Case[6] (bottom) Thermal Resistance (°C/W)
			4 Layer Board[5]	2 Layer Board[4]	
7050	4	Soldered down	43.6	229	2.6
7050	4	Not soldered down	191	263	2.6
7050	4	No center pad	142	273	29.8
5032	4	No center pad	96.8	199	24
3225	4	No center pad	109	212	27
2520	4	No center pad	117	222	26

Notes:
4. Test boards compliant with JESD51-3.
5. Test boards compliant with JESD51-7.
6. Referenced to bottom of case.

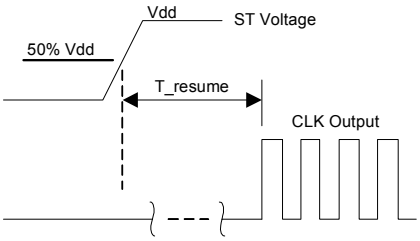
Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensibility Level	MSL1

Startup and Resume Timing Diagram



T_start: Time to start from power-off
(ST/OE Mode)



T_resume: Time to resume from ST
(ST Mode Only)

Programmable Drive Strength

The SiT9003 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the SiTime Applications Note section; http://www.sitime.com/support/application-notes.

EMI Reduction by Slowing Rise/Fall Time

Figure 1 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

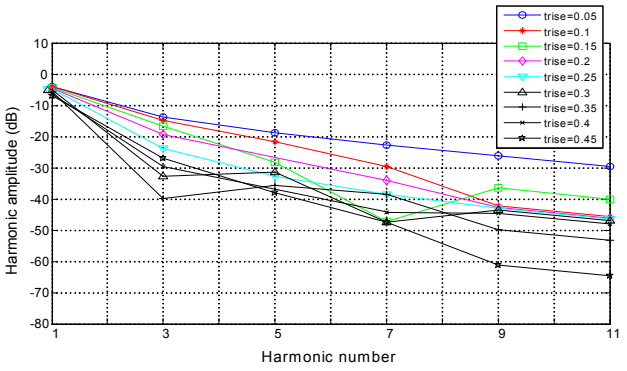


Figure 1. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to increase rise/fall time (edge rate) of the input clock. Some chipsets would require faster rise/fall time in order to reduce their sensitivity to this type of jitter. The SiT9003 provides up to 3 additional high drive strength settings for very fast rise/fall time. Refer to the Rise/Fall Time Tables to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V SiT9003 device with default drive strength setting, the typical rise/fall time is 1.1ns for 15 pF output load. The typical rise/fall time slows down to 2.9ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.9ns by then increasing the drive strength setting on the SiT9003.

The SiT9003 can support up to 60 pF or higher in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the Rise/Tall Time Tables to determine the proper drive strength for the desired combination of output load vs. rise/fall time

SiT9003 Drive Strength Selection

Tables 1 through 4 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the SiT9003 nominal supply voltage (1.8V, 2.5V, 2.8V, 3.3V).
2. Select the capacitive load column that matches the application requirement (15 pF to 60 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 1 through 4, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max Frequency} = \frac{1}{5 \times \text{Trf_20/80}}$$

Where Trf_20/80 is the typical rise/fall time at 20% to 80% Vdd

Example 1

Calculate f_{MAX} for the following condition:

- Vdd = 3.3V (Table 1)
- Capacitive Load: 30 pF
- Desired Tr/f time = 1.6ns (rise/fall time part number code = Z)

Part number for the above example:

SiT9003AI**Z**14-33EB-105.12345

Drive strength code is inserted here. Default setting is "-"

Rise and Fall Time Tables

Table 1. Rise/Fall Times, VDD = 3.3V ±10%, T = 40°C to 85°C

Drive Strength		Unit	Load (pF)			
			15	30	45	60
U	Max.	ns	2.4	3.5	5.5	6.4
	Typ.	ns	1.7	2.8	4.3	5.4
x or "–": Default	Max.	ns	2.0	2.5	3.9	4.8
	Typ.	ns	1.1	2.0	2.9	3.8
Z	Max.	ns	1.2	2.0	3.0	3.7
	Typ.	ns	0.8	1.6	2.2	2.9
H	Max.	ns	0.9	1.7	2.5	3.0
	Typ.	ns	0.6	1.3	1.9	2.3

Table 2. Rise/Fall Times, VDD = 2.8V ±10%, T = 40°C to 85°C

Drive Strength		Unit	Load (pF)			
			15	30	45	60
U	Max.	ns	2.5	4.1	6.0	7.3
	Typ.	ns	2.0	3.2	4.8	5.9
X	Max.	ns	2.2	3.0	4.5	5.4
	Typ.	ns	1.3	2.2	3.3	4.3
x or "–": Default	Max.	ns	2.0	2.4	3.5	4.3
	Typ.	ns	1.0	1.7	2.5	3.2
H	Max.	ns	1.2	1.9	2.9	3.6
	Typ.	ns	0.7	1.5	2.0	2.6

Table 3. Rise/Fall Times, VDD = 2.5V ±10%, T = 40°C to 85°C

Drive Strength		Unit	Load (pF)			
			15	30	45	60
U	Max.	ns	2.8	4.6	6.8	8.3
	Typ.	ns	2.1	3.6	5.2	6.4
X	Max.	ns	2.3	3.3	5.0	5.9
	Typ.	ns	1.4	2.5	3.7	4.7
x or "–": Default	Max.	ns	2.0	2.6	3.4	4.8
	Typ.	ns	1.1	1.9	2.8	3.6
H	Max.	ns	1.3	2.2	3.3	4.0
	Typ.	ns	0.9	1.6	2.3	2.9

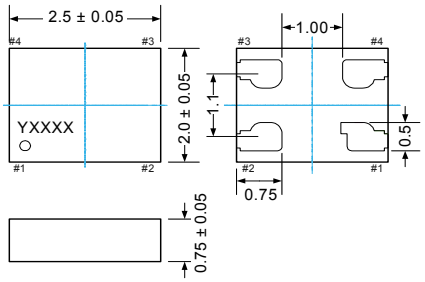
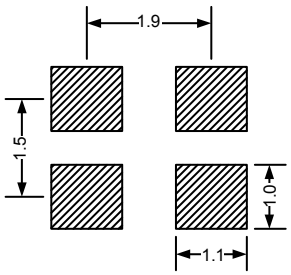
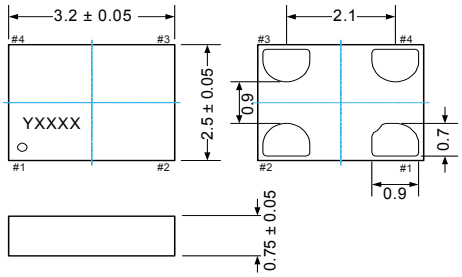
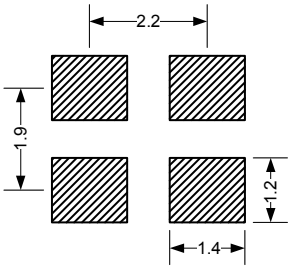
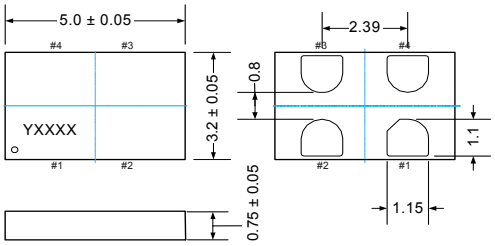
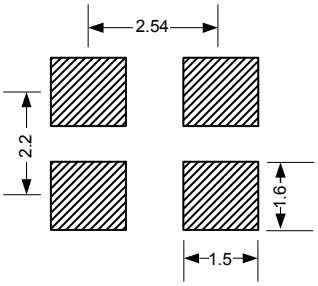
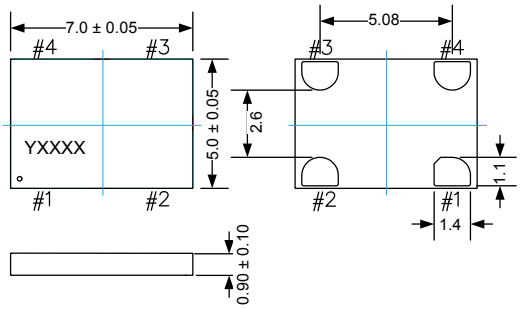
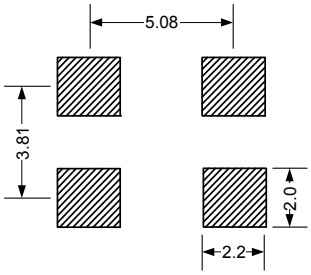
Table 4. Rise/Fall Times, VDD = 1.8V ±5%, T = 40°C to 85°C

Drive Strength		Unit	Load (pF)			
			15	30	45	60
U	Max.	ns	4.2	6.8	9.4	12.1
	Typ.	ns	3.1	5.1	7.3	9.2
X	Max.	ns	3.2	4.9	6.9	8.7
	Typ.	ns	2.3	3.7	5.3	6.5
Z	Max.	ns	2.7	3.9	5.5	6.7
	Typ.	ns	1.7	2.9	4.2	5.2
x or "–": Default	Max.	ns	2.5	3.3	4.6	5.7
	Typ.	ns	1.4	2.4	3.4	4.3

Note:

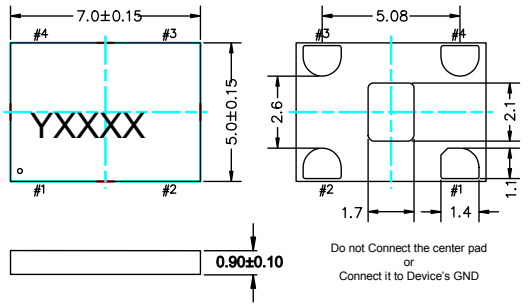
7. All rise/fall times are measured for the thresholds of 20% to 80% of VDD.

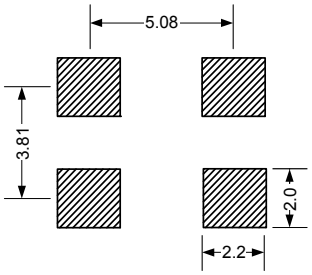
Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[8]	Recommended Land Pattern (Unit: mm)[9]
2.5 x 2.0 x 0.75 mm	
	
3.2 x 2.5 x 0.75 mm	
	
5.0 x 3.2 x 0.75 mm	
	
7.0 x 5.0 x 0.90 mm	
	

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)[8]	Recommended Land Pattern (Unit: mm)[9]
7.0 x 5.0 x 0.90 mm (with Center-Pad)	





Notes:

8. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
9. A capacitor of value 0.1 µF between Vdd and GND is required.

Ordering Information

The Part No. Guide is for reference only. To customize and build an exact part number, use the SiTime Part Number Generator.

SiT9003AC-14-18EB-66.66600T

Part Family
"SiT9003"

Revision Letter
"A" is the revision

Temperature Range
"C" Commercial, -20 to 70ºC
"I" Industrial, -40 to 85ºC

Output Drive Strength
"–" Default (datasheet limits)
See "Drive Strength Settings"
"U"
"X"
"Z"
"H"

Package Size
"1" 2.5 x 2.0 mm
"2" 3.2 x 2.5 mm
"3" 5.0 x 3.2 mm
"4" 7.0 x 5.0 mm (With Center Pad)
"8" 7.0 x 5.0 mm (Without Center Pad)

Frequency Stability
"3" for ±50 PPM
"4" for ±100 PPM

Packaging
"T" and "Y" ordering codes for appropriate T&R. Please refer to the table below.
Leave Blank for Bulk

Frequency
1.00000 to 110.00000 MHz

Spread Spectrum Percentage
"B" for ±0.25%
"D" for ±0.50%
"O" for -0.50%
"Q" for -1.0%

Feature Pin
"E" for Output Enable
"S" for Standby
"D" for Spread Disable

Supply Voltage
"18" for 1.8V
"25" for 2.5V
"28" for 2.8V
"33" for 3.3V

Available Spread Options vs. Temperature and Frequency

Spread Percentage	Temperature Range	
	C = -20 to 70°C	I = -40 to 85°C
B = ±0.25%	1-110 MHz	
D = ±0.50%	1-75 MHz	–
O = -0.50%	1-110 MHz	
Q = -1.0%	1-75 MHz	–

Ordering Codes for Supported Tape & Reel Packing Method

Device Size	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
2.5 x 2.0 mm	T	Y	–	–
3.2 x 2.5 mm	T	Y	–	–
5.0 x 3.2 mm	T	Y	–	–
7.0 x 5.0 mm	–	–	T	Y

Revision History

Version	Release Date	Change Summary
1.62	8/20/13	Added drive strength settings
1.7	11/18/13	Revised rise and fall time tables, added 7050 package diagram with center pad, add thermal considerations.

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