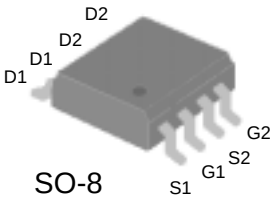
N AND P-CHANNEL ENHANCEMENT-MODE POWER MOSFETS

Simple drive requirement

Low on-resistance

Fast switching performance



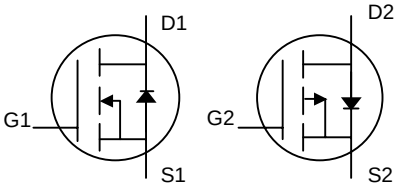
SO-8

N-CH	BV_{DSS}	35V
	$R_{DS(ON)}$	36mΩ
	I_D	5.8A
P-CH	BV_{DSS}	-35V
	$R_{DS(ON)}$	68mΩ
	I_D	-4.3A

Description

Advanced Power MOSFETs from Silicon Standard provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SSM4513M is in the SO-8 package, which is widely preferred for commercial and industrial surface mount applications, and is well-suited for most low voltage applications.



This device is available with Pb-free lead finish (second-level interconnect) as SSM4513GM.

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	35	-35	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D @ T_A=25°C	Continuous Drain Current[3]	5.8	-4.3	A
I_D @ T_A=70°C	Continuous Drain Current[3]	4.7	-3.4	A
I_{DM}	Pulsed Drain Current[1]	20	-20	A
P_D @ T_A=25°C	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/°C
T_{STG}	Storage Temperature Range	-55 to 150		°C
T_J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter		Value	Unit
Rthj-a	Thermal Resistance Junction-ambient[3]	Max.	62.5	°C/W

N-ch Electrical Characteristics @ T_j=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	35	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I_D=1mA	-	0.03	-	V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=5A	-	-	36	mΩ
		V_{GS}=4.5V, I_D=3A	-	-	60	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	3	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=5A	-	7	-	S
I_{DSS}	Drain-Source Leakage Current (T_j=25°C)	V_{DS}=30V, V_{GS}=0V	-	-	1	uA
	Drain-Source Leakage Current (T_j=70°C)	V_{DS}=24V, V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=5A	-	6	10	nC
Q_{gs}	Gate-Source Charge	V_{DS}=28V	-	2	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	3	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=15V	-	8	-	ns
t_r	Rise Time	I_D=1A	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω,V_{GS}=10V	-	16	-	ns
t_f	Fall Time	R_D=15Ω	-	3	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	470	750	pF
C_{oss}	Output Capacitance	V_{DS}=25V	-	90	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	60	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=1.7A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time	I_S=5A, V_{GS}=0V	-	17	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	11	-	nC

P-ch Electrical Characteristics @ T_j=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-35	-	-	V
$\Delta BV_{DSS}/\Delta Tj$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I_D=-1mA	-	-0.03	-	V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-4A	-	-	68	mΩ
		V_{GS}=-4.5V, I_D=-2A	-	-	100	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1	-	-3	V
g_{fs}	Forward Transconductance	V_{DS}=-10V, I_D=-4A	-	6	-	S
I_{DSS}	Drain-Source Leakage Current (Tj=25°C)	V_{DS}=-30V, V_{GS}=0V	-	-	-1	uA
	Drain-Source Leakage Current (Tj=70°C)	V_{DS}=-24V, V_{GS}=0V	-	-	-25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=-4A	-	6	10	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-28V	-	1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-4.5V	-	4	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=-15V	-	8	-	ns
t_r	Rise Time	I_D=-1A	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω , V_{GS}=-10V	-	20	-	ns
t_f	Fall Time	R_D=15Ω	-	4	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	410	660	pF
C_{oss}	Output Capacitance	V_{DS}=-25V	-	95	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	70	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=-1.7A, V_{GS}=0V	-	-	-1.2	V
t_{rr}	Reverse Recovery Time	I_S=-4A, V_{GS}=0V	-	21	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=-100A/μs	-	16	-	nC

Notes:

1.Pulse width limited by max. junction temperature.

2.Pulse width ≤300us , duty cycle ≤2%.

3.Surface mounted on 1 in^2 copper pad of FR4 board , t ≤10sec ; 135°C/W when mounted on min. copper pad.

N-channel

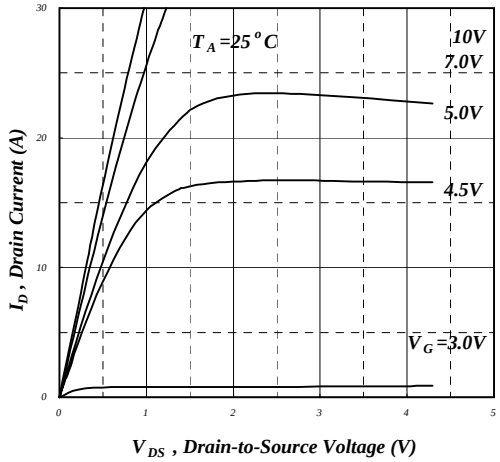


Fig 1. Typical Output Characteristics

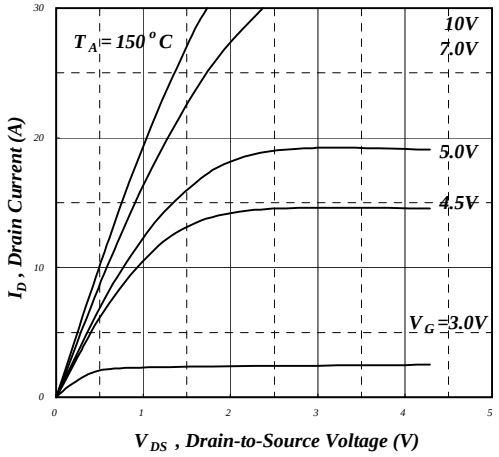


Fig 2. Typical Output Characteristics

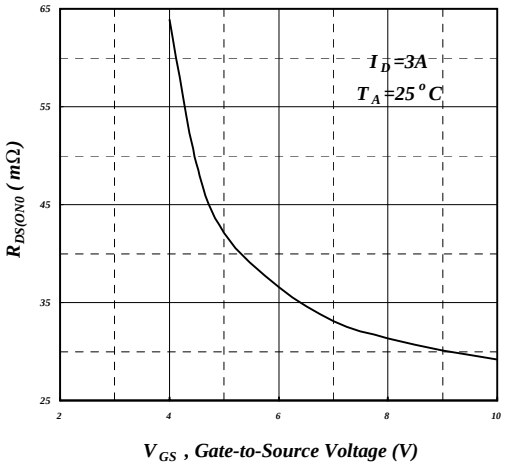


Fig 3. On-Resistance vs. Gate Voltage

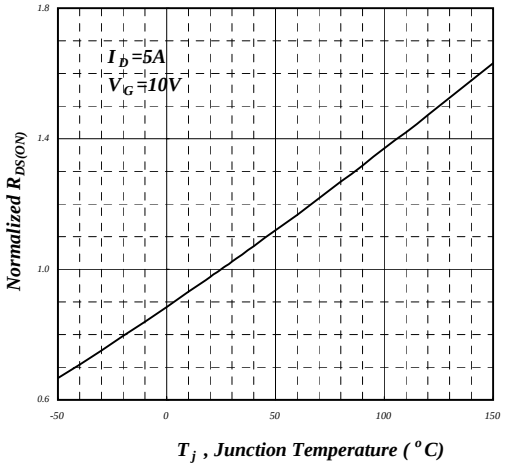


Fig 4. Normalized On-Resistance vs. Junction Temperature

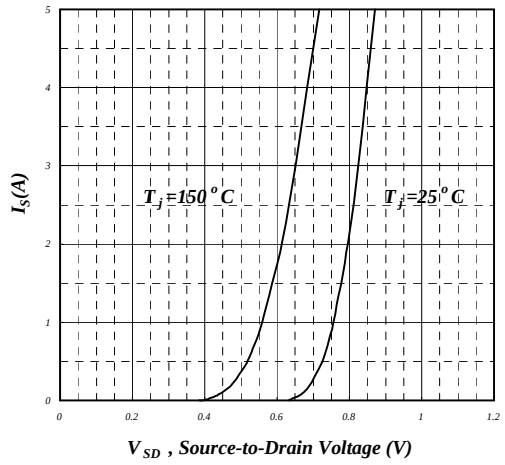


Fig 5. Forward Characteristic of Reverse Diode

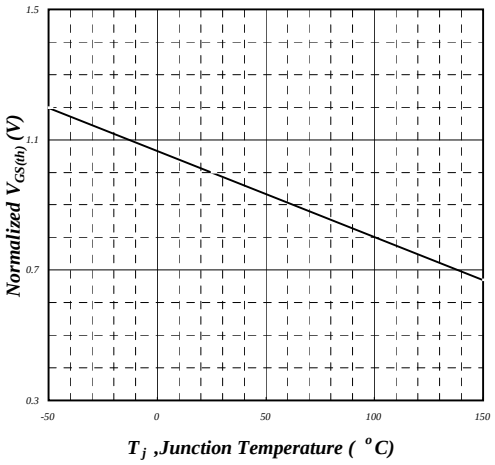


Fig 6. Gate Threshold Voltage vs. Junction Temperature

N-channel

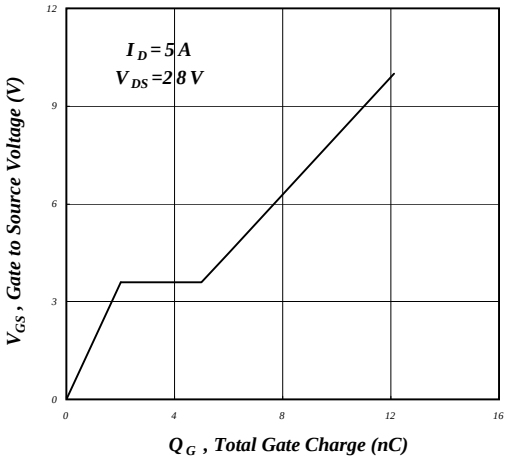


Fig 7. Gate Charge Characteristics

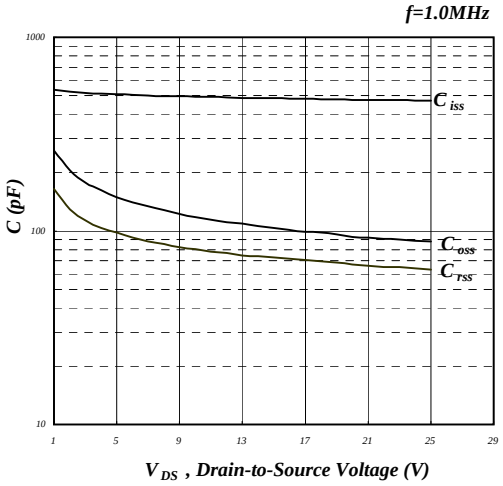


Fig 8. Typical Capacitance Characteristics

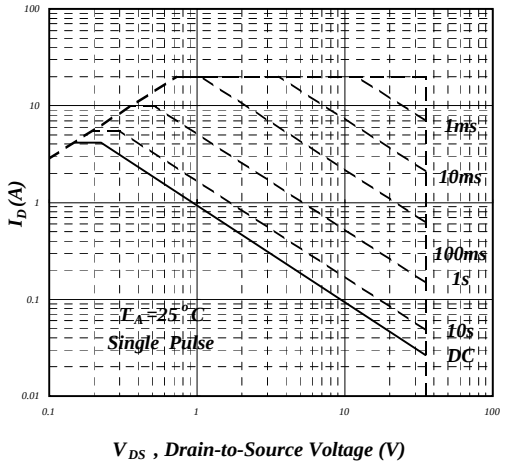


Fig 9. Maximum Safe Operating Area

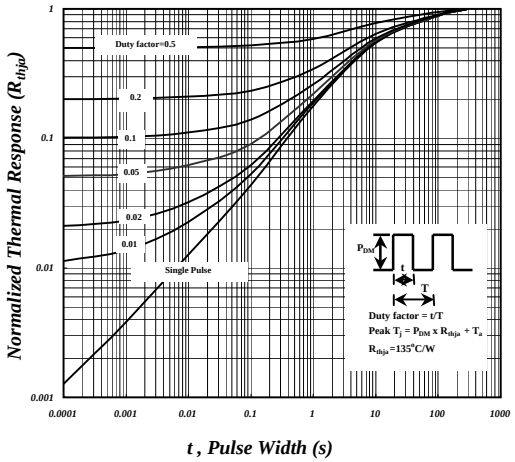


Fig 10. Effective Transient Thermal Impedance

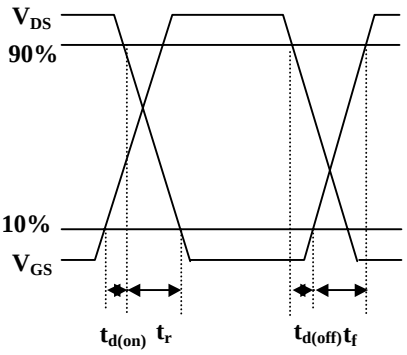


Fig 11. Switching Time Waveform

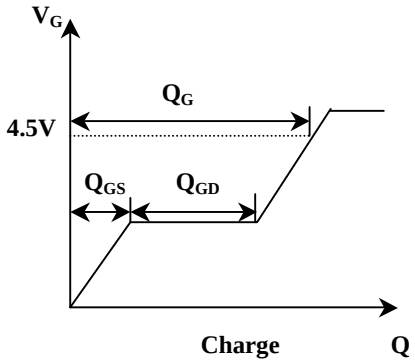


Fig 12. Gate Charge Waveform

P-Channel

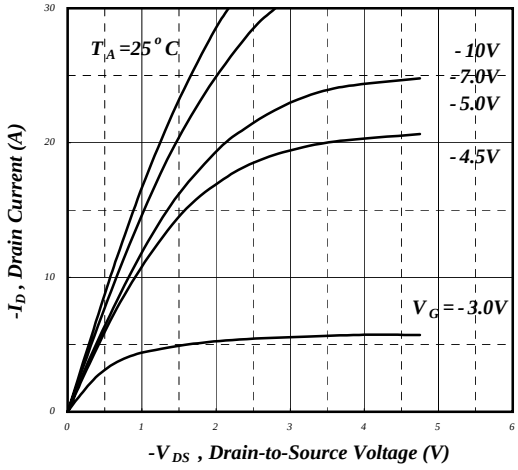


Fig 1. Typical Output Characteristics

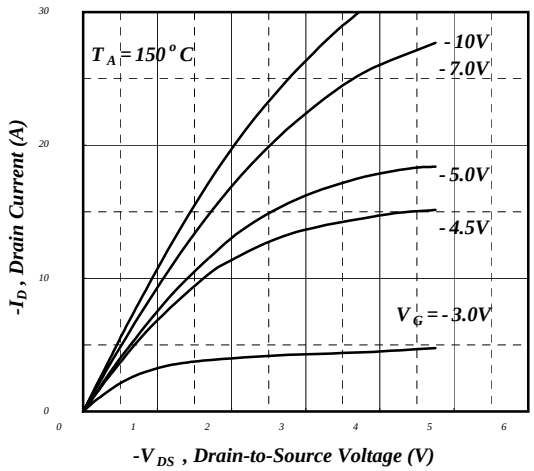


Fig 2. Typical Output Characteristics

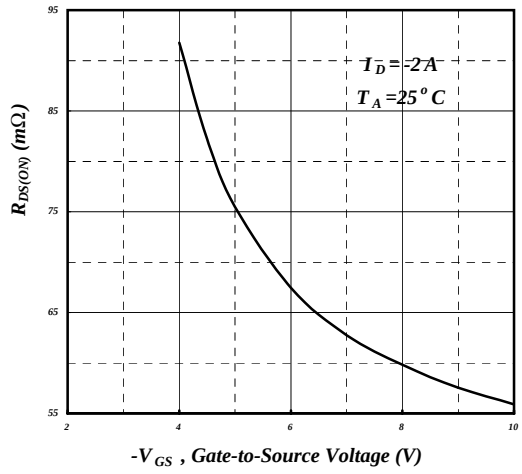


Fig 3. On-Resistance vs. Gate Voltage

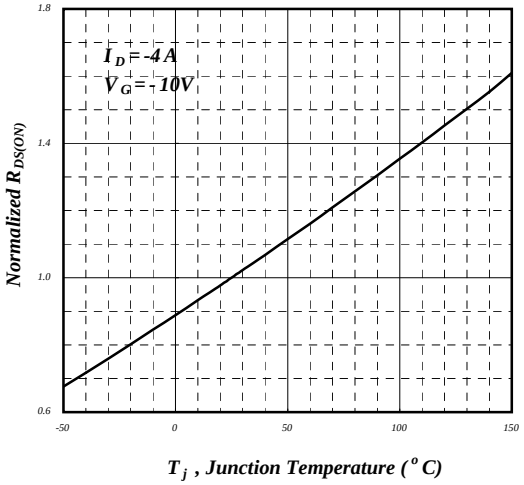
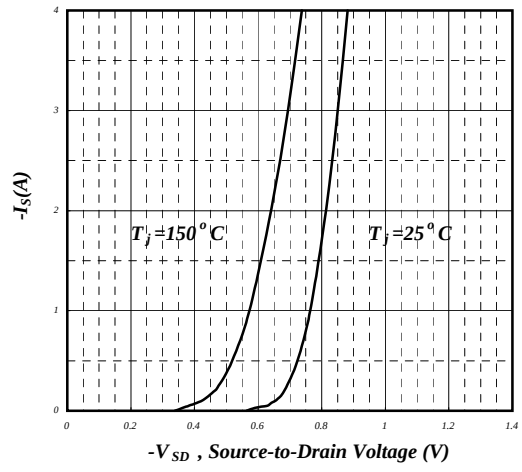


Fig 4. Normalized On-Resistance v.s. Junction Temperature



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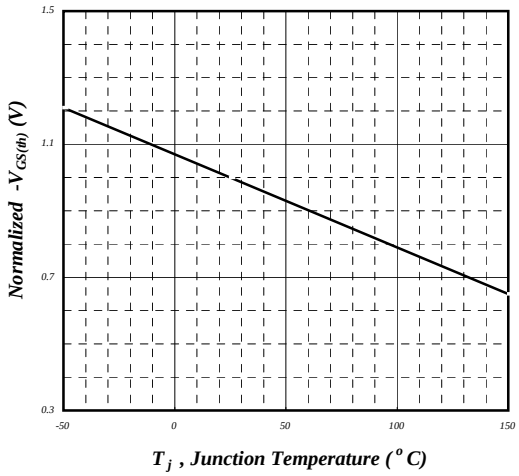


Fig 6. Gate Threshold Voltage vs. Junction Temperature

P-Channel

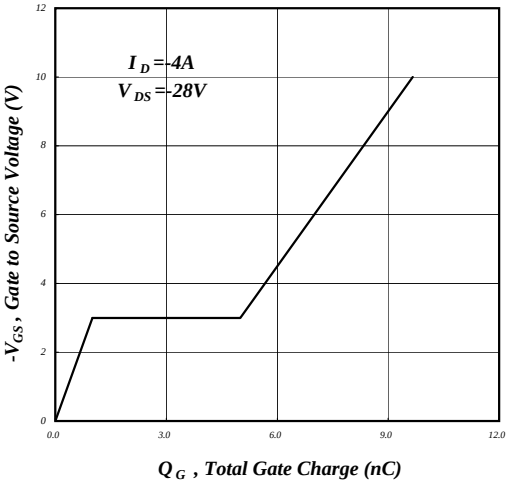
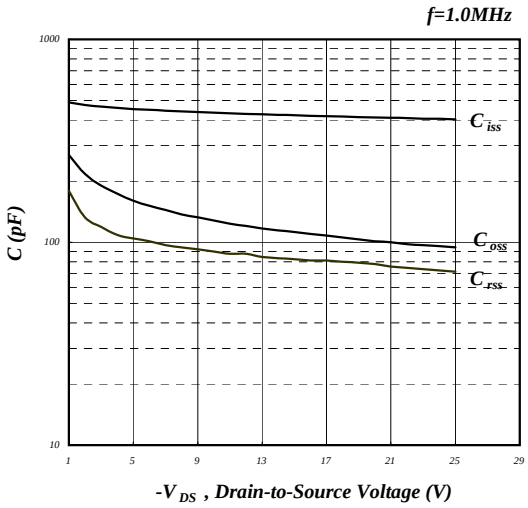


Fig 7. Gate Charge Characteristics



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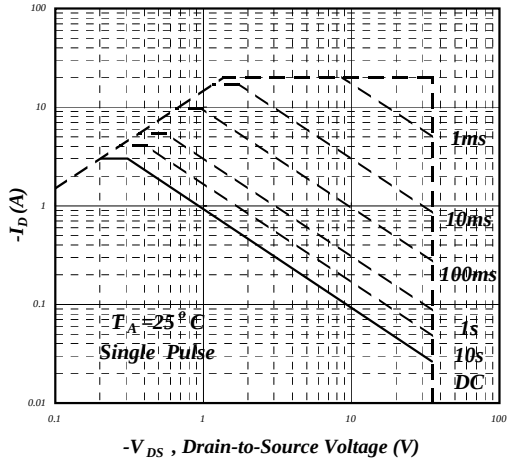

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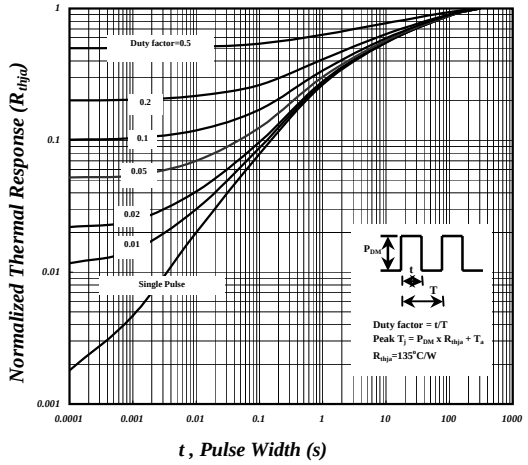

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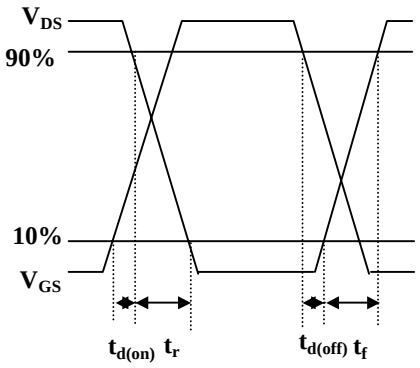

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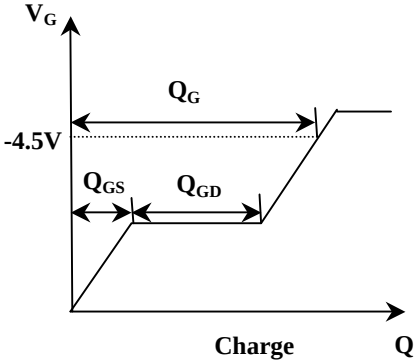

Fig 12. Gate Charge Waveform