ACT8847

Rev 5, 15-Nov-12

Advanced PMU for Multi-core Application Processors

FEATURES

INTEGRATED POWER SUPPLIES

- **Four DC/DC Step-Down (Buck) Regulators**
  - **2 x 2.8A, 2 x 1.5A**
- **Five Low-Noise LDOs**
  - **2 x 150mA, 3 x 350mA**
- **Three Low-Input Voltage LDOs**
  - **1 x 150mA, 2 x 350mA**
- **One Low IQ Keep-Alive LDO**
- **Backup Battery Charger**

SYSTEM CONTROL AND INTERFACE

- **Six General Purpose I/O with PWM Drivers**
- **I²C Serial Interface**
- **Interrupt Controller**

SYSTEM MANAGEMENT

- **Reset Interface and Sequencing Controller**
  - **Power on Reset**
  - **Soft / Hard Reset**
  - **Watchdog Supervision**
  - **Multiple Sleep Modes**
- **Thermal Management Subsystem**

APPLICATIONS

- **Tablet PC**
- **Mobile Internet Devices (MID)**
- **Ebooks**
- **Personal Navigation Devices**

GENERAL DESCRIPTION

The ACT8847 is a complete, cost effective, and highly-efficient *ActivePMU™* power management solution optimized for the power, voltage sequencing and control requirements of Samsung Exynos 4210 (S5PC210/S5PV310) and other application processors. (Please See Ordering Information Section and its Appendix.)

The ACT8847 features four fixed-frequency, current-mode, synchronous PWM step-down converters that achieve peak efficiencies of up to 97%. These regulators operate with a fixed frequency of 2.25MHz, minimizing noise in sensitive applications and allowing the use of small external components. These buck regulators supply up to 2.8A of output current and can fully satisfy the power and control requirements of the multi-core application processor. Dynamic Voltage Scaling (DVS) is supported either by dedicated control pins, or through I2C interface to optimize the energy-per-task performance for the processor. This device also include eight low-noise LDOs (up to 350mA per LDO), one always-ON LDO and an integrated backup battery charger to provide a complete power system for the processor.

The power sequence and reset controller provides power-on reset, SW-initiated reset, and power cycle reset for the processor. It also features the watchdog supervisory function. Multiple sleep modes with autonomous sleep and wake-up sequence control are supported.

The thermal management and protection subsystem allows the host processor to manage the power dissipation of the PMU and the overall system dynamically. The PMU provides a thermal warning to the host processor when the temperature reaches a certain threshold such that the system can turn off some of the non-essential functions, reduce the clock frequency and etc to manage the system temperature.

The ACT8847 is available in a compact, Pb-Free and RoHS-compliant TQFN66-48 package.

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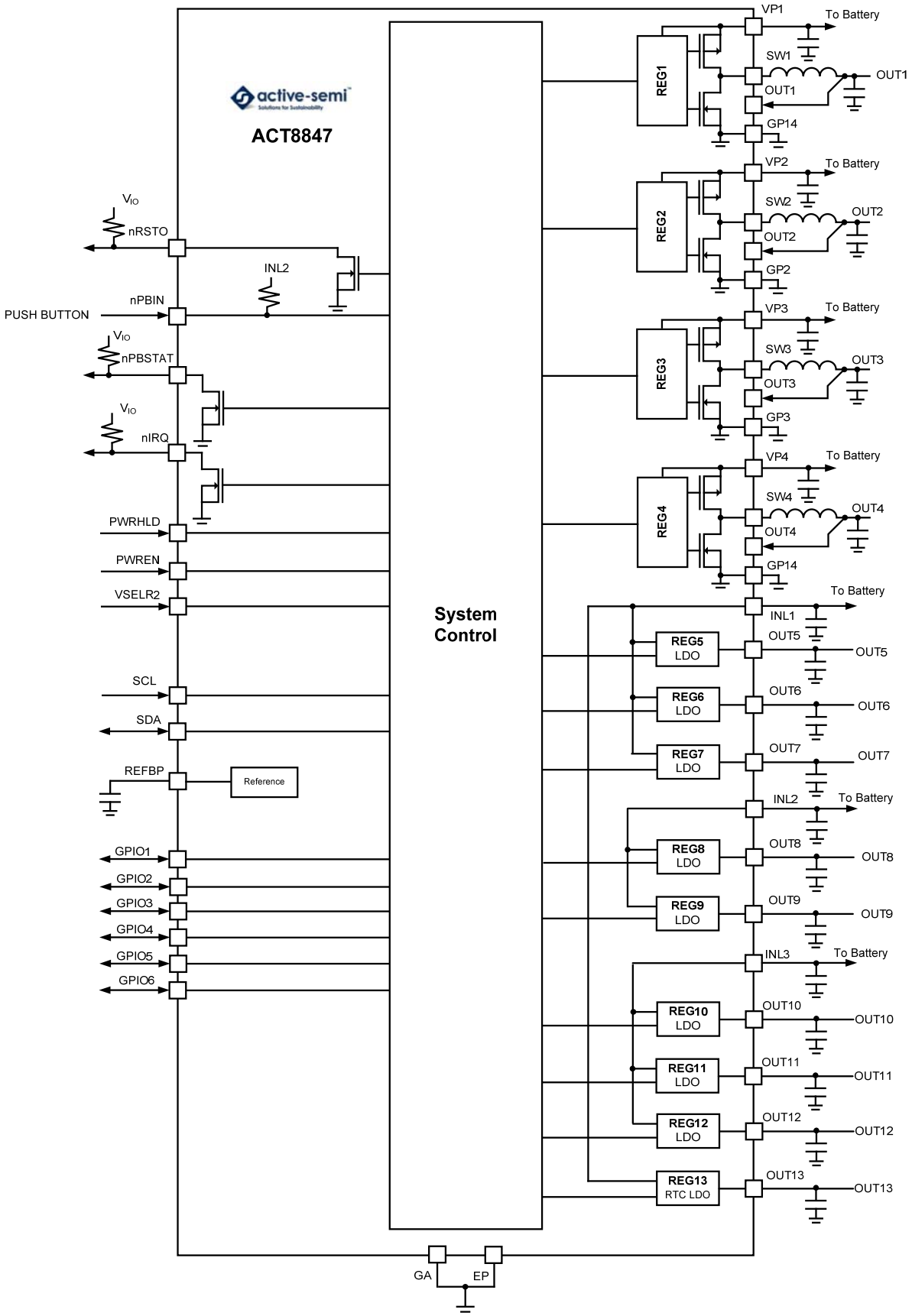
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FUNCTIONAL BLOCK DIAGRAM



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ORDERING INFORMATION①

PART NUMBER	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{OUT4}	V_{OUT5}	V_{OUT6}	V_{OUT7}	V_{OUT8}	V_{OUT9}	V_{OUT10}	V_{OUT11}	V_{OUT12}	V_{OUT13}
ACT8847QM171-T	1.2V	1.2V	1.1V	1.1V	1.1V	1.1V	3.3V	1.8V	3.3V	1.2V	1.1V	1.8V	1.8V
ACT8847QM174-T	1.5V	1.2V	1.1V	1.1V	1.1V	1.1V	3.3V	1.8V	3.3V	1.5V	1.1V	1.8V	1.8V
ACT8847QM211-T	1.3V	1.1V	1.5V	OFF	OFF	OFF	3.3V	1.8V	2.5V	OFF	2.8V	OFF	3.3V
ACT8847QM401-T	1.05V	1.3V	1.05V	1.0V	1.8V	1.8V	1.8V	3.3V	1.2V	1.1V	1.0V	OFF	1.0V
ACT8849QM411-T	1.2V	1.5V	2.0V	2.8V	1.8V	1.8V	2.8V	1.8V	1.8V	1.0V	1.5V	1.0V	No Use

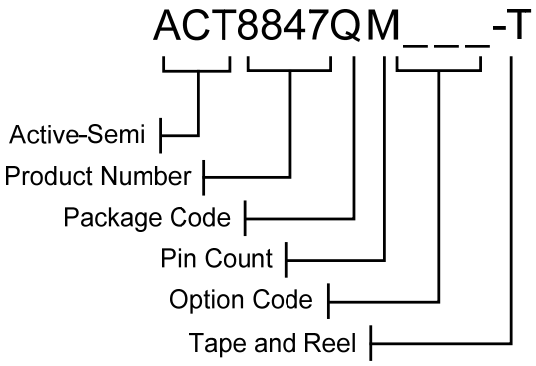
PACKAGE	PINS	TEMPERATURE RANGE
TQFN66-48	48	-40°C to +85°C

①: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

②: ACT8847QM174-T is dedicated to S5PV310 application.

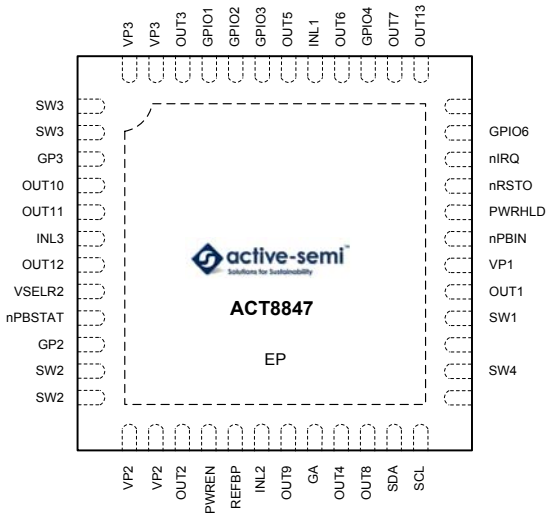
③: ACT8847 Data Sheet is described according to ACT8847QM171-T application; please see the Appendix of ACT8847QM211-T for its specification.

④: ACT8847QM401-T and ACT8849QM411-T is the association application for Samsung Exynos 4412/ 4212 platforms; please see the Appendix of ACT8847QM401-T for its specification.



PIN CONFIGURATION

TOP VIEW



Thin - QFN (TQFN66-48)

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PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1, 2	SW3	Switch Node for REG3.
3	GP3	Power Ground for REG3. Connect GP14, GP2, GP3, and GA together at a single point as close to the IC as possible.
4	OUT10	REG10 output. Bypass it to ground with a 2.2µF capacitor.
5	OUT11	REG11 output. Bypass it to ground with a 2.2µF capacitor.
6	INL3	Power input for REG10, REG11 and REG12.
7	OUT12	REG12 output. Bypass it to ground with a 2.2µF capacitor.
8	VSELR2	Output Voltage Selection for REG2. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage.
9	nPBSTAT	Active-Low Open-Drain Push-Button Status Output. nPBSTAT is asserted low whenever the nPBIN is pushed, and is high-Z otherwise.
10	GP2	Power ground for REG2. Connect GP14, GP2, GP3, and GA together at a single point as close to the IC as possible.
11, 12	SW2	Switch Node for REG2.
13, 14	VP2	Power input for REG2. Bypass to GP2 with a high quality ceramic capacitor placed as close to the IC as possible.
15	OUT2	Output Voltage Sense for REG2.
16	PWREN	Power enable input.
17	REFBP	Reference Bypass. Connect a 0.047µF ceramic capacitor from REFBP to GA. This pin is discharged to GA in shutdown.
18	INL2	Power Input for REG8, REG9.
19	OUT9	REG9 output. Bypass it to ground with a 2.2µF capacitor.
20	GA	Analog Ground.
21	OUT4	Output voltage sense for REG4.
22	OUT8	REG8 output. Bypass it to ground with a 2.2µF capacitor.
23	SDA	Data Input for I^2C Serial Interface. Data is read on the rising edge of SCL.
24	SCL	Clock Input for I^2C Serial Interface.
25	VP4	Power input for REG4. Bypass to GP14 with a high quality ceramic capacitor placed as close to the IC as possible.

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PIN DESCRIPTIONS CONT'D

PIN	NAME	DESCRIPTION
26	SW4	Switch Node for REG4.
27	GP14	Power Ground for REG1 and REG4. Connect GP14, GP2, GP3, and GA together at a single point as close to the IC as possible.
28	SW1	Switch Node for REG1.
29	OUT1	Output Voltage Sense for REG1.
30	VP1	Power Input for REG1. Bypass to GP14 with a high quality ceramic capacitor placed as close to the IC as possible.
31	nPBIN	Master Enable Input. Drive nPBIN to GA through a 50kΩ resistor to enable the IC, drive nPBIN directly to GA to assert a Manual-Reset condition.
32	PWRHLD	Power hold Input. PWRHLD is internally pulled down to GA through a 900kΩ resistor.
33	nRSTO	Open-Drain Reset Output.
34	nIRQ	Open-Drain Interrupt Output.
35	GPIO6	General Purpose I/O #6. Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the *PWM LED Drive* section for more information.
36	GPIO5	General Purpose I/O #5. Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the *PWM LED Driver* section for more information.
37	OUT13	REG13 output. Bypass it to ground with a 2.2µF capacitor.
38	OUT7	REG7 output. Bypass it to ground with a 2.2µF capacitor.
39	GPIO4	General Purpose I/O #4. Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the *PWM LED Driver* section for more information.
40	OUT6	REG6 output. Bypass it to ground with a 2.2µF capacitor.
41	INL1	Power Input for REG5, REG6, REG7.
42	OUT5	REG5 output. Bypass it to ground with a 2.2µF capacitor.
43	GPIO3	General Purpose I/O #3. Configured as PWM LED driver output for up to 6mA current with programmable frequency and duty cycle. See the *PWM LED Drier* section for more information.
44	GPIO2	General Purpose I/O #2. Configured as VSELR4 for Voltage Selection of REG4. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage.
45	GPIO1	General Purpose I/O #1. Configured as VSELR3 for Voltage Selection of REG3. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage.
46	OUT3	Output Voltage Sense for REG3.
47,48	VP3	Power input for REG3. Bypass to GP3 with a high quality ceramic capacitor placed as close to the IC as possible.
EP	EP	Exposed Pad. Must be soldered to ground on PCB.

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ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
INL1, INL2, INL3 to GA; VP1, SW1, OUT1 to GP14; VP2, SW2, OUT2 to GP2; VP3, SW3, OUT3 to GP3; VP4, SW4, OUT4 to GP14	-0.3 to 6	V
GP14, GP2, GP3 to GA	-0.3 to + 0.3	V
OUT5, OUT6, OUT7, OUT13 to GA	-0.3 to INL1 + 0.3	V
OUT8, OUT9, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, VSELR2, nPBIN, nRSTO, nIRQ, nPBSTAT, PWREN, PWRHLD, REFBP, SCL, SDA to GA	-0.3 to INL2 + 0.3	V
OUT10, OUT11, OUT12 to GA	-0.3 to INL3 + 0.3	V
Junction to Ambient Thermal Resistance	21	°C/W
Operating Ambient Temperature Range	-40 to 85	°C
Operating Junction Temperature	-40 to 125	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

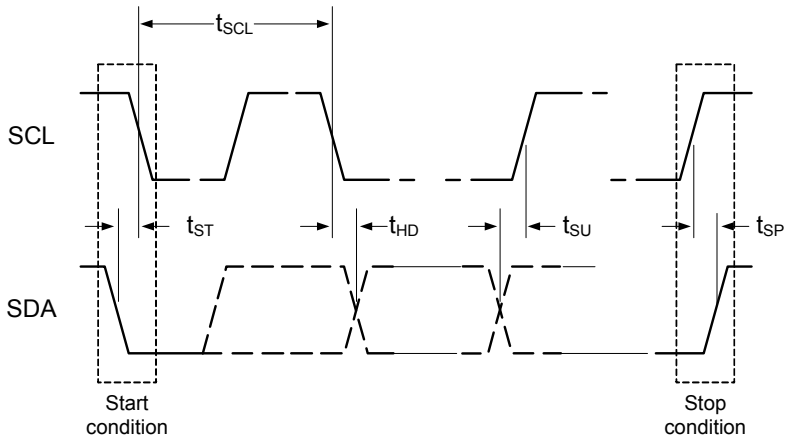
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I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{INL2} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{INL2} = 3.1V to 5.5V, T_A = -40ºC to 85ºC			0.35	V
SCL, SDA Input High	V_{INL2} = 3.1V to 5.5V, T_A = -40ºC to 85ºC	1.55			V
SDA Leakage Current				1	µA
SCL Leakage Current				1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Period, t_{SCL}		1.5			µs
SDA Data Setup Time, t_{SU}		100			ns
SDA Data Hold Time, t_{HD}		300			ns
Start Setup Time, t_{ST}	For Start Condition	100			ns
Stop Setup Time, t_{SP}	For Stop Condition	100			ns

Figure 1:
I²C Compatible Serial Bus Timing



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GLOBAL REGISTER MAP

BLOCK	ADDRESS		BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
SYS	0x00	NAME	nBATLEVMSK	nBATSTAT	VBATDAT	*Reserved*	BATLEV[3]	BATLEV[2]	BATLEV[1]	BATLEV[0]
		DEFAULT①	0	R	R	0	0	0	0	0
SYS	0x01	NAME	nTMSK	TSTAT	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT①	0	R	0	0	0	0	0	0
REG1	0x10	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG1	0x12	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	0	0	R
REG2	0x20	NAME	*Reserved*	*Reserved*	VSET0[5]	VSET0[4]	VSET0[3]	VSET0[2]	VSET0[1]	VSET0[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG2	0x21	NAME	*Reserved*	*Reserved*	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG2	0x22	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	1	0	1	0	0	0	R
REG3	0x30	NAME	*Reserved*	*Reserved*	VSET0[5]	VSET0[4]	VSET0[3]	VSET0[2]	VSET0[1]	VSET0[0]
		DEFAULT①	0	0	0	1	0	1	0	0
REG3	0x31	NAME	*Reserved*	*Reserved*	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	0	1	0	1	0	0
REG3	0x32	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	1	0	1	0	1	0	R
REG4	0x40	NAME	*Reserved*	*Reserved*	VSET0[5]	VSET0[4]	VSET0[3]	VSET0[2]	VSET0[1]	VSET0[0]
		DEFAULT①	0	0	0	1	0	1	0	0
REG4	0x41	NAME	*Reserved*	*Reserved*	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	0	1	0	1	0	0
REG4	0x42	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PHASE	nFLTMSK	OK
		DEFAULT①	1	1	0	1	0	1	0	R
REG5	0x50	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	0	1	0	0
REG5	0x51	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	1	0	1	0	R
REG6	0x58	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	0	1	0	0
REG6	0x59	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	1	0	R
REG7	0x60	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	1	1	0	0	1
REG7	0x61	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	1	0	R
REG8	0x68	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	0	0	1	0	0
REG8	0x69	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	1	0	1	0	R

①: Default values of ACT8847QM171-T.

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GLOBAL REGISTER MAP CONT'D

BLOCK	ADDRESS		BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
REG9	0x70	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG9	0x71	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	1	0	1	0	R
REG10	0x80	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG10	0x81	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	1	0	1	0	R
REG11	0x90	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	0	1	0	0
REG11	0x91	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	1	0	1	0	R
REG12	0xA0	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	1	1	0	0	1	0	0
REG12	0xA1	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	DIS	nFLTMSK	OK
		DEFAULT①	1	1	0	0	0	1	0	R
REG13	0xB1	NAME	ON	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT①	1	0	0	0	0	0	0	0
PB	0xC0	NAME	PBAMSK	PBDMSK	*Reserved*	*Reserved*	*Reserved*	*Reserved*	WDSREN	WDPCEN
		DEFAULT①	0	0	0	0	0	0	0	0
PB	0xC1	NAME	INTADR [7]	INTADR [6]	INTADR [5]	INTADR [4]	INTADR [3]	INTADR [2]	INTADR [1]	INTADR [0]
		DEFAULT①	R	R	R	R	R	R	R	R
PB	0xC2	NAME	PBASTAT	PBDSTAT	PBDAT	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT①	R	R	R	R	R	R	R	R
PB	0xC3	NAME	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	SIPC
		DEFAULT①	0	0	0	0	0	0	0	0
PB	0xC5	NAME	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	PCSTAT	SRSTAT
		DEFAULT①	0	0	0	0	0	0	R	R
GPIO6	0xE3	NAME	PWM6EN	FRE6[2]	FRE6[1]	FRE6[0]	DUTY6[3]	DUTY6[2]	DUTY6[1]	DUTY6[0]
		DEFAULT①	0	0	0	0	0	0	0	0
GPIO5	0xE4	NAME	PWM5EN	FRE5[2]	FRE5[1]	FRE5[0]	DUTY5[3]	DUTY5[2]	DUTY5[1]	DUTY5[0]
		DEFAULT①	0	0	0	0	0	0	0	0
GPIO3	0xF4	NAME	PWM3EN	FRE3[2]	FRE3[1]	FRE3[0]	DUTY3[3]	DUTY3[2]	DUTY3[1]	DUTY3[0]
		DEFAULT①	0	0	0	0	0	0	0	0
GPIO4	0xF5	NAME	PWM4EN	FRE4[2]	FRE4[1]	FRE4[0]	DUTY4[3]	DUTY4[2]	DUTY4[1]	DUTY4[0]
		DEFAULT①	0	0	0	0	0	0	0	0

①: Default values of ACT8847QM171-T.

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REGISTER AND BIT DESCRIPTIONS

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
SYS	0x00	[7]	nBATLEVMSK	R/W	Battery Voltage Level Interrupt Mask. Set this bit to 1 to unmask the interrupt. See the *Programmable Battery Voltage Monitor* section for more information
SYS	0x00	[6]	nBATSTAT	R	Battery Voltage Status. Value is 1 when BATLEV interrupt is generated, value is 0 otherwise.
SYS	0x00	[5]	VBATDAT	R	Battery Voltage Monitor real time status. Value is 1 when VBAT < BATLEV, value is 0 otherwise.
SYS	0x00	[4]	-	R/W	Reserved.
SYS	0x00	[3:0]	BATLEV	R/W	Battery Voltage Detect Threshold. Defines the BATLEV voltage threshold. See the *Programmable Battary Voltage Monitor* section for more information.
SYS	0x01	[7]	nTMSK	R/W	Thermal Interrupt Mask. Set this bit to 1 to unmask the interrupt.
SYS	0x01	[6]	TSTAT	R	Thermal Interrupt Status. Value is 1 when a thermal interrupt is generated, value is 0 otherwise.
SYS	0x01	[5:0]	-	R/W	Reserved.
REG1	0x10	[7:6]	-	R	Reserved.
REG1	0x10	[5:0]	VSET0	R/W	Primary Output Voltage Selection. See the *Output Voltage Programming* section for more information
REG1	0x12	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG1	0x12	[6:3]	-	R	Reserved.
REG1	0x12	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG1	0x12	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG1	0x12	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG2	0x20	[7:6]	-	R	Reserved.
REG2	0x20	[5:0]	VSET0	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information
REG2	0x21	[7:6]	-	R	Reserved.
REG2	0x21	[5:0]	VSET1	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information.
REG2	0x22	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG2	0x22	[6:3]	-	R	Reserved.
REG2	0x22	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG2	0x22	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG2	0x22	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG3	0x30	[7:6]	-	R	Reserved.
REG3	0x30	[5:0]	VSET0	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG3	0x31	[7:6]	-	R	Reserved.
REG3	0x31	[5:0]	VSET1	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information.
REG3	0x32	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG3	0x32	[6:3]	-	R	Reserved.
REG3	0x32	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG3	0x32	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG3	0x32	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG4	0x40	[7:6]	-	R	Reserved.
REG4	0x40	[5:0]	VSET0	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information
REG4	0x41	[7:6]	-	R	Reserved.
REG4	0x41	[5:0]	VSET1	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information.
REG4	0x42	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG4	0x42	[6:3]	-	R	Reserved.
REG4	0x42	[2]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG4	0x42	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG4	0x42	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG5	0x50	[7:6]	-	R	Reserved.
REG5	0x50	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG5	0x51	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG5	0x51	[6:3]	-	R	Reserved.
REG5	0x51	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG5	0x51	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG5	0x51	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG6	0x58	[7:6]	-	R	Reserved.
REG6	0x58	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG6	0x59	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG6	0x59	[6:3]	-	R	Reserved.
REG6	0x59	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG6	0x59	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG6	0x59	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG7	0x60	[7:6]	-	R	Reserved.
REG7	0x60	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG7	0x61	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG7	0x61	[6:3]	-	R	Reserved.
REG7	0x61	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG7	0x61	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG7	0x61	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG8	0x68	[7:6]	-	R	Reserved.
REG8	0x68	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG8	0x69	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG8	0x69	[6:3]	-	R	Reserved.
REG8	0x69	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG8	0x69	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG8	0x69	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG9	0x70	[7:6]	-	R	Reserved.
REG9	0x70	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG9	0x71	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG9	0x71	[6:3]	-	R	Reserved.
REG9	0x71	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG9	0x71	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG9	0x71	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG10	0x80	[7:6]	-	R	Reserved.

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BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG10	0x80	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG10	0x81	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG10	0x81	[6:3]	-	R	Reserved.
REG10	0x81	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG10	0x81	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG10	0x81	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG11	0x90	[7:6]	-	R	Reserved.
REG11	0x90	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG11	0x91	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG11	0x91	[6:3]	-	R	Reserved.
REG11	0x91	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG11	0x91	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG11	0x91	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG12	0xA0	[7:6]	-	R	Reserved.
REG12	0xA0	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG12	0xA1	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG12	0xA1	[6:3]	-	R	Reserved.
REG12	0xA1	[2]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG12	0xA1	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG12	0xA1	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG13	0xB1	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG13	0xB1	[6:0]	-	R	Reserved.
PB	0xC0	7	nPBAMSK	R/W	nPBIN Assertion Interrupt Control. Set this bit to 1 to generate an interrupt when nPBIN is asserted.
PB	0xC0	6	nPBDMSK	R/W	nPBIN De-assertion Interrupt Control. Set this bit to 1 to generate an interrupt when nPBIN is de-asserted.
PB	0xC0	[5:2]	-	R	Reserved.
PB	0xC0	1	WDSREN	R/W	Watchdog Soft-Reset Enable. Set this bit to 1 to enable watchdog function. When the watchdog timer expires, the PMU commences a soft-reset routine. This bit is automatically reset to 0 when entering sleep mode.

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REGISTER AND BIT DESCRIPTIONS CONT'D

BLOCK	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
PB	0xC0	[5:2]	-	R	Reserved.
PB	0xC0	1	WDSREN	R/W	Watchdog Soft-Reset Enable. Set this bit to 1 to enable watchdog function. When the watchdog timer expires, the PMU commences a soft-reset routine. This bit is automatically reset to 0 when entering sleep mode.
PB	0xC0	0	WDPCEN	R/W	Watchdog Power-Cycle Enable. Set this bit to 1 to enable watchdog function. When watchdog timer expires, the PMU commence a power cycle. This bit is automatically reset to 0 when entering sleep mode.
PB	0xC1	[7:0]	INTADR	R	Interrupt Address. It holds the address of the block that triggers the interrupt. This byte defaults to 0xFF and is automatically set to 0xFF after being read. Bit 7 is the MSB while Bit 0 is the LSB.
PB	0xC2	7	PBASTAT	R	nPBIN Assertion Interrupt Status. The value of this bit is 1 if the nPBIN Assertion Interrupt is triggered.
PB	0xC2	6	PBDSTAT	R	nPBIN De-assertion Interrupt Status. The value of this bit is 1 if the nPBIN De-assertion Interrupt is triggered.
PB	0xC2	5	PBASTAT	R	nPBIN Status bit. This bit contains the real-time status of the nPBIN pin. The value of this bit is 1 if nPBIN is asserted, and is 0 if nPBIN is de-asserted.
PB	0xC2	[4:0]	-	R	Reserved.
PB	0xC3	[7:1]	-	R	Reserved.
PB	0xC3	0	SIPC	R/W	Software Initiated Power Cycle. When this bit is set, the PMU commences a power cycle after 8ms delay.
PB	0xC5	[7:2]	-	R	Reserved.
PB	0xC5	1	PCSTAT	R/W	Power-cycle Flag. The value of this bit is 1 after a power cycle. This bit is automatically cleared to 0 after read.
PB	0xC5	0	SRSTAT	R/W	Soft-reset Flag. The value of this bit is 1 after a soft-reset. This bit is automatically cleared to 0 after read.
GPIO6	0xE3	[7]	PWM6EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO6.
GPIO6	0xE3	[6:4]	FRE6	R/W	PWM Frequency Selection Bits for GPIO6. See the Table 6 for code to frequency cross.
GPIO6	0xE3	[3:0]	DUTY6	R/W	Duty Cycle Selection Bits for GPIO6. See the Table 7 for code to duty cross.
GPIO5	0xE4	[7]	PWM5EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO5.
GPIO5	0xE4	[6:4]	FRE5	R/W	PWM Frequency Selection Bits for GPIO5. See the Table 6 for code to frequency cross.
GPIO5	0xE4	[3:0]	DUTY5	R/W	Duty Cycle Selection Bits for GPIO5. See the Table 7 for code to duty cross.
GPIO3	0xF4	[7]	PWM3EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO3.
GPIO3	0xF4	[6:4]	FRE3	R/W	PWM Frequency Selection Bits for GPIO3. See the Table 6 for code to frequency cross.
GPIO3	0xF4	[3:0]	DUTY3	R/W	Duty Cycle Selection Bits for GPIO3. See the Table 7 for code to duty cross.
GPIO4	0xF5	[7]	PWM4EN	R/W	PWM Function Enable. Set 1 to enable PWM function of GPIO4.
GPIO4	0xF5	[6:4]	FRE4	R/W	PWM Frequency Selection Bits for GPIO4. See the Table 6 for code to frequency cross.
GPIO4	0xF5	[3:0]	DUTY4	R/W	Duty Cycle Selection Bits for GPIO4. See the Table 7 for code to duty cross.

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SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(V_{INL2} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		3.0		5.5	V
UVLO Threshold Voltage	V_{INL2} Rising	2.6	2.8	3.0	V
UVLO Hysteresis	V_{INL2} Hysteresis		200		mV
Operating Supply Current	All Regulators Enabled but no load		0.6	1.2	mA
Shutdown Supply Current	All Regulators Disabled except REG13		10	20	µA
Oscillator Frequency		2.0	2.25	2.5	MHz
Logic High Input Voltage		1.4			V
Logic Low Input Voltage				0.4	V
Leakage Current	V[nIRQ] = V[nRSTO] = 4.2V			1	µA
Low Level Output Voltage	nIRQ, nRSTO, ISINK = 5mA			0.3	V
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis			20		°C

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STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = V_{VP3} = V_{VP4} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
UVLO Threshold	Input Voltage Rising	2.5	2.6	2.7	V
UVLO Hysteresis	Input Voltage Falling		100		mV
Standby Supply Current	V_{OUT} = 103%, Regulator Enabled		72	100	µA
Shutdown Current	V_{VP} = 5.5V, Regulator Disabled		0	2	µA
Output Voltage Accuracy	V_{OUT} ≥ 1.0V, I_{OUT} = 10mA	-1%	V_{NOM}①	1%	V
	V_{OUT} < 1.0V, I_{OUT} = 10mA	-10		10	mV
Line Regulation	V_{VP} = Max (V_{NOM}① +1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation REG1/4	I_{OUT} = 10mA to IMAX②		1.70		%/A
Load Regulation REG2/3	I_{OUT} = 10mA to IMAX②		1.00		%/A
Power Good Threshold	V_{OUT} Rising		93		%V_{NOM}
Power Good Hysteresis	V_{OUT} Falling		2		%V_{NOM}
Switching Frequency	V_{OUT} ≥ 20% of V_{NOM}	2	2.25	2.5	MHz
	V_{OUT} = 0V		550		kHz
Soft-Start Period			400		µs
Minimum On-Time			75		ns
REG1 AND REG4					
Maximum Output Current		1.5			A
Current Limit		1.8	2.2	2.7	A
PMOS On-Resistance	I_{SW} = -100mA		0.11		Ω
NMOS On-Resistance	I_{SW} = 100mA		0.08		Ω
SW Leakage Current	V_{VP} = 5.5V, V_{SW} = 0 or 5.5V		0	2	µA
Input Capacitor			4.7		µF
Output Capacitor			33		µF
Power Inductor		1.0	2.2	3.3	µH
REG2 AND REG3					
Maximum Output Current		2.8			A
Current Limit		3.5	4.2		A
PMOS On-Resistance	I_{SW} = -100mA		0.07		Ω
NMOS On-Resistance	I_{SW} = 100mA		0.08		Ω
SW Leakage Current	V_{VP} = 5.5V, V_{SW} = 0 or 5.5V		0	2	µA
Input Capacitor			10		µF
Output Capacitor			44		µF
Power Inductor		0.5	1	2.2	µH

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

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LOW-NOISE LDO ELECTRICAL CHARACTERISTICS

(V_{INL1} = V_{INL2} = 3.6V, C_{OUT5} = C_{OUT6} = C_{OUT7} = C_{OUT8} = C_{OUT9} = 2.2µF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.5		5.5	V
Output Voltage Accuracy	V_{OUT} ≥ 1.0V, I_{OUT} = 10mA	-1	V_{NOM}①	1	%
	V_{OUT} < 1.0V, I_{OUT} = 10mA	-10		10	mV
Line Regulation	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V		0.5		mV
Load Regulation	I_{OUT} = 1mA to IMAX②		0.1		V/A
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		75		dB
	f = 10kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		65		
Supply Current per Output	Regulator Enabled		25		µA
	Regulator Disabled		0	2	
Soft-Start Period	V_{OUT} = 3.0V		140		µs
Power Good Threshold	V_{OUT} Rising		92		%
Power Good Hysteresis	V_{OUT} Falling		3.5		%
Output Noise	I_{OUT} = 20mA, f = 10Hz to 100kHz, V_{OUT} = 1.2V		30		$µV_{RMS}$
Discharge Resistance	LDO Disabled, DIS[ ] = 1		1.5		kΩ
LDO rated at 150mA (REG5 & REG6)					
Dropout Voltage③	I_{OUT} = 80mA, V_{OUT} > 3.1V		140	280	mV
Maximum Output Current		150			mA
Current Limit④	V_{OUT} = 95% of regulation voltage	180			mA
Recommend Output Capacitor			2.2		µF
LDO rated at 350mA (REG7, REG8 & REG9)					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		140	280	mV
Maximum Output Current		350			mA
Current Limit④	V_{OUT} = 95% of regulation voltage	400			mA
Recommend Output Capacitor			2.2		µF

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher).

④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 50% (typ.)

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LOW-INPUT VOLTAGE LDO ELECTRICAL CHARACTERISTICS

(V_{INL3} = 3.6V, C_{OUT10} = C_{OUT11} = C_{OUT12} = 2.2μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		1.7		5.5	V
Output Voltage Accuracy	V_{OUT} ≥ 1.0V, I_{OUT} = 10mA	-1	V_{NOM}①	1	%
	V_{OUT} < 1.0V, I_{OUT} = 10mA	-10		10	mV
Line Regulation	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V		0.5		mV
Load Regulation	I_{OUT} = 1mA to IMAX②		0.1		V/A
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		50		dB
	f = 10kHz, I_{OUT} = 20mA, V_{OUT} = 1.2V		40		
Supply Current per Output	Regulator Enabled		22		μA
	Regulator Disabled		0	2	
Soft-Start Period	V_{OUT} = 3.0V		100		μs
Power Good Threshold	V_{OUT} Rising		92		%
Power Good Hysteresis	V_{OUT} Falling		3.5		%
Output Noise	I_{OUT} = 20mA, f = 10Hz to 100kHz, V_{OUT} = 1.2V		30		$μV_{RMS}$
Discharge Resistance	LDO Disabled, DIS[ ] = 1		1.5		kΩ
LDO rated at 150mA (REG10)					
Dropout Voltage③	I_{OUT} = 80mA, V_{OUT} > 3.1V		100	200	mV
Maximum Output Current		150			mA
Current Limit④	V_{OUT} = 95% of regulation voltage	180			mA
Recommend Output Capacitor			2.2		μF
LDO rated at 350mA (REG11 & REG12)					
Dropout Voltage③	I_{OUT} = 160mA, V_{OUT} > 3.1V		100	200	mV
Maximum Output Current		350			mA
Current Limit④	V_{OUT} = 95% of regulation voltage	400			mA
Recommend Output Capacitor			2.2		μF

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher).

④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage. Under heavy overload conditions the output current limit folds back by 50% (typ)

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LOW-POWER(ALWAYS-ON) LDO ELECTRICAL CHARACTERISTICS

(V_{INL1} = 3.6V, C_{OUT13} = 1μF, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REG13 — V_{NOM} = 1.8V					
Operating Voltage Range		2.5		5.5	V
Output Voltage Accuracy		-3	V_{NOM} ①	3	%
Line Regulation	V_{INL1} = Max (V_{OUT} + 0.2V, 2.5V) to 5.5V		13		mV
Supply Current from V_{INL1}			5		μA
Maximum Output current		50			mA
Recommend Output Capacitor		0.47			μF

PWM LED DRIVER ELECTRICAL CHARACTERISTICS

(V_{INL2} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Current	100% Duty Cycle	6	10	16	mA
Output Low Voltage	Feed in with 6mA			0.35	V
Leakage Current	Sinking from 5.5V source			1	μA
PWM Frequency	FRE[2:0] = 000		0.25		Hz
PWM Duty Adjustment	DUTY[3:0] = 0000 to 1111	6.26		100	%

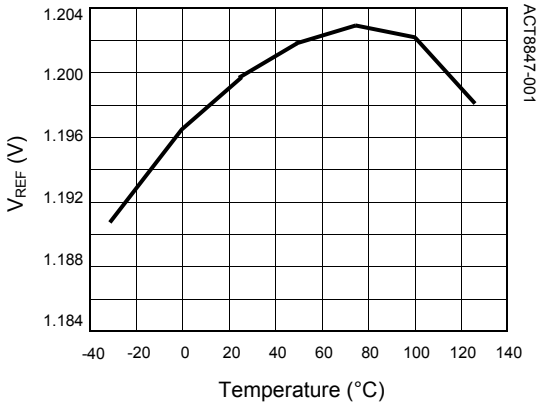
①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

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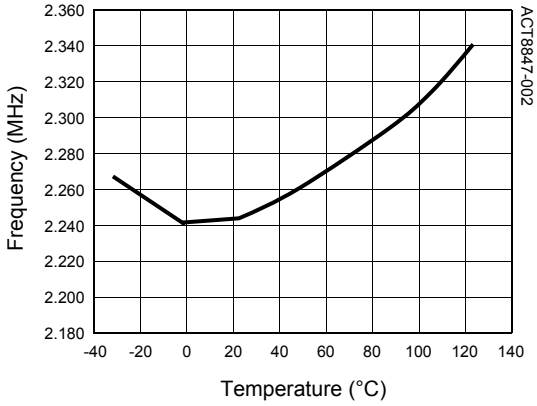
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, unless otherwise specified.)

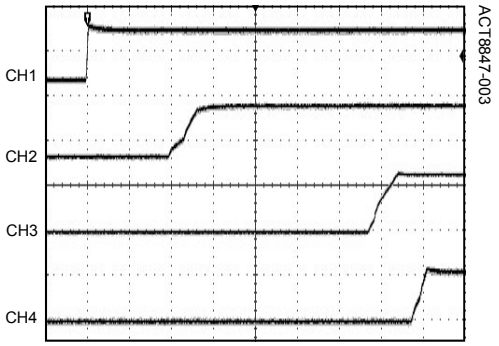
V_{REF} vs. Temperature



Frequency vs. Temperature

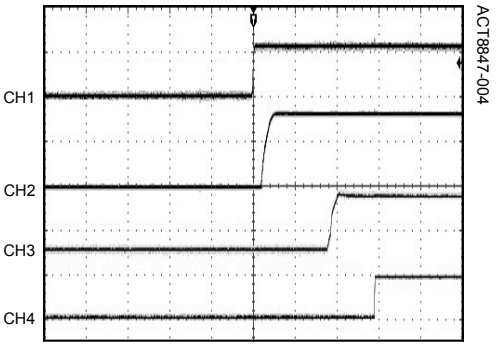


Startup of OUT6/4/2/3



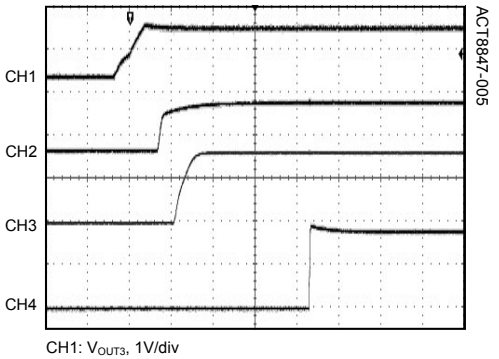
CH1: V_{OUT6}, 1V/div
CH2: V_{OUT4}, 1V/div
CH3: V_{OUT2}, 1V/div
CH4: V_{OUT3}, 1V/div
TIME: 400µs/div

Startup of OUT5/7/1/12



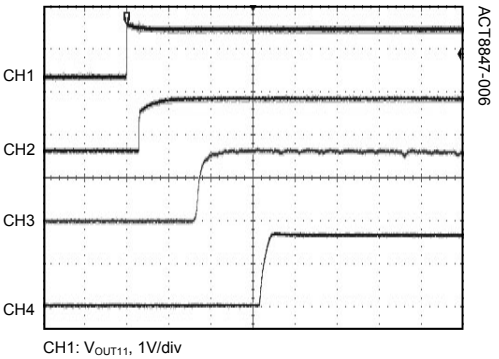
CH1: V_{OUT5}, 1V/div
CH2: V_{OUT7}, 2V/div
CH3: V_{OUT1}, 1V/div
CH4: V_{OUT12}, 2V/div
TIME: 400µs/div

Startup of OUT3/5/7/12



CH1: V_{OUT3}, 1V/div
CH2: V_{OUT5}, 1V/div
CH3: V_{OUT7}, 2V/div
CH4: V_{OUT12}, 1V/div
TIME: 200µs/div

Startup of OUT11/10/8/9



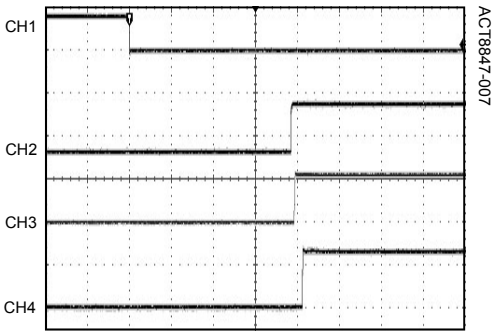
CH1: V_{OUT11}, 1V/div
CH2: V_{OUT10}, 1V/div
CH3: V_{OUT8}, 500mV/div
CH4: V_{OUT9}, 2V/div
TIME: 400µs/div

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TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

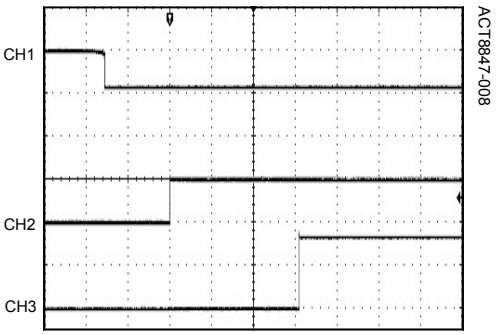
(T_A = 25°C, unless otherwise specified.)

Startup of nPBIN, OUT6/4/2



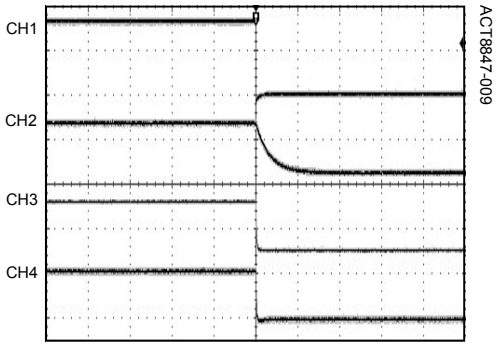
CH1: V_{nPBIN}, 2V/div
CH2: V_{OUT6}, 1V/div
CH3: V_{OUT4}, 1V/div
CH4: V_{OUT2}, 1V/div
TIME: 10ms/div

Startup of nPBIN, OUT6, nRSTO



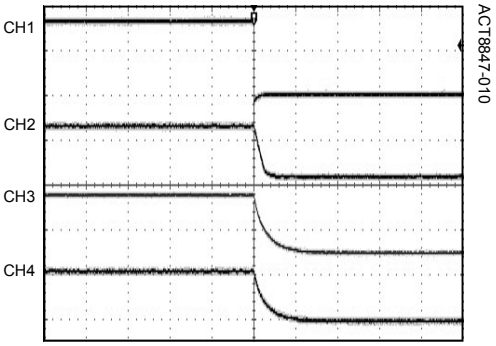
CH1: V_{nPBIN}, 2V/div
CH2: V_{OUT6}, 1V/div
CH3: V_{nRSTO}, 2V/div
TIME: 20ms/div

Sleep of PWREN, OUT3/5/11



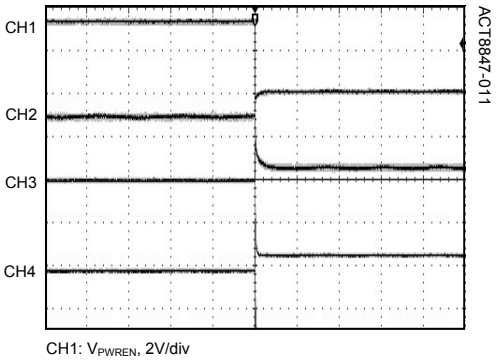
CH1: V_{PWREN}, 2V/div
CH2: V_{OUT3}, 1V/div
CH3: V_{OUT5}, 1V/div
CH3: V_{OUT11}, 1V/div
TIME: 1ms/div

Sleep of PWREN, OUT4/2/3



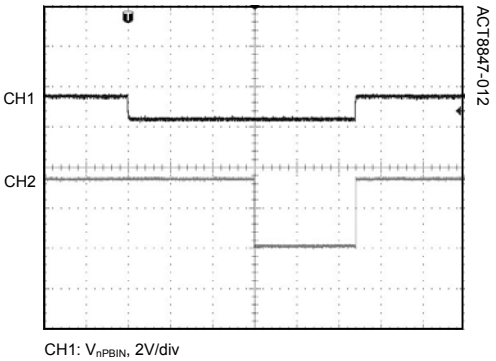
CH1: V_{PWREN}, 2V/div
CH2: V_{OUT4}, 1V/div
CH3: V_{OUT2}, 1V/div
CH3: V_{OUT3}, 1V/div
TIME: 1ms/div

Sleep of PWREN, OUT10/8/9



CH1: V_{PWREN}, 2V/div
CH2: V_{OUT10}, 1V/div
CH3: V_{OUT8}, 1V/div
CH3: V_{OUT9}, 2V/div
TIME: 1ms/div

nPBIN and nPBSTAT



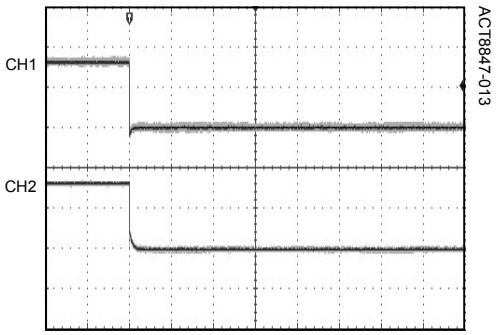
CH1: V_{nPBIN}, 2V/div
CH2: $V_{nPBSTAT}$, 2V/div
TIME: 10ms/div

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TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

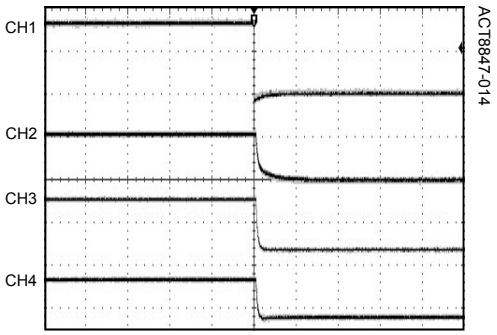
(T_A = 25°C, unless otherwise specified.)

Shutdown of PWRHOLD and nRSTO



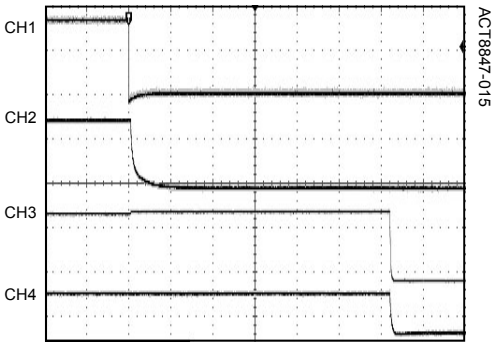
CH1: $V_{PWRHOLD}$, 2V/div
CH2: V_{nRSTO}, 2V/div
TIME: 2ms/div

Shutdown of PWRHOLD and OUT11/10/8



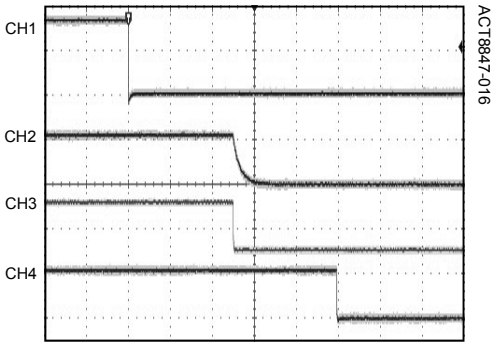
CH1: $V_{PWRHOLD}$, 2V/div
CH2: V_{OUT11}, 1V/div
CH3: V_{OUT10}, 1V/div
CH3: V_{OUT8}, 2V/div
TIME: 400µs/div

Shutdown of PWRHOLD and OUT9/7/12



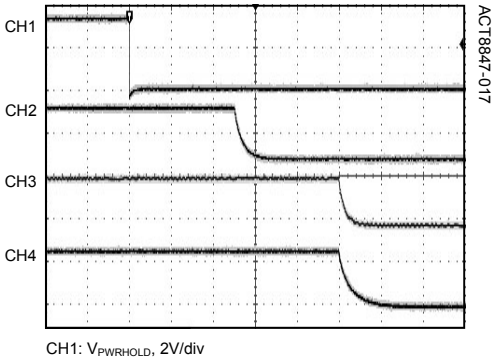
CH1: $V_{PWRHOLD}$, 2V/div
CH2: V_{OUT9}, 2V/div
CH3: V_{OUT7}, 2V/div
CH3: V_{OUT12}, 2V/div
TIME: 400µs/div

Shutdown of PWRHOLD and OUT3/5/6



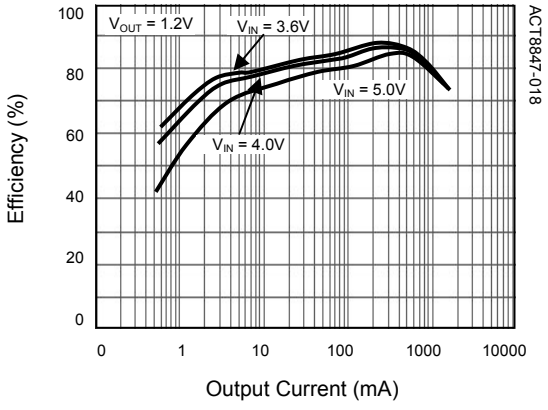
CH1: $V_{PWRHOLD}$, 2V/div
CH2: V_{OUT3}, 1V/div
CH3: V_{OUT5}, 1V/div
CH3: V_{OUT6}, 1V/div
TIME: 2ms/div

Shutdown of PWRHOLD and OUT1/4/2



CH1: $V_{PWRHOLD}$, 2V/div
CH2: V_{OUT1}, 1V/div
CH3: V_{OUT4}, 1V/div
CH3: V_{OUT2}, 1V/div
TIME: 1ms/div

REG1 Efficiency vs. Output Current

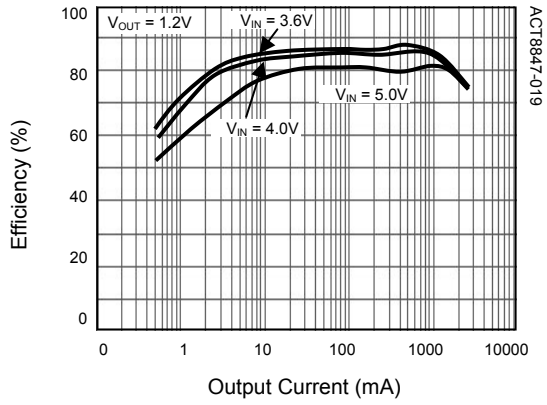


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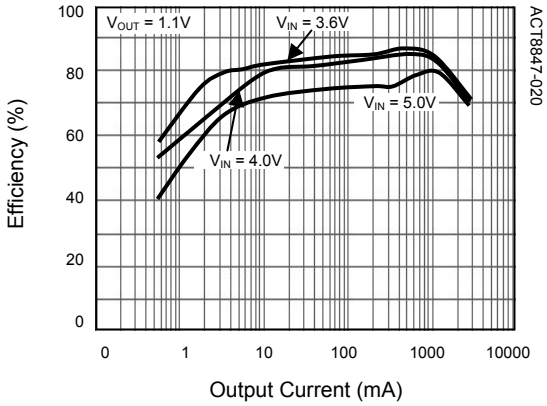
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

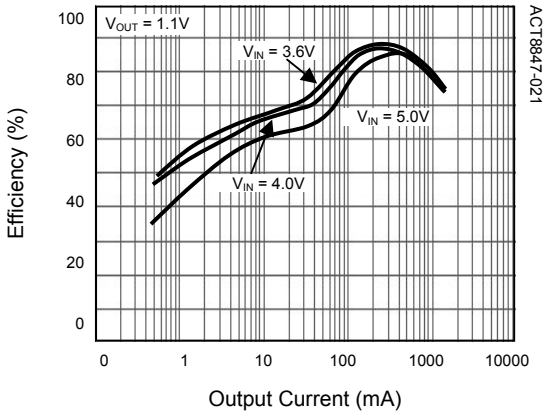
REG2 Efficiency vs. Output Current



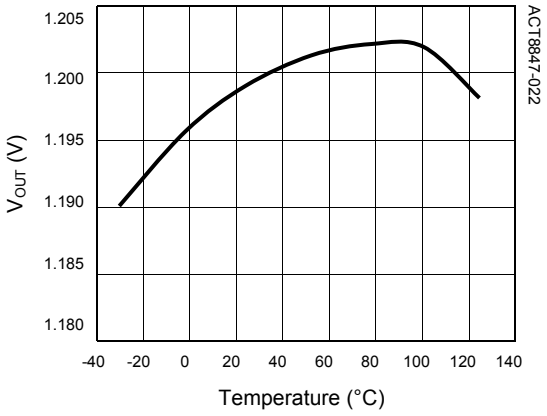
REG3 Efficiency vs. Output Current



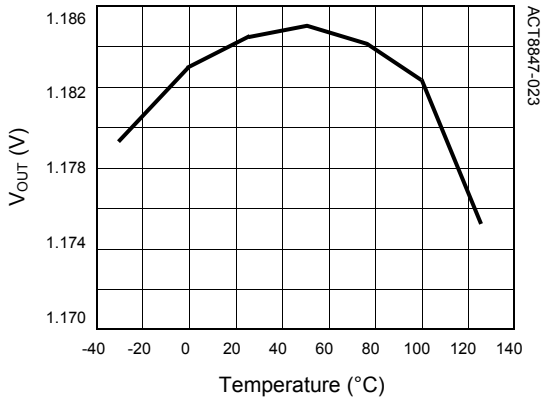
REG4 Efficiency vs. Output Current



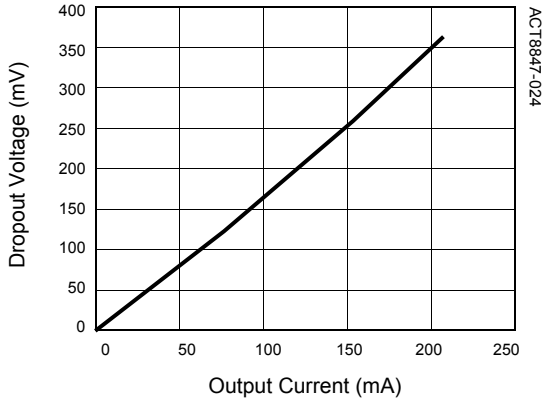
REG10 @ 10mA vs. Temperature



V_{OUT10} @ 150mA vs. Temperature



REG5/6 Dropout Voltage vs. I_{OUT}

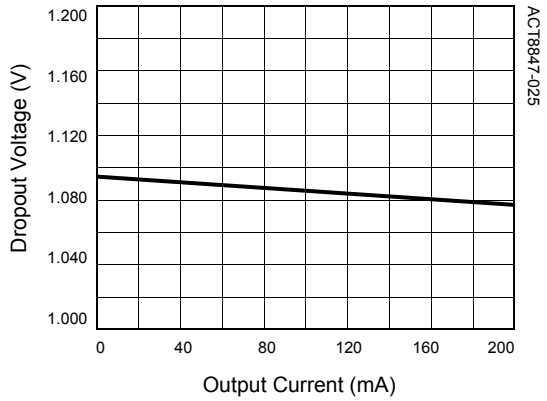


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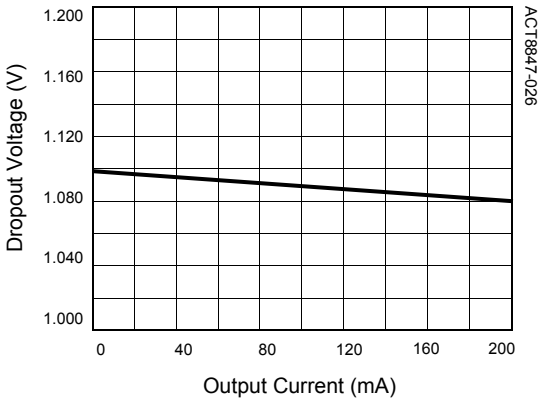
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

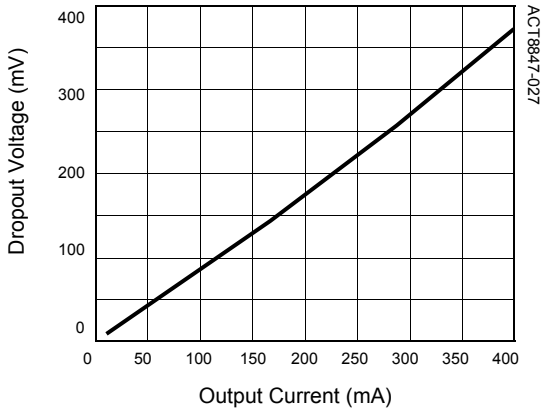
REG5 V_{OUT} vs. I_{OUT}



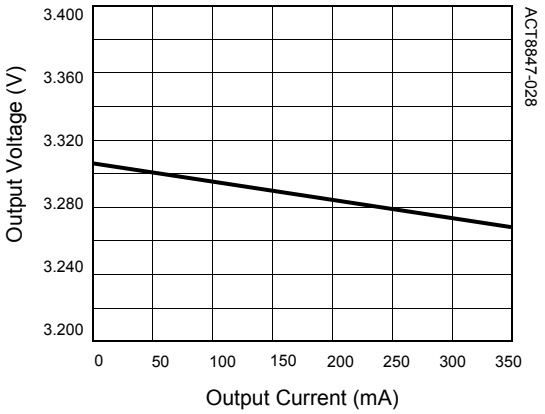
REG6 V_{OUT} vs. I_{OUT}



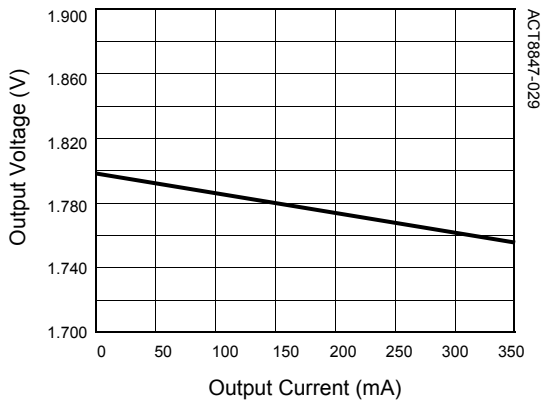
REG7/8/9 Dropout Voltage vs. I_{OUT}



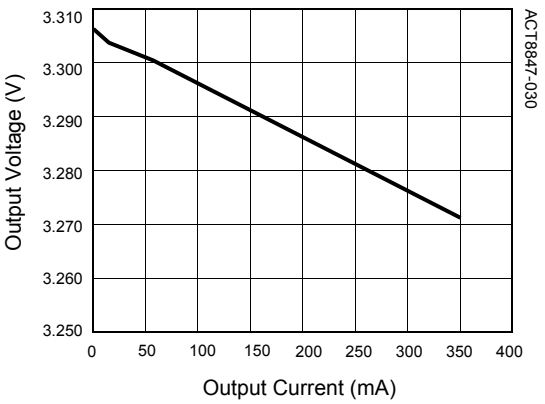
REG7 V_{OUT} vs. I_{OUT}



REG8 V_{OUT} vs. I_{OUT}



REG9 V_{OUT} vs. I_{OUT}

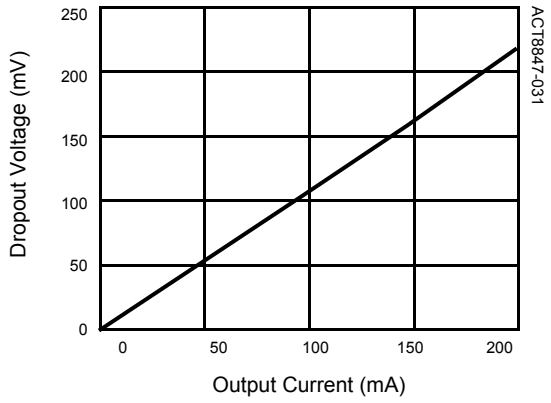


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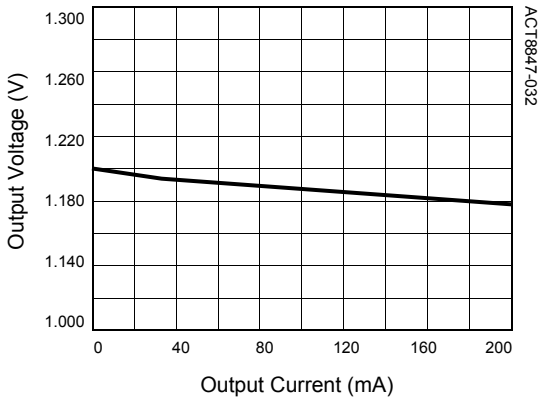
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

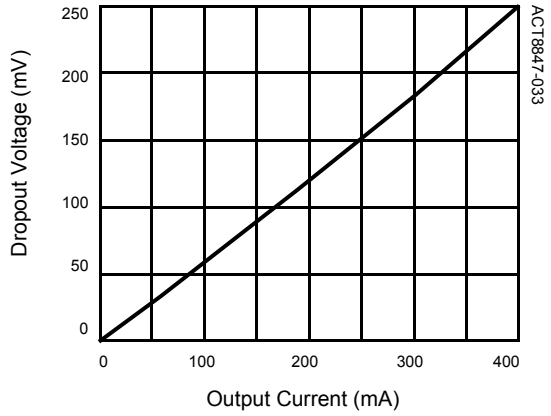
REG10 Dropout Voltage vs. I_{OUT}



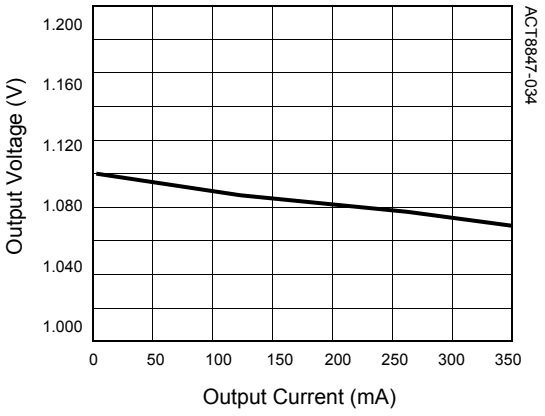
REG10 V_{OUT} vs. I_{OUT}



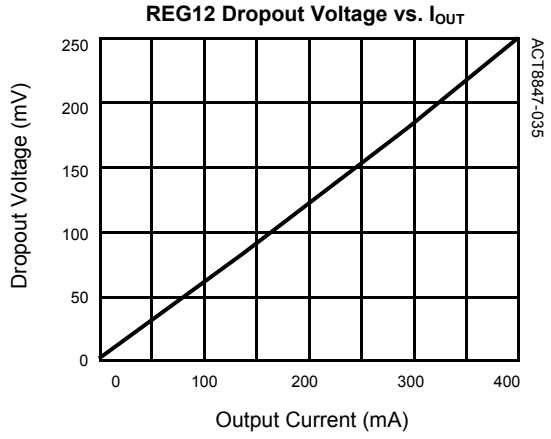
REG11 Dropout Voltage vs. I_{OUT}



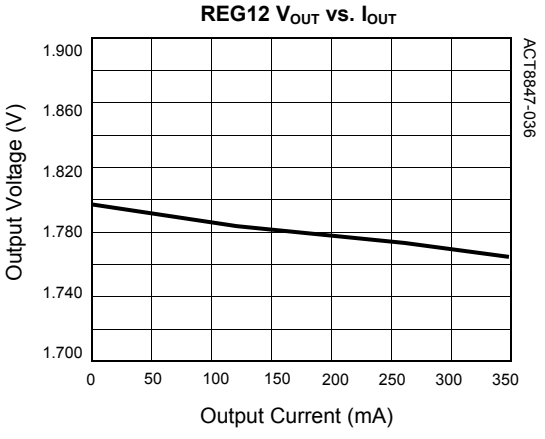
REG11 V_{OUT} vs. I_{OUT}



REG12 Dropout Voltage vs. I_{OUT}



REG12 V_{OUT} vs. I_{OUT}



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SYSTEM CONTROL INFORMATION

Interfacing with the Samsung S5PC210/S5PV310 processors

The ACT8847 is optimized for the Samsung S5PC210/S5PV310 and other application processors, supporting both the power domains as well as the signal interface. The following paragraphs describe how to design ACT8847 with the S5PC210/S5PV310 processors.

While the ACT8847 supports many possible configurations for powering these processors, one of the most common configurations is detailed in this datasheet. In general, this document refers to the ACT8847 pin names and functions. However, in cases where the description of interconnections between these devices benefits by doing so, both the ACT8847 pin names and the S5PC210/S5PV310 processors pin names are provided. When this is done, the S5PC210/S5PV310 pin names are located after the ACT8847 pin names, and are italicized and located inside parentheses. For example, PWREN (*XPWRRGTON*) refers to the logic signal applied to the ACT8847's PWREN input, identifying that it is driven from the S5PC210's XPWRRGTON output.

Table 1:

ACT8847 and Samsung S5PC210 Power Domains

ACT8847 REGULATOR	POWER DOMAIN	DEFAULT VOLTAGE	MAX CURRENT	POWER UP ORDER	ON/OFF @ SLEEP	TYPE
REG1	VDD_MEM, VDD12_SLP_ON	1.2V	1.5A	7	ON	DC/DC Step Down
REG2	VDD_ARM	1.2V	2.8A	3	OFF	DC/DC Step Down
REG3	VDD_G3D	1.1V	2.8A	4	OFF	DC/DC Step Down
REG4	VDD_INT	1.1V	1.5A	2	OFF	DC/DC Step Down
REG5	VDD_PLL	1.1V	150mA	5	OFF	Low-Noise LDO
REG6	VDD_ALIVE	1.1V	150mA	1	ON	Low-Noise LDO
REG7	VDD33_SLP_ON	3.3V	350mA	6	ON	Low-Noise LDO
REG8	VDD18_SLP_OFF	1.8V	350mA	11	OFF	Low-Noise LDO
REG9	VDD33_SLP_OFF	3.3V	350mA	12	OFF	Low-Noise LDO
REG10	VDD12_SLP_OFF	1.2V	150mA	10	OFF	Low Input-Voltage LDO
REG11	VDD11_SLP_OFF	1.1V	350mA	9	OFF	Low Input-Voltage LDO
REG12	VDD18_SLP_ON	1.8V	350mA	8	ON	Low Input-Voltage LDO
REG13	VDD_RTC	1.8V	50mA	0	ON	Always-ON LDO

Table 2:

ACT8847 and Samsung S5PC210 Power Mode

Power Mode	Control State	Power Domain State	Quiescent Current
ALL ON	PWRHLD is asserted, PWREN is asserted	All Regulators ON	0.6mA
SLEEP	PWRHLD is asserted, PWREN is de-asserted	REG1/6/7/12/13 are ON, all other regulators are off.	200µA
SHUTDOWN	PWRHLD is de-asserted, PWREN is de-asserted, VINL2 > 2.6V	REG13 is ON, all other regulators are off.	10µA
ALL OFF	PWRHLD is de-asserted, PWREN is de-asserted, VINL2 < 2.2V	All regulators off.	5µA

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Table 3:

ACT8847 and S5PC210 Signal Interface①

ACT8847	DIRECTION	SAMSUNG S5PC210
PWREN	←	XPWRRGTON
SCL	←	Xi2cSCL[0]
SDA	↔	Xi2cSDA[0]
VSELR2	←	DVS_GPIO1
GPIO1/VSELR3	←	DVS_GPIO2
GPIO2/VSELR4	←	DVS_GPIO3
nRSTO	→	XnRESET
nIRQ	→	XEINT0
nPBSTAT	→	XEINT1
PWRHLD	→	XPSHOLD

①: Typical connections shown, actual connections may vary.

Control Signals

Enable Inputs

The ACT8847 features a variety of control inputs, which are used to enable and disable outputs depending upon the desired mode of operation. PWREN, PWRHLD are logic inputs, while nPBIN is a unique, multi-function input.

nPBIN Multi-Function Input

The ACT8847 features the nPBIN multi-function pin, which combines system enable/disable control with a hardware reset function. Select either of the two pin functions by asserting this pin, either through a direct connection to GA, or through a 50kΩ resistor to GA, as shown in Figure 2.

Manual Reset Function

The second major function of the nPBIN input is to provide a manual-reset input for the processor. To manually-reset the processor, drive nPBIN directly to GA through a low impedance (less than 2.5kΩ). An internal timer detects the duration of the MR event:

Short Press / Soft-Reset:

If the MR is asserted for less than 4s, ACT8847 commences a soft-reset operation where nRSTO immediately asserts low, then remains asserted low until the nPBIN input is de-asserted and the reset time-out period expires. A status bit, SRSTAT[ ] , is set after a soft-reset event. The SRSTAT[ ] bit is automatically cleared to 0 after read. After Short Press, set WDSREN[ ] to 1 about 1s after nRSTO de-assert then clear WDSREN[ ] for properly shutdown sequence.

Long Press / Power-cycle:

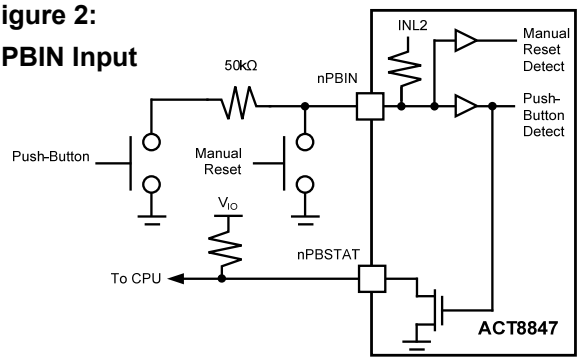
If the MR is asserted for more than 4s, ACT8847 commences a power cycle routine in which case all regulators are turned off and then turned back on. A status bit, PCSTAT[ ], is set after the power cycle. The PCSTAT[ ] bit is automatically cleared to 0 after read.

nPBSTAT Output

nPBSTAT is an open-drain output that reflects the state of the nPBIN input; nPBSTAT is asserted low whenever nPBIN is asserted, and is high-Z otherwise. This output is typically used as an interrupt signal to the processor, to initiate a software-programmable routine such as operating mode selection or to open a menu. Connect nPBSTAT to an appropriate supply voltage through a 10kΩ or greater resistor.

Figure 2:

nPBIN Input



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nRSTO Output

nRSTO is an open-drain output which asserts low upon startup or when manual reset is asserted via the nPBIN input. When asserted on startup, nRSTO remains low until reset time-out period expires. When asserted due to manual-reset, nRSTO immediately asserts low, then remains asserted low until the nPBIN input is de-asserted and the reset time-out period expires.

Connect a 10kΩ or greater pull-up resistor from nRSTO to an appropriate voltage supply.

nIRQ Output

nIRQ is an open-drain output that asserts low any time an interrupt is generated. Connect a 10kΩ or greater pull-up resistor from nIRQ to an appropriate voltage supply. nIRQ is typically used to drive the interrupt input of the system processor.

Many of the ACT8847's functions support interrupt-generation as a result of various conditions. These are typically masked by default, but may be unmasked via the I^2C interface. For more information about the available fault conditions, refer to the appropriate sections of this datasheet.

Push-Button Control

The ACT8847 is designed to initiate a system enable sequence when the nPBIN multi-function input is asserted. Once this occurs, a power-on sequence commences, as described below. The power-on sequence must complete and the microprocessor must take control (by asserting PWRHLD) before nPBIN is de-asserted. If the microprocessor is unable to complete its power-up routine successfully before the user releases the push-button, the ACT8847 automatically shuts the system down. This provides protection against accidental or momentary assertions of the push-button. If desired, longer “push-and-hold” times can be implemented by simply adding an additional time delay before asserting PWREN or PWRHLD.

Control Sequences

The ACT8847 features a variety of control sequences that are optimized for supporting system enable and disable, as well as SLEEP mode of the Samsung S5PC210 / S5PV310 processors.

Enabling/Disabling Sequence

A typical enable sequence is initiated whenever the nPBIN is asserted low via 50KΩ resistance. The power control diagram is shown in Figure 3. During the boot sequence, the microprocessor must assert PWRHLD (*XPSHOLD*), and PWREN *(XPWRRGTON)*, to ensure that the system remains powered after nPBIN is released. Once the power-up routine is completed, the system remains enabled after the push-button is released as long as PWRHLD is asserted high. If the processor does not assert PWRHLD before the user releases the push-button, the boot-up sequence is terminated and all regulators are disabled. This provides protection against "false-enable", when the push-button is accidentally depressed, and also ensures that the system remains enabled only if the processor successfully completes the boot-up sequence.

As with the enable sequence, a typical disable sequence is initiated when the user presses the push-button, which interrupts the processor via the nPBSTAT output. The actual disable sequence is completely software-controlled, but typically involved initiating various “clean-up” processes before the processor finally de-asserts PWRHLD.

SLEEP Mode Sequence

The ACT8847 supports S5PC210 / S5PV310 processors’ SLEEP mode operation. Once a successful power-up routine has been completed, SLEEP mode may be initiated through a variety of software-controlled mechanisms.

SLEEP mode is typically initiated when the user presses the push-button during normal operation. Pressing the push-button asserts the nPBIN input, which asserts the nPBSTAT output, which interrupts the processor. In response to this interrupt the processor should de-assert PWREN*(XPWRRGTON)*, disabling REG2/3/4/5/8/9/10/11. PWRHLD should remain asserted during SLEEP mode so that REG1/6/7/12 remain enabled.

The ACT8847 wakes up from SLEEP mode when either the push-button and/or PWREN *(XPWRRGTON)* is asserted. In either case, REG2/3/4/5/8/9/10/11 are enable which allow the system to resume normal operation.

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Watch-Dog Supervision

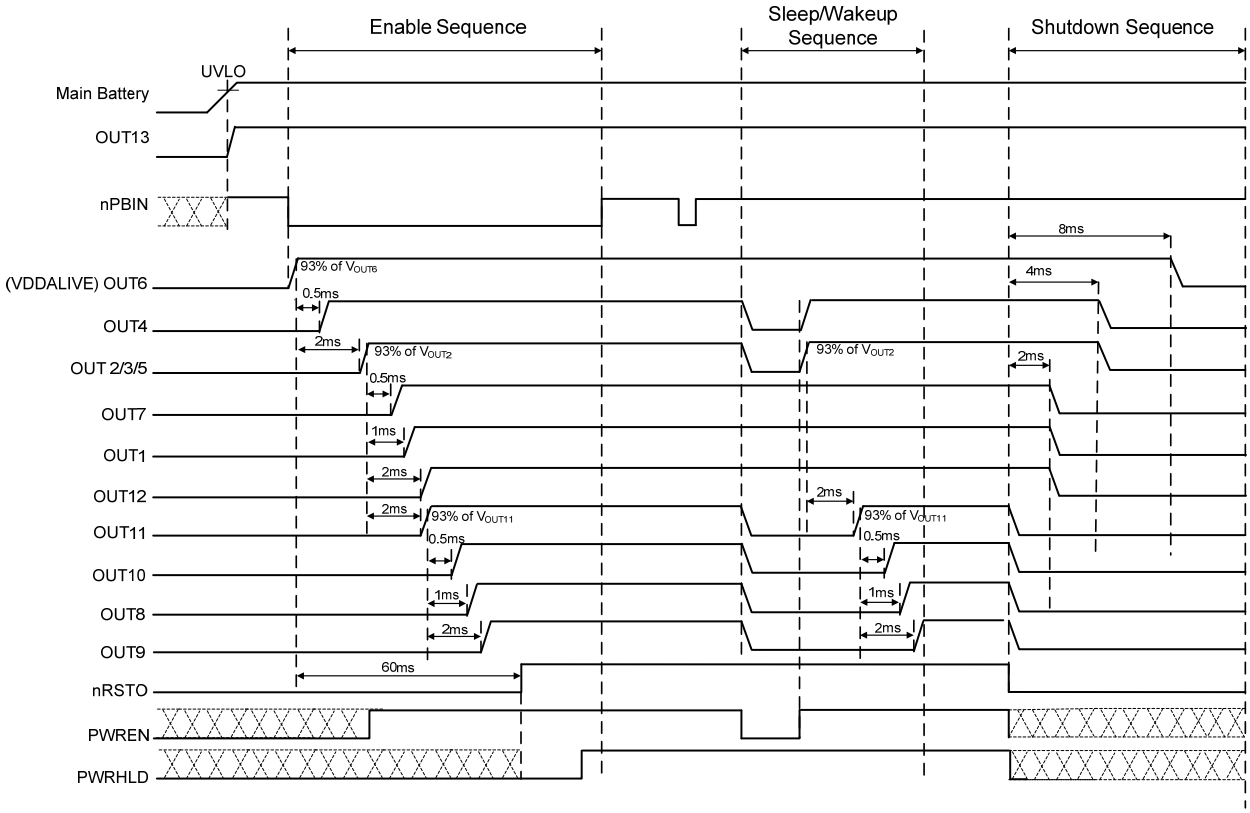
The ACT8847 features a watchdog supervisory function. An internal watchdog timer of 4s is unmasked by setting either WDSREN[ ] or WDPCEN [ ] bit to one. Once enabled, the watchdog timer is reset whenever there is I2C activity for the PMU. In the case where the system software stops responding and that there is no I2C transactions for 4s, the watchdog timer expires. As a result, the PMU either perform a soft-reset or power cycle, depending on whether WDSREN [ ] or WDPCEN [ ] is set.

Software-Initiated Power Cycle

ACT8847 supports software-initiated power cycle. Once the SIPC[ ] bit is set, the PMU waits for 8ms and then initiate a power cycle to restart the entire system.

Figure 3:

Power Control Sequence



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FUNCTIONAL DESCRIPTION

I²C Interface

The ACT8847 features an I²C interface that allows advanced programming capability to enhance overall system performance. To ensure compatibility with a wide range of system processors, the I²C interface supports clock speeds of up to 400kHz ("Fast-Mode" operation) and uses standard I²C commands. I²C write-byte commands are used to program the ACT8847, and I²C read-byte commands are used to read the ACT8847's internal registers. The ACT8847 always operates as a slave device, and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation, [1011010x].

SDA is a bi-directional data line and SCL is a clock input. The master device initiates a transaction by issuing a START condition, defined by SDA transitioning from high to low while SCL is high. Data is transferred in 8-bit packets, beginning with the MSB, and is clocked-in on the rising edge of SCL. Each packet of data is followed by an "Acknowledge" (ACK) bit, used to confirm that the data was transmitted successfully.

For more information regarding the I²C 2-wire serial interface, go to the NXP website: http://www.nxp.com.

Housekeeping Functions

Programmable battery Voltage Monitor

The ACT8847 features a programmable battery-voltage monitor, which monitors the voltage at INL2 (which should be connected directly to the battery) and compares it to a programmable threshold voltage. The VBATMON comparator is designed to be immune to noise resulting from switching, load transients, etc. The BATMON comparator is disable by default; to enable it, set the BATLEV[3:0] register to one of the value in Table 4. Note that there is a 200mV hysteresis between the rising and falling threshold for the comparator. The VBATDAT [ ] bit reflects the output of the BATMON comparator. The value of VBATDAT[ ] is 1 when V_{INL2} < BATLEV; value is 0 otherwise.

The VBATMON comparator can generate an interrupt when V_{INL2} is lower than BATLEV[ ] voltage. The interrupt is masked by default by can be unmasked by setting VBATMSK[ ] = 1.

Table 4:
BATLEV Falling Threshold

BATLEV[3:0]	BATLEV Falling Threshold
0000	2.5
0001	2.6
0010	2.7
0011	2.8
0100	2.9
0101	3.0
0110	3.1
0111	3.2
1000	3.3
1001	3.4
1010	3.5
1011	3.6
1100	3.7
1101	3.8
1110	3.9
1111	4.0

Thermal Protection

The ACT8847 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions.

Thermal Interrupt

If the thermal interrupt is unmasked (by setting nTMSK[ ] to 1), ACT8847 can generate an interrupt when the die temperature reaches 120°C (typ).

Thermal Protection

If the ACT8847 die temperature exceeds 160°C, the thermal protection circuitry disables all regulators and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ).

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STEP-DOWN DC/DC REGULATORS

General Description

REG1, REG2, REG3, and REG4 are fixed-frequency, current-mode, synchronous PWM step-down converters that achieves peak efficiencies of up to 97%. These regulators operate with a fixed frequency of 2.25MHz, minimizing noise in sensitive applications and allowing the use of small external components. Additionally, REG1, REG2, REG3, and REG4 are available with a variety of standard and custom output voltages, and may be software-controlled via the I^2C interface for systems that require advanced power management functions.

100% Duty Cycle Operation

REG1, REG2, REG3, and REG4 are capable of operating at up to 100% duty cycle. During 100% duty cycle operation, the high-side power MOSFETs are held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

Operating Mode

By default, REG1, REG2, REG3, and REG4 operate in fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving mode at light loads in order to save power.

Synchronous Rectification

REG1, REG2, REG3, and REG4 each feature integrated synchronous rectifiers, maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Soft-Start

REG1, REG2, REG3, and REG4 include internal 400 us soft-start ramps which limit the rate of change of the output voltage, minimizing input inrush current and ensuring that the output powers up in a monotonic manner that is independent of loading on the outputs. This circuitry is effective any time the regulator is enabled, as well as after responding to a short-circuit or other fault condition.

Compensation

REG1, REG2, REG3, and REG4 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guide lines described below when choosing external components.

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 10µF ceramic capacitor is recommended for each regulator in most applications.

Output Capacitor Selection

REG1, REG2, REG3, and REG4 were designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR. REG1, REG2, REG3 and REG4 are designed to operate with 33uF or 44uF output capacitor over most of their output voltage ranges, although more capacitance may be desired depending on the duty cycle and load step requirements.

Two of the most common dielectrics are Y5V and X5R. Whereas Y5V dielectrics are inexpensive and can provide high capacitance in small packages, their capacitance varies greatly over their voltage and temperature ranges and are not recommended for DC/DC applications. X5R and X7R dielectrics are more suitable for output capacitor applications, as their characteristics are more stable over their operating ranges, and are highly recommended.

Inductor Selection

REG1, REG2, REG3, and REG4 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. These devices were optimized for operation with 2.2µH or 1µH inductors. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%.

Configuration Options

Output Voltage Programming

By default, each regulator powers up and regulates to its default output voltage. For REG2, REG3 and REG4, the output voltage is selectable by setting corresponding VSEL pin that when VSEL is low, output voltage is programmed by VSET0[ ] bits, and when VSEL is high, output voltage is programmed by VSET1[ ] bits. Also, once the system is enabled, each regulator's output voltage may be independently programmed to a different value. Program the output voltages via the I^2C serial interface by writing to the regulator's VSET0[ ] register if VSEL is low or VSET1[ ] register if VSEL is high as shown in Table 5.

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Enable / Disable Control

During normal operation, each buck may be enabled or disabled via the I²C interface by writing to that regulator's ON[ ] bit.

OK[ ] and Output Fault Interrupt

Each DC/DC features a power-OK status bit that can be read by the system microprocessor via the I²C interface. If an output voltage is lower than the power-OK threshold, typically 7% below the programmed regulation voltage, that regulator's OK[ ] bit will be 0.

If a DC/DC's nFLTMSK[ ] bit is set to 1, the ACT8847 will interrupt the processor if that DC/DC's output voltage falls below the power-OK threshold. In this case, nIRQ will assert low and remain asserted until either the regulator is turned off or back in regulation, and the OK[ ] bit has been read via I²C.

PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors.

Step-down DC/DCs exhibit discontinuous input current, so the input capacitors should be placed as close as possible to the IC, and avoiding the use of via if possible. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple via. The output node for each regulator should be connected to its corresponding OUTx pin through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. Finally, the exposed pad should be directly connected to the backside ground plane using multiple via to achieve low electrical and thermal resistance.

Table 5:

REGx/VSET[ ] Output Voltage Setting

REGx/VSET[2:0]	REGx/VSET[5:3]							
	000	001	010	011	100	101	110	111
000	0.600	0.800	1.000	1.200	1.600	2.000	2.400	3.200
001	0.625	0.825	1.025	1.250	1.650	2.050	2.500	3.300
010	0.650	0.850	1.050	1.300	1.700	2.100	2.600	3.400
011	0.675	0.875	1.075	1.350	1.750	2.150	2.700	3.500
100	0.700	0.900	1.100	1.400	1.800	2.200	2.800	3.600
101	0.725	0.925	1.125	1.450	1.850	2.250	2.900	3.700
110	0.750	0.950	1.150	1.500	1.900	2.300	3.000	3.800
111	0.775	0.975	1.175	1.550	1.950	2.350	3.100	3.900

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LOW-NOISE, LOW-DROPOUT LINEAR REGULATORS

General Description

ACT8847 features eight low-noise, low-dropout linear regulators (LDOs) that supply up to 350mA. Three of these LDOs (REG10, REG11, and REG12) supports extended input voltage range down to 1.7V. Each LDO has been optimized to achieve low noise and high-PSRR.

Output Current Limit

Each LDO contains current-limit circuitry featuring a current-limit fold-back function. During normal and moderate overload conditions, the regulators can support more than their rated output currents. During extreme overload conditions, however, the current limit is reduced by approximately 30%, reducing power dissipation within the IC.

Compensation

The LDOs are internally compensated and require very little design effort, simply select input and output capacitors according to the guidelines below.

Input Capacitor Selection

Each LDO requires a small ceramic input capacitor to supply current to support fast transients at the input of the LDO. Bypassing each INL pin to GA with 1µF. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

Output Capacitor Selection

Each LDO requires a small 2.2µF ceramic output capacitor for stability . For best performance, each output capacitor should be connected directly between the output and GA pins, as close to the output as possible, and with a short, direct connection. High quality ceramic capacitors such as X7R and X5R dielectric types are strongly recommended.

Configuration Options

Output Voltage Programming

By default, each LDO powers up and regulates to its default output voltage. Once the system is enabled, each output voltage may be independently programmed to a different value by writing to the regulator's VSET[ ] register via the I^2C serial interface as shown in Table 5.

Enable / Disable Control

During normal operation, each LDO may be enabled or disabled via the I^2C interface by writing to that LDO's ON[ ] bit.

Output Discharge

Each of the LDOs features an optional output discharge function, which discharges the output to ground through a 1.5kΩ resistance when the LDO is disabled. This feature may be enabled or disabled by setting DIS[ ]; set DIS[ ] to 1 to enable this function, clear DIS[ ] to 0 to disable it.

OK[ ] and Output Fault Interrupt

Each LDO features a power-OK status bit that can be read by the system microprocessor via the interface. If an output voltage is lower than the power-OK threshold, typically 11% below the programmed regulation voltage, the value of that regulator's OK[ ] bit will be 0.

If a LDO's nFLTMSK[ ] bit is set to 1, the ACT8847 will interrupt the processor if that LDO's output voltage falls below the power-OK threshold. In this case, nIRQ will assert low and remain asserted until either the regulator is turned off or back in regulation, and the OK[ ] bit has been read via I^2C.

PCB Layout Considerations

The ACT8847's LDOs provide good DC, AC, and noise performance over a wide range of operating conditions, and are relatively insensitive to layout considerations. When designing a PCB, however, careful layout is necessary to prevent other circuitry from degrading LDO performance.

A good design places input and output capacitors as close to the LDO inputs and output as possible, and utilizes a star-ground configuration for all regulators to prevent noise-coupling through ground. Output traces should be routed to avoid close proximity to noisy nodes, particularly the SW nodes of the DC/DCs.

REFBP is a noise-filtered reference, and internally has a direct connection to the linear regulator controller. Any noise injected onto REFBP will directly affect the outputs of the linear regulators, and therefore special care should be taken to ensure that no noise is injected to the outputs via REFBP. As with the LDO output capacitors, the REFBP bypass capacitor should be placed as close to the IC as possible, with short, direct connections to the star-ground. Avoid the use of via whenever possible. Noisy nodes, such as from the DC/DCs, should be routed as far away from REFBP as possible.

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ALWAYS-ON LDO (REG13)

General Description

REG13 is an always-on, low-dropout linear regulator (LDO) that is optimized for RTC and backup-battery applications. REG13 features low-quiescent supply current, current-limit protection, and reverse-current protection, and is ideally suited for always-on power supply applications, such as for a real-time clock, or as a backup-battery or super-cap charger.

Reverse-Current Protection

REG13 features internal circuitry that limits the reverse supply current to less than 1μA when the input voltage falls below the output voltage, as can be encountered in backup-battery charging applications. REG13's internal circuitry monitors the input and the output, and disconnects internal circuitry and parasitic diodes when the input voltage falls below the output voltage, greatly minimizing backup battery discharge.

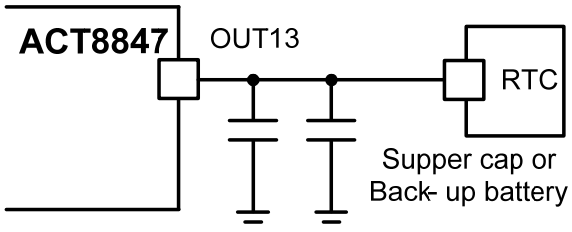
Typical Application

Voltage Regulators

REG13 is ideally suited for always-on voltage-regulation applications, such as for real-time clock and memory keep-alive applications. This regulator requires only a small ceramic capacitor with a minimum capacitance of 0.47μF for stability. For best performance, the output capacitor should be connected directly between the output and GA, with a short and direct connection.

Figure 4:

Typical Application of RTC LDO



Backup Battery Charging

REG13 features a constant current-limit, which protects the IC under output short-circuit conditions as well as provides a constant charge current, when operating as a backup battery charger.

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PWM LED DRIVERS

The GPIO3, the GPIO4, the GPIO5, and the GPIO6 are configured as PWM LED drivers, which could support up to 6mA current with programmable frequency and duty cycle. Set PWMxEN[ ] bit to "1" to enable PWM function of GPIOx.

PWM Frequence Selection

Each LED driver may be independently programmed to a different frequency by writing to the GPIO's FRE[2:0] register via the I^2C serial interface as shown in Table 6.

Table 6:

GPIOx/FRE[ ] PWM Frequency Setting

GPIOx/FRE[2:0]	PWM Frequency [Hz]
000	0.25
001	0.5
010	1
011	2
100	128
101	256

PWM Duty Cycle Selection

Each LED driver may be independently programmed to a different duty cycle by writing to the GPIO's DUTY[3:0] register via the I^2C serial interface as shown in Table 7.

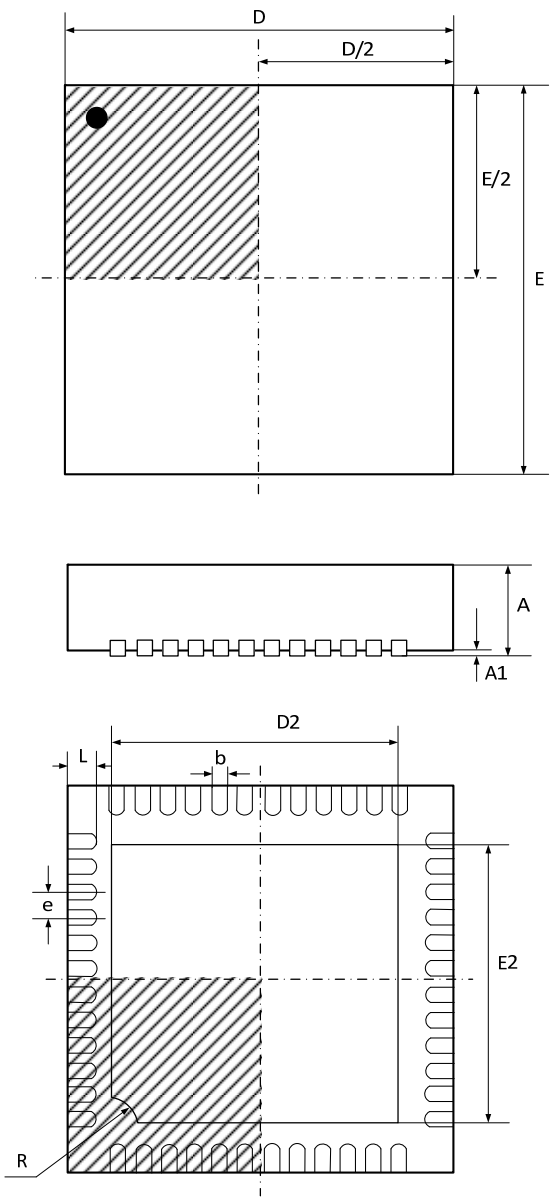
Table 7:

GPIOx/DUTY[ ] PWM Frequency Setting

GPIOx/DUTY[3:0]	PWM Duty Cycle [%]
0000	6.25
0001	12.5
0010	18.75
0011	25
0100	31.25
0101	37.5
0110	43.75
0111	50
1000	56.25
1001	62.5
1010	68.75
1011	75
1100	81.25
1101	87.5
1110	93.75
1111	100

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TQFN66-48 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.032	0.036
A1	0.200 REF		0.008 REF	
b	0.150	0.250	0.006	0.010
D	6.00		0.24	
E	6.00		0.24	
D2	4.15	4.40	0.166	0.176
E2	4.15	4.40	0.166	0.176
e	0.400 BSC		0.016 BSC	
L	0.300	0.500	0.012	0.020
R	0.300		0.012	

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