DATA SHEET

SAA5288
TV microcontroller with full screen On Screen Display (OSD)

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TV microcontroller with full screen On Screen Display (OSD)

SAA5288

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TV microcontroller with full screen On Screen Display (OSD)

SAA5288

1 FEATURES

1.1 General

- On-chip TV control tuning
- Hardware and software compatible with SAA5290, SAA5291 and SAA5296
- Single +5 V power supply
- RGB interface to standard decoder ICs, push-pull output drive
- SDIP52 package
- Single crystal oscillator for display and microcontroller.

1.2 Microcontroller

- 80C51 microcontroller core
- 16 kbyte mask programmed ROM
- 256 bytes of microcontroller RAM
- Eight 6-bit Pulse Width Modulator (PWM) outputs for control of TV analog signals
- One 14-bit PWM for Voltage Synthesis tuner control
- Four 8-bit Analog-to-Digital Converters (ADCs)
- 2 high current open-drain outputs for directly driving LED's etc.
- Switchable bit or byte-oriented I^2C-bus interface.

1.3 Display

- Single page (1024×8) on-board On Screen Display (OSD) memory
- Double size width and height capability for OSD
- Enhanced display features including meshing, shadowing and additional display attributes
- 260 characters in mask programmed ROM
- Display clock derived internally to reduce peripheral components to a minimum
- Automatic FRAME output control with manual override
- Standby mode for display hardware
- 525-line and 625-line display
- 12×10 character matrix
- Stable Display via slave synchronization to Horizontal Sync and Vertical Sync.

2 GENERAL DESCRIPTION

The SAA5288 is a microcontroller for use in televisions with an OSD generator compatible with the Economy Teletext/TV microcontroller family (SAA5290, SAA5291, SAA5296 etc.). TV control facilities are provided by an on-chip industry standard 80C51 microcontroller and a 1 kbyte DRAM is included for OSD memory.

Hardware and software compatibility with the Economy Teletext/TV microcontroller family minimizes the changes required to develop a TV control function for areas where teletext is not broadcast.

The device cannot acquire Teletext but is based on a Teletext device. Therefore, throughout this document references are made to Teletext especially when describing the Display/OSD section. The Display/OSD section is fully compatible with a Teletext display and has all the features associated with Teletext (i.e. double height/width, flash, teletext boxes, graphics, etc.). The Display section is described with reference to Teletext to allow software compatibility with the Economy Teletext/TV microcontroller family.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	4.5	5.0	5.5	V
I_{DDM}	microcontroller supply current	–	15	30	mA
I_{DDA}	analogue supply current	–	8	15	mA
I_{DDT}	display supply current	–	15	30	mA
f_{xtal}	crystal frequency	–	12	–	MHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA5288PS/nnn	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1

5 BLOCK DIAGRAM

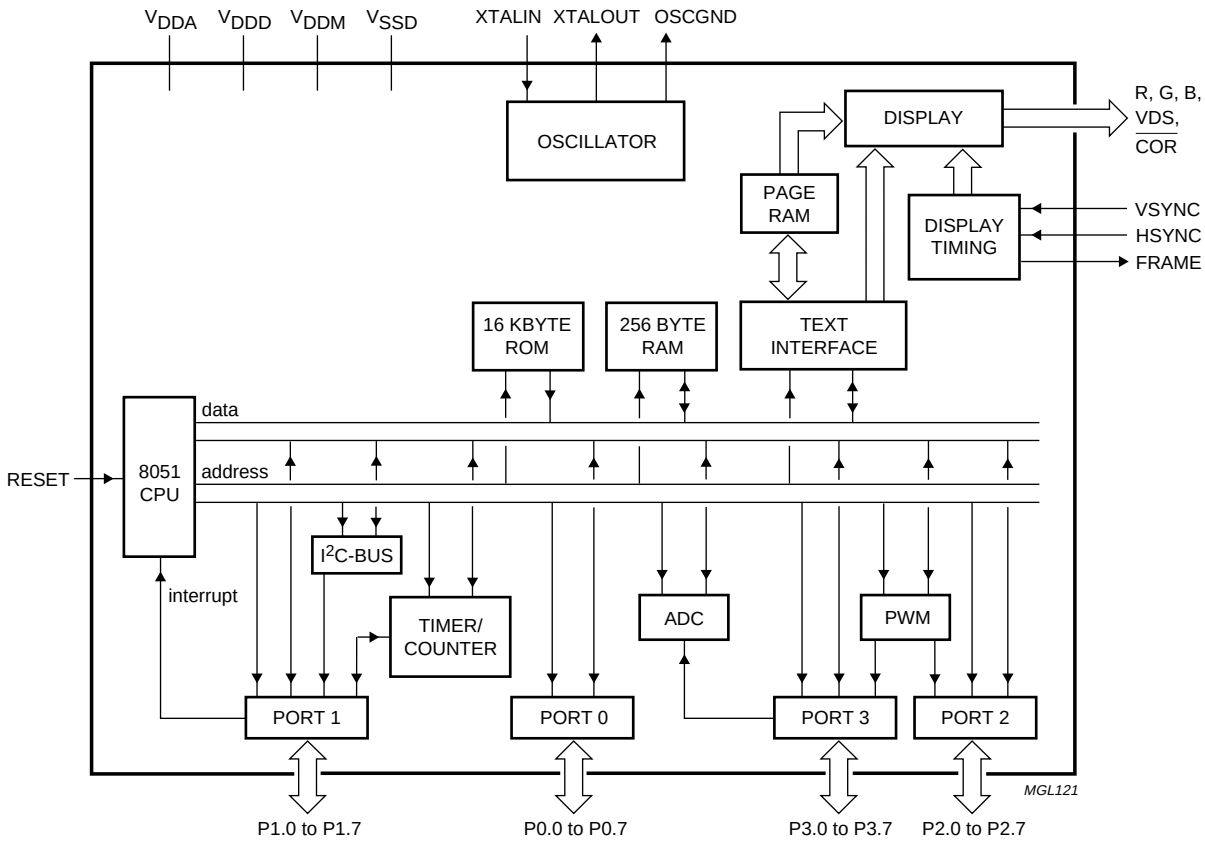


Fig.1 Block diagram.

6 PINNING INFORMATION

6.1 Pinning

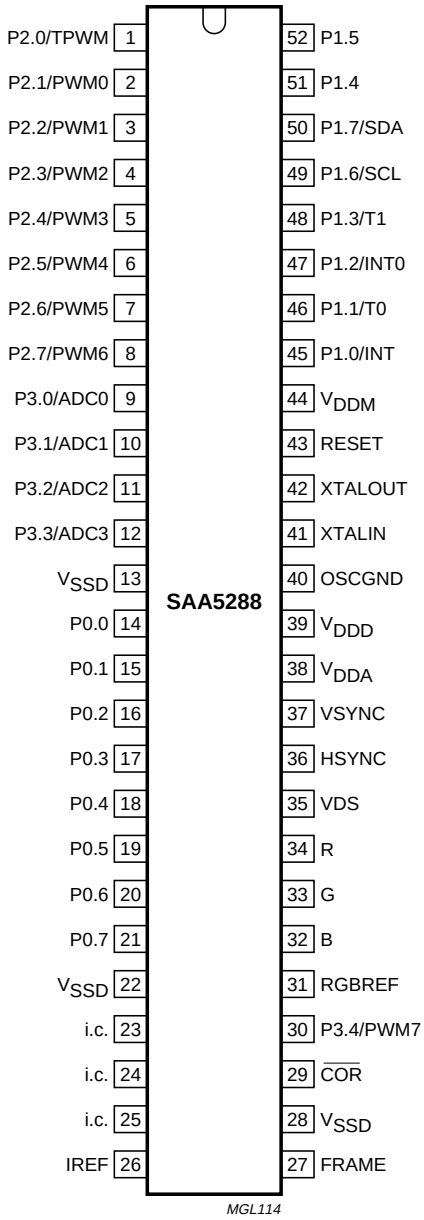


Fig.2 Pin configuration.

6.2 Pin description

Table 1 SDIP52 package

SYMBOL	PIN	DESCRIPTION
P2.0/TPWM	1	**Port 2.** 8-bit open-drain bidirectional port with alternative functions. P2.0/TPWM is the output for the 14-bit high precision PWM. P2.1/PWM0 to P2.7/PWM6 are the outputs for the 6-bit PWMs 0 to 6.
P2.1/PWM0	2	
P2.2/PWM1	3	
P2.3/PWM2	4	
P2.4/PWM3	5	
P2.5/PWM4	6	
P2.6/PWM5	7	
P2.7/PWM6	8	
P3.0/ADC0	9	**Port 3.** 8-bit open-drain bidirectional port with alternative functions. P3.0/ADC0 to P3.3/ADC3 are the inputs for the software ADC facility. P3.4/PWM7 is the output for the 6-bit PWM7.
P3.1/ADC1	10	
P3.2/ADC2	11	
P3.3/ADC3	12	
P3.4/PWM7	30	
V_{SSD}	13	Digital ground
P0.0	14	**Port 0.** 8-bit open-drain bidirectional port. P0.5 and P0.6 have 10 mA current sinking capability for direct drive of LEDs.
P0.1	15	
P0.2	16	
P0.3	17	
P0.4	18	
P0.5	19	
P0.6	20	
P0.7	21	
V_{SSD}	22	Digital ground.
i.c.	23	Internally connected; this pin should be connected to digital ground.
i.c.	24	Internally connected; this pin should be connected to digital ground.
i.c.	25	Internally connected; this pin should be connected to digital ground.
IREF	26	Reference current input for analog current generator, connected to V_{SSA} via a 27 kΩ resistor.

SYMBOL	PIN	DESCRIPTION
FRAME	27	De-interlace output synchronised with the VSYNC pulse to produce a non-interlaced display by adjustment of the vertical deflection circuits.
V_{SSD}	28	Internally connected; this pin should be connected to digital ground.
$\overline{COR}$	29	Open-drain, active LOW output which allows selective contrast reduction of the TV picture to enhance a mixed mode display.
RGBREF	31	DC input voltage to define the output HIGH level on the RGB pins.
B	32	Pixel rate output of the BLUE colour information.
G	33	Pixel rate output of the GREEN colour information.
R	34	Pixel rate output of the RED colour information.
VDS	35	Video/data switch push-pull output for dot rate fast blanking.
HSYNC	36	Schmitt trigger input for a TTL level version of the horizontal sync pulse; the polarity of this pulse is programmable by register bit TXT1.H POLARITY.
VSYNC	37	Schmitt trigger input for a TTL level version of the vertical sync pulse; the polarity of this pulse is programmable by register bit TXT1.V POLARITY.
V_{DDA}	38	+5 V display power supply.
V_{DDD}	39	+5 V display power supply.
OSCGND	40	Crystal oscillator ground.
XTALIN	41	12 MHz crystal oscillator input.
XTALOUT	42	12 MHz crystal oscillator output.
RESET	43	If the reset input is HIGH for at least 3 machine cycles (36 oscillator periods) while the oscillator is running, the device is reset; this pin should be connected to V_{DDM} via a 2.2 μF capacitor.
V_{DDM}	44	+5 V microcontroller power supply.
P1.0/INT1	45	**Port 1.** 8-bit open-drain bidirectional port with alternative functions. P1.0/INT1 is external interrupt 1, can be triggered on the rising/falling edge of pulse. P1.1/T0 is the counter/timer 0. P1.2/INT0 is the external interrupt 0. P1.3/T1 is the counter/timer 1. P1.7/SDA is the serial data port for the I^2C-bus. P1.6/SCL is the serial clock input for the I^2C-bus.
P1.1/T0	46	
P1.2/INT0	47	
P1.3/INT1	48	
P1.6/SCL	49	
P1.7/SDA	50	
P1.4	51	
P1.5	52	

7 FUNCTIONAL DESCRIPTION

7.1 Microcontroller

The functionality of the microcontroller used with this family is described with reference to the industry-standard 80C51 microcontroller. A full description of its functionality can be found in *"80C51-Based; 8-bit Microcontrollers, Data Handbook IC20"*. Using the 80C51 as a reference, the changes made to this family fall into two categories:

- Features not supported by the SAA5288
- Features found on the SAA5288 but not supported by the 80C51.

7.2 80C51 features not supported

7.2.1 Interrupt priority

The IP SFR is not implemented and all interrupts are treated with the same priority level. The normal priority of interrupts is maintained within the level.

Table 2 Interrupts and vector address

INTERRUPT SOURCE	VECTOR ADDRESS (HEX)
Reset	000
External INT0	003
Timer 0	00B
External INT1	013
Timer 1	01B
Byte I²C-bus	02B
Bit I²C-bus	053

7.2.2 Off-chip memory

The SAA5288 does not support the use of off-chip program memory or off-chip data memory.

7.2.3 Idle and Power-down modes

Idle and Power-down modes are not supported. Consequently, the respective bits in PCON are not available.

7.2.4 UART function

The 80C51 UART is not available. As a consequence the SCON and SBUF SFRs are removed and the ES bit in the IE SFR is unavailable.

7.3 Additional features

The following features are provided in addition to the standard 80C51 features.

7.3.1 Interrupts

The external INT1 interrupt is modified to generate an interrupt on both the rising and falling edges of the INT1 pin, when EX1 bit is set. This facility allows for software pulse-width measurement for handling of a remote control.

7.3.2 Bit Level I²C-bus Interface

For reasons of compatibility with the SAA5290, SAA5291, SAA5291A and SAA5491 all contain a bit level serial I/O which supports the I²C-bus. P1.6/SCL and P1.7/SDA are the serial I/O pins. These two pins meet the I²C-bus specification concerning the input levels and output drive capability see *"The I²C-bus and how to use it (including specifications)"*. Consequently, these two pins have an open-drain output configuration. All the four following modes of the I²C-bus are supported.

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

Three SFRs support the function of the bit-level I²C-bus hardware: S1INT, S1BIT and S1SCS and are enabled by setting register bit TXT8.I²C SELECT to logic 0.

7.3.3 Byte Level I²C-bus Interface

The byte level serial I/O supports the I²C-bus protocol. P1.6/SCL and P1.7/SDA are the serial I/O pins. These two pins meet the I²C-bus specification concerning the input levels and output drive capability. Consequently, these two pins have an open-drain output configuration.

The byte level I²C-bus serial port is identical to the I²C-bus serial port on the 8xC552. The operation of the subsystem is described in detail in the 8xC552 data sheet described in *"80C51-Based; 8-bit Microcontrollers Data Handbook IC20"*.

Four SFRs support the byte level I²C-bus hardware: S1CON, S1STA, S1DAT and S1ADR. They are enabled by setting register bit TXT8. I²C SELECT to logic 1.

7.3.4 LED support

Port pins P0.5 and P0.6 have a 10 mA current sinking capability to enable LEDs to be driven directly.

7.3.5 6-BIT PWM DACS

Eight 6-bit DACs are available to allow direct control of analogue sections of the television.

Each low resolution 6-bit DAC is controlled by its associated Special Function Register (PWM0 to PWM7). The PWM outputs are alternative functions of Port 2 and P3.4. The PWE bit in the SFR for the port corresponding to the PWM should be set to logic 1 for correct operation of the PWM, e.g. if PWM0 is to be used, P2.1 should be set to logic 1 setting the port pin to high-impedance.

7.3.5.1 Pulse Width Modulator Registers (PWM0 to PWM7)

Table 3 Pulse Width Modulator Registers (see Table 10 for addresses)

7	6	5	4	3	2	1	0
PWE	–	PV5	PV4	PV3	PV2	PV1	PV0

Table 4 Description of PWMn bits (n = 0 to 7)

BIT	SYMBOL	DESCRIPTION
7	PWE	If PWE is set to a logic 1, the corresponding PWM is active and controls its assigned port pin. If PWE is set to la logic 0, the port pin is controlled by the corresponding bit in the port SFR.
6	–	not used
5	PV5	The output of the PWM is a pulse of period 21.33 μs with a pulse HIGH time determined by the binary value of these 6-bits multiplied by 0.33 μs. PV5 is the most significant bit.
4	PV4	
3	PV3	
2	PV2	
1	PV1	
0	PV0	

7.3.6 14-BIT PWM DAC

One 14-bit DAC is available to allow direct control of analogue sections of the television. The 14-bit PWM is controlled using Special Function Registers TDACL and TDACH.

The output of the TPWM is a pulse of period 42.66 μs. The 7 most significant bits, TDACH.TD13 (MSB) to TDACH.TD8 and TDACL.TD7, alter the pulse width between 0 and 42.33 μs, in much the same way as in the 6-bit PWMs. The 7 least significant bits, TDACL.TD6 to TDACL.TD0 (LSB), extend certain pulses by a further 0.33 μs, e.g. if the 7 least significant bits are given the value 01H, then 1 in 128 cycles is extended. If the 7 least significant bits are given the value 02H, then 2 in 128 cycles is extended, and so forth.

The TPWM will not start to output a new value until after writing a value to TDACH. Therefore, if the value is to be changed, TDACL should be written to before TDACH.

7.3.6.1 TPWM High Byte Register (TDACH)

Table 5 TPWM High Byte Register (SFR address D3H)

7	6	5	4	3	2	1	0
PWE	–	TD13	TD12	TD11	TD10	TD9	TD8

Table 6 Description of TDACH bits

BIT	SYMBOL	DESCRIPTION
7	PWE	If PWE is set to a logic 1, the TPWM is active and controls port line P2.0. If PWE is set to a logic 0, the port pin is controlled by the corresponding bit in the port SFR.
6	–	not used
5	TD13	These 6-bits along with bit TD7 in the TDACL register control the pulse width period. TD13 is the most significant bit.
4	TD12	
3	TD11	
2	TD10	
1	TD9	
0	TD8	

7.3.6.2 TPWM Low Byte Register (TDACL)

Table 7 TPWM Low Byte Register (SFR address D2H)

7	6	5	4	3	2	1	0
TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

Table 8 Description of TDACL bits

BIT	SYMBOL	DESCRIPTION
7	TD7	This bit is used with bits TD13 to TD8 in the TDACH register to control the pulse width period.
6 to 0	TD6 to TD0	These 7-bits extend certain pulses by a further 0.33 μs.

7.3.7 SOFTWARE ADC

Up to 4 successive approximation ADCs can be implemented in software by making use of the on-chip 8-bit DAC and multiplexed voltage comparator. The software ADC uses 4 analog inputs which are multiplexed with P3.0 to P3.3.

Table 9 ADC input channel selection

CH1	CH0	INPUT PIN
0	0	P3.3/ADC3
0	1	P3.0/ADC0
1	0	P3.1/ADC1
1	1	P3.2/ADC2

The control of the ADC is achieved using the Special Function Registers SAD and SADB.

SAD.CH1 and SAD.CH0 select one of the four inputs to pass to the comparator. The other comparator input comes from the DAC, whose value is set by SAD.SAD7 (MSB) to SAD.SAD4 and SADB.SAD3 to SADB.SAD0 (LSB). The setting of the value SAD.SAD7 to SAD.SAD4 must be performed at least 1 instruction cycle before the setting of SAD.ST to ensure comparison is made using the correct SAD.SAD7 to SAD.SAD4 value.

The output of the comparator is SAD.VHI, and is valid after 1 instruction cycle following the setting of SAD.ST to logic 1.

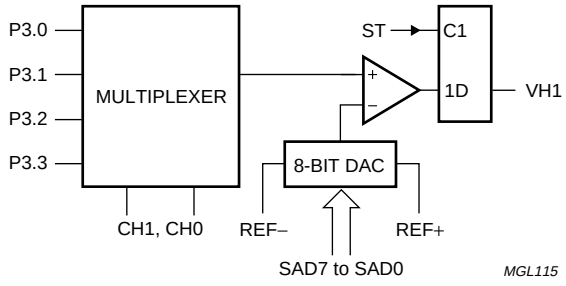


Fig.3 SAD block diagram.

7.4 Microcontroller Interfacing

The 80C51 communicates with the peripheral functions using Special Function Registers which are addressed as RAM locations. The registers in the teletext decoder appear as normal SFRs in the microcontroller memory map, but are written to using an internal serial bus. The SFR map is given in Section 7.4.1 and the SFR bit description is given in Section 7.4.2.

7.4.1 Special Function Register map

Table 10 Special Function Register map; note 1

SYMBOL	NAME	DIRECT ADDRESS (HEX)	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE (HEX)
			7	6	5	4	3	2	1	0	
ACC[2]	Accumulator	E0	E7	E6	E5	E4	E3	E2	E1	E0	00
			–	–	–	–	–	–	–	–	
B[2]	B register	F0	F7	F6	F5	F4	F3	F2	F1	F0	00
			–	–	–	–	–	–	–	–	
DPTR:	Data Pointer (2 bytes):										
DPH	High byte	83	–	–	–	–	–	–	–	–	00
DPL	Low byte	82	–	–	–	–	–	–	–	–	00
IE[2][3]	Interrupt Enable	A8	AF	AE	AD	AC	AB	AA	A9	A8	00
			EA	ES1	ES2	*	ET1	EX1	ET0	EX0	
P0[2]	Port 0	80	87	86	85	84	83	82	81	80	FF
			–	–	–	–	–	–	–	–	
P1[2]	Port 1	90	97	96	95	94	93	92	91	90	FF
			–	–	–	–	–	–	–	–	
P2[2]	Port 2	A0	A7	A6	A5	A4	A3	A2	A1	A0	FF
			–	–	–	–	–	–	–	–	
P3[2][3]	Port 3	B0	–	–	–	–	B3	B2	B1	B0	FF
			–	–	–	–	–	–	–	–	
PCON[3]	Power Control	87	–	*	–	*	GF1	GF0	–	–	10
PSW[2]	Program Status Word	D0	D7	D6	D5	D4	D3	D2	D1	D0	00
			CY	AC	F0	RS1	RS0	OV	*	P	

SYMBOL	NAME	DIRECT ADDRESS (HEX)	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE (HEX)
			7	6	5	4	3	2	1	0	
PWM0[3]	Pulse Width Modulator 0	D5	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM1[3]	Pulse Width Modulator 1	D6	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM2[3]	Pulse Width Modulator 2	D7	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM3[3]	Pulse Width Modulator 3	DC	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM4[3]	Pulse Width Modulator 4	DD	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM5[3]	Pulse Width Modulator 5	DE	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM6[3]	Pulse Width Modulator 6	DF	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
PWM7[3]	Pulse Width Modulator 7	D4	PWE	*	PV5	PV4	PV3	PV2	PV1	PV0	40
S1ADR[3]	Serial I²C-bus address	DB	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	GC	00
S1CON [2][3][4]	Serial I²C-bus control	D8	DF	DE	DD	DC	DB	DA	D9	D8	
			CR2	ENSI	STA	STO	SI	AA	CR1	CR0	00
S1SCS [2][3][5]	Serial I²C-bus control	D8	DF	DE	DD	DC	DB	DA	D9	D8	
			SDI	SCI	CLH	BB	RBF	WBF	STR	ENS	E0
S1DAT [3][4]	Serial I²C-bus data	DA	DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0	00
S1INT [3][5]	Serial I²C-bus Interrupt	DA	SI	–	–	–	–	–	–	–	7F
S1STA [3][4]	Serial I²C-bus status	D9	STAT4	STAT3	STAT2	STAT1	STAT0	0	0	0	F8
S1BIT [3][5]	Serial I²C-bus data	D9	SDO/SDI	–	–	–	–	–	–	–	7F

SYMBOL	NAME	DIRECT ADDRESS (HEX)	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE (HEX)
			7	6	5	4	3	2	1	0	
SAD[2][3]	Software ADC (MSB)	E8	EF	EE	ED	EC	EB	EA	E9	E8	00
			VHI	CH1	CH0	ST	SAD7	SAD6	SAD5	SAD4	
SADB [2][3]	Software ADC (LSB)	98	9F	9E	9D	9C	9B	9A	99	98	00
			–	–	–	–	SAD3	SAD2	SAD1	SAD0	
SP	Stack Pointer	81	8F	8E	8D	8C	8B	8A	89	88	07
TCON[2]	Timer/counter control	88	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00
TDACH	TPWM High byte	D3	PWE	*	TD13	TD12	TD11	TD10	TD9	TD8	40
TDACL	TPWM Low byte	D2	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	00
TH0	Timer 0 High byte	8C	TH07	TH06	TH05	TH04	TH03	TH02	TH01	TH00	00
TH1	Timer 1 High byte	8D	TH17	TH16	TH15	TH14	TH13	TH12	TH11	TH10	00
TL0	Timer 0 Low byte	8A	TL07	TL06	TL05	TL04	TL03	TL02	TL01	TL00	00
TL1	Timer 1 Low byte	8B	TL17	TL16	TL15	TL14	TL13	TL12	TL11	TL10	00
TMOD	Timer/counter mode	89	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00
			Timer 1				Timer 0				
TXT0[3]	Teletext Register 0	C0	*	*	AUTO FRAME	*	DISPLAY STATUS ROW ONLY	DISABLE FRAME	*	*	00
TXT1[3]	Teletext Register 1	C1	*	*	*	*	*	FIELD POLARITY	H POLARITY	V POLARITY	00
TXT4[3]	Teletext Register 4	C4	*	*	EAST/$\overline{\text{WEST}}$	DISABLE DBL HT	B MESH ENABLE	C MESH ENABLE	TRANS ENABLE	SHADOW ENABLE	00
TXT5[3]	Teletext Register 5	C5	BKGND OUT	BKGND IN	$\overline{\text{COR}}$ OUT	$\overline{\text{COR}}$ IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN	03

SYMBOL	NAME	DIRECT ADDRESS (HEX)	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE (HEX)
			7	6	5	4	3	2	1	0	
TXT6(3)	Teletext Register 6	C6	BKGND OUT	BKGND IN	$\overline{\text{COR}}$ OUT	$\overline{\text{COR}}$ IN	TEXT OUT	TEXT IN	PICTURE ON OUT	PICTURE ON IN	03
TXT7(3)	Teletext Register 7	C7	STATUS ROW TOP	CURSOR ON	REVEAL	$\overline{\text{TOP}}$/ BOTTOM	DOUBLE HEIGHT	BOX ON 24	BOX ON 1–23	BOX ON 0	00
TXT8(3)	Teletext Register 8	C8	I^2C SELECT	*	*	*	*	*	*	*	00
TXT9(3)	Teletext Register 9	C9	CURSOR FREEZE	CLEAR MEMORY	*	R4	R3	R2	R1	R0	00
TXT10(3)	Teletext Register 10	CA	*	*	C5	C4	C3	C2	C1	C0	00
TXT11(3)	Teletext Register 11	CB	D7	D6	D5	D4	D3	D2	D1	D0	00
TXT12(3)	Teletext Register 12	CC	$\overline{*}$	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TXT ON	*	0XXXX X00B
TXT13 (2)(3)	Teletext Register 13	B8	BF	BE	BD	BC	BB	BA	B9	B8	00
			*	PAGE CLEARING	525 DISPLAY	*	*	*	*	OSD I/F busy	
TXT16(3)	Teletext Register 16	CF	*	Y2	Y1	Y0	*	*	X1	X0	00
TXT17(3)	Teletext Register 17	B9	*	*	*	FORCE 625	FORCE 525	SCREEN COL2	SCREEN COL1	SCREEN COL0	00

Notes

1. The asterisk (*) indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. SFRs are bit addressable.
3. SFRs are modified or added to the 80C51 SFRs.
4. This register is used for Byte Orientated I^2C-bus, TXT8. I^2C SELECT = 1.
5. This register is used for Bit Orientated I^2C-bus, TXT8. I^2C SELECT = 0.

7.4.2 Special Function Registers bit description

Table 11 SFR bit descriptions

REGISTER	FUNCTION
Interrupt Enable Register (IE)	
EA	disable all interrupts (logic 0) or use individual interrupt enable bits (logic 1)
ES1	bit I^2C-bus interrupt enable (logic 1)
ES2	byte I^2C-bus interrupt enable (logic 1)
ET1	enable Timer 1 overflow interrupt (logic 1)
EX1	enable external interrupt 1 (logic 1)
ET0	enable Timer 0 overflow interrupt (logic 1)
EX0	enable external interrupt 0 (logic 1)
Power Control Register (PCON)	
GF1	general purpose flag 1
GF0	general purpose flag 0
Program Status Word (PSW)	
CY	carry flag
AC	auxiliary carry flag
F0	flag 0
RS1, RS0	register bank select control bits
OV	overflow flag
P	parity flag
6-bit Pulse Width Modulator Control Registers (PWM0 to PWM7)	
PWE	activate this PWM and take control of respective port pin (logic 1)
PV5 to PV0	binary value sets high time of PWM output
Serial Interface Slave Address Register (S1ADR)	
ADR6 to ADR0	I^2C-bus slave address to which the device will respond
GC	enables response to the I^2C-bus general call address
Serial Interface Control Register (S1CON)	
CR2 to CR0	clock rate bits
ENSI	I^2C-bus interface enable
STA	start condition flag
STO	stop condition flag
SI	interrupt flag
AA	assert acknowledge flag

REGISTER	FUNCTION
Serial Interface Data Register (S1DAT)	
DAT7 to DAT0	I^2C-bus data
Serial Interface Status Register (S1STA) - READ only	
STAT4 to STAT0	I^2C-bus interface status
Serial Interface Data Register (S1BIT) - READ	
SDI	I^2C-bus data bit input
Serial Interface Data Register (S1BIT) - WRITE	
SDO	I^2C-bus data bit output
Serial Interface Interrupt Register (S1INT)	
SI	I^2C-bus interrupt flag
Serial Interface Control Register (S1SCS) - READ	
SDI	serial data input at SDA
SCI	serial clock input at SCL
CLH	clock LOW-to-HIGH transition flag
BB	bus busy flag
RBF	read bit finished flag
WBF	write bit finished flag
STR	clock stretching enable (logic 1)
ENS	enable serial I/O (logic 1)
Serial Interface Control Register (S1SCS) - WRITE	
SDO	serial data output at SDA
SCO	serial clock output at SCL
CLH	clock LOW-to-HIGH transition flag
STR	clock stretching enable (logic 1)
ENS	enable serial I/O (logic 1)
Software ADC Control Register (SAD)	
VHI	comparator output indicating that analogue input voltage greater than DAC voltage (logic 1)
CH1 and CH0	ADC input channel selection bits, see Table 11
ST	initiate voltage comparison (logic 1); this bit is automatically reset to logic 0
SAD7 to SAD4	4 MSB’s of DAC input value
Software ADC Control Register (SADB)	
SAD3 to SAD0	4 LSB’s of DAC input value

REGISTER	FUNCTION
Timer/Counter Control Register (TCON)	
TF1	Timer 1 overflow flag
TR1	Timer 1 run control bit
TF0	Timer 0 overflow flag
TR0	Timer 0 run control bit
IE1	Interrupt 1 edge flag
IT1	Interrupt 1 type control bit
IE0	Interrupt 0 edge flag
IT0	Interrupt 0 type control bit
14-bit PWM MSB Register (TDACH)	
PWE	activate this 14-bit PWM and take over port pin (logic 1)
TD13 to TD8	6 MSBs of 14-bit number to be output by the 14-bit PWM
14-bit PWM LSB Register (TDACL)	
TD7 to TD0	8 LSBs of 14-bit number to be output by the 14-bit PWM
Timer 0 High byte (TH0)	
TH07 to TH00	8 MSBs of Timer 0 16-bit counter
Timer 1 High byte (TH1)	
TH17 to TH10	8 MSBs of Timer 1 16-bit counter
Timer 0 Low byte (TL0)	
TL07 to TL00	8 LSBs of Timer 0 16-bit counter
Timer 1 Low byte (TL1)	
TL17 to TL10	8 LSBs of Timer 1 16-bit counter
Timer/Counter Mode Control Register (TMOD)	
GATE	gating control
C/$\overline{T}$	counter or timer selector
M1, M0	mode control bits
Teletext Register 0 (TXT0) - WRITE only	
AUTO FRAME	FRAME output switched off automatically if any video displayed (logic 1)
DISPLAY STATUS ROW ONLY	display row 24 only (logic 1)
DISABLE FRAME	FRAME output always low (logic 1)

REGISTER	FUNCTION
Teletext Register 1 (TXT1) - WRITE only	
FIELD POLARITY	VSYNC in first half of the line (logic 0) or second half of the line (logic 1) at start of even field
H POLARITY	HSYNC input positive-going (logic 0) or negative-going (logic 1)
V POLARITY	VSYNC input positive-going (logic 0) or negative-going (logic 1)
PRD4 to PRD0	page request data
Teletext Register 4 (TXT4) - WRITE only	
EAST/ $\overline{\text{WEST}}$	western languages selected (logic 0) or Eastern languages selected (logic 1)
DISABLE DBL HGHT	disable display of double height teletext control codes (logic 1) in OSD boxes
B MESH ENABLE	enable meshing of area with black background (logic 1)
C MESH ENABLE	enable meshing of area with other background colours (logic 1)
TRANS ENABLE	set black background to transparent i.e. video is displayed (logic 1)
SHADOW ENABLE	enable south-east shadowing (logic 1)
Teletext Register 5 (TXT5) - WRITE only	
BKGND OUT	background colour displayed outside teletext boxes (logic 1)
BKGND IN	background colour displayed inside teletext boxes (logic 1)
$\overline{\text{COR}}$ OUT	COR output active outside teletext boxes (logic 1)
$\overline{\text{COR}}$ IN	COR output active inside teletext boxes (logic 1)
TEXT OUT	text displayed outside teletext boxes (logic 1)
TEXT IN	text displayed inside teletext boxes (logic 1)
PICTURE ON OUT	video picture displayed outside teletext boxes (logic 1)
PICTURE ON IN	video picture displayed inside teletext boxes (logic 1)
Teletext Register 6 (TXT6) - WRITE only	
See TXT5	this register has the same meaning as TXT5 but is only invoked if either newsflash (C5) or subtitle (C6) bit in row 25 of the basic page memory is set
Teletext Register 7 (TXT7) - WRITE only	
STATUS ROW TOP	display row 24 below (logic 0) or above (logic 1) teletext page
CURSOR ON	display cursor at location pointed to by TXT9 and TXT10 (logic 1)
REVEAL	display characters in areas with the conceal attribute set (logic 1)
$\overline{\text{TOP}}$/BOTTOM	display rows 0 to 11 (logic 0) or 12 to 23 (logic 1) when the double height bit is set
DOUBLE HEIGHT	display each character as twice normal height (logic 1)
BOX ON 24	enable teletext boxes in memory row 24 (logic 1)
BOX ON 1-23	enable teletext boxes in memory rows 1 to 23 (logic 1)
BOX ON 0	enable teletext boxes in memory row 0 (logic 1)

REGISTER	FUNCTION
Teletext Register 8 (TXT8)	
I^2C SELECT	select bit I^2C-bus (logic 0) or byte I^2C-bus (logic 1)
Teletext Register 9 (TXT9) - WRITE only	
CURSOR FREEZE	locks current cursor position (logic 1)
CLEAR MEMORY	write 20H into every location in display memory (logic 1)
R4 to R0	memory row to be accessed by TXT11
Teletext Register 10 (TXT10) - WRITE only	
C5 to C0	memory column to be accessed by TXT11
Teletext Register 11 (TXT11)	
D7 to D0	data byte written to, or read from display memory
Teletext Register 12 (TXT12) - READ only	
ROM VER R4 to R0	mask programmable identification for character set
DISPLAY ON	power has been applied to the display hardware (logic 1)
Teletext Register 13 (TXT13)	
PAGE CLEARING	set when software requested page clear in progress
525 DISPLAY	set to logic 1 when 525-line syncs are driving the display
OSD I/F Busy	OSD interface busy; logic 1 indicates that TXT Registers 0 to 16 can not currently be accessed
Teletext Register 16 (TXT16) - WRITE only	
Y2 to Y0	sets vertical position of display area
X1 to X0	sets horizontal position of display area
Teletext Register 17 (TXT17) - Write only	
FORCE 625	force display to 625-line mode
FORCE 525	force display to 525-line mode
SCREEN COL 2 to 0	defines colour displayed instead of TV picture and black background

7.5 The display

7.5.1 Introduction

The capabilities of the display are based on the requirements of level 1 teletext, with some enhancements for use with locally generated on screen displays.

The display consists of 25 rows each of 40 characters, with the characters displayed being those from rows 0 to 24 of the basic page memory. If the TXT.7 STATUS ROW TOP bit is set row 24 is displayed at the top of the screen, followed by row 0, but normally memory rows are displayed in numerical order.

The display memory stores 8-bit character codes which correspond to a number of displayable characters and control characters, which are normally displayed as spaces. The character set of the device is described in more detail in Section 8.

7.5.2 Character matrix

Each character is defined by a matrix 12 pixels wide and 10 pixels high. When displayed, each pixel is $^{1}/_{12}$ ms wide and 1 TV line, in each field, high.

7.5.3 Page attributes

Columns 0 to 9 of row 25 of the memory are treated by the display as if they contain display control information from teletext page headers. The bits which affect the display are shown in Table 12. Columns 0 to 4 are not used.

If C5 (newsflash) or C6 (subtitle) is set the display uses the display mode defined in register TXT6. C7 (suppress header) causes the header row (row 0) to be displayed as if every character was a space. C10 (inhibit display) displays every character on all rows as if it was a space. C12 to C14 (language control bits) cause certain character codes to be interpreted differently (see Section 7.5.5).

Table 12 Page attributes

COLUMN	PAGE ATTRIBUTE FIELD							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
5	0	0	0	0	C6	C5	0	0
6	0	0	0	0	C10	0	0	C7
7	0	0	0	0	C14	C13	C12	0
8	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0

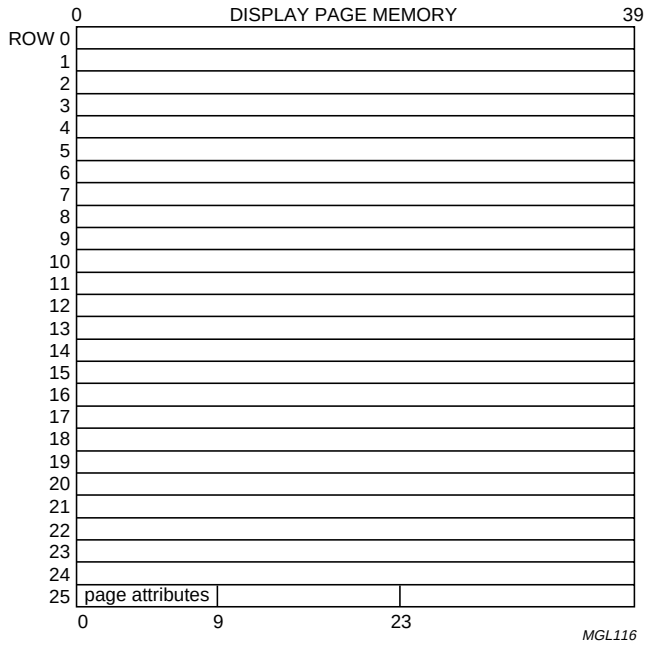


Fig.4 Display page organisation.

7.5.4 EAST/WEST SELECTION

In common with their predecessors, these devices store teletext pages as a series of 8-bit character codes which are interpreted as either control codes (to change colour, invoke flashing etc.) or displayable characters. When the control characters are excluded, this gives an addressable set of 212 characters at any given time.

More characters than this were required to give the language coverage required from the first version of the device. The TXT4. East/West bit was introduced to allow the meanings of character codes D0H to FFH to be changed, depending on where in Europe the device was to be used. This bit is still used with the other language variants, although the name East/West may not make much sense.

7.5.5 NATIONAL OPTION CHARACTERS

The interpretation of some character codes between 20H and 7FH depends on the C12 to C14 language control bits stored in row 25 of the display page.

The interpretation of the C12 to C14 language control bits is dependant on the East/West bit.

7.6 The twist attribute

In many of the character sets, the ‘twist’ serial attribute (code 1BH) can be used to switch to an alternative basic character code table, e.g. to change from the Hebrew alphabet to the Arabic alphabet on an Arabic/Hebrew device. For some national option languages the alternative code table is the default, and a twist control character will switch to the first code table.

The display hardware on the devices allows one language to invoke the alternative code table by default when the East/West register bit is a logic 0 and another when the bit is a logic 1. In all of the character sets defined so far, the language which invokes the alternative code table is the same for either setting of the East/West bit.

7.6.1 ON SCREEN DISPLAY SYMBOLS

In the character sets, character codes 80H to 9FH are OSD symbols. An editor is available to allow these characters to be redefined by the customer.

7.6.2 LANGUAGE GROUP IDENTIFICATION

The devices have a readable register TXT12 which contains a 5-bit identification code TXT12.ROM VER R4 to TXT12.ROM VER R0 which is intended for use in identifying which character set the device is using.

7.6.3 525-LINE OPERATION

When used with 525-line display syncs, the devices modify their displays such that the bottom line is omitted from each character cell. The character sets have been designed to be readable under these circumstances and anyone designing OSD symbols is advised to consider this mode of operation.

7.6.4 CONTROL CHARACTERS

Character codes 00H to 1FH, B0H to B7H and BCH to BFH are interpreted as control characters which can be used to change the colour of the characters, the background colour, the size of characters, and various other features. All control characters are normally displayed as spaces.

The alphanumerics colour control characters (00H to 07H) are used to change colour of the characters displayed.

The graphics control characters (10H to 17H) change the colour of the characters and switch the display into a mode where the codes in columns 2, 3, 6 and 7 of the character table (see the character table above) are displayed as the block mosaic characters in columns 2a, 3a, 6a and 7a. The display of mosaics is switched off using one of the alphanumerics colour control characters.

The ‘new background’ character (1DH) the background colour of the display sets the background colour equal to the current foreground colour. The ‘black background’ character (1CH) changes the background colour to black independently of the current foreground colour.
The background colour control characters in the upper half of the code table (B0H to B7H) are additions to the normal display control characters which allow the background colour to be changed to any colour with a single control character and independently of the foreground colour. The background colour is changed from the position of the background colour control character.

Displayable characters between a ‘flash’ (08H) and a ‘steady’ (09H) control character will flash on and off.

Displayable characters between a ‘conceal display’ (18H) character and an alphanumerics or graphics control character are displayed as spaces, unless the TXT7.REVEAL bit is set.

The ‘contiguous graphics’ (19H) and ‘separated graphics’ (1AH) characters control the way in which mosaic shapes are displayed. The difference between the two is shown in Fig.5.

Control characters encountered between a ‘hold graphics’ (1EH) control character and a ‘release graphics’ (1FH) control character are displayed as the last character displayed in graphics mode, rather than as spaces. From the hold graphics character until the first character displayed in graphics mode the held character is a space.

The ‘start box’ (0BH) and ‘end box’ (0AH) characters are used to define teletext boxes. Two start box characters are required to begin a teletext box, with the box starting between the 2 characters. The box ends after an end box character has been encountered.

The display can be set up so that different display modes are invoked inside and outside teletext boxes e.g. text inside boxes but TV outside. This is described in Section 7.6.5.

The ‘normal size’ (0CH), ‘double height’ (0DH), ‘double width’ (0EH) and ‘double size’ (0FH) control characters are used to change the size of the characters displayed. If any double height (or double size) characters are displayed on a row the whole of the next row is displayed as spaces. Double height display is not possible on either row 23 or row 24.

The character in the position occupied by the right hand half of a double width (or double size) character is ignored, unless it is a control character in which case it takes effect on the next character displayed. This allows double width to be used to produce a display in which blank spaces do not appear when character attributes are changed.

The size implying OSD (BCH to BFH) control characters have been included in this device to allow OSD messages to be generated easily. These characters are described in full later in this document.

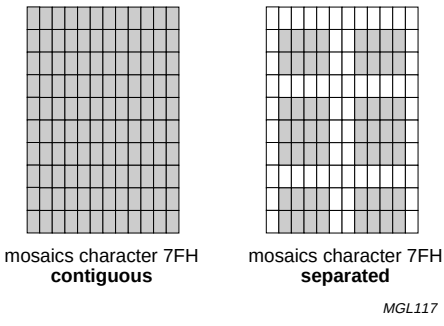


Fig.5 Contiguous and separated mosaics.

7.6.5 DISPLAY MODES

The device signals the TV's display circuits to display the R, G and B outputs of the device, rather than the video picture, by outputting a logic 1 on the VDS output. The way in which this signal is switched is controlled by the bits in the TXT5 and TXT6 SFRs. There are 3 control functions: text on, background on and picture on. Separate sets of bits are used inside and outside teletext boxes so that different display modes can be invoked. Also, different SFRs are used depending on whether the newsflash (C5) or subtitle (C6) bits in row 25 of the basic page memory are set (SFR TXT6) or not (SFR TXT5). This allows the software to set up the type of display required on newsflash and subtitle pages (e.g. text inside boxes, TV picture outside) this will be invoked without any further software intervention when such a page is acquired.

When teletext box control characters are present in the page memory, whichever is relevant of the 'Boxes On Row 0', 'Boxes On Row 1 - 23' and 'Boxes On Row 24' SFR bits in TXT17 must be set if the display mode is to change in the box. These bits are present to allow boxes in certain areas of the screen to be disabled so that teletext boxes can be used for the display of $\overline{\text{OSD}}$ messages without the danger of subtitles in boxes, which may also be in the page memory, being displayed. The use of teletext boxes for $\overline{\text{OSD}}$ messages has been superseded in this device by the OSD box concept, described later, but these bits remain to allow teletext boxes to be used, if required.

The $\overline{\text{COR}}$ bits in the TXT5 and TXT6 SFRs control when the $\overline{\text{COR}}$ output of the device is activated (pulled-down). This output is intended to act on the TV's display circuits to reduce the contrast of the video display when it is active. The result of contrast reduction is to improve the readability of the text in a mixed text and video display.

The bits in the TXT5 and TXT6 SFRs allow the display to be set up so that, for example, the areas inside teletext boxes will be contrast reduced when a subtitle is being displayed but that the rest of the screen will be displayed as normal video.

Setting the shadow TXT4.SHADOW ENABLE bit will add a 'south east' shadow to the text, significantly enhancing its readability in mix mode. Shadowing is shown in Fig.6.

The readability of text can also be enhanced using 'meshing'. Meshing causes the VDS signal to switch so that when the text background colour should be displayed every other pixel is displayed from the video picture. Text foreground pixels are always displayed.
The TXT4.BMESH bit enables meshing on areas of the screen within the text display area with black as the background colour.

The TXT4.CMESH bit has the same effect on areas with other background colours. Meshing can only be invoked in areas displayed in text mode i.e. where the TXT5.TEXT IN and TXT5.BKGND IN bits are both set to logic 1, and in OSD boxes. Meshed text can also be shadowed. Meshing is illustrated in Fig.6.

The TXT4.TRANS bit causes areas of black background colour to become transparent i.e. video is displayed instead of black background. Black background transparency can also only be invoked in areas displayed in text mode i.e. where the TXT5.TEXT IN and TXT5.BKGND IN bits are both set to logic 1, and in OSD boxes.

Table 13 Display control bits

PICTURE ON	TEXT ON	BACKGROUND ON	EFFECT
0	0	X	text mode, black screen
0	1	0	text mode, background always black
0	1	1	text mode
1	0	X	TV mode
1	1	0	mixed text and TV mode
1	1	1	text mode, TV picture outside text area

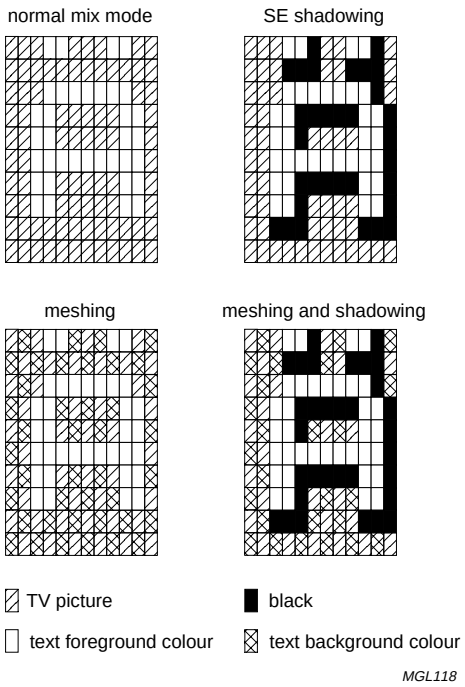


Fig.6 Meshing and shadowing.

Table 14 Enhanced display mode selection

SHADOW	TRANS	BMESH	CMESH	DISPLAY
0	0	0	0	normal, unshadowed, unmeshed text
0	0	0	1	text with coloured backgrounds meshed, black background solid
0	0	1	0	text with coloured backgrounds solid, black background meshed
0	0	1	1	text with all backgrounds meshed
0	1	X	0	text with coloured backgrounds solid, black background transparent
0	1	X	1	text with coloured backgrounds meshed, black background transparent
1	0	0	1	shadowed text with coloured backgrounds meshed, black background solid
1	0	1	0	shadowed text with coloured backgrounds solid, black background meshed
1	0	1	1	shadowed text with all backgrounds meshed
1	1	X	0	shadowed text with coloured backgrounds solid, black background transparent
1	1	X	1	shadowed text with coloured backgrounds meshed, black background transparent

7.7 On Screen Display boxes

The size implying OSD control characters (BCH to BFH) are intended to allow OSD messages to be displayed. OSD boxes are not the same as teletext boxes created using the teletext boxing control characters (0AH and 0BH).

When one of these characters occurs the display size changes appropriately (to normal size for BCH, double height for BDH, double width for BEH and double size for BFH) and an OSD box starts from the next character position (‘set after’). The OSD box ends either at the end of the row of text or at the next size implying OSD character. When an OSD box is ended using another size implying OSD character the box ends at the position of the control character (‘set at’). This arrangement allows displays to be created without blank spaces at the ends of the OSD boxes.

To prevent teletext control characters from affecting the display of the OSD message the flash, teletext box, conceal, separated graphics, twist and hold graphics functions are all reset at the start of an OSD box, as they are at the start of the row. In order to allow the most commonly used display attributes to be set-up before the box starts the foreground colour, background colour and mosaics on/off attributes are not reset.

The text within an OSD box is always displayed in text mode i.e. as if the Text On and Bkgnd On bits are both set to a logic 1. The type of display produced inside an OSD box is, therefore, dependant on the states of the TXT4.SHADOW ENABLE, TXT4.TRANS ENABLE, TXT4.BMESH ENABLE and TXT4.CMESH ENABLE register bits, as described previously. OSD boxes can only be displayed in TV mode i.e. when the Picture On SFR bit is a logic 1 and the Text On SFR bit is a logic 0, both inside and outside text boxes and for both normal and newsflash/subtitle pages. The display of OSD boxes is not affected by the C7, suppress header, and C10, inhibit display, control bits stored in row 25 of the page memory.

7.8 Screen colour

The register bits TXT17.SCREEN COL2-0 can be used to define a colour to be displayed in place of the TV picture and the black background colour. If the bits are all set to 0, the screen colour is defined as ‘transparent’ and the TV picture and background colour are displayed as normal.

Screen colour is displayed from 10.5 to 62.5 μs after the active edge of the HSync input and on TV lines 23 to 310 inclusive, for a 625-line display, and lines 17 to 260 inclusive for a 525-line display.

When the screen colour has been redefined, no TV picture is displayed so the Frame de-interlace output can be activated, if the SFR bits controlling FRAME are set up to allow this.

Table 15 Screen colours

SCREEN COL 2	SCREEN COL 1	SCREEN COL 0	SCREEN COLOUR
0	0	0	transparent
0	0	1	red
0	1	0	green
0	1	1	yellow
1	0	0	blue
1	0	1	magenta
1	1	0	cyan
1	1	1	white

7.9 Cursor

If the TXT7.CURSOR ON bit is set, a cursor is displayed. The cursor operates by reversing the background and foreground colours in the character position pointed to by the active row and column bits in the TXT9 and TXT10 SFRs.

Setting the TXT9.CURSOR FREEZE bit, causes the cursor to stay in its current position, no matter what happens to the active row and column positions. This means that the software can read data from the memory (e.g. TOP table information) without affecting the position of the cursor.

7.10 Other display features

Setting the TXT7.DOUBLE HEIGHT bit causes the normal height of all display characters to be doubled and the whole of the display area to be occupied by half of the display rows. Characters normally displayed double height will be displayed quadruple height when this bit is set. Rows 12 to 24 can be enlarged, rather than rows 0 to 11, by setting the TXT7.$\overline{\text{TOP}}$/BOTTOM bit.

This feature can be used for either a user controlled 'enlarge' facility or to provide very large characters for the OSD.

The display of rows 0 to 23 can be disabled by setting the TXT0.DISPLAY STATUS ROW ONLY bit.

The Fastext prompt row (packet 24) can be displayed from the extension packet memory by setting the TXT0.DISPLAY X/24 bit. When this bit is set the data displayed on display row 24 is taken from row 0 in the extension packet memory.

When the display from extension packet block option is enabled, the display will revert to row 24 of the basic page memory if bit 3 of the link control byte in packet 27 is set.

7.11 Display timing

The display synchronises to the device's HSync and VSync inputs. A typical configuration is shown in Fig.7.

The HSync and VSync signals are derived from the signals driving the deflection coils of the TV. Locking the display to the signals from the scan circuits allows the device to give a stable display under almost all signal conditions.

The polarity of the input signals which the device is expecting can be set using the TXT1.H polarity and TXT1.V polarity bits. If the polarity bit is a logic 0, a positive going signal is expected and if it is a logic 1, a negative going signal is expected.

7.12 Horizontal timing

Every time an HSync pulse is received the display resynchronizes to its leading edge. To get maximum display stability, the HSync input must have fast edges, free of noise to ensure that there is no uncertainty in the timing of the signal to which the display synchronisation circuits must lock.

The display area starts 17.2 μs into the line and lasts for 40 μs. The display area will be in the centre of the screen if the HSync pulse is aligned with line flyback signal. Therefore, it is better to derive HSync directly from the line flyback or from an output of the line output transformer than from, say, slicing the sandcastle signal as this would introduce delays which would shift the display to the right.

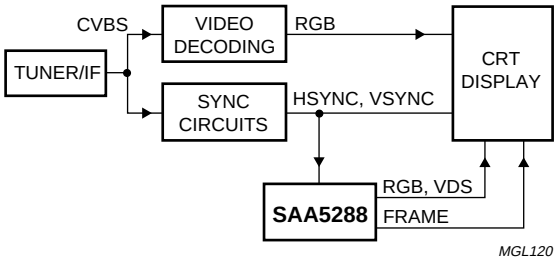


Fig.7 Timing configuration.

7.13 Vertical timing

The vertical display timing also resynchronizes to every sync pulse received. This means that the device can produce a stable display on both 625 and 525-line screens. Display starts on the 41st line of each field and continues for 250 lines, or until the end of the field.

Normally, television displays are interlaced, i.e. only every other TV line is displayed on each field. It is normal to de-interlace teletext displays to prevent the displayed characters flickering up and down. In many TV designs this is achieved by modulating the vertical deflection current slightly in such a way that odd fields are shifted up and even fields are shifted down on the screen so that lines 1 and 314, 2 and 315 etc. are overlaid. The FRAME output is provided to facilitate this.

If the active edge of Vsync occurs in the first half of a TV line this is an even field and the FRAME output should be a logic 0 for this field. Similarly, if VSync is in the second half of the line this is an odd field and FRAME should be a logic 1. The algorithm used to derive FRAME is such that a consistent output will be obtained no matter where the VSync signal is relative to the HSync signal, even if VSync occurs at the start and mid-points of a line.

Setting the TXT0.DISABLE FRAME bit forces the FRAME output to a logic 0. Setting the TXT0.AUTO FRAME bit causes the FRAME output to be active when just text is being displayed but to be forced to 0 when any video is being displayed. This allows the de-interlacing function to take place with virtually no software intervention.

Some TV architectures do not use the FRAME output but accomplish the de-interlacing function in the vertical deflection IC, under software control, by delaying the start of the scan for one field by half a line, so that lines in this field are moved up by one TV line. In such TVs, VSync may occur in the first half of the line at the start of an odd field and in the second half of the line at the start of an even field. In order to obtain correct de-interlacing in these circumstances, theTXT1.FIELD POLARITY must be set to reverse the assumptions made by the vertical timing circuits on the timing of VSync in each field. The start of the display may be delayed by a line. The ‘Field Polarity’ bit does not affect the FRAME output.

7.14 Display position

The position of the display relative to the HSync and VSync inputs can be varied over a limited range to allow for optimum TV set-up.

The horizontal position is controlled by the X0 and X1 bits in SFR TXT16. Table 16 gives the time from the active edge of the HSync signal to the start of the display area for each setting of X0 and X1.

Table 16 Display horizontal position

X1	X0	HSYNC DISPLAY (μs)
0	0	17.2
0	1	16.2
1	0	15.2
1	1	14.2

The line on which the display area starts depends on whether the display is 625-line or 525-line and on the setting of the Y0 to Y2 bits in SFR TXT16. Table 17 gives the first display line for each setting of Y0 to Y2, for both 625 and 525-line display.

On the other field, the display starts on the equivalent line.

Table 17 Display vertical position

Y2	Y1	Y0	FIRST LINE FOR DISPLAY	
			625-LINE	525-LINE
0	0	0	42	28
0	0	1	44	30
0	1	0	46	32
0	1	1	48	34
1	0	0	34	20
1	0	1	36	22
1	1	0	38	24
1	1	1	40	26

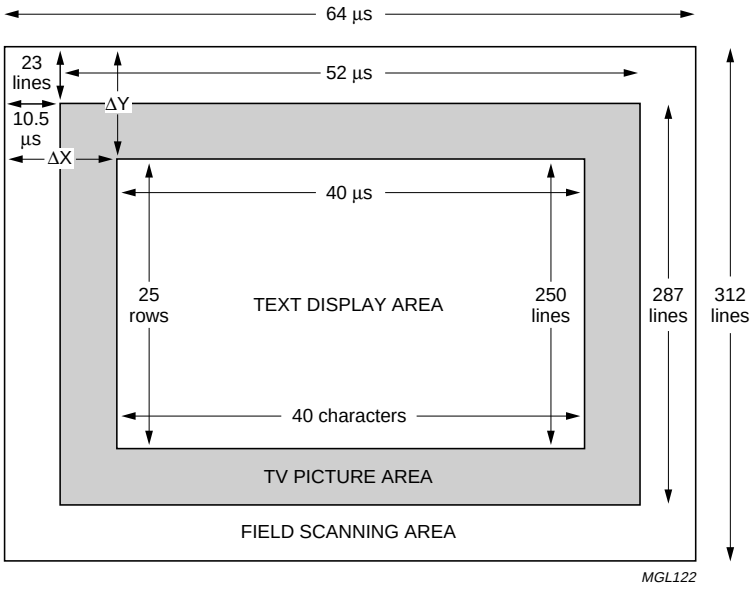


Fig.8 625-line display format.

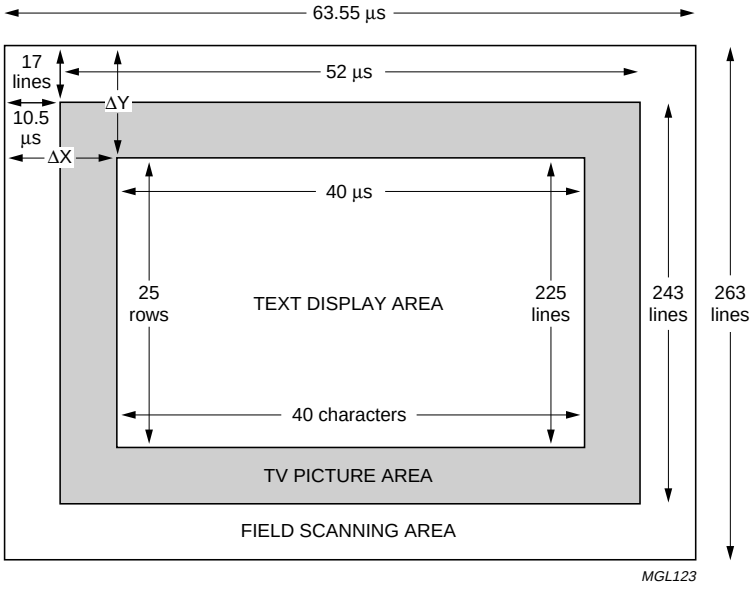
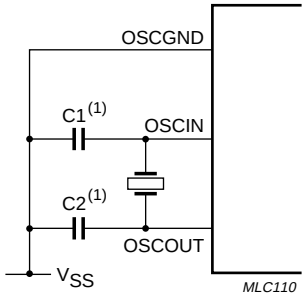


Fig.9 525-line display format.

7.15 Clock generator

The oscillator circuit is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between OSCIN and OSCOUT is basically an inverter biased to the transfer point. A crystal must be used as the feedback element to complete the oscillator circuitry. It is operated in parallel resonance. OSCIN is the high gain amplifier input and OSCOUT is the output.

To drive the device externally OSCIN is driven from an external source and OSCOUT is left open-circuit.



(1) The values of C1 and C2 depend on the crystal specification: C1 = C2 = $2C_L$.

Fig.10 Oscillator circuit.

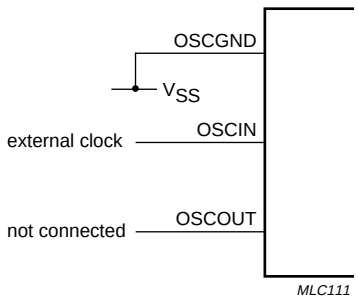


Fig.11 Oscillator circuit driven from external source.

8 CHARACTER SETS

The two Pan-European character sets are shown in Figs.13 and 14. The character sets for Russian, Greek/Turkish, Arabic/English/French, Thai and Arabic/Hebrew are available on request.

8.1 Pan-European

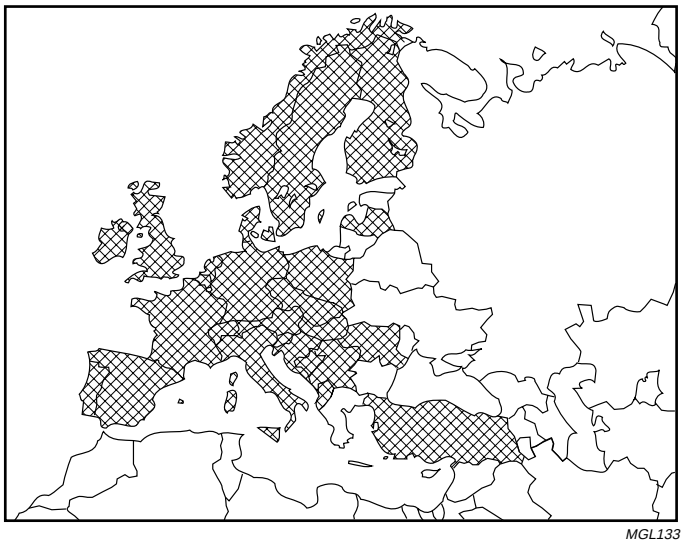


Fig.12 Pan-European geographical coverage.

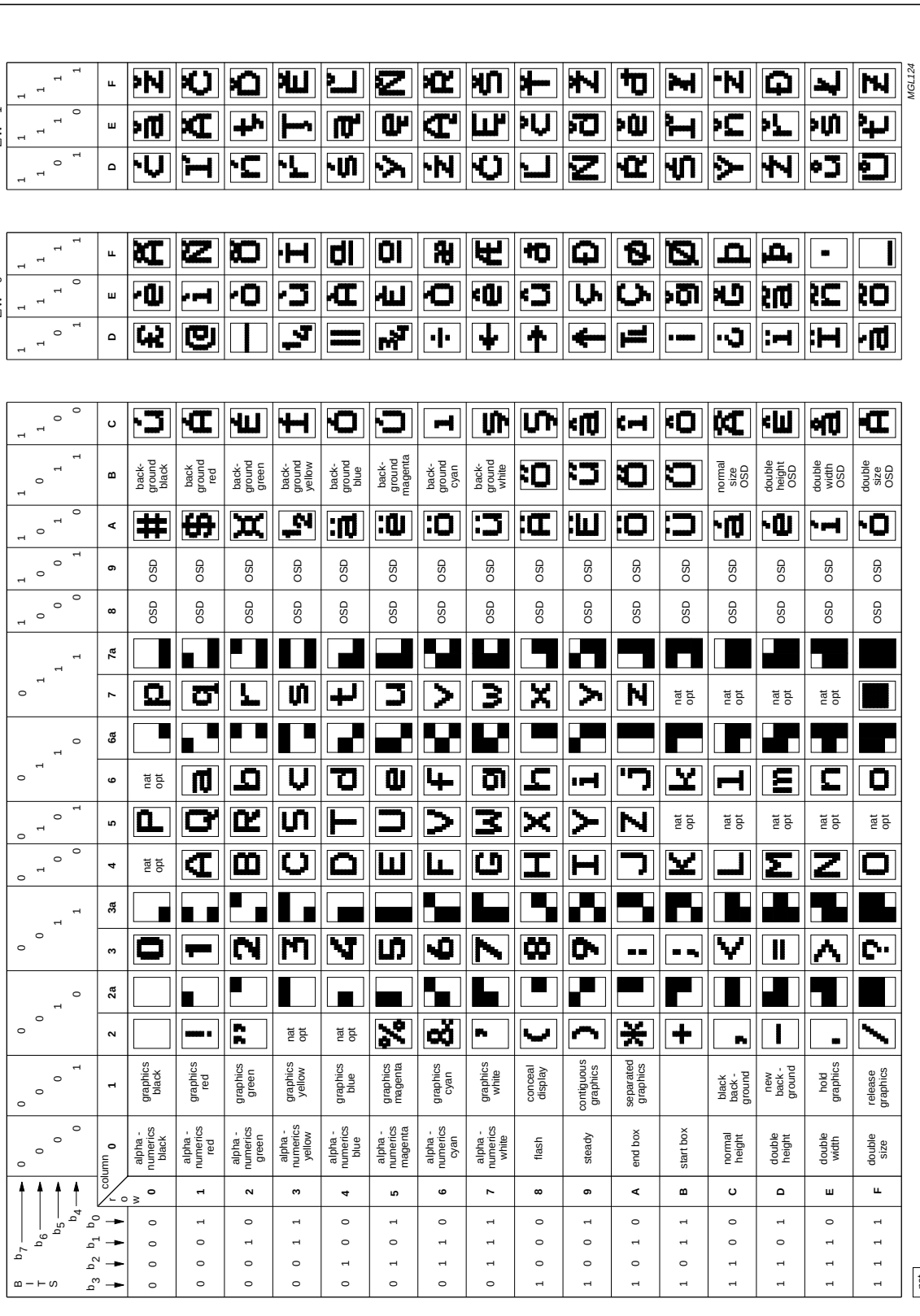


Fig.13 Pan-European basic character set.

LANGUAGE	E/W	C12	C13	C14	CHARACTER												
					23	24	40	5B	5C	5D	5E	5F	60	7B	7C	7D	7E
ENGLISH(1)	0	0	0	0	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN(1)	0	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH(1)	0	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN(1)	0	0	1	1	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH(1)	0	1	0	0	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç
SPANISH(1)	0	1	0	1	ç	$	¡	á	é	í	ó	ú	¿	ü	ñ	è	à
TURKISH(1)	0	1	1	0	Ţ	ğ	İ	Ş	Ö	Ç	Ü	Ğ	ı	ş	ö	ç	ü
ENGLISH(2)	0	1	1	1	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
POLISH(1)	1	0	0	0	#	ń	ą	Ż	ś	ł	ć	ó	ę	ż	ś	ł	ź
GERMAN(1)	1	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
ESTONIAN(1)	1	0	1	0	#	õ	Š	Ä	Ö	Ž	Ü	Õ	š	ä	ö	ž	ü
GERMAN(2)	1	0	1	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
GERMAN(2)	1	1	0	0	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SERBO-CROAT(1)	1	1	0	1	#	Ë	Č	Ć	Ž	Đ	Š	ë	č	ć	ž	đ	š
CZECH(1)	1	1	1	0	#	ů	č	ť	ž	ý	í	ř	é	á	ě	ú	š
RUMANIAN(1)	1	1	1	1	#	¤	Ţ	Â	Ş	Ă	Î	ı	ţ	â	ş	ă	î

MGL125

(1) This language conforms to the EBU document SP492 or where superseded ETSI document pr ETS 300 706 with respect to C12/C13/C14 definition.

(2) This language is included for backward compatibility with previous generation of Philips teletext decoders.

Fig.14 National option characters.

8.2 Russian

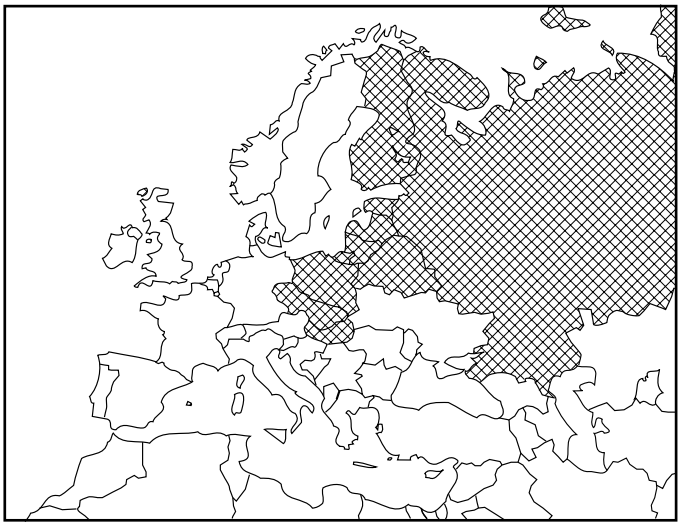


Fig.15 Russian geographical coverage.

8.3 Greek/Turkish

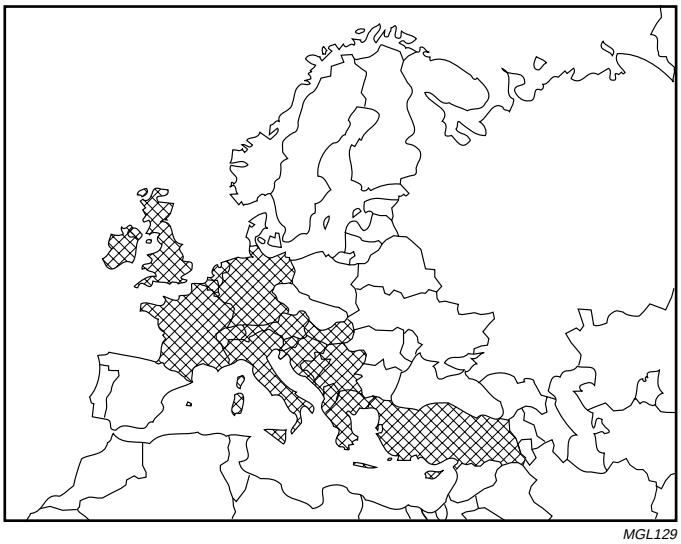


Fig.16 Greek/Turkish geographical coverage.

8.4 Arabic/English/French

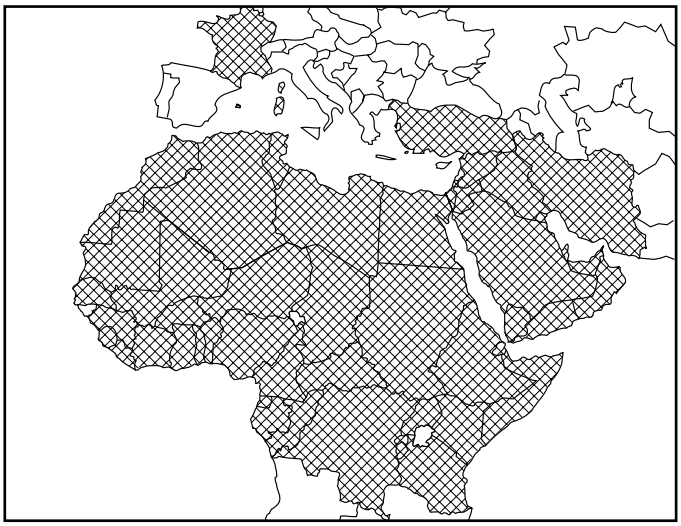


Fig.17 Arabic/English/French geographical coverage.

8.5 Thai

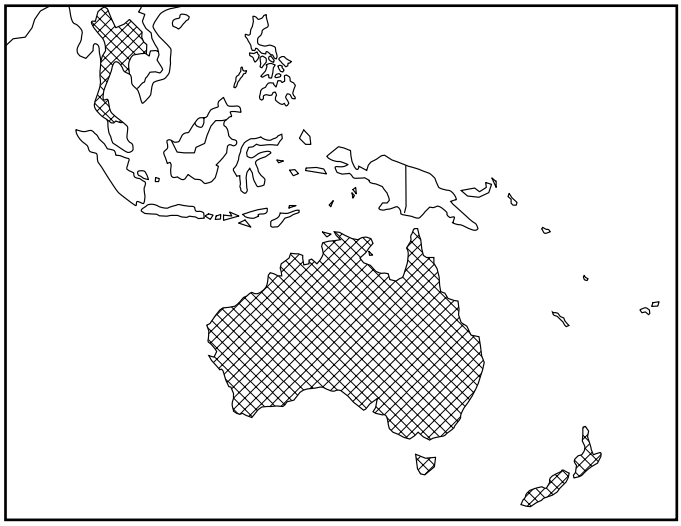


Fig.18 Thai geographical coverage.

8.6 Arabic/Hebrew

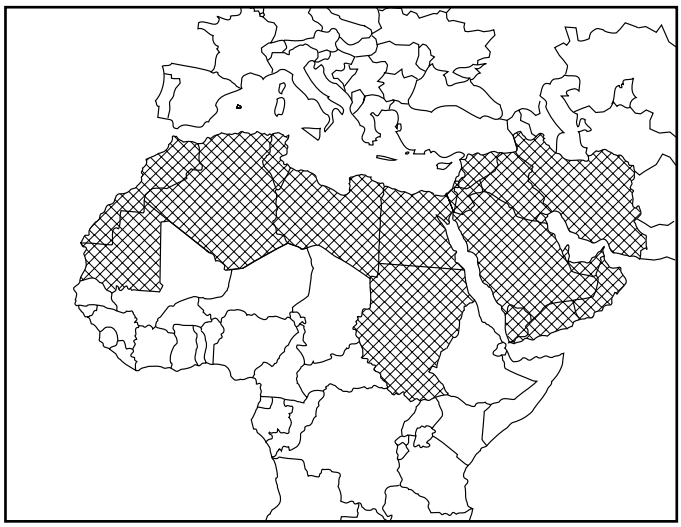


Fig.19 Arabic/Hebrew geographical coverage.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)		–0.3	+6.5	V
V_I	input voltage (any input)	note 1	–0.3	V_{DD} + 0.5	V
V_O	output voltage (any output)	note 1	–0.3	V_{DD} + 0.5	V
I_O	output current (each output)		–	±10	mA
I_{IOK}	DC input or output diode current		–	±20	mA
T_{amb}	operating ambient temperature		–20	+70	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. This value has an absolute maximum of 6.5 V independent of V_{DD}.

10 CHARACTERISTICS

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = –20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DDM}	microcontroller supply current		–	15	30	mA
I_{DDA}	analog supply current		–	8	15	mA
I_{DDT}	display supply current		–	15	30	mA
Digital inputs						
RESET						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{DD}$ – 0.1	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	4	pF
HSYNC AND VSYNC						
$V_{th(f)}$	switching threshold falling		$0.2V_{DD}$	–	–	V
$V_{th(r)}$	switching threshold rising		–	–	$0.8V_{DD}$	V
V_{hys}	hysteresis voltage		–	$0.33V_{DD}$	–	V
C_I	input capacitance		–	–	4	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs						
R, G AND B; note 1						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –2 mA	V_{RGBREF} – 0.3	V_{RGBREF}	V_{RGBREF} + 0.4	V
$\lvert Z_O \rvert$	output impedance		–	–	150	Ω
C_L	load capacitance		–	–	50	pF
I_O	DC output current		–	–	–4	mA
t_r	output rise time	between 10 and 90%; C_L = 50 pF	–	–	20	ns
t_f	output fall time	between 90 and 10%; C_L = 50 pF	–	–	20	ns
VDS						
V_{OL}	LOW-level output voltage	I_{OL} = 1.6 mA	0	–	0.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –1.6 mA	V_{DD} – 0.3	–	V_{DD} + 0.4	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	between 10 and 90%; C_L = 50 pF	–	–	20	ns
t_f	output fall time	between 90 and 10%; C_L = 50 pF	–	–	20	ns
R, G, B AND VDS						
t_{skew}	skew delay between any two pins		–	–	20	ns
$\overline{COR}$ (OPEN-DRAIN OUTPUT)						
V_{OH}	HIGH-level pull-up output voltage		–	–	V_{DD}	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	0	–	0.5	V
I_{OL}	LOW-level output current		–	–	2	mA
C_L	load capacitance		–	–	25	pF
FRAME						
V_{OH}	HIGH-level output voltage	I_{OL} = 8 mA	0	–	0.5	V
V_{OL}	LOW-level output voltage	I_{OL} = –8 mA	V_{DD} – 0.5	–	V_{DD}	V
I_{OL}	LOW-level output current		–8	–	+8	mA
C_L	load capacitance		–	–	100	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input/outputs						
P0.0 TO P0.4, P0.7, P1.0 TO P1.5, P2.0 TO P2.7 AND P3.0 TO P3.4						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{DD} – 0.1$	V
V_{IH}	HIGH-level input voltage		$0.2V_{DD} + 0.9$	–	$V_{DD} + 0.3$	V
C_I	input capacitance		–	–	4	pF
V_{OL}	LOW-level output voltage	I_{OL} = 3.2 mA	0	–	0.45	V
C_L	load capacitance		–	–	50	pF
P0.5 AND P0.6						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{DD} – 0.1$	V
V_{IH}	HIGH-level input voltage		$0.2V_{DD} + 0.9$	–	$V_{DD} + 0.3$	V
C_I	input capacitance		–	–	4	pF
V_{OL}	LOW-level output voltage	I_{OL} = 10 mA	0	–	0.45	V
C_L	load capacitance		–	–	50	pF
P1.6 AND P1.7						
V_{IL}	LOW-level input voltage		–0.3	–	+1.5	V
V_{IH}	HIGH-level input voltage		3.0	–	$V_{DD} + 0.3$	V
C_I	input capacitance		–	–	5	pF
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	0	–	0.5	V
C_L	load capacitance		–	–	400	pF
t_f	output fall time	between 3 and 1 V	–	–	200	ns
Analog inputs						
IREF						
R_{gnd}	resistor to ground		–	27	–	kΩ
RGBREF; note 1						
V_I	input voltage		–0.3	–	V_{DD}	V
I_I	DC input current		–	–	12	mA
ADC0, ADC1 and ADC2						
V_{IL}	LOW-level input voltage		–0.3	–	V_{DD}	V
Crystal oscillator						
OSCIN						
V_{IL}	LOW-level input voltage		–0.3	–	$0.2V_{DD} – 0.1$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.3$	V
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OSCOUT						
C_O	output capacitance		–	–	10	pF
CRYSTAL SPECIFICATION; note 2						
f_{xtal}	nominal frequency		–	12	–	MHz
C_L	load capacitance		–	32	–	pF
C1	series capacitance	T_{amb} = 25 °C	–	18.5	–	fF
C0	parallel capacitance	T_{amb} = 25 °C	–	4.9	–	pF
R_r	resonance resistance	T_{amb} = 25 °C	–	35	–	Ω
T_{xtal}	temperature range		–20	+25	+70	°C
X_j	adjustment tolerance	T_{amb} = 25 °C	–	–	$\pm 50 \times 10^{-6}$	
X_d	drift		–	–	$\pm 30 \times 10^{-6}$	

Notes

1. All RGB current is sourced from the RGBREF pin. The maximum effective series resistance between RGBREF and the R, G and B pins is 150 Ω.
2. Crystal order number 4322 143 05561.

11 CHARACTERISTICS FOR THE I²C-BUS INTERFACE

SYMBOL	PARAMETER	INPUT	OUTPUT	I²C-BUS SPECIFICATION
SCL timing				
$t_{HD;STA}$	START condition hold time	≥4.0 µs	note 1	≥4.0 µs
t_{LOW}	SCL LOW time	≥4.7 µs	note 1	≥4.7 µs
t_{HIGH}	SCL HIGH time	≥4.0 µs	≥4.0 µs; note 2	≥4.0 µs
t_{rC}	SCL rise time	≤1.0 µs	note 3	≤1.0 µs
t_{fC}	SCL fall time	≤0.3 µs	≤0.3 µs; note 4	≤0.3 µs
SDA timing				
$t_{SU;DAT1}$	data set-up time	≥250 ns	note 1	≥250 ns
$t_{HD;DAT}$	data hold time	≥0 ns	note 1	≥0 ns
$t_{SU;STA}$	repeated START set-up time	≥4.7 µs	note 1	≥4.7 µs
$t_{SU;STO}$	STOP condition set-up time	≥4.0 µs	note 1	≥4.0 µs
t_{BUF}	bus free time	≥4.7 µs	note 1	≥4.7 µs
t_{rD}	SDA rise time	≤1.0 µs	note 3	≤1.0 µs
t_{fD}	SDA fall time	≤0.3 µs	≤0.3 µs; note 4	≤0.3 µs

Notes

1. This parameter is determined by the user software. It must comply with the I²C-bus specification.
2. This value gives the auto-clock pulse length which meets the I²C-bus specification for the special crystal frequency. Alternatively, the SCL pulse must be timed by software.
3. The rise time is determined by the external bus line capacitance and pull-up resistor. It must be less than 1 µs.
4. The maximum capacitance on bus lines SDA and SCL is 400 pF.

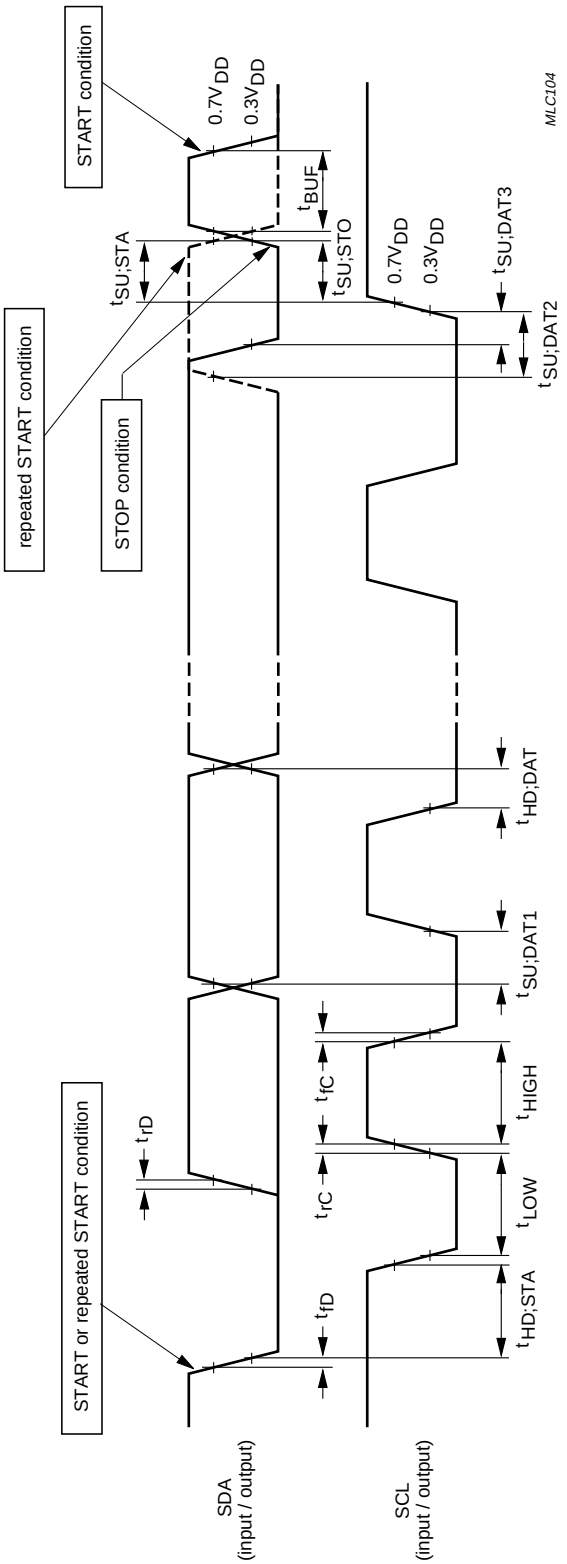


Fig.20 I²C-bus interface timing.

12 QUALITY SPECIFICATIONS

This device will meet Philips Semiconductors General Quality Specification for Business group *"Consumer Integrated Circuits SNW-FQ-611-Part E"*; *"Quality Reference Handbook, order number 9398 510 63011"*. The principal requirements are shown in Tables 18 to 20.

Table 18 Acceptance tests per lot; note 1

TEST	REQUIREMENTS
Mechanical	cumulative target: <80 ppm
Electrical	cumulative target: <80 ppm

Table 19 Processability tests (by package family); note 2

TEST	REQUIREMENTS
solderability	<7% LTPD
mechanical	<15% LTPD
solder heat resistance	<15% LTPD

Table 20 Reliability tests (by process family); note 3

TEST	CONDITIONS	REQUIREMENTS
operational life	168 hours at T_j = 150 °C	<1000 FPM at T_j = 70 °C
humidity life	temperature, humidity, bias 1000 hours, 85 °C, 85% RH (or equivalent test)	<2000 FPM
temperature cycling performance	$T_{stg(min)}$ to $T_{stg(max)}$	<2000 FPM

Table 21 Reliability tests (by device type)

TEST	CONDITIONS	REQUIREMENTS
ESD and latch-up	ESD Human body model 100 pF, 1.5 kΩ	2000 V
	ESD Machine model 200 pF, 0 Ω	200 V
	latch-up	100 mA, $1.5 \times V_{DD}$ (absolute maximum)

Notes to Table 16 to 18

1. ppm = fraction of defective devices, in parts per million.
2. LTPD = Lot Tolerance Percent Defective.
3. FPM = fraction of devices failing at test condition, in Failures Per Million.

13 APPLICATION INFORMATION

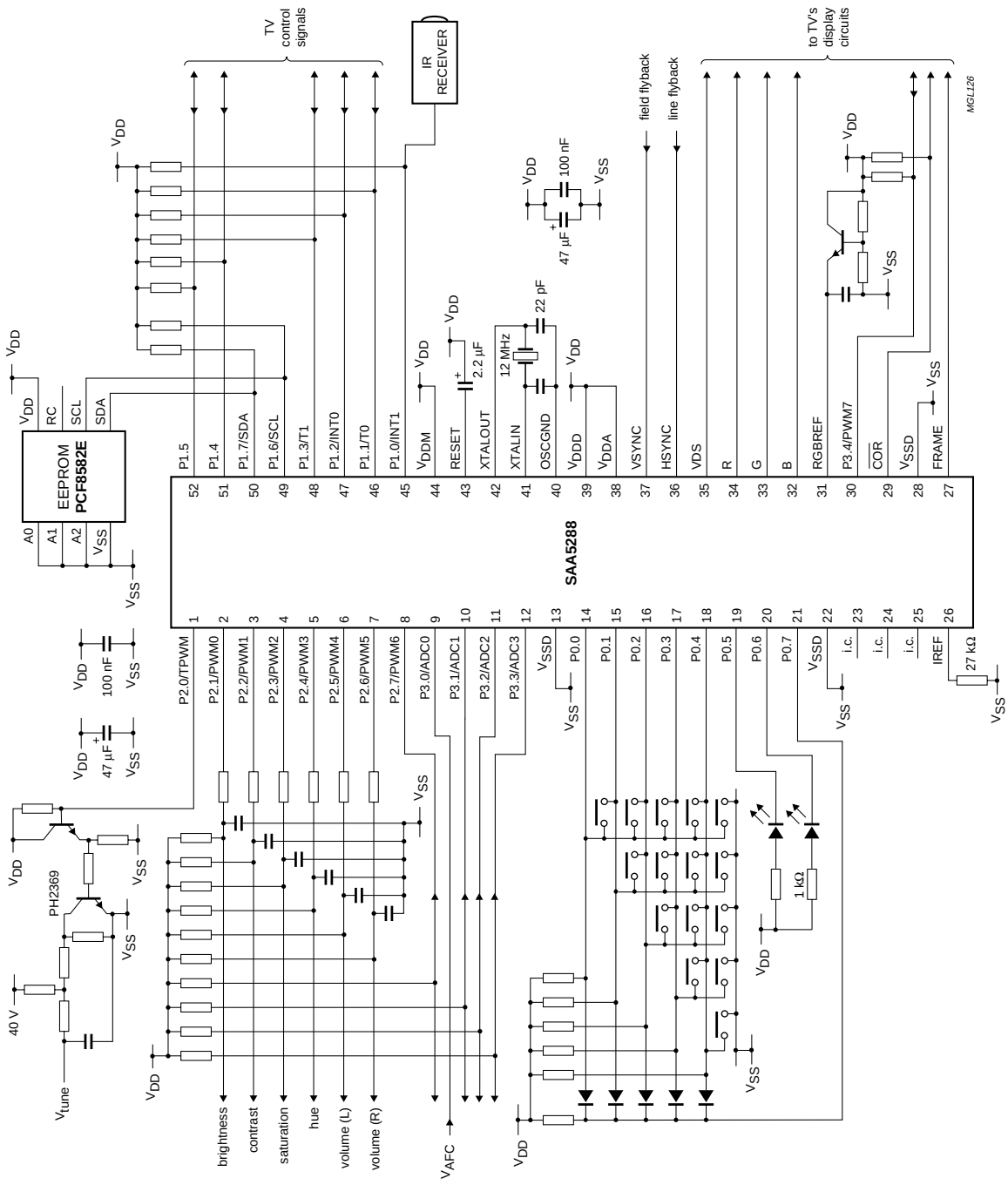


Fig.21 Application diagram.

14 EMC GUIDELINES

If possible, a ground plane under the whole IC should be present, i.e. no signal tracks running underneath the IC as shown in Fig.22.

The ground plane under the IC should be connected by the widest possible connection back to the ground connection of the PCB, and electrolytic decoupling capacitor. It should preferably not connect to other grounds on the way and no wire links should be present in this connection. The use of wire links increases ground bounce by introducing inductance into the ground, thereby reducing the electrolytic capacitor's decoupling efficiency.

The supply pins should be decoupled at the pin, to the ground plane under the IC. This is easily accomplished when using SM capacitors (which are also most effective at high frequencies).

Each supply pin should be connected separately to the power connection of the PCB, preferably via at least one wire link which:

1. May be replaced by a ferrite or inductor at a later point if necessary
2. Will introduce a small amount of inductance.

Signals connected to the +5 V supply e.g. via pull-up resistors, should be connected to the +5 V supply before the wire link to the IC (i.e. not the IC side). This will prevent if from being polluted and conduct or radiate noise onto signal lines, which may then radiate themselves.

OSCGND should connect only to the crystal load capacitors (and not GND).

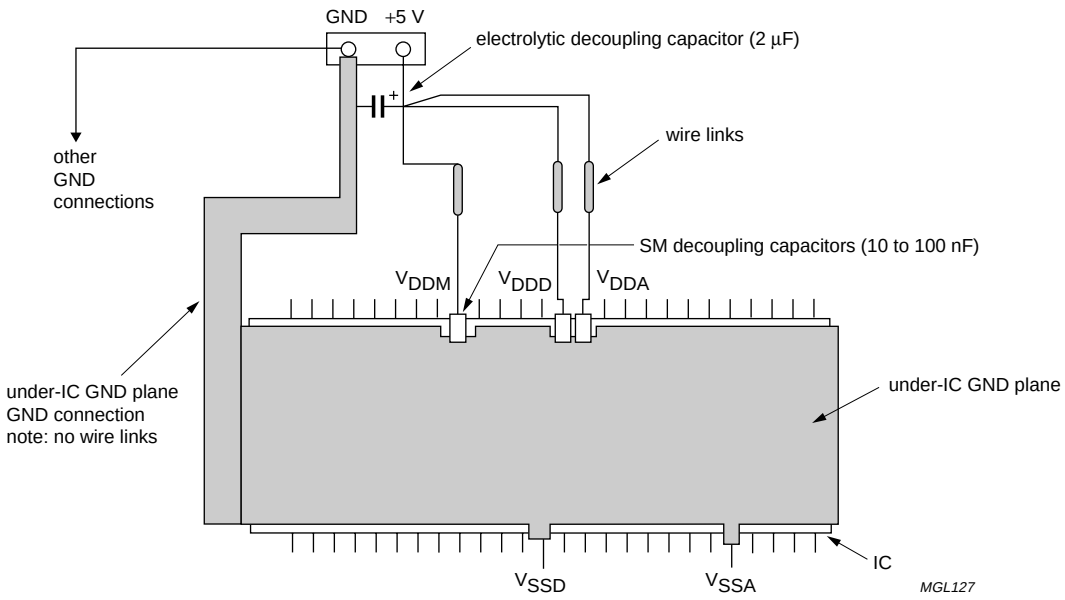
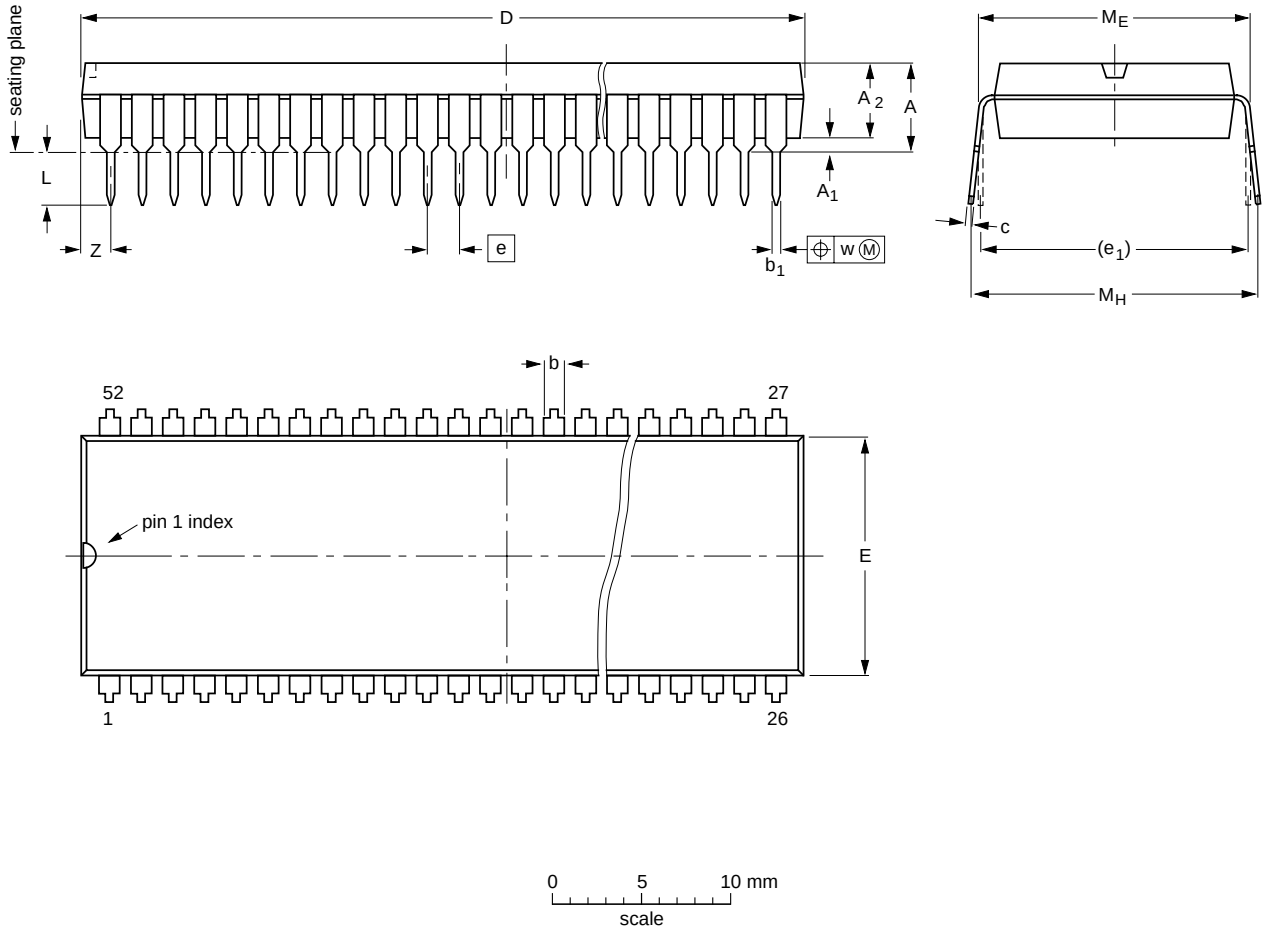


Fig.22 Power supply and GND connections for SOT247-1.

15 PACKAGE OUTLINE

SDIP52: plastic shrink dual in-line package; 52 leads (600 mil) **SOT247-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	47.9 47.1	14.0 13.7	1.778	15.24	3.2 2.8	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT247-1						~~90-01-22~~ 95-03-11

16 SOLDERING

16.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

16.2 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

16.3 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

17 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

18 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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