60V, 1.2A Synchronous Monolithic Buck Regulator with 6µA Quiescent Current

FEATURES

- **Wide Input Voltage Range: 3V to 60V**
- **Fast Minimum Switch-On Time: 30ns**
- **Ultralow Quiescent Current Burst Mode Operation:**
  - **6µA I_Q Regulating $12V_{IN}$ to $3.3V_{OUT}$**
  - **$10mV_{P-P}$ Output Ripple at No Load**
- **Synchronizable/Programmable Fixed Frequency Forced Continuous Mode Operation: 300kHz to 2.2MHz**
- **High Efficiency Synchronous Operation:**
  - **92% Efficiency at 0.5A, $5V_{OUT}$ from $12V_{IN}$**
  - **90% Efficiency at 0.5A, $3.3V_{OUT}$ from $12V_{IN}$**
- **Low Dropout: 360mV at 0.5A**
- **Low EMI**
- Accurate 1V Enable Pin Threshold
- Internal Soft-Start and Compensation
- Power Good Flag
- Small Thermally Enhanced 16-Lead MSOP Package and 10-Lead (3mm × 3mm) DFN Packages
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- 12V Automotive Systems
- 12V and 24V Commercial Vehicles
- 48V Electric and Hybrid Vehicles
- Industrial Supplies

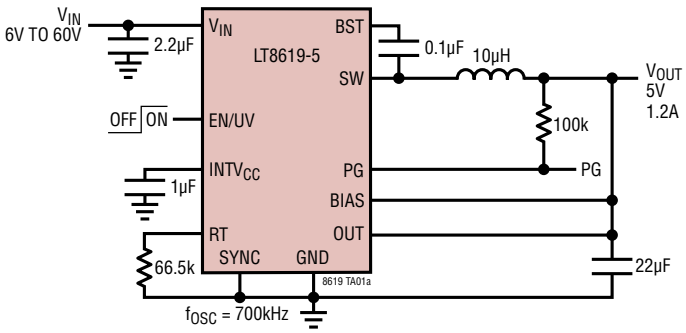
DESCRIPTION

The LT®8619 is a compact, high efficiency, high speed synchronous monolithic step-down switching regulator that consumes only 6µA of quiescent current. The LT8619 can deliver 1.2A of continuous current. Top and bottom power switches are included with all necessary circuitry to minimize the need for external components. Low ripple Burst Mode® operation enables high efficiency down to very low output currents while keeping the output ripple to $10mV_{P-P}$. A SYNC pin allows forced continuous mode operation synchronized to an external clock. Internal compensation with peak current mode topology allows the use of small inductors and results in fast transient response and good loop stability. The EN/UV pin has an accurate 1V threshold and can be used to program V_{IN} undervoltage lockout or to shut down the LT8619, reducing the input supply current to below 0.6µA. The PG flag signals when V_{OUT} is within ±7.5% of the programmed output voltage. The LT8619 is available in a small 16-lead MSOP and 10-lead 3mm × 3mm DFN packages with exposed pad for low thermal resistance.

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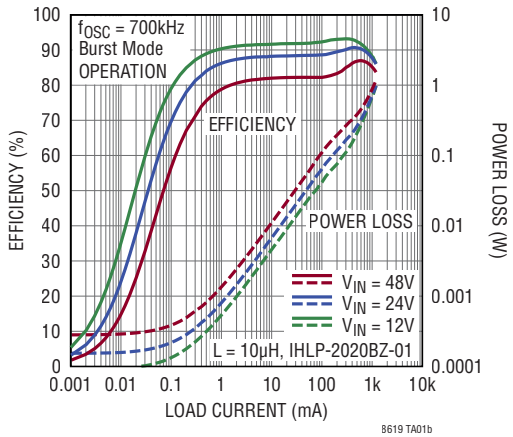
TYPICAL APPLICATION

5V, 1.2A Step-Down Converter



L = VISHAY IHLP-2020BZ-01
C_{OUT} = TDK C3225X7R1C226K250

Efficiency at V_{OUT} = 5V



Rev. C

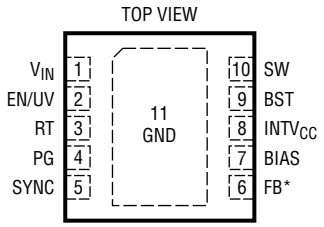
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{IN}, EN/UV 60V
BIAS.....30V
BST Pin Above SW Pin.....4V
PG, SYNC, OUT. 6V
FB 2V

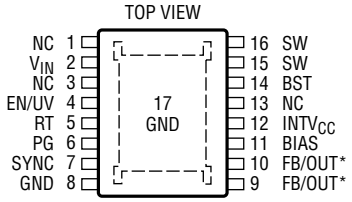
Operating Junction Temperature (Note 3)
LT8619E, LT8619E-5..... –40°C to 125°C
LT8619I, LT8619I-5..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

θ_{JA} = 43°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSOP

θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

*FB FOR LT8619, OUT FOR LT8619-5

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8619EDD#PBF	LT8619EDD#TRPBF	LGNP	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT8619IDD#PBF	LT8619IDD#TRPBF	LGNP	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT8619EMSE#PBF	LT8619EMSE#TRPBF	8619	16-Lead Plastic MSOP	–40°C to 125°C
LT8619IMSE#PBF	LT8619IMSE#TRPBF	8619	16-Lead Plastic MSOP	–40°C to 125°C
LT8619EMSE-5#PBF	LT8619EMSE-5#TRPBF	86195	16-Lead Plastic MSOP	–40°C to 125°C
LT8619IMSE-5#PBF	LT8619IMSE-5#TRPBF	86195	16-Lead Plastic MSOP	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LT8619EMSE#WPBF	LT8619EMSE#WTRPBF	8619	16-Lead Plastic MSOP	–40°C to 125°C
LT8619IMSE#WPBF	LT8619IMSE#WTRPBF	8619	16-Lead Plastic MSOP	–40°C to 125°C
LT8619EMSE-5#WPBF	LT8619EMSE-5#WTRPBF	86195	16-Lead Plastic MSOP	–40°C to 125°C
LT8619IMSE-5#WPBF	LT8619IMSE-5#WTRPBF	86195	16-Lead Plastic MSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V_{EN/UV}$ = 2V unless otherwise noted (Notes 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Loop						
V_{IN} Minimum Input Voltage					3.0	V
V_{IN} Quiescent Current at No Load	V_{IN} = 12V, $V_{EN/UV}$ = 0V	 ●		0.6 0.6	1.0 3.0	µA µA
	V_{IN} = 12V, V_{OUT} = 3.3V, R_T = 66.5k, BIAS = V_{OUT}, V_{SYNC} = 0V	 ●		6 6	10 18	µA µA
	V_{IN} = 12V, V_{OUT} = 3.3V, R_T = 66.5k, BIAS = V_{OUT}, Floats SYNC			10		µA
	V_{IN} = 12V, V_{OUT} = 3.3V, R_T = 66.5k, BIAS = V_{OUT}, V_{SYNC} = $INTV_{CC}$			3		mA
V_{IN} Current in Regulation	V_{IN} = 12V, V_{OUT} = 3.3V, R_T = 66.5k, BIAS = V_{OUT}, V_{SYNC} = 0V I_{LOAD} = 100µA I_{LOAD} = 1mA	 ● ●		 38 320	 65 400	 µA µA
BIAS Pin Current Consumption	V_{IN} = 12V, V_{BIAS} = 3.3V, I_{LOAD} = 0.5A, f_{OSC} = 700kHz			2.2		mA
Regulated Output Voltage	LT8619-5, V_{IN} = 12V, V_{SYNC} = $INTV_{CC}$, No Load	 ●	4.975 4.925	5.0 5.0	5.025 5.075	V
Feedback Voltage	LT8619, V_{IN} = 12V, V_{SYNC} = $INTV_{CC}$, No Load	 ●	0.796 0.788	0.8 0.8	0.804 0.812	V V
Feedback Voltage Line Regulation	LT8619, V_{IN} = 4V to 50V, V_{SYNC} = $INTV_{CC}$ (Note 5) LT8619-5, V_{IN} = 6V to 50V, V_{SYNC} = $INTV_{CC}$ (Note 5)	● ●		±0.004 ±0.004	±0.03 ±0.03	%/V %/V
Feedback Pin Input Current	LT8619, V_{FB} = 0.8V				±20	nA
Minimum On-Time	LT8619, I_{LOAD} = 0.5A, V_{SYNC} = $INTV_{CC}$	●		30	60	ns
Minimum Off-Time			100	150	180	ns
Top Switch Peak Current Limit		●	1.5	1.75	2.0	A
Bottom Switch Current Limit				1.8		A
Bottom Switch Reverse Current Limit	V_{SYNC} = $INTV_{CC}$			0.55		A
Soft-Start Duration	V_{IN} = 12V, V_{OUT} = 3.3V, No Load, C_{OUT} = 22µF			0.2		ms
EN/UV to PG High Delay	C_{INTVCC} = 1µF, V_{OUT} = 3.3V, No Load, C_{OUT} = 22µF			0.66		ms
EN/UV to PG Low Delay				10		µs
Oscillator and SYNC						
Operating Frequency	R_T = 162k	●	260	300	340	kHz
	R_T = 66.5k	●	630	700	770	kHz
	R_T = 20k	●	1.9	2.0	2.1	MHz
Synchronization Frequency	$f_{SYNC} \geq f_{OSC}$	●	0.3		2.2	MHz
SYNC Threshold	Frequency Synchronization Burst Mode Operation Floats SYNC Pin, Pulse-Skipping Mode Forced Continuous Mode		 0.35 1.6	1 0.6 1.2 2.0	 0.95 2.4	V V V V
SYNC Pin Current	Built-In Sourcing Current, V_{SYNC} = 0V Built-In Sinking Current, V_{SYNC} = 3.3V			–0.2 3.0		µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V_{EN/UV}$ = 2V unless otherwise noted (Notes 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch, Logic and Power Good						
Top Switch On-Resistance	I_{LOAD} = 0.1A			0.45		Ω
Bottom Switch On-Resistance	I_{LOAD} = 0.1A			0.22		Ω
EN/UV Power-On Threshold	EN/UV Rising	●	0.94	1.0	1.1	V
EN/UV Power-On Hysteresis				40		mV
EN/UV Shutdown Threshold	EN/UV Falling	●	0.34	0.56	0.92	V
EN/UV Pin Current	$V_{EN/UV}$ = 2V		–100		100	nA
Overvoltage Threshold	V_{FB}/V_{OUT} Rising Wrt. Regulated V_{FB}/V_{OUT}			3.75		%
Positive Power Good Threshold	V_{FB}/V_{OUT} Rising Wrt. Regulated V_{FB}/V_{OUT}	●	5	7.5	10	%
Negative Power Good Threshold	V_{FB}/V_{OUT} Rising Wrt. Regulated V_{FB}/V_{OUT}	●	–5	–7.5	–10	%
Positive Power Good Delay	LT8619, V_{FB} = 0.8V ↑ 0.9V to PG Low LT8619-5, V_{OUT} = 5V ↑ 5.6V to PG Low LT8619, V_{FB} = 0.9V ↓ 0.8V to PG High LT8619-5, V_{OUT} = 5.6V ↓ 5V to PG High			60 60 35 35		µs µs µs µs
Negative Power Good Delay	LT8619, V_{FB} = 0.8V ↓ 0.7V to PG Low LT8619-5, V_{OUT} = 5V ↓ 4.4V to PG Low LT8619, V_{FB} = 0.7V ↑ 0.8V to PG High LT8619-5, V_{OUT} = 4.4V ↑ 5V to PG High			60 60 35 35		µs µs µs µs
PG Leakage	V_{PG} = 3.3V, Power Good				±100	nA
PG V_{OL}	I_{PG} = 100µA	●		0.01	0.3	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All Voltages are referenced to ground unless otherwise specified.

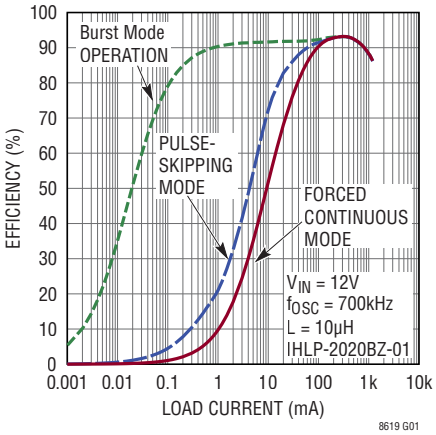
Note 3: The LT8619 is tested under pulse load conditions such that $T_J \approx T_A$. The LT8619E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT8619I is guaranteed over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

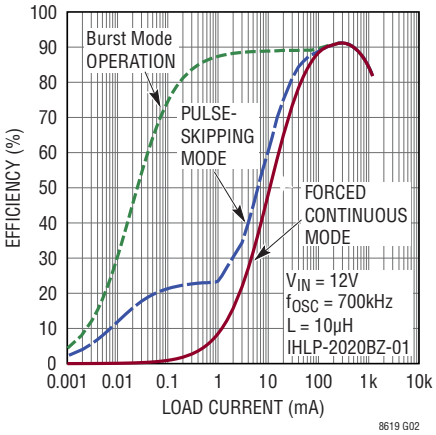
Note 5: Guaranteed by design, not subject to test.

TYPICAL PERFORMANCE CHARACTERISTICS

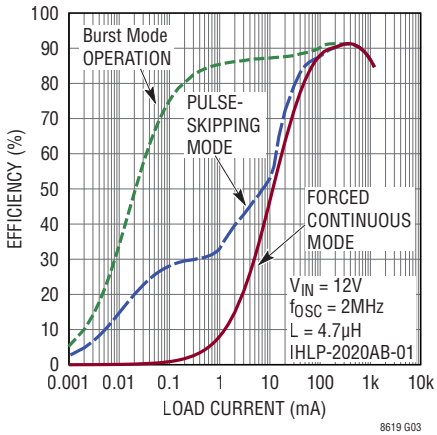
700kHz Efficiency at V_{OUT} = 5V



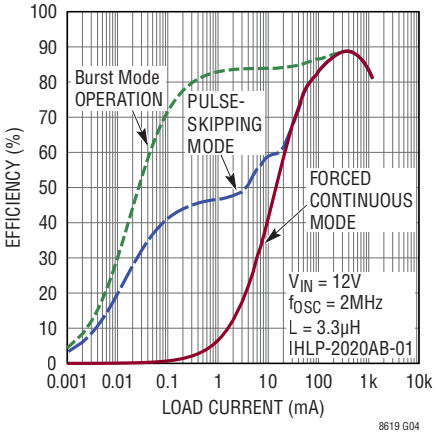
700kHz Efficiency at V_{OUT} = 3.3V



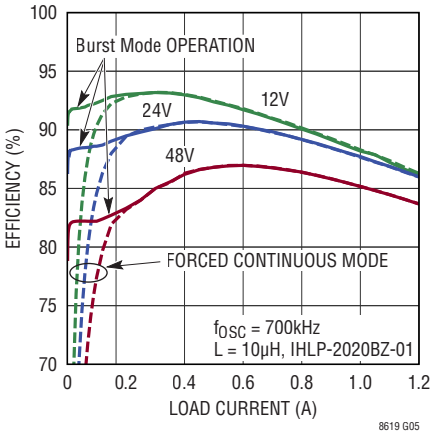
2MHz Efficiency at V_{OUT} = 5V



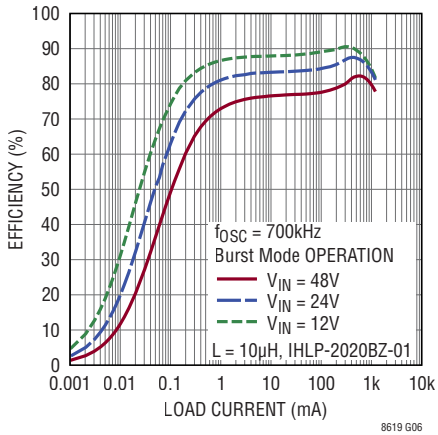
2MHz Efficiency at V_{OUT} = 3.3V



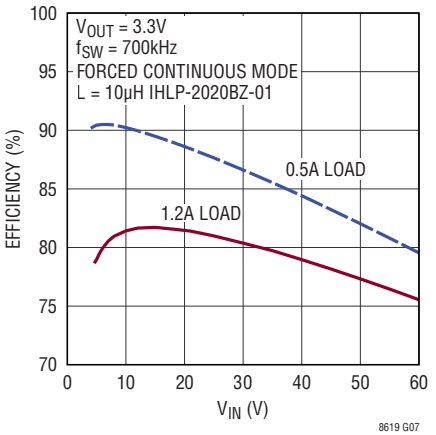
Efficiency at V_{OUT} = 5V



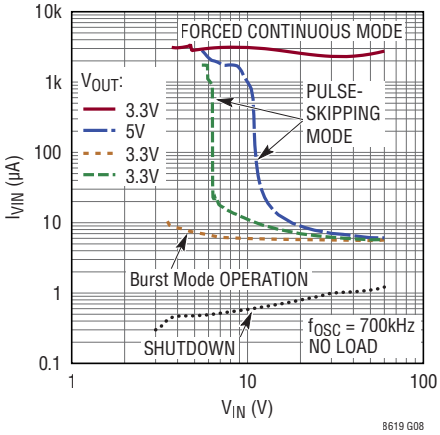
Efficiency at V_{OUT} = 3.3V



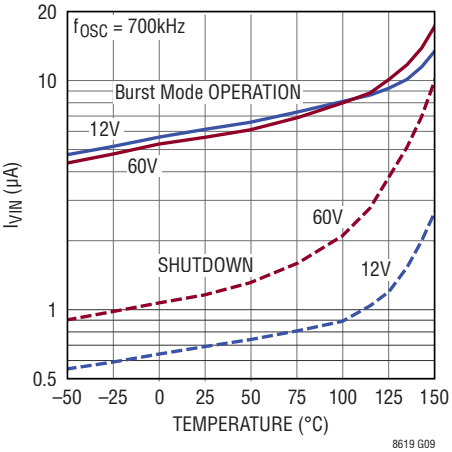
Efficiency vs V_{IN}



No Load I_{VIN} at 700kHz

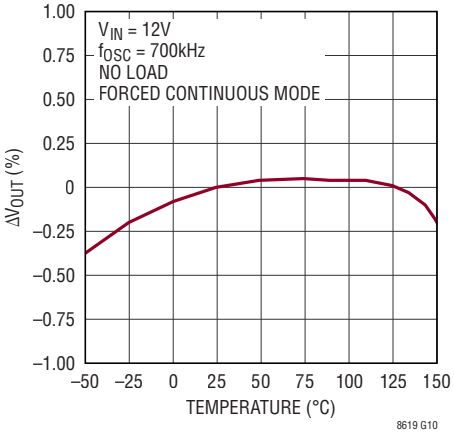


No Load I_{VIN} vs Temperature

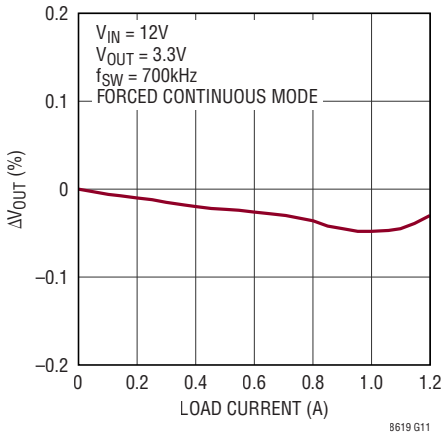


TYPICAL PERFORMANCE CHARACTERISTICS

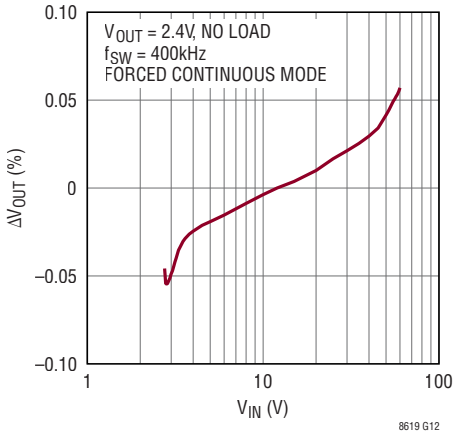
V_{OUT} = 3.3V



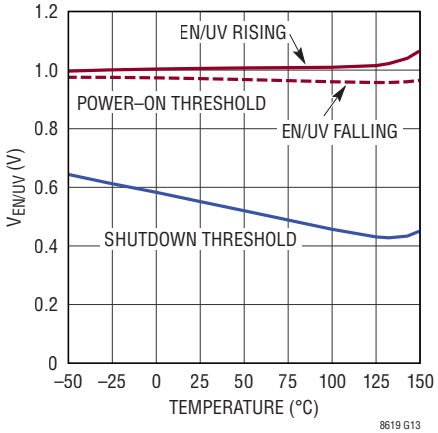
Load Regulation



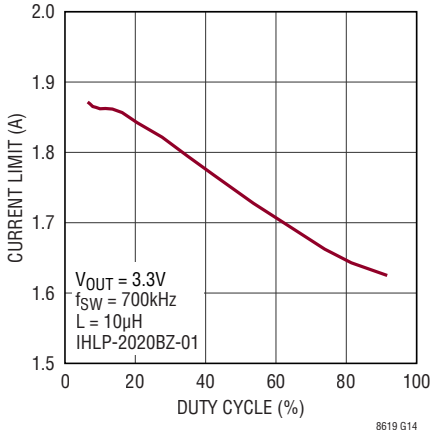
Line Regulation



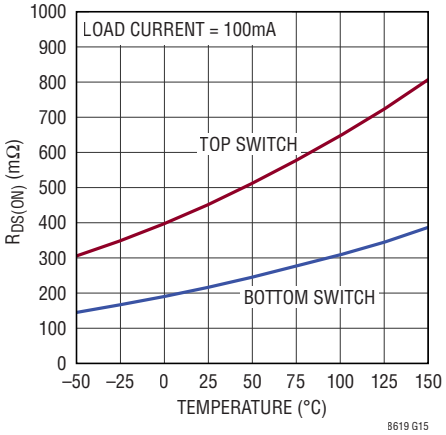
EN/UV Threshold



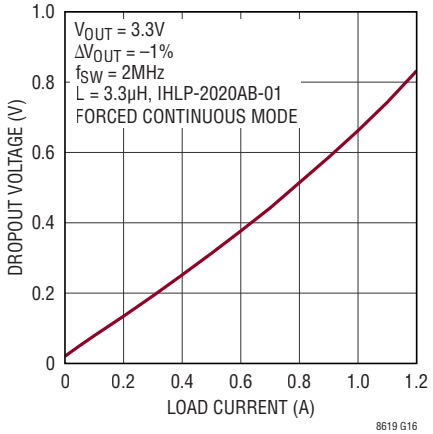
Top FET Current Limit vs Duty Cycle



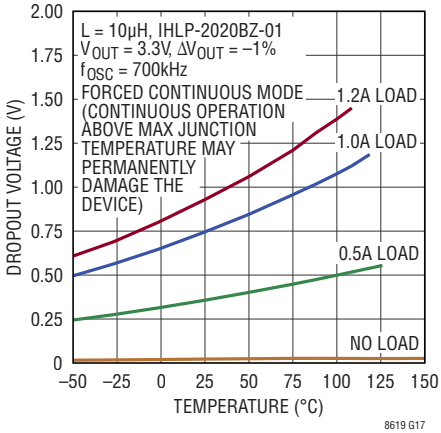
Switch Resistance



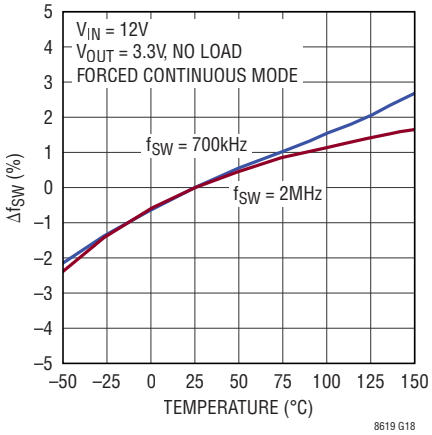
Dropout



Dropout vs Temperature

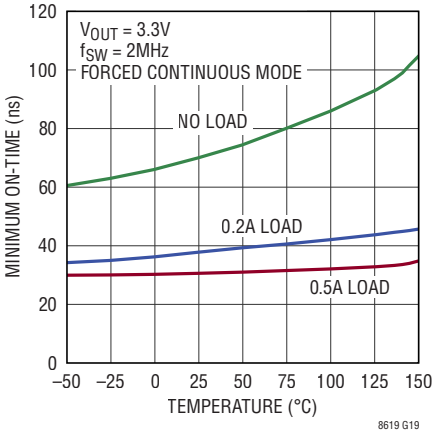


f_{SW}

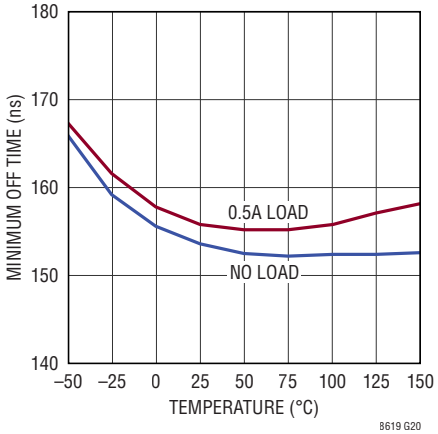


TYPICAL PERFORMANCE CHARACTERISTICS

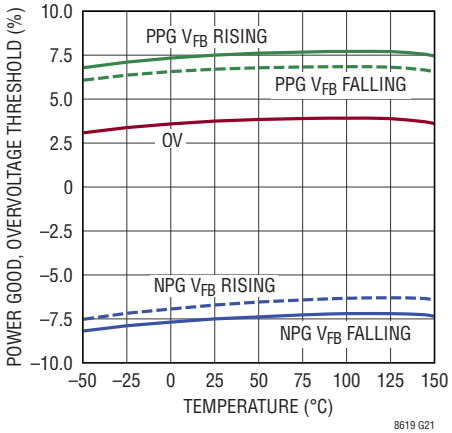
Minimum On-Time



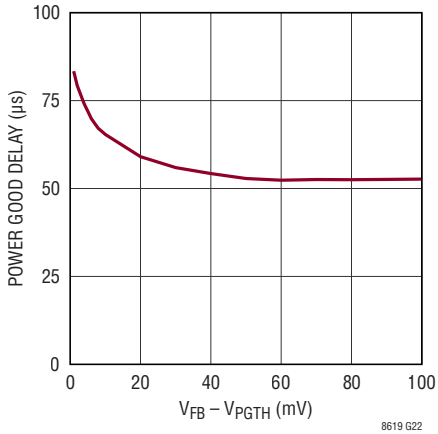
Minimum Off-Time



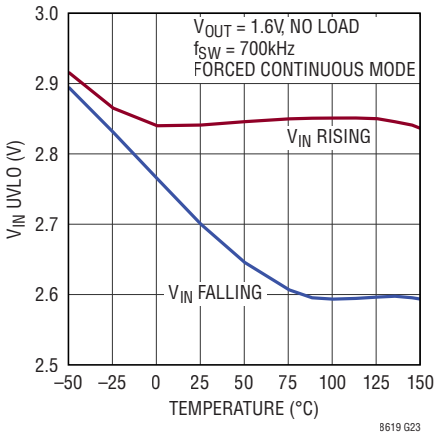
Power Good, Overvoltage Threshold



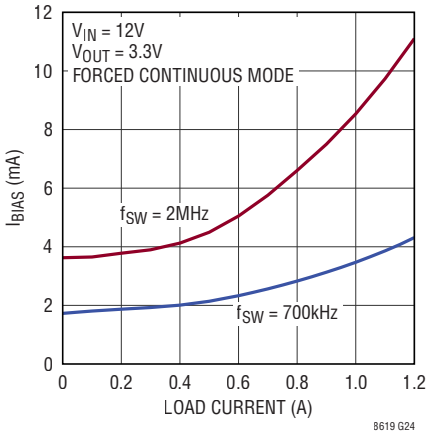
Power Good Delay



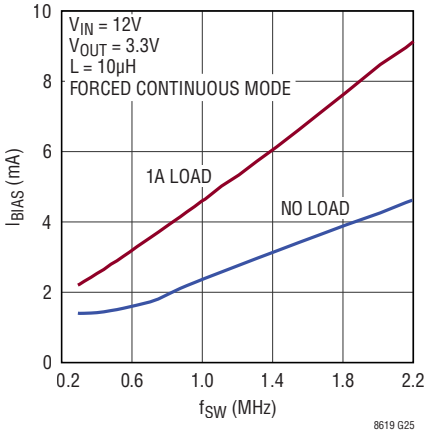
V_{IN} UVLO



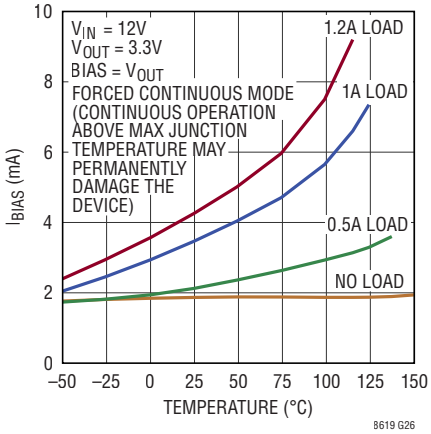
I_{BIAS} vs Load



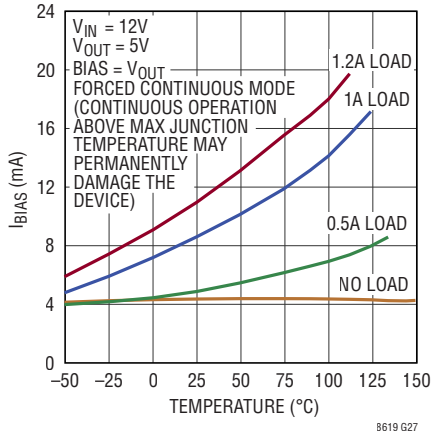
I_{BIAS} vs f_{SW}



I_{BIAS} at 700kHz vs Temperature

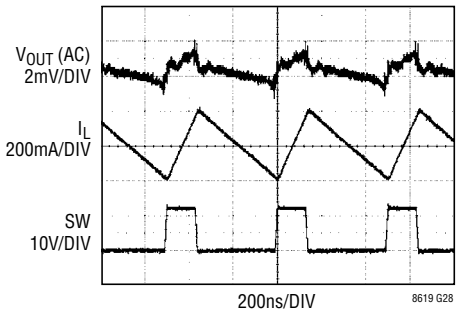


I_{BIAS} at 2MHz vs Temperature



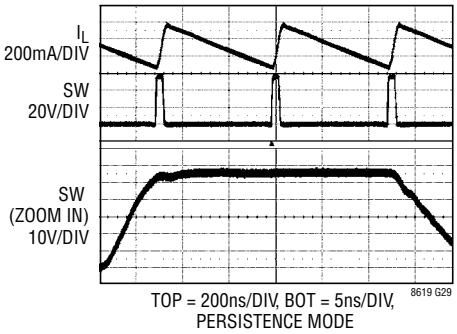
TYPICAL PERFORMANCE CHARACTERISTICS

Forced Continuous Mode No Load Switching Waveform



V_{IN} = 12V, V_{OUT} = 3.3V
f_{SW} = 2MHz, L = 3.3µH, C_{OUT} = 22µF

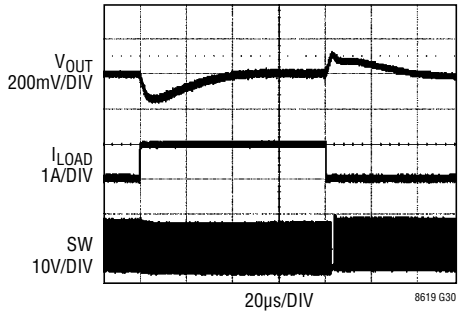
Forced Continuous Mode Switching Waveform at Minimum On-time



TOP = 200ns/DIV, BOT = 5ns/DIV,
PERSISTENCE MODE

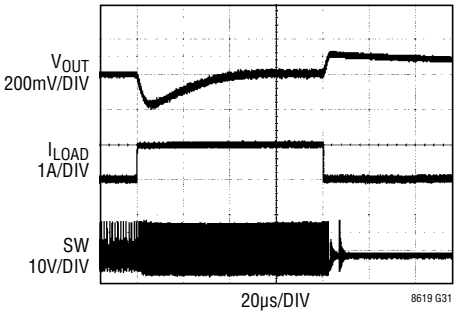
V_{IN} = 53.7V, V_{OUT} = 3.3V, 0.5A LOAD
f_{SW} = 2MHz, L = 3.3µH, C_{OUT} = 22µF

Forced Continuous Mode Transient Load Step from 10mA to 1A



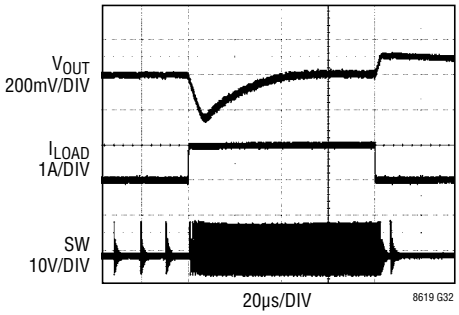
V_{IN} = 12V, V_{OUT} = 3.3V
f_{OSC} = 2MHz, L = 3.3µH, C_{OUT} = 22µF

Pulse-Skipping Mode Transient Load Step from 10mA to 1A



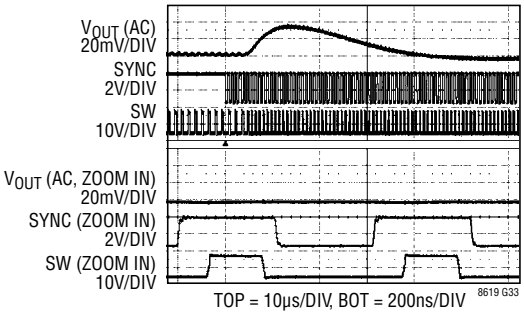
V_{IN} = 12V, V_{OUT} = 3.3V
f_{OSC} = 2MHz, L = 3.3µH, C_{OUT} = 22µF

Bust Mode Transient Load Step from 10mA to 1A



V_{IN} = 12V, V_{OUT} = 3.3V
f_{OSC} = 2MHz, L = 3.3µH, C_{OUT} = 22µF

Forced Continuous Mode Frequency Synchronization

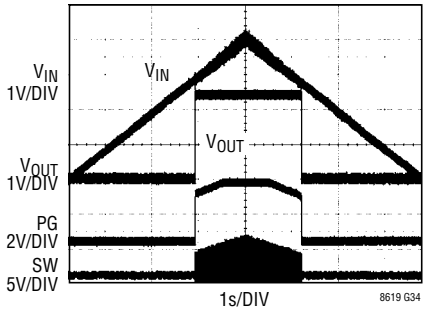


TOP = 10µs/DIV, BOT = 200ns/DIV

V_{IN} = 12V, V_{OUT} = 3.3V, NO LOAD
f_{OSC} = 700kHz, L = 10µH, C_{OUT} = 22µF
f_{SW} (FREE RUNNING) = 700kHZ, f_{SYNC} = 1.2MHz

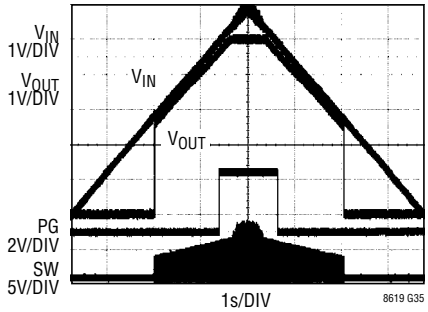
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OUT} = 2.4V Start-Up Dropout Performance



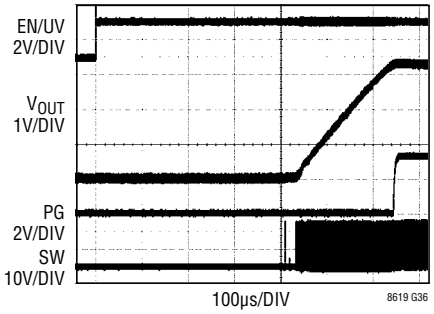
V_{OUT} = 2.4V, 10Ω LOAD
f_{SW} = 400kHz, L = 15µH, C_{OUT} = 47µF
PG 100k PULL-UP BY $INTV_{CC}$
FORCED CONTINUOUS MODE

V_{OUT} = 5V Start-Up Dropout Performance



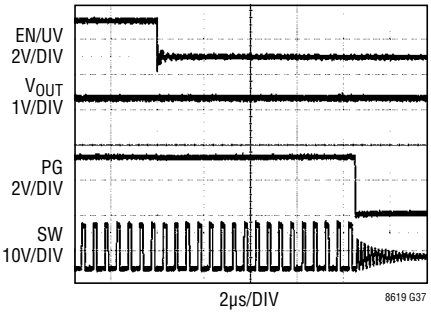
V_{OUT} = 5V, 10Ω LOAD
f_{SW} = 700kHz, L = 10µH, C_{OUT} = 22µF
PG 100k PULL-UP BY $INTV_{CC}$
FORCED CONTINUOUS MODE

EN/UV Start-Up



V_{IN} = 12V, V_{OUT} = 3.3V, NO LOAD
f_{OSC} = 2MHz, L = 3.3µH, C_{OUT} = 22µF
FORCED CONTINUOUS MODE

EN/UV Shut Down



V_{IN} = 12V, V_{OUT} = 3.3V, NO LOAD
f_{OSC} = 2MHz, L = 3.3µH, C_{OUT} = 22µF
FORCED CONTINUOUS MODE

PIN FUNCTIONS (DFN/MSOP)

NC (Pin 1, 3, 13, MSOP Only): No Connect. These pins are not connected to the internal circuitry.

V_{IN} (Pin 1/Pin 2): The V_{IN} pin supplies current to the LT8619 internal circuitry and to the internal topside power switch. Be sure to place the positive terminal of the input bypass capacitor as close as possible to the V_{IN} pin, and the negative capacitor terminal as close as possible to the GND pin.

EN/UV (Pin 2/Pin 4): The LT8619 is shut down when this pin is low and active when this pin is high. The EN/UV pin power-on threshold is 1V. When forced below 0.56V, the IC is put into a low current shutdown mode. Tie to V_{IN} if shutdown feature is not used. An external resistor divider from V_{IN} can be used to program the V_{IN} UVLO.

RT (Pin 3/Pin 5): A resistor is tied between RT and ground to set the switching frequency. When synchronizing, the R_T resistor should be chosen to set the LT8619 switching frequency equal to or below the synchronization frequency. Do not apply external voltage to this pin.

PG (Pin 4/Pin 6): Open-Drain Power Good Output. PG remains low until the FB pin is within ±7.5% of the final regulation voltage. The PG pull-up resistor can be connected to the $INTV_{CC}$, V_{OUT} or an external supply voltage that is lower than 6V.

SYNC (Pin 5/Pin 7): External Clock Synchronization Input. Tie to a clock source for synchronization to an external frequency. During clock synchronization, the controller enters forced continuous mode. Ground the SYNC pin for Burst Mode operation. Connect to $INTV_{CC}$ to enable forced continuous mode operation. Floating this pin will enable pulse-skipping mode operation. During start-up, the controller is forced to run in pulse-skipping mode. When in pulse-skipping or forced continuous mode operation, the I_Q will be much higher compared to Burst Mode operation.

FB (Pin 6/Pin 9, 10, LT8619 Only): The LT8619 regulates the FB pin to 0.8V. Connect the feedback resistor divider tap to this pin. Also, connect a phase lead capacitor between FB and V_{OUT}. Typically, this capacitor is between 4.7pF to 10pF. Do not apply an external voltage to this pin.

OUT (Pin 9, 10, LT8619-5 MSOP Only): Connect to the regulator output V_{OUT}. The LT8619-5 regulates the OUT pin to 5V. This pin connects to the internal 10MΩ feedback divider that programs the fixed output voltage.

BIAS (Pin 7/Pin 11): The internal regulator will draw current from BIAS instead of V_{IN} when the BIAS pin is tied to a voltage higher than 3.1V. For switching regulator output voltages of 3.3V and above, this pin should be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT}, use a 1µF local bypass capacitor on this pin.

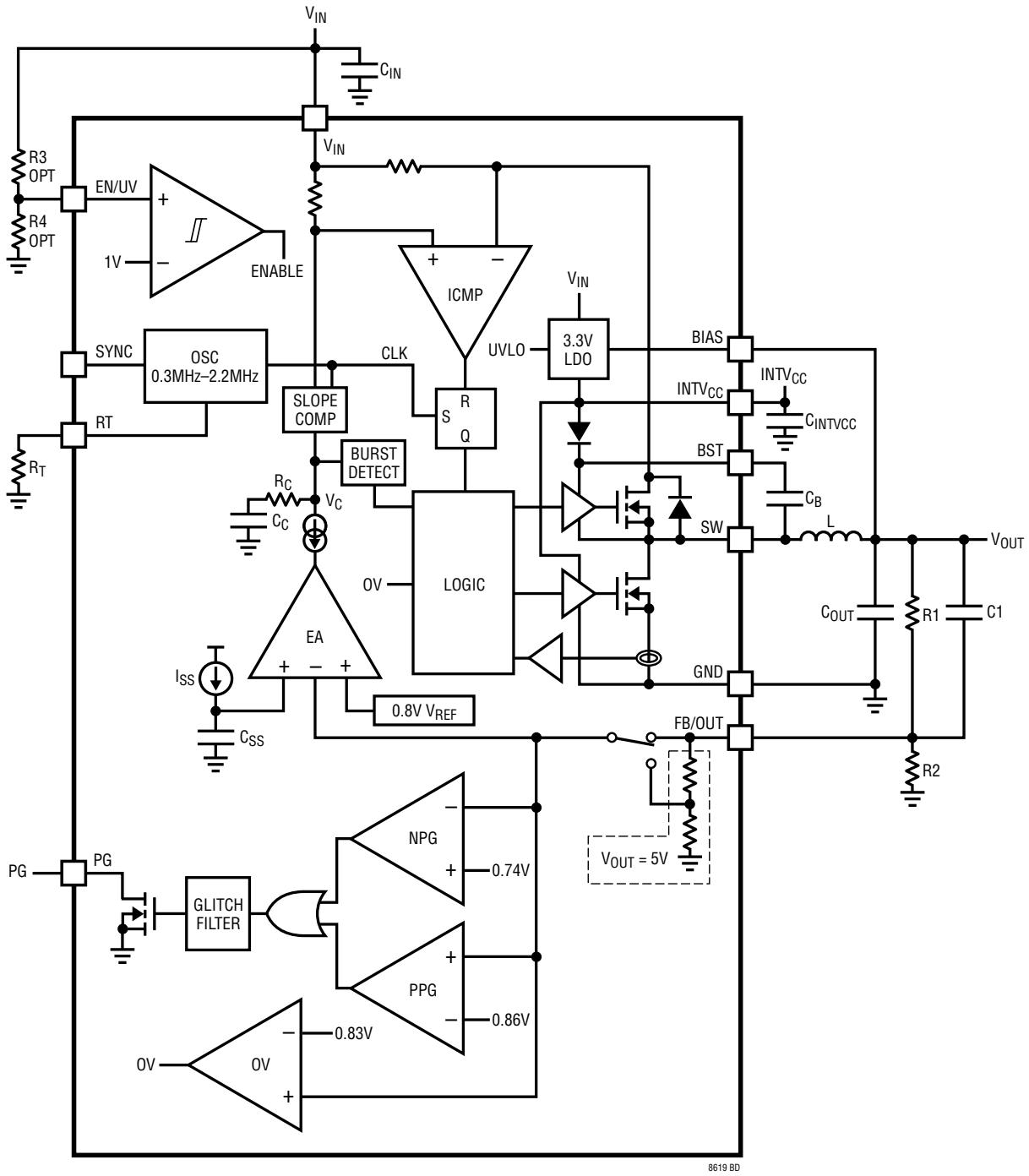
$INTV_{CC}$ (Pin 8/Pin 12): Internal 3.3V Regulator Output. The internal power drivers and control circuits are powered from this voltage. $INTV_{CC}$ maximum output current is 20mA. $INTV_{CC}$ current will be supplied from BIAS if V_{BIAS} > 3.1V, otherwise current will be drawn from V_{IN}. Voltage on $INTV_{CC}$ will vary between 2.8V and 3.3V when V_{BIAS} is between 3.0V and 3.5V. Decouple this pin to GND with at least a 1µF low ESR ceramic capacitor. Do not load the $INTV_{CC}$ pin with external circuitry.

BST (Pin 9/Pin 14): This pin is used to provide a drive voltage, higher than the input voltage, to the topside power switch. Place a 0.1µF boost capacitor as close as possible to the IC.

SW (Pin 10/Pin 15, 16): The SW pin is the output of the internal power switches. Connect this pin to the inductor and boost capacitor. This node should be kept small on the PCB for good performance.

GND (Exposed Pad Pin 11/Pin 8, Exposed Pad Pin 17): Ground. The exposed pad must be connected to the negative terminal of the input capacitor and soldered to the PCB in order to lower the thermal resistance.

BLOCK DIAGRAM



OPERATION

The LT8619 is a monolithic, constant frequency current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the internal VC node. The error amplifier servos the VC node by comparing the voltage on the FB pin with an internal 0.8V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the VC voltage until the average inductor current matches the new load current. When the top power switch turns off, the bottom power switch turns on until the next clock cycle begins or inductor current falls to zero (Burst Mode operation or pulse-skipping mode). If overload conditions result in more than 1.8A flowing through the bottom switch, the next clock cycle will be delayed until the switch current returns to a safe level.

If the EN/UV pin is low, the LT8619 is shut down and draws less than 0.6µA from the input. When the EN/UV pin is above 1V, the switching regulator starts operation. First, the internal LDO powers up, followed by the switching regulator 200µs soft-start ramp. During the soft-start phase, the switcher operates in pulse-skipping mode and gradually switches to forced continuous mode when V_{OUT} approaches the set point (if SYNC pin is forced high or connected to an external clock). Typically, upon EN/UV rising edge, it takes about 660µs for the switcher output voltage to reach regulation and PG to be asserted.

To optimize efficiency at light loads, configure the LT8619 to operate in Burst Mode by grounding the SYNC pin. At light load, in between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current. In a typical application, 6µA will be consumed from the supply when regulating with no load. Float the SYNC pin to enable pulse-skipping mode operation. While in pulse-skipping mode, the oscillator operates continuously and the bottom power switch turns off when the inductor current falls to zero. During light loads, switch pulses are skipped to regulate the output and the quiescent current will be higher than Burst Mode operation. Connecting the SYNC pin to $INTV_{CC}$ enables forced continuous mode operation. In forced continuous mode, the inductor current is allowed to reverse and the switcher operates at a fixed frequency. If a clock is applied to the SYNC pin, the part operates in forced continuous mode and synchronizes to the external clock frequency; with the rising SW signal synchronized to the external clock positive edge.

To improve efficiency across all loads, supply current to internal circuitry can be sourced from the BIAS pin when biased above 3.1V. Else, the internal circuitry will draw current from V_{IN}. The BIAS pin should be connected to V_{OUT} if the LT8619 output is programmed to 3.3V or above.

An overvoltage comparator, OV, guards against transient overshoots. If V_{FB} is higher than 0.83V, the OV comparator trips, disables the top MOSFET and turns on the bottom power switch until the next clock cycle begins or the inductor reverse current reaches 0.55A. With high reverse current, both top and bottom MOSFETs shut off till the next cycle. Positive and negative power good comparators pull the PG pin low if the FB voltage varies more than ±7.5% (typical) from the set point.

The oscillator reduces the LT8619's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the inductor current when the output voltage is lower than the programmed value which occurs during overcurrent conditions.

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Achieving Ultralow Quiescent Current

To enhance efficiency at light loads, the LT8619 enters into Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and output ripple voltage. In Burst Mode operation the LT8619 delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode the LT8619 consumes less than 6µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT8619 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. For a typical application, when the output is not loaded, by maximizing the time between pulses, the regulator quiescent approaches 6µA. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current (See FB Resistor Network section).

While in Burst Mode operation, the current limit of the top switch is approximately 380mA resulting in output voltage ripple shown in Figure 2. Increasing the output capacitance will decrease the output ripple proportionally. As load ramps upward from zero, the switching frequency will increase but only up to the switching frequency programmed by the resistor at the RT pin as shown in Figure 1. The output load at which the LT8619 reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice.

For some applications it is desirable for the LT8619 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First, the minimum inductor current clamp present in Burst Mode operation is removed, providing a smaller packet of charge to the output capacitor and reduce the output ripple voltage. For a given load, the chip awake more often, resulting in higher supply current compared to Burst Mode operation. Second is that full switching frequency is reached at lower output load than in Burst Mode operation (see Figure 3). To enable pulse-skipping mode, leave the SYNC pin floating. Tying the SYNC pin to $INTV_{CC}$ node enables the programmed switching frequency at no load.

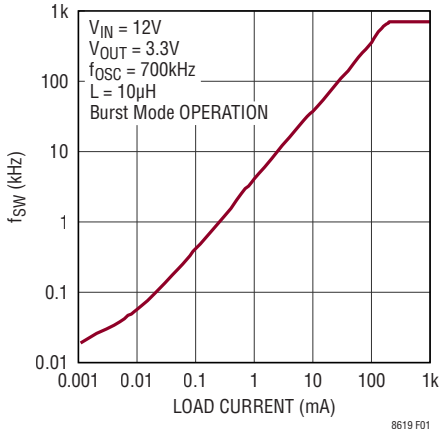


Figure 1. Burst Frequency vs Load Current

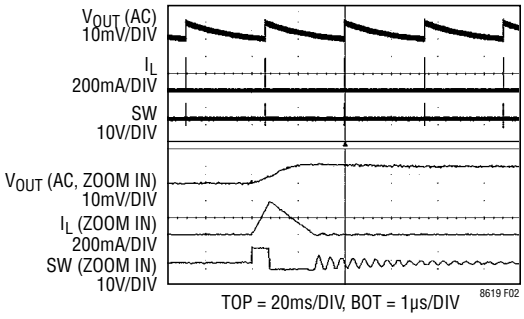


Figure 2. Burst Mode Operation Waveform with V_{IN} = 12V, V_{OUT} = 3.3V at No Load, R_T = 66.5k, L = 10µH, C_{OUT} = 22µF

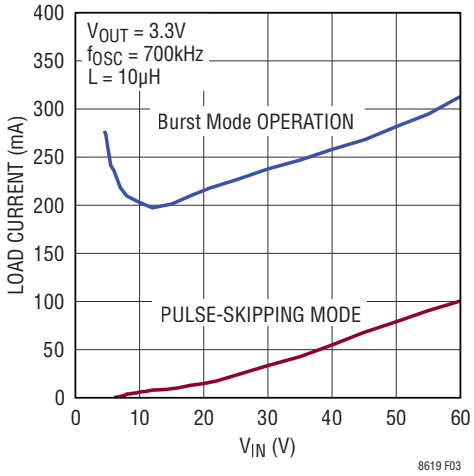


Figure 3. Minimum Load for Full Frequency Operation vs V_{IN} in Burst Mode Operation and Pulse-Skipping Mode Setting

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FB Resistor Network

The output voltage is programmed with a resistor divider between V_{OUT} and the FB pin. Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT}}{0.8V} - 1\right)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

If low input quiescent current and good light-load efficiency are desired, use a large resistor value for the FB resistor divider. The current flowing in the divider acts as a load current, and will increase the no-load input current to the converter, which is approximately:

$$I_Q = 5.2\mu A + \left(\frac{V_{OUT}}{R1+R2}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{\eta}\right)$$

where 5.2µA is the quiescent current of the LT8619 and the second term is the current in the feedback divider reflected to the input of the buck operating at its light load efficiency, η. For a 3.3V application with R1 = 1M and R2 = 316k, the feedback divider draws 2.5µA from V_{OUT}. With V_{IN} = 12V and η = 85%, this adds 0.8µA to the 5.2µA quiescent current resulting in 6µA quiescent current from the 12V supply. Note that this equation implies that the no-load current is a function of V_{IN}; this is plotted in the Typical Performance Characteristics section.

When using large FB resistors, a 4.7pF to 10pF phase lead capacitor, C1, should be connected from V_{OUT} to FB.

Setting the Switching Frequency

The LT8619 uses a constant frequency PWM architecture that can be programmed to switch from 300kHz to 2.2MHz by using a resistor tied from the RT pin to ground. The R_T resistor required for a desired oscillator frequency can be roughly obtain using:

$$R_T = \frac{50.07}{f_{OSC}} - 5$$

where R_T is in kΩ and f_{OSC} is the desired switching frequency in MHz.

Table 1 and Figure 4 show the typical R_T value for a desired oscillator frequency.

Table 1. Oscillator Frequency vs R_T Value (1% Standard Value)

f_{OSC} (MHz)	R_T (kΩ)	f_{OSC} (MHz)	R_T (kΩ)
0.3	162	1.4	30.9
0.4	121	1.6	26.1
0.5	95.3	1.8	22.6
0.6	78.7	2.0	20.0
0.7	66.5	2.2	17.8
0.8	57.6		
0.9	51.1		
1.0	45.3		
1.2	36.5		

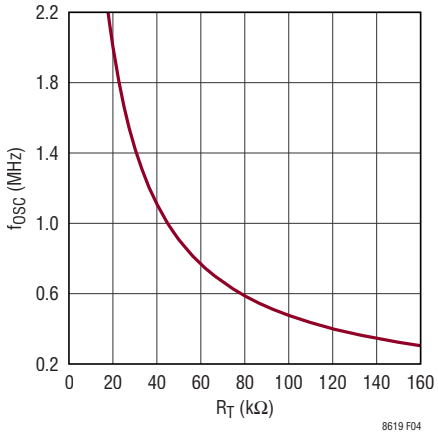


Figure 4. Oscillator Frequency vs R_T Value

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

For force continuous mode operation, the highest oscillator frequency ($f_{OSC(MAX)}$) for a given application can be approximately given by the 1st order equation:

$$f_{OSC(MAX)} = \frac{I_{LOAD}R_{SW(BOT)} + V_{OUT}}{t_{ON(MIN)}\left(V_{IN} - I_{LOAD}R_{SW(TOP)} + I_{LOAD}R_{SW(BOT)}\right)}$$

Where V_{IN} is the input voltage, V_{OUT} is the output voltage, $R_{SW(TOP)}$ and $R_{SW(BOT)}$ are the internal switch on resistance (~0.45Ω, ~0.22Ω, respectively) and $t_{ON(MIN)}$

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is the minimum top switch on-time at the loading condition as shown in Figure 5. Figure 6 shows the relationship between the maximum input voltage vs the switching frequency. If a smaller R_T is selected, to ensure that the regulator is switching at the higher frequency as illustrated in Figure 4, the maximum input supply voltage has to be lowered; and it needs to be further reduced if the load is decreased or removed.

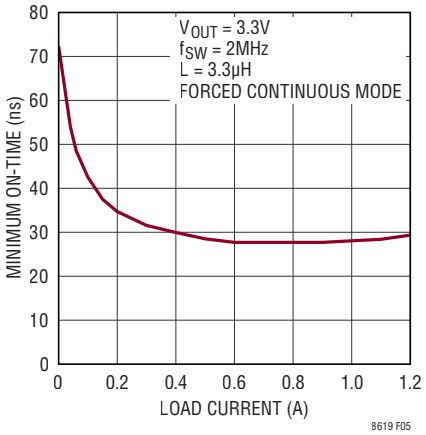


Figure 5. Minimum On-Time vs Load Current

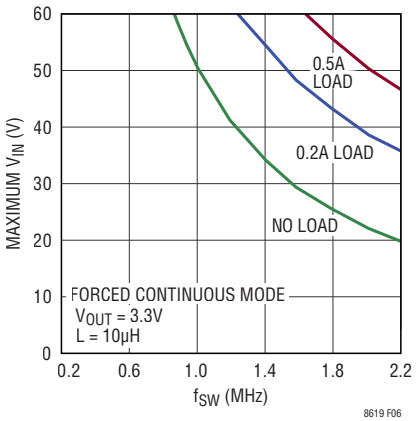


Figure 6. Forced Continuous Mode Maximum Input Voltage vs Switching Frequency

High Supply Operation

For Burst Mode operation or pulse-skipping mode, V_{IN} voltage may go as high as the absolute maximum rating of 60V regardless of the frequency setting; however, the LT8619 will reduce the switching frequency as necessary to regulate the output voltage.

For forced continuous mode, if there is a momentarily V_{IN} voltage surge higher than the voltage shown in Figure 6, resulting in minimum on-time operation, an overvoltage comparator guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the V_{FB} voltage rises by more than 3.75% above its nominal value, the top MOSFET is turned off and the bottom MOSFET is turned on. At this moment, the output voltage continues to increase until the inductor current reverses. The actual peak output voltage will be higher than 3.75%, depending on external components value, loading condition and output voltage setting. The bottom MOSFET remains on continuously until the inductor current exceeds the bottom MOSFET reverse current or overvoltage condition is cleared. With high reverse current, both top and bottom MOSFETs shut off till the next clock cycle.

Low Supply Operation

The LT8619 is designed to remain operational during short line transients when the input voltage may briefly dip below 3.0V. Below this voltage, the $INTV_{CC}$ voltage might drop to a point that is not able to provide adequate gate drive voltage to turn on the MOSFET. The LT8619 has two circuits to detect this undervoltage condition. A UVLO comparator monitors the $INTV_{CC}$ voltage to ensure that it is above 2.8V during startup; once in regulation, the chip continues to operate as long as $INTV_{CC}$ stays above 2.65V. If this UVLO comparator trips, the chip is shut down until $INTV_{CC}$ recovers. Another comparator monitors the V_{IN} supply voltage, add a resistor divider from V_{IN} to EN/UV to turn off the regulator if V_{IN} dips below the undesirable voltage.

The LT8619 is capable of a maximum duty cycle of greater than 99%, and the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In deep dropout, the loop attempt to turn on the top switch continuously. However, the top switch gate drive is biased from the floating boot-strap capacitor C_B, which normally recharges during each off cycle; in dropout, this capacitor loses its refresh cycle and charge depleted. A comparator detects the drop in boot-strap capacitor voltage, forces the top switch off and recharges the capacitor.

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For low V_{IN} applications that cannot allow deviation from the programmed oscillator frequency, use the following formula to set the switching frequency:

$$V_{IN(MIN)} = \frac{V_{SW(BOT)} + V_{OUT}}{1 - t_{OFF(MIN)} \bullet f_{OSC}} + V_{SW(TOP)} - V_{SW(BOT)}$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.54V, ~0.264V, respectively at maximum load), f_{OSC} is the oscillating frequency (set by R_T), and $t_{OFF(MIN)}$ is the minimum switching off-time. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

Inductor Selection and Maximum Output Current

The LT8619 is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions the LT8619 safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is:

$$L = 2\frac{V_{OUT} + V_{SW(BOT)}}{f_{OSC}}$$

where f_{OSC} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.264V) and L is the inductor value in µH.

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus one-half of inductor ripple current:

$$I_{SAT} > I_{LOAD(MAX)} + \frac{\Delta I_{L(MAX)}}{2}$$

where $I_{LOAD(MAX)}$ is the maximum output load for a given application and $\Delta I_{L(MAX)}$ is the inductor ripple current as calculated in the following equation:

$$\Delta I_{L(MAX)} = \frac{1}{f_{OSC} \bullet L} V_{OUT}\left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

As a quick example, an application requiring 1A output current should use an inductor with an RMS rating of greater than 1A and an I_{SAT} of greater than 1.5A. During long duration overload or short-circuit conditions, the inductor RMS rating requirement is greater to avoid overheating of the inductor. To push for high efficiency, select an inductor with low series resistance (DCR), preferably below 0.04Ω, and the core material should be intended for high frequency application. However, achieving this requires a large size inductor. An inductor with DCR around 0.1Ω is generally a good compromise for both efficiency and board area, at the expense of trimming 1% to 2% from the efficiency number.

The LT8619 limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is at least 1.5A. The inductor value must then be sufficient to supply the desired maximum output current ($I_{LOAD(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current:

$$I_{LOAD(MAX)} = I_{LIM} - \frac{\Delta I_L}{2}$$

Therefore, the maximum output current that the LT8619 will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{LOAD(MAX)}$) given the switching frequency, and maximum input voltage used in the desired application.

In order to achieve higher light load efficiency, more energy must be delivered to the output during single small pulses in Burst Mode operation such that the LT8619 can

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stay in sleep mode longer between each pulse. This can be achieved by using a larger value inductor, and should be considered independent of switching frequency when choosing an inductor. For example, while a lower inductor value would typically be used for a high switching frequency application, if high light load efficiency is desired, a higher inductor value should be chosen.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower and the LT8619 may operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that low inductance may result in discontinuous mode operation, which further reduces maximum load current.

For details of maximum output current and discontinuous operation, see Analog Devices Application Note 44.

Input Capacitor

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT8619 and to force this very high frequency switching current into a tight local loop, minimizing EMI. In continuous mode, the input capacitor RMS current is given by:

$$I_{RMS(MAX)} \approx I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}\left(V_{IN}-V_{OUT}\right)}}{V_{IN}}$$

This equation has a maximum RMS current at V_{IN} = $2V_{OUT}$, where $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$.

Bypass the input of the LT8619 circuit with a 2.2µF to 10µF ceramic capacitor of X7R or X5R type placed as close as possible to the V_{IN} and GND pin. Y5V types have poor performance over temperature and applied voltage, and should not be used. Note that larger input capacitance is required when a lower switching frequency is used.

If the input power source has high impedance, or there is significant inductance due to long wires or cables, a ceramic input capacitor combined with the trace or cable inductance forms a high quality (underdamped) tank circuit. If the LT8619 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8619's voltage rating. This situation is easily avoided (see Analog Devices Application Note 88), by adding a lossy electrolytic capacitor in parallel with the ceramic capacitor.

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8619 to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8619's control loop. The current slew rate of a regulator is limited by the inductor and feedback loop. When the amount of current required by the load changes, the initial current deficit must be supplied by the output capacitor until the feedback loop reacts and compensates for the load changes. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. For good starting values, see the Typical Application section.

Transient performance can be improved with a higher value capacitor and the addition of a feedforward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. See the Typical Application in this data sheet for suggested capacitor values.

Ceramic Capacitors

When choosing a capacitor, special attention should be given to the manufacturer's data sheet in order to accurately calculate the effective capacitance under the relevant bias voltage and operating temperature conditions. Ceramic dielectrics can offer near ideal performance as

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an output capacitor, i.e. high volumetric efficiency with extremely low equivalent resistance. There is a downside however; the high K dielectric material exhibits a substantial temperature and voltage coefficient, meaning that its capacitance varies depending on the operating temperature and applied voltage. X7R capacitors provide a range intermediate capacitance values which varies only ±15% over the temperature range of –55°C to 125°C. The Y5V capacitance can vary from 22% to –82% over the –30°C to 85°C temperature range and should not be used for the LT8619 application.

Figure 7 shows the voltage coefficient of four different ceramic 22µF capacitors, all of which are rated for 16V operation. Note that with the exception of the X7R in the 1210 and 1812 package, the capacitors lose more than 30% of their capacitance when biased at more than half of the rated voltage. Typically, as the package size increases, the bias voltage coefficient decreases. If the voltage coefficient of a big ceramic capacitor in a particular package size is not acceptable; multiple smaller capacitors with less voltage coefficient can be placed in parallel as an effective means of meeting the capacitance requirement. *Not All Capacitors are Interchangeable*. A wrong capacitor selection can degrade the circuit performance considerably.

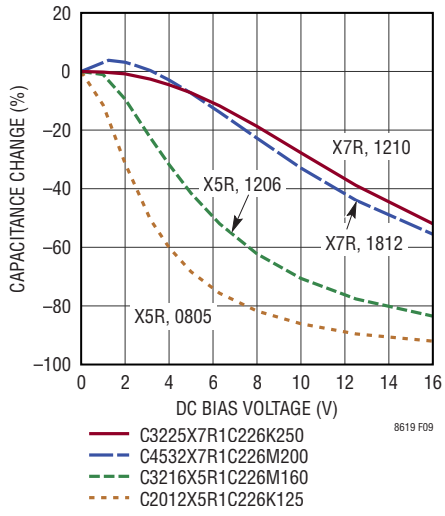


Figure 7. Ceramic Capacitor Voltage Coefficient

Ceramic capacitors can also cause problems due to their piezoelectric nature. During Burst Mode operation, the switching frequency depends on the load current, and at very light loads the LT8619 can excite the ceramic capacitor at frequencies that may generate audible noise. Since the LT8619 operates at a lower inductor current during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, consider using a high performance tantalum or electrolytic capacitor at the output instead. Low noise ceramic capacitors are also available.

Ceramic capacitors are also susceptible to mechanical stress which can result in significant loss of capacitance. The most common sources of mechanical stress includes bending or flexure of the PCB, contact pressure during in circuit parameter testing, and direct contact by a soldering iron tip. Consult the manufacturer's application notes for additional information regarding ceramic capacitor handling.

Enable Pin

The LT8619 is in shutdown when the EN/UV pin is low and active when the pin is high. The power-on threshold of the EN comparator is 1.0V, with 40mV of hysteresis, once EN/UV drops below this power-on threshold, the MOSFETs are disabled, but the internal biasing circuit stays alive. When forced below 0.56V, all the internal blocks are disabled and the IC is put into a low current shutdown mode. The EN/UV pin can be tied to V_{IN} if the shutdown feature is not used.

Adding a resistor divider from V_{IN} to EN/UV programs the LT8619 to regulate the output only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(EN/UV)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN/UV)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This

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threshold can be adjusted by setting the values R3 and R4 such that they satisfy the following equation:

$$V_{IN(EN/UV)} = \left(1 + \frac{R3}{R4}\right) \bullet 1V$$

where the LT8619 will remain off until V_{IN} is above $V_{IN(EN/UV)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN/UV)}$.

When in Burst Mode operation for light load currents, the current through the $V_{IN(EN/UV)}$ resistor network can easily be greater than the supply current consumed by the LT8619. Therefore, the $V_{IN(EN/UV)}$ resistors should be large enough to minimize their impact on efficiency at low loads.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.3V supply from V_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply enough current for the LT8619's circuitry and must be bypassed to ground with at least a 1µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. To improve efficiency the internal LDO can draw current from the BIAS pin when the BIAS pin is at 3.1V or higher. Typically the BIAS pin can be tied to the output of the switching regulator, or can be tied to an external supply which must also be at 3.3V or above. If BIAS is connected to a supply other than V_{OUT}, be sure to bypass with a local ceramic capacitor. If the BIAS pin is below 3.0V, the internal LDO will consume current from V_{IN}. Applications with high input voltage and high switching frequency where the internal LDO pulls current from V_{IN} will increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the $INTV_{CC}$ pin.

Output Power Good

When the LT8619's output voltage is within the ±7.5% window of the regulation point, the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal open-drain transistor will pull the PG pin low. The PG pin is also actively pulled low during several fault conditions: EN/UV pin is below 1V, $INTV_{CC}$ drops below its UVLO threshold, V_{IN} is too low, or thermal shutdown.

Synchronization

Synchronizing the LT8619 oscillator to an external frequency can be done by connecting a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 2V (up to 6V). During frequency synchronization, the part operates in forced continuous mode with the SW rising edge synchronized to the SYNC positive edge. The LT8619 may be synchronized over a 300kHz to 2.2MHz range. The R_T resistor must be chosen to set the LT8619 switching frequency equal or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the R_T should be selected for 500kHz.

Start-Up Inrush Current, Short-Circuit Protection

Upon start-up, the internal soft-start action regulates the V_{OUT} slew rate; the LT8619 provides the maximum rated output current to charge up the output capacitor as quickly as possible. During start-up, if the output is overloaded, the regulator continues to provide the maximum sourcing current to overcome the output load, but at the same time, the bottom switch current is monitored such that if the inductor current is beyond the safe levels, switching of the top switch will be delay until such time as the inductor current falls to safe levels.

Once the soft-start period has expired and the FB voltage is higher than 0.74V, the LT8619 switching frequency will be folded back if the external load pulls down the output. At the same time, the bottom switch current will continue to be monitored to limit the short-circuit current. Figure 8 shows the frequency foldback transfer curve and Figure 9 shows the short circuit waveform. During this overcurrent condition, if the SYNC pin is connected to a clock source, the LT8619 will get out from the synchronization mode.

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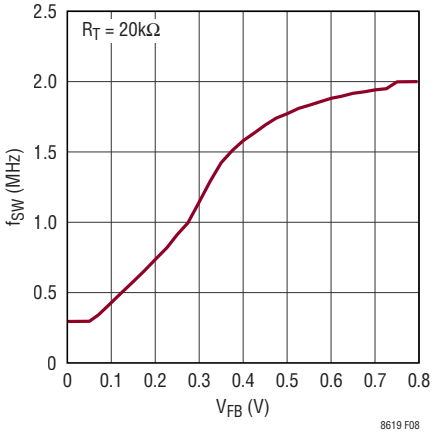


Figure 8. Frequency Foldback Transfer Function

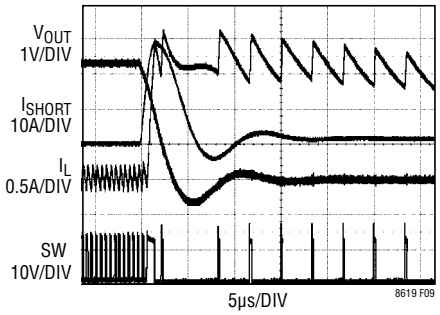


Figure 9. Short-Circuit Waveform with V_{IN} = 12V, V_{OUT} = 3.3V, f_{OSC} = 2MHz, L = 4.7µH, C_{OUT} = 22µF

Reversed Input Protection

Load protection may be necessary in systems where the output will be held high when the input to the LT8619 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LT8619's output. If the V_{IN} pin is allowed to float and the EN/UV pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT8619's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate several µA in this state. If the EN/UV pin is grounded the SW pin current will drop to near 1µA. However, if the V_{IN} pin is grounded while the output is held high, regardless of EN/UV, parasitic body diodes inside the LT8619 can pull current from the output through the SW pin and the V_{IN} pin. Figure 10 shows a connection of the V_{IN} and EN/UV pins that will allow the LT8619 to run only when the input voltage is present and that protects against a shorted or reversed input.

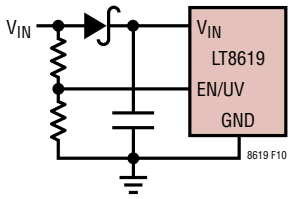


Figure 10. Reverse V_{IN} Protection

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board (PCB) layout. Figure 11 and Figure 12 show the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT8619's V_{IN}, SW, GND pins, and the input capacitor. The loop formed by these components should be as small as possible by placing the capacitor adjacent to the V_{IN} and GND pins. When using a physically large input capacitor, the resulting loop may become too large in which case using a small case/value capacitor placed close to the V_{IN} and GND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BST nodes should be as small as possible. Finally, keep the FB and RT nodes small so that the ground traces will shield them from the SW and BST nodes. The exposed pad on the bottom of the package must be soldered to ground so that the pad is connected to ground electrically and also acts as a heat sink thermally. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT8619 to additional ground planes within the circuit board and on the bottom side.

High Temperature Output Current Considerations

The maximum practical continuous load that the LT8619 can drive, while rated at 1.2A, actually depends upon both the internal current limit (refer to the Typical Performance Characteristics section) and the internal temperature which depends on operating conditions, PCB layout and airflow.

APPLICATIONS INFORMATION

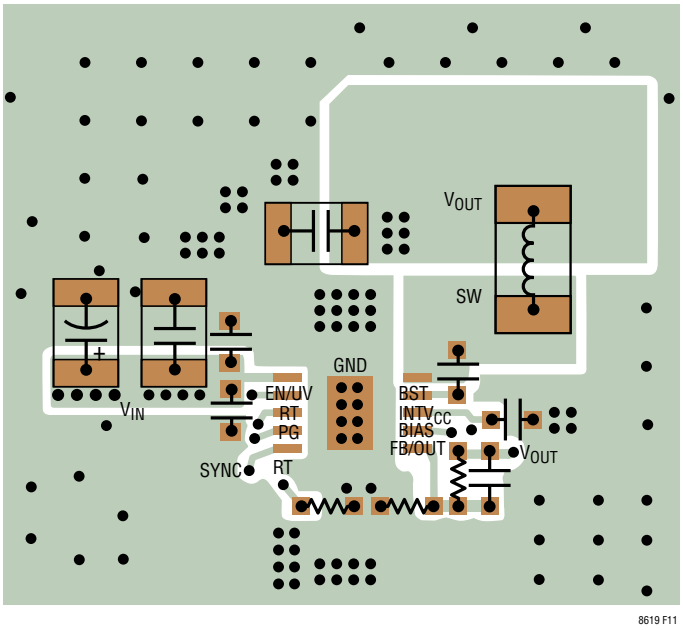


Figure 11. Recommended PCB Layout for LT8619 10-Pin DFN

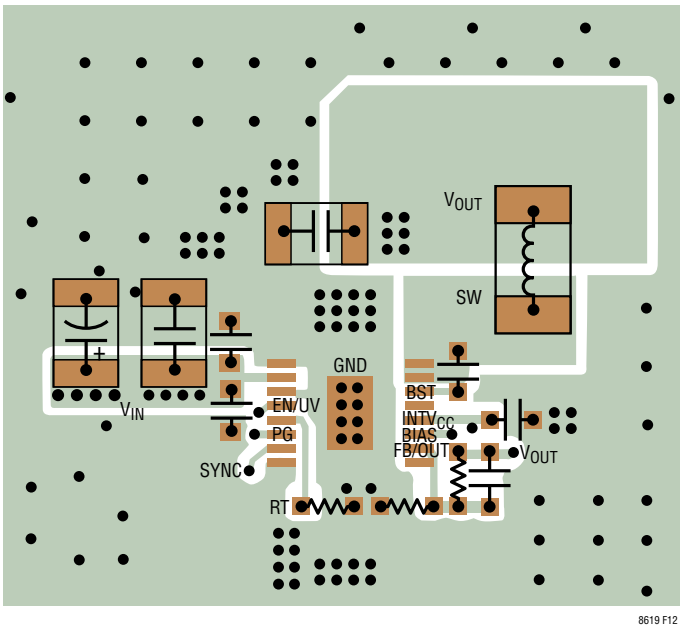


Figure 12. Recommended PCB Layout for LT8619 16-Pin MSOP

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For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8619. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8619. Placing additional vias can reduce thermal resistance further. Figure 13 shows the rise in case temperature vs load current. Note that a higher ambient temperature will result in bigger case temperature rise as shown in Figure 14. Power dissipation within the LT8619 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8619 power dissipation by the thermal resistance from junction to ambient.

Figure 15 shows the typical derating maximum output current curve. As with any monolithic switching regulator, the PCB layout, thermal resistance, air flow, other heat sources in the vicinity affect how efficiently heat can be removed from the die and radically change the die junction temperature. The actual LT8619 switcher output voltage and current sourcing capability might deviate from the performance curve stated in this data sheet. When pushing the LT8619 to its limit, verify its operation in the actual environment. **AT HIGH AMBIENT TEMPERATURE, CONTINUOUS OPERATION ABOVE THE MAXIMUM OPERATION JUNCTION TEMPERATURE MAY IMPAIR DEVICE RELIABILITY OR PERMANENTLY DAMAGE THE DEVICE.**

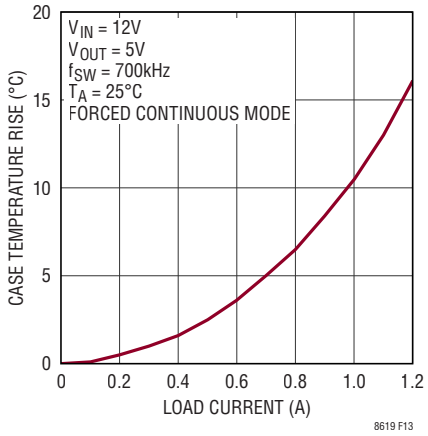


Figure 13. Case Temperature Rise vs Load Current

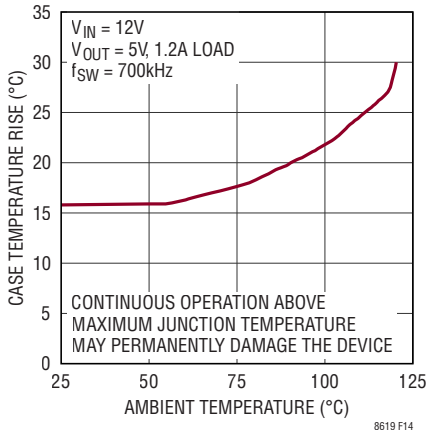


Figure 14. Case Temperature Rise vs Ambient Temperature

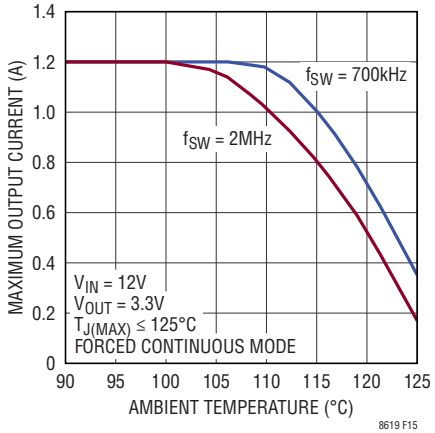
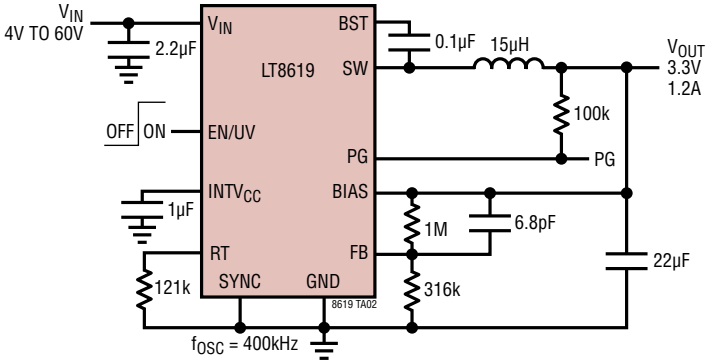


Figure 15. LT8619 Derating Maximum Output Current with Junction Temperature Less Than 125°C

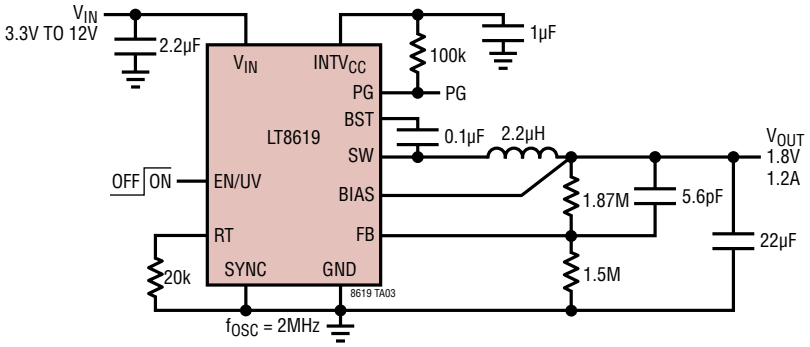
TYPICAL APPLICATIONS

3.3V 400kHz Step-Down Converter



L = VISHAY IHLP-3232CZ-11
C_{OUT} = TDK C3225X7R1C226K250

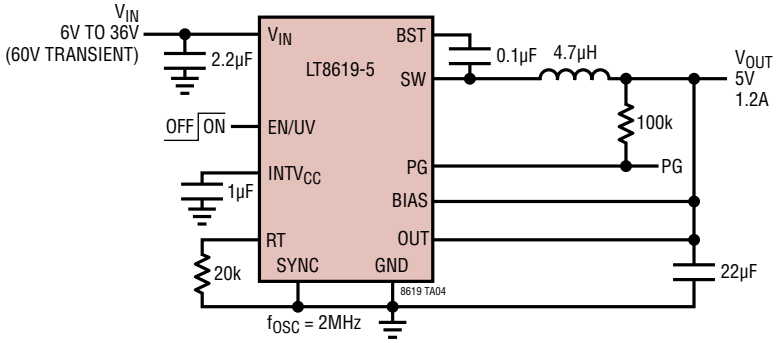
1.8V 2MHz Step-Down Converter



L = VISHAY IHLP-2020AB-01
C_{OUT} = TDK C3225X7R1C226K250

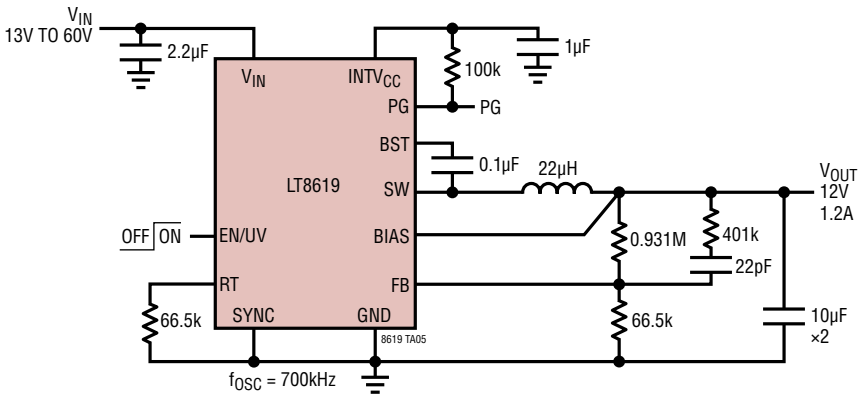
TYPICAL APPLICATIONS

5V 2MHz Step-Down Converter



L = VISHAY IHLP-2020BZ-01
C_{OUT} = TDK C3225X7R1C226K250

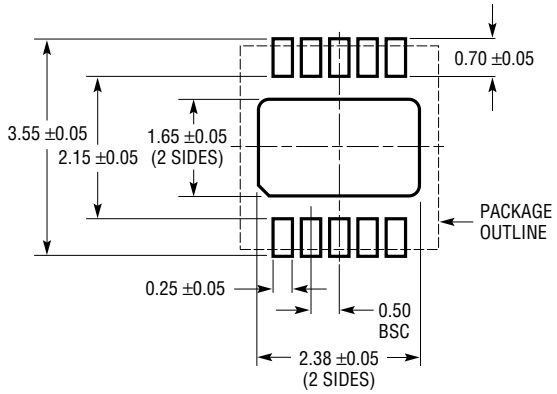
12V 700kHz Step-Down Converter



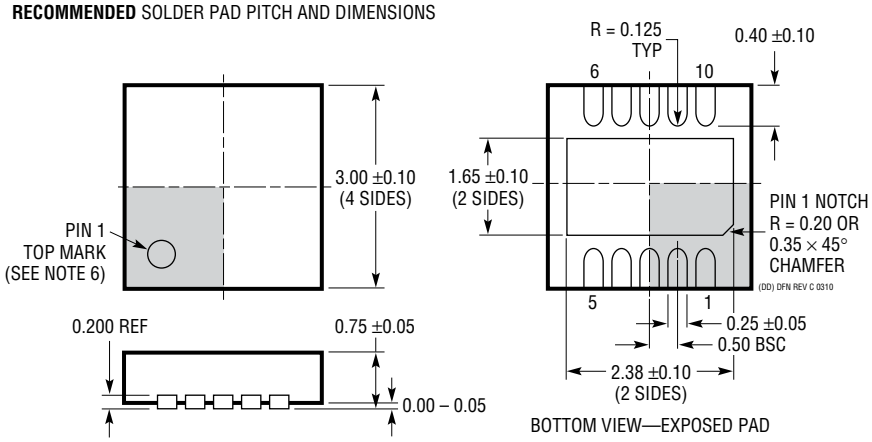
L = VISHAY IHLP-2020CZ-11
C_{OUT} = MURATA GRM32ER7YA106K

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

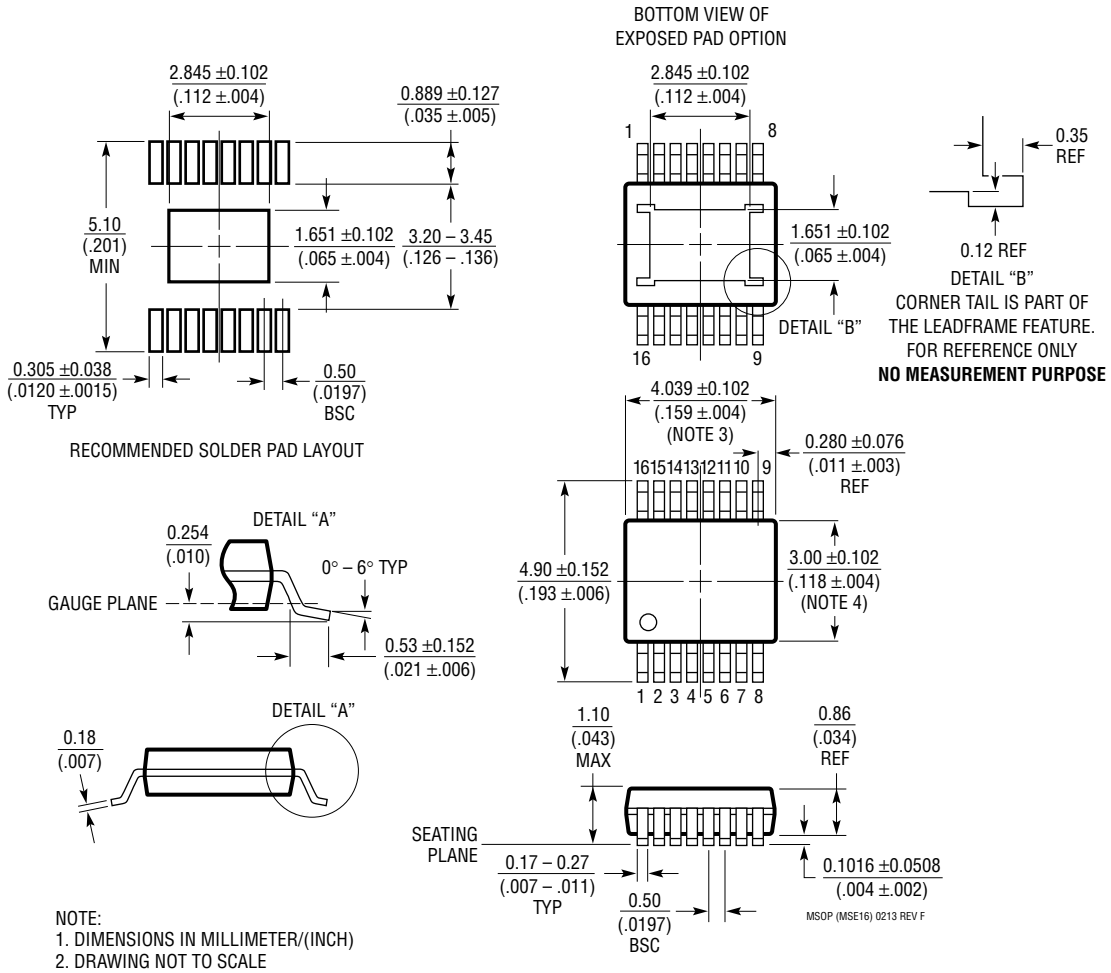


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

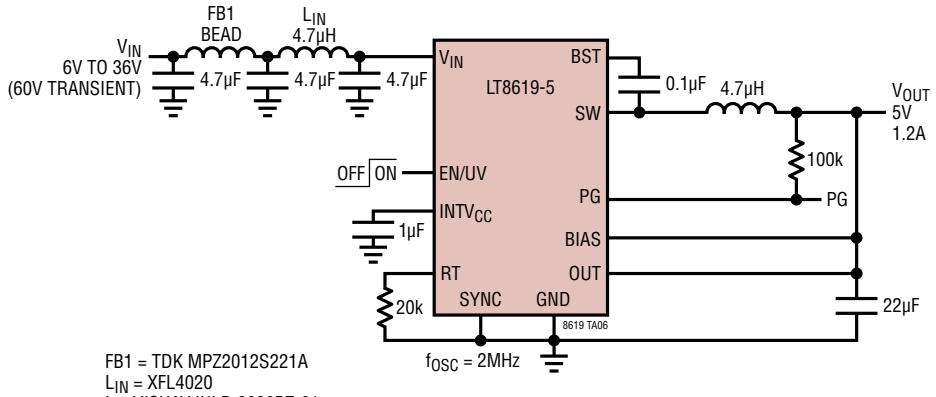
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/18	Clarified SYNC Threshold Units	3
		Clarified Efficiency at V_{OUT} = 5V	5
B	10/19	Clarified Conditions on V_{IN} Quiescent Current at No Load and In Regulation	3
		Added Note 5 to Feedback Voltage Line Regulation	3
		Added Note 5	4
C	01/21	AEC-Q100 Qualified for Automotive Applications	1
		#W Materials added on	2

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TYPICAL APPLICATION

Ultralow EMI 5V 2MHz Step-Down Converter



FB1 = TDK MPZ2012S221A
L_{IN} = XFL4020
L = VISHAY IHLP-2020BZ-01
C_{OUT} = TDK C3225X7R1C226K250

RELATED PARTS

PART	DESCRIPTION	COMMENTS
LT8602	42V, Quad Output (2.5A + 1.5A + 1.5A + 1.5A) 95% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 25µA	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, 6mm × 6mm QFN-40
LT8609/LT8609A	42V, 2A, 94% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-10E
LT8610	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step- Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E
LT8610A/LT8610AB	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step- Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E
LT8610AC	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step- Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E
LT8611	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step- Down DC/DC Converter with I_Q = 2.5µA and Input/Output Current Limit/Monitor	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 5mm QFN-24
LT8612	42V, 6A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 3.0µA, I_{SD} < 1µA, 3mm × 6mm QFN-28
LT8613	42V, 6A, 96% Efficiency, 2.2MHz Synchronous Micropower Step- Down DC/DC Converter with Current Limiting	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 3.0µA, I_{SD} < 1µA, 3mm × 6mm QFN-28
LT8614	42V, 4A, 96% Efficiency, 2.2MHz Synchronous Silent Switcher Step- Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN-18
LT8616	42V, Dual 2.5A + 1.5A, 95% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 5µA, I_{SD} < 1µA, TSSOP-28E, 3mm × 6mm QFN-28
LT8620	65V, 2.5A, 94% Efficiency, 2.2MHz Synchronous Micropower Step- Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 65V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, ISD < 1µA, MSOP-16E, 3mm × 5mm QFN-24
LT8640/LT8640-1	42V, 5A, 96% Efficiency, 3MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN-18

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