Stereo 2.6W Audio Amplifier (With Gain Control)

Features

- **Low Operating Current with 6mA**
- **Improved Depop Circuitry to Eliminate Turn-On Transients in Outputs**
- **High PSRR**
- **Internal Gain Control, Eliminate External Components**
- **2.6W Per Channel Output Power into 3Ω Load at 5V, BTL Mode**
- **Multiple Input Modes Allowable Selected by HP/$\overline{\text{LINE}}$ Pin (APA2030)**
- **Two Output Modes Allowable with BTL and SE Modes Selected by SE/$\overline{\text{BTL}}$ Pin (for APA2030 only)**
- **Low Current Consumption in Shutdown Mode (50μA)**
- **Short Circuit Protection**
- **TSSOP-24P (APA2030), TSSOP-20P, and TQFN3x3-16 (APA2031) with Thermal Pad Packages.**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

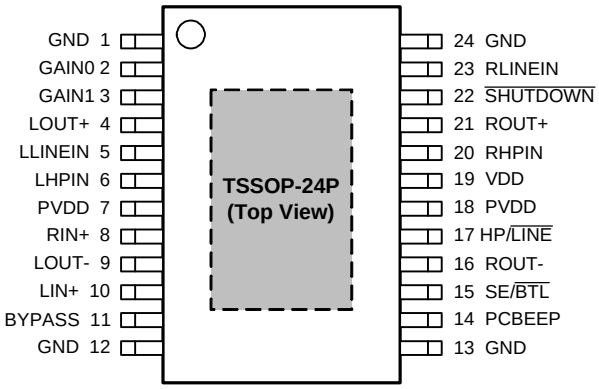
- **Notebook PCs**
- **LCD Monitor**

General Description

APA2030/1 is a monolithic integrated circuit, which provides internal gain control, and a stereo bridged audio power amplifiers capable of producing 2.6W (1.9W) into 3Ω with less than 10% (1.0%) THD+N. By controlling the two gain setting pins, Gain0 and Gain1, the amplifier can provide 6dB, 10dB, 15.6dB, and 21.6dB gain settings. The advantage of internal gain setting can be less components and PCB area. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in APA2030/1, that reduces pops and clicks noise during power up or shutdown mode operation. It also improves the power off pop noise and protects the chip from being destroyed by over temperature and short current failure. To simplify the audio system design, APA2030 combines a stereo bridge-tied loads ($\overline{\text{BTL}}$) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/$\overline{\text{BTL}}$ input control pin signal. In addition, the multiple input selections are used for portable audio system. The APA2031 eliminates both input selection and single-end (SE) mode function to simplify the design and save the PCB space.

Pin Configuration

APA2030

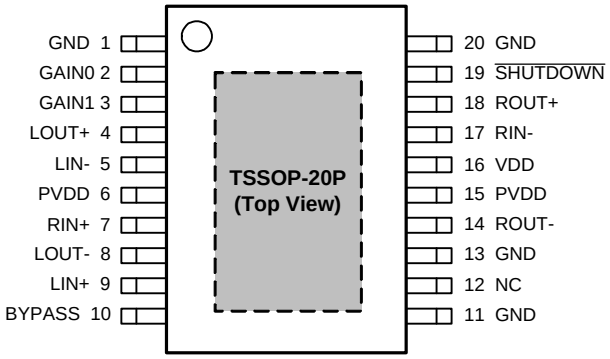


= ThermalPad (connected the ThermalPad to GND plane for better heat dissipation)

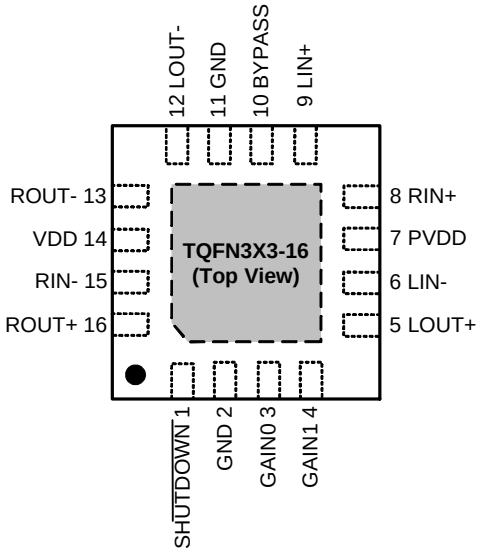
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Pin Configuration (Cont.)

APA2031



= ThermalPad (connected the ThermalPad to GND plane for better heat dissipation)



Ordering and Marking Information

APA2030 □□□-□□□ APA2031 Assembly Material Handling Code Temperature Range Package Code	Package Code R : TSSOP-24P (APA2030) / TSSOP-20P (APA2031) QB : TQFN3x3-16 (APA2031) Operating Ambient Temperature Range I : - 40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA2030 R : APA2030 XXXXX	XXXXX - Date Code
APA2031 R : APA2031 XXXXX	XXXXX - Date Code
APA2031 QB : APA 2031 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

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Absolute Maximum Ratings (Note 1)

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
	Supply Voltage Range, VDD, PVDD	-0.3V to 6V	V
	Input Voltage Range at SE/$\overline{BTL}$, HP/$\overline{LINE}$, $\overline{SHUTDOWN}$,	-0.3V to V_{DD}	V
T_A	Operating Ambient Temperature Range	-40 °C to 85 °C	°C
T_J	Maximum Junction Temperature	Internal Limited	
T_{STG}	Storage Temperature Range	-65 °C to 150 °C	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260 °C	°C
P_D	Power dissipation	Internal Limited	

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance from Junction to Ambient in Free Air (Note 2) TSSOP-24P TSSOP-20P TQFN3x3-16	 45 48 55	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. * 5 in^2 printed circuit board with 2oz trace and copper pad through 9 25mil diameter vias. The thermal pad on the TSSOP_P and TQFN3x3-16 packages with solder on the printed circuit board.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{DD}	Supply Voltage	4.5V to 5.5V	V

Electrical Characteristics

(V_{DD}=5V, -20°C<T_A<85°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	APA2030 / 2031			Unit
			Min.	Typ.	Max.	
V_{DD}	Supply Voltage		3.3	-	5.5	V
I_{DD}	Supply Current	SE/$\overline{BTL}$ = 0V	-	6	12	mA
		SE/$\overline{BTL}$ = 5V	-	4	8	mA
I_{SD}	Supply Current in Shutdown Mode	$\overline{SHUTDOWN}$ = 0V	-	50	300	µA
V_{IH}	High Level Threshold Voltage	$\overline{SHUTDOWN}$, GAIN0, GAIN1	2	-	-	V
		SE/$\overline{BTL}$, HP/$\overline{LINE}$	4	-	-	V
V_{IL}	Low level Threshold Voltage	$\overline{SHUTDOWN}$, GAIN0, GAIN1	-	-	0.8	V
		SE/$\overline{BTL}$, HP/$\overline{LINE}$	-	-	3	V

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Electrical Characteristics (Cont.)

(V_{DD}=5V, -20°C<T_A<85°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	APA2030/2031			Unit
			Min.	Typ.	Max.	
I_I	Input Current	$\overline{SHUTDOWN}$, SE/$\overline{BTL}$, HP/$\overline{LINE}$, GAIN0, GAIN1	-	5	-	nA
V_{ICM}	Common Mode Input Voltage		V_{DD}-1.0	-	-	V
V_{OS}	Output Differential Voltage		-	5	-	mV
	PC-BEEP Trigger Level		-	1	-	Vp.p
R_{BYPASS}	BYPASS Equivalent Resistance		-	250	-	kΩ

Operating Characteristics, BTL mode

V_{DD}=5V, T_A=25°C, R_L=4W, Gain=6dB, (Unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2030 / 2031			Unit
			Min.	Typ.	Max.	
P_O	Maximum Output Power	THD+N=10%, f_{in}=1kHz, R_L=3Ω	-	2.6	-	W
		THD+N =10%, f_{in}=1kHz, R_L=4Ω	-	2.3	-	W
		THD+N =10%, f_{in}=1kHz, R_L=8Ω	-	1.5	-	W
		THD+N =1%, f_{in}=1kHz, R_L=3Ω	-	1.9	-	W
		THD+N =1%, f_{in}=1kHz, R_L=4Ω	-	1.7	-	W
		THD+N =1%, f_{in}=1kHz, R_L=8Ω	1	1.1	-	W
THD+N	Total Harmonic Distortion Plus Noise	P_O=1.1W, R_L=4Ω f_{in}=1kHz	-	0.05	-	%
		P_O=0.7W, R_L=8Ω, f_{in}=1kHz	-	0.04	-	%
PSRR	Power Ripple Rejection Ratio	V_{IN}=0.2Vrms, R_L=8Ω, C_B=0.47µF, f_{in} =120Hz	-	85	-	dB
Crosstalk	Channel Separation	f_{in} =1kHz, C_B=0.47µF,	-	95	-	dB
	HP/$\overline{LINE}$ Input Separation	f_{in} =1kHz, C_B=0.47µF,	-	80	-	dB
S/N	Signal to Noise Ratio	P_O=1.1W, R_L=8Ω , A_weighting	-	105	-	dB

Operating Characteristics, SE mode (for APA2030 only)

V_{DD}=5V, T_A=25°C, R_L=32W, Gain=4, 1dB, (Unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2030			Unit
			Min.	Typ.	Max.	
P_O	Maximum Output Power	THD+N=10%, f_{in}=1kHz, R_L=32Ω	-	110	-	mW
		THD+N =1%, f_{in}=1kHz, R_L=32Ω	-	90	-	mW
THD+N	Total Harmonic Distortion Plus Noise	P_O=75mW, R_L=32Ω, f_{in}=1kHz	-	0.03	-	%
PSRR	Power Ripple Rejection Ratio	V_{IN}=0.2Vrms, R_L=32Ω, C_B=0.47µF, f_{in} =120,	-	55	-	dB
	SE/$\overline{BTL}$ Attenuation		-	80	-	dB

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Electrical Characteristics (Cont.)

Operating Characteristics, SE mode (for APA2030 only)

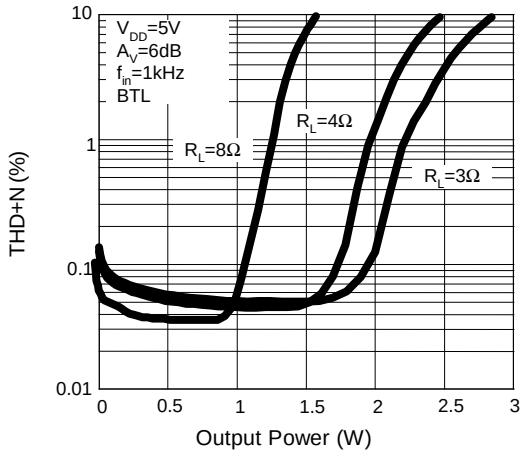
V_{DD}=5V, T_A=25°C, R_L=32Ω, Gain=4, 1dB, (Unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2030			Unit
			Min.	Typ.	Max.	
Crosstalk	Channel Separation	f_{in} =1kHz, C_B=0.47μF,	-	65	-	dB
	HP/$\overline{\text{LINE}}$ Input Separation	f_{in} =1kHz, C_B=0.47μF, BTL	-	80	-	dB
S/N	Signal to Noise Ratio	P_O=75mW, R_L=32Ω, A_weighting	-	100	-	dB

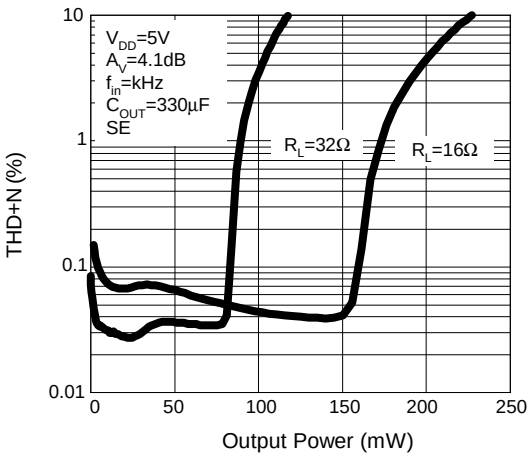
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Typical Operating Characteristics

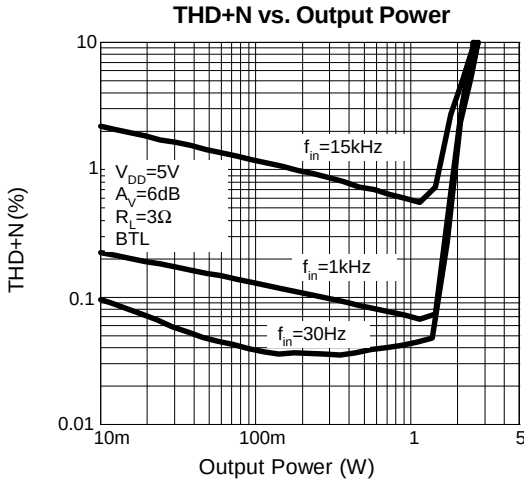
THD+N vs. Output Power



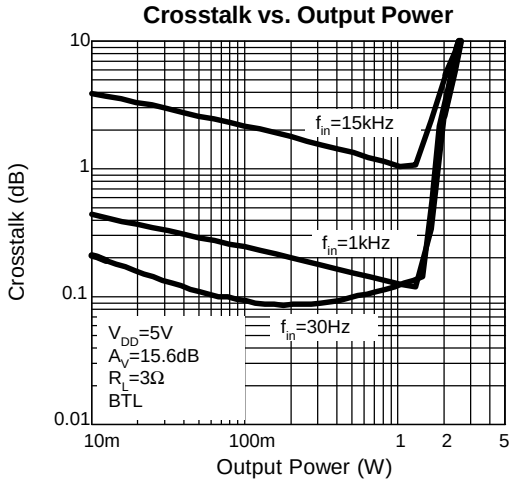
THD+N vs. Output Power



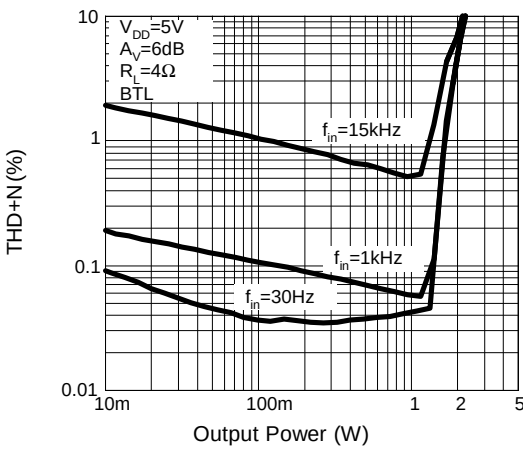
THD+N vs. Output Power



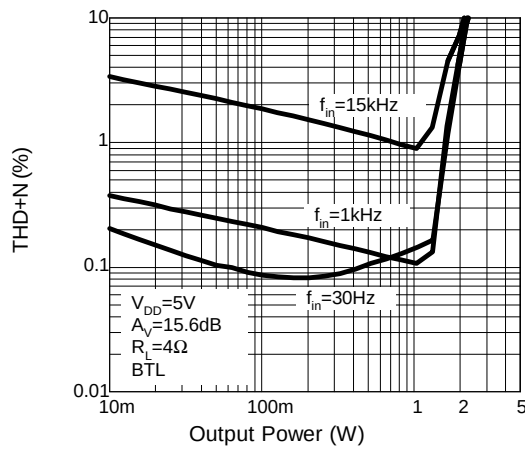
Crosstalk vs. Output Power



THD+N vs. Output Power

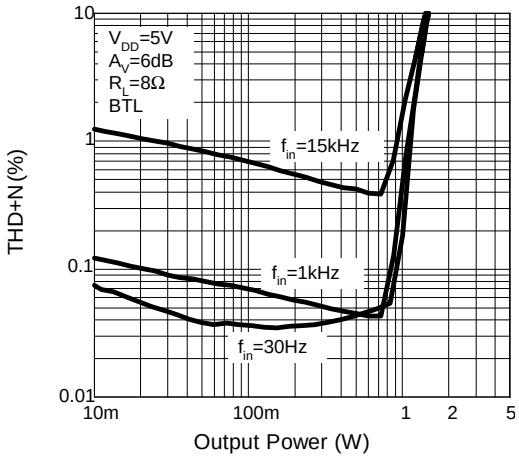


THD+N vs. Output Power

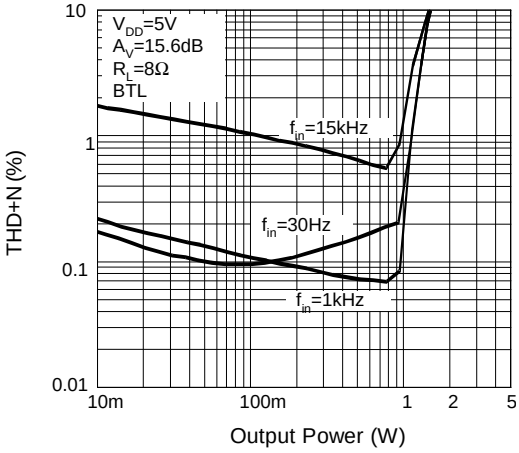


Typical Operating Characteristics (Cont.)

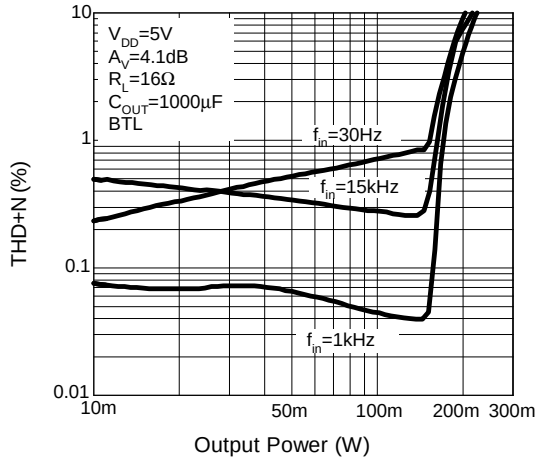
THD+N vs. Output Power



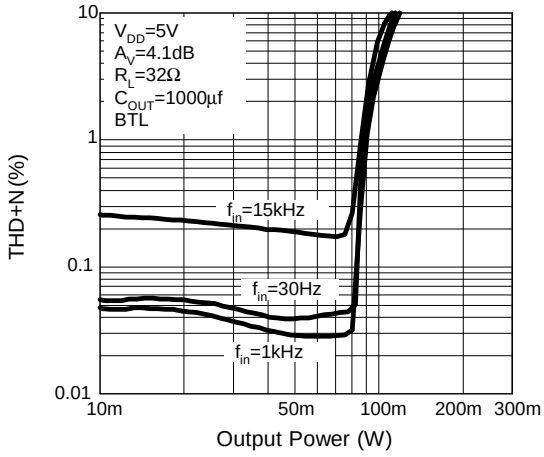
THD+N vs. Output Power



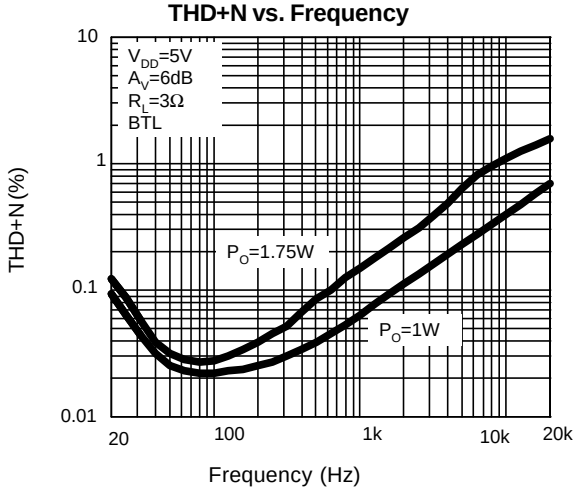
THD+N vs. Output Power



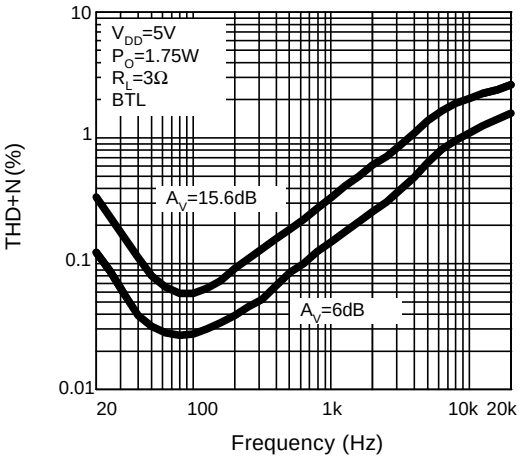
THD+N vs. Output Power



THD+N vs. Frequency



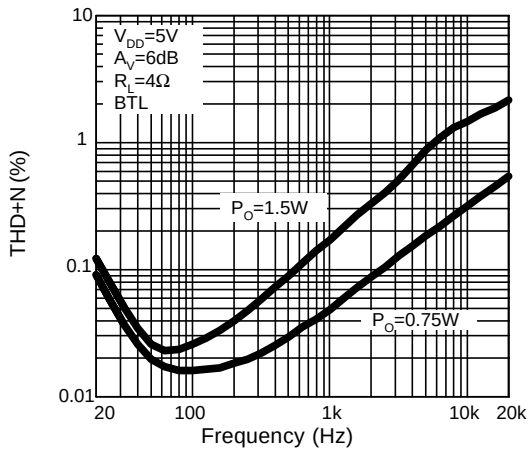
THD+N vs. Frequency



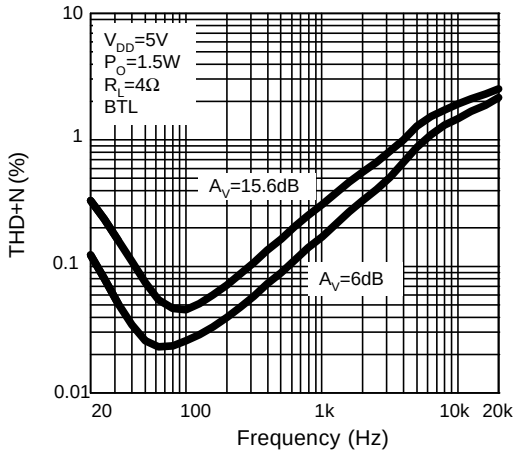
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Typical Operating Characteristics (Cont.)

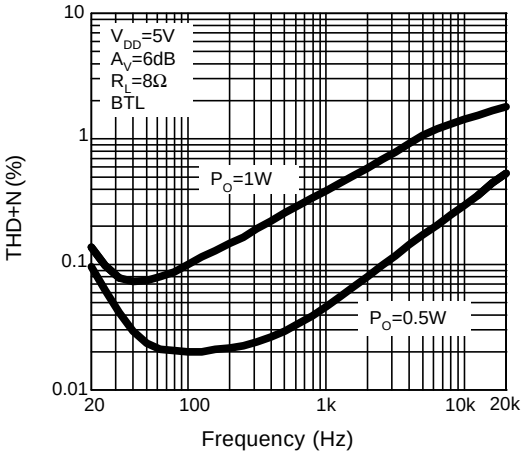
THD+N vs. Frequency



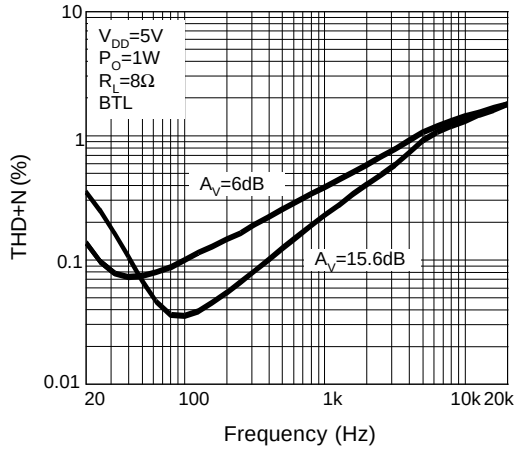
THD+N vs. Frequency



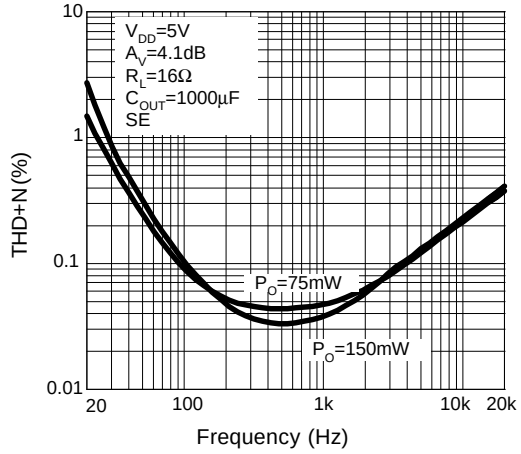
THD+N vs. Frequency



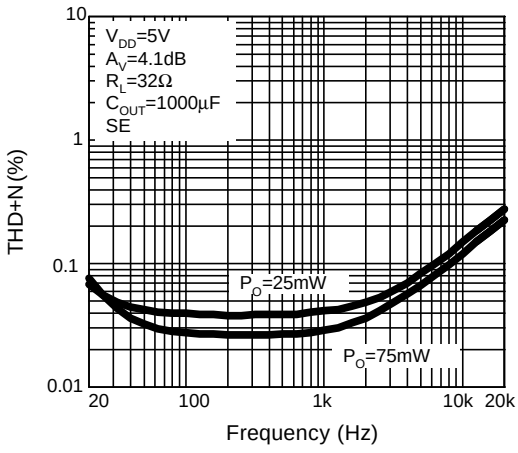
THD+N vs. Frequency



THD+N vs. Frequency



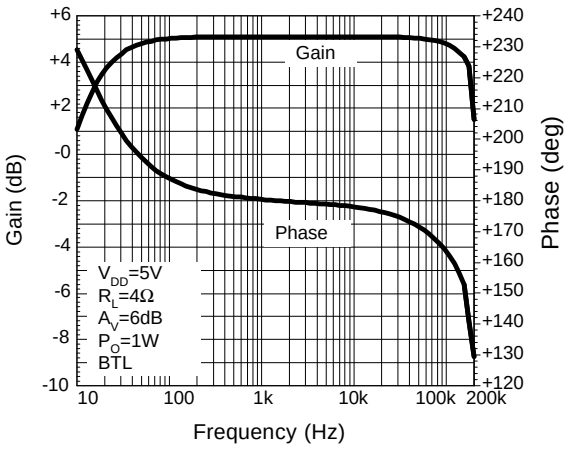
THD+N vs. Frequency



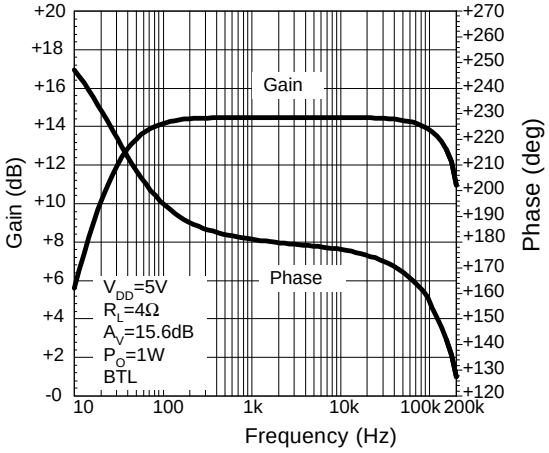
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Typical Operating Characteristics (Cont.)

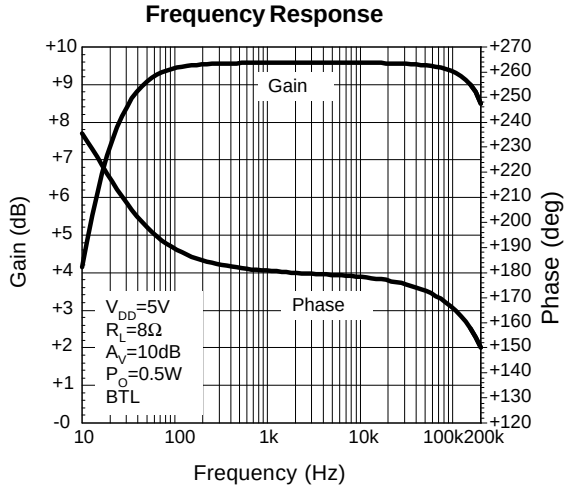
Frequency Response



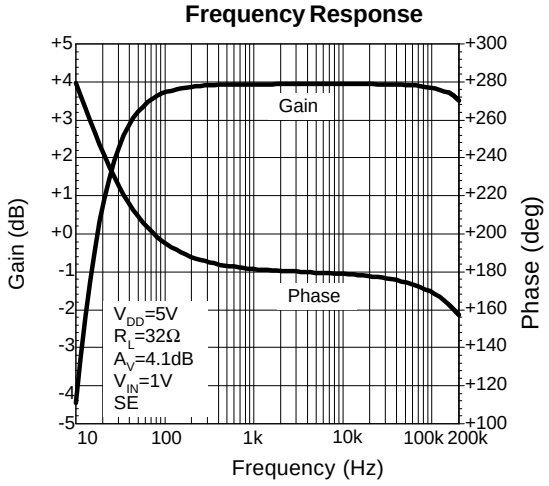
Frequency Response



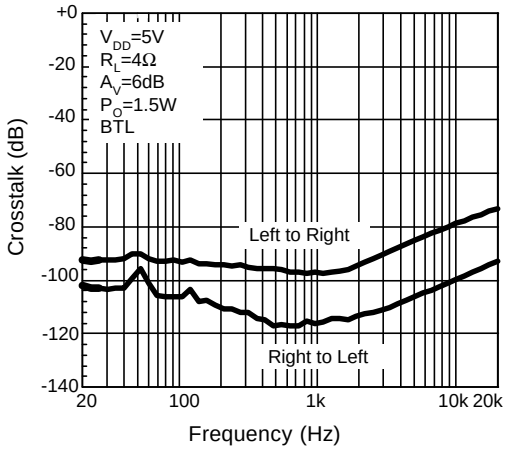
Frequency Response



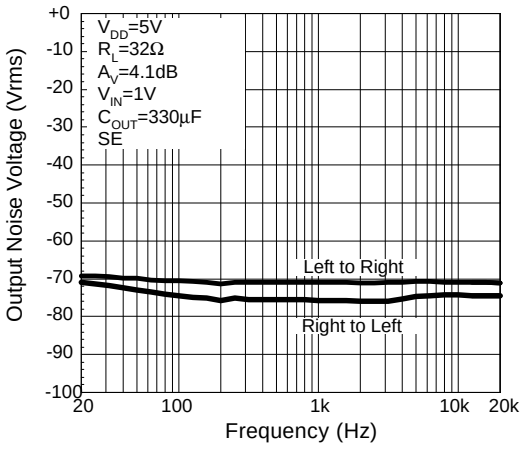
Frequency Response



Crosstalk vs. Frequency



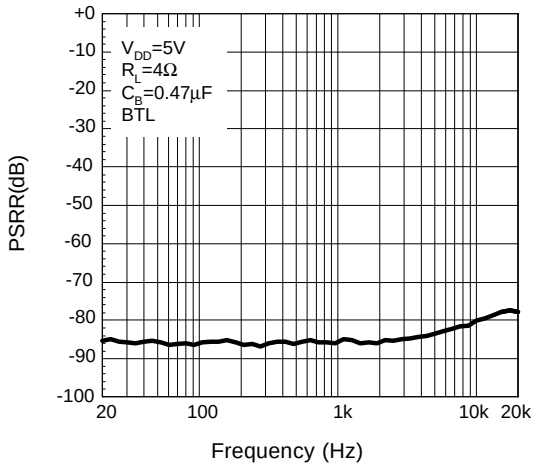
Crosstalk vs. Frequency



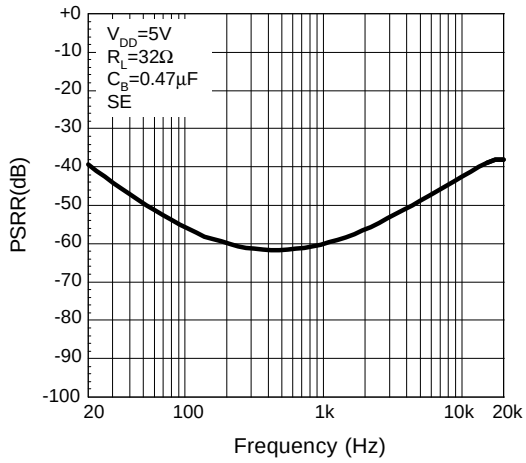
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Typical Operating Characteristics (Cont.)

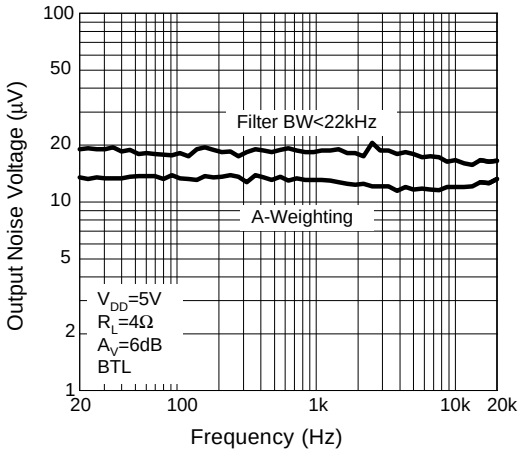
PSRR vs. Frequency



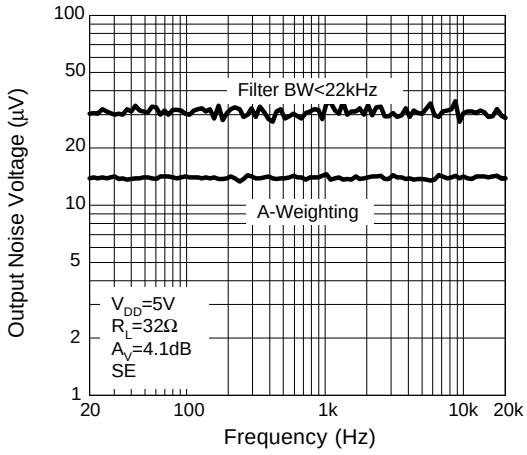
PSRR vs. Frequency



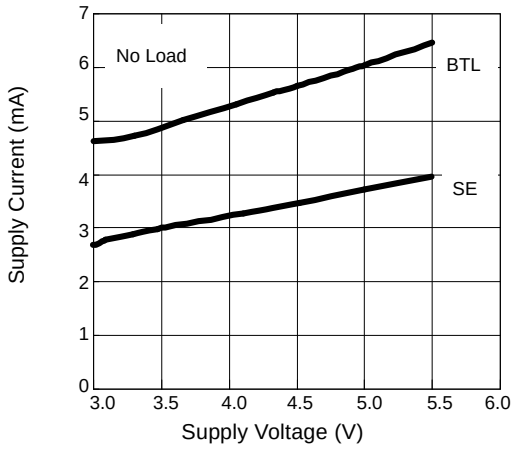
Output Noise Voltage vs. Frequency



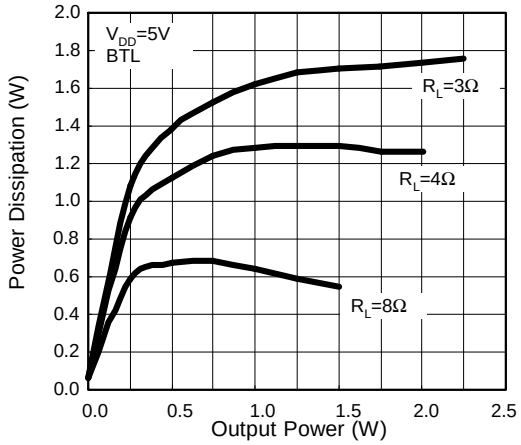
Output Noise Voltage vs. Frequency



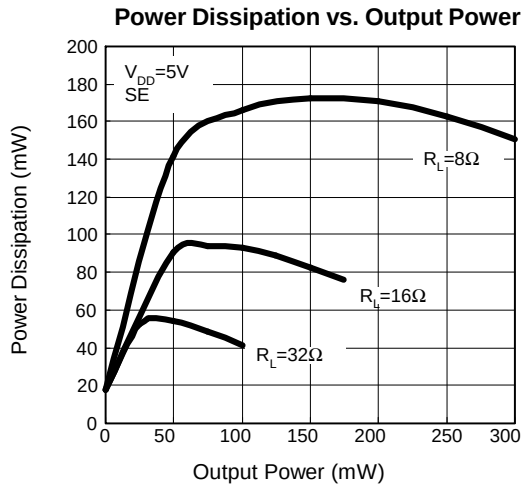
Supply Current vs. Supply Voltage



Power Dissipation vs. Output Power



Typical Operating Characteristics (Cont.)



Pin Description

APA2030

PIN		CONFIG.	FUNCTION
TSSOP-24P			
NO.	NAME		
1,12,13,24	GND	-	Ground connection, connected to thermal pad.
2	GAIN0	I/P	Input signal for internal gain setting.
3	GAIN1	I/P	Input signal for internal gain setting.
4	LOUT+	O/P	Left channel positive output in BTL mode and SE mode.
5	LLINEIN	I/P	Left channel line input terminal, selected when HP/LINE is held low.
23	RLINEIN	I/P	Right channel line input terminal, selected when HP/LINE is held low.
6	LHPIN	O/P	Left channel headphone input terminal, selected when HP/LINE is held high.
7,18	PVDD	-	Supply voltage only for power amplifier.
8	RIN+	I/P	Right channel positive signal input when differential signal is accepted.
9	LOUT-	O/P	Left channel negative output in BTL mode and high impedance in SE mode.
10	LIN+	I/P	Left channel positive signal input when differential signal is accepted.
11	BYPASS	-	Bypass voltage.
14	PCBEEP	I/P	PC-beep signal input.
15	SE/$\overline{\text{BTL}}$	I/P	Output mode control input pin, high for SE output mode and low for BTL mode.
16	ROUT-	O/P	Right channel negative output in BTL mode and high impedance in SE mode.
17	HP/$\overline{\text{LINE}}$	I/P	Multi-input selection input, headphone mode when held high, line-in mode when held low.
19	VDD	-	Supply voltage for internal circuit excepting power amplifier.
20	RHPIN	I/P	Right channel headphone input terminal, selected when HP/LINE is held high.
21	ROUT+	O/P	Right channel positive output in BTL mode and SE mode.
22	$\overline{\text{SHUTDOWN}}$	I/P	It will be into shutdown mode when pull low.
23	RLINEIN	I/P	Right channel line input terminal, selected when HP/LINE is held low.

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Pin Description (Cont.)

APA2031

PIN		NAME	CONFIG.	FUNCTION
NO.				
TSSOP-20P	TQFN3x3-16			
1,11,13,20	2,11	GND	-	Ground connection, connected to thermal pad.
2	3	GAIN0	I/P	Input signal for internal gain setting.
3	4	GAIN1	I/P	Input signal for internal gain setting.
4	5	LOUT+	O/P	Left channel positive output.
5	6	LIN-	I/P	Left channel negative audio signal input.
6,15	7	PVDD	-	Supply voltage only for power amplifier.
7	8	RIN+	I/P	Right channel positive audio signal input.
8	12	LOUT-	O/P	Left channel negative output.
9	9	LIN+	I/P	Left channel positive audio signal input.
10	10	BYPASS	-	Bypass voltage.
12	-	NC	-	No connection.
14	13	ROUT-	O/P	Right channel negative output.
16	14	VDD	-	Supply voltage for internal circuit excepting power amplifier.
17	15	RIN-	I/P	Right channel negative audio signal input.
18	16	ROUT+	O/P	Right channel positive output.
19	1	$\overline{\text{SHUTDOWN}}$	I/P	It will be into shutdown mode when pull low.

Control Input Table (for APA2030 only)

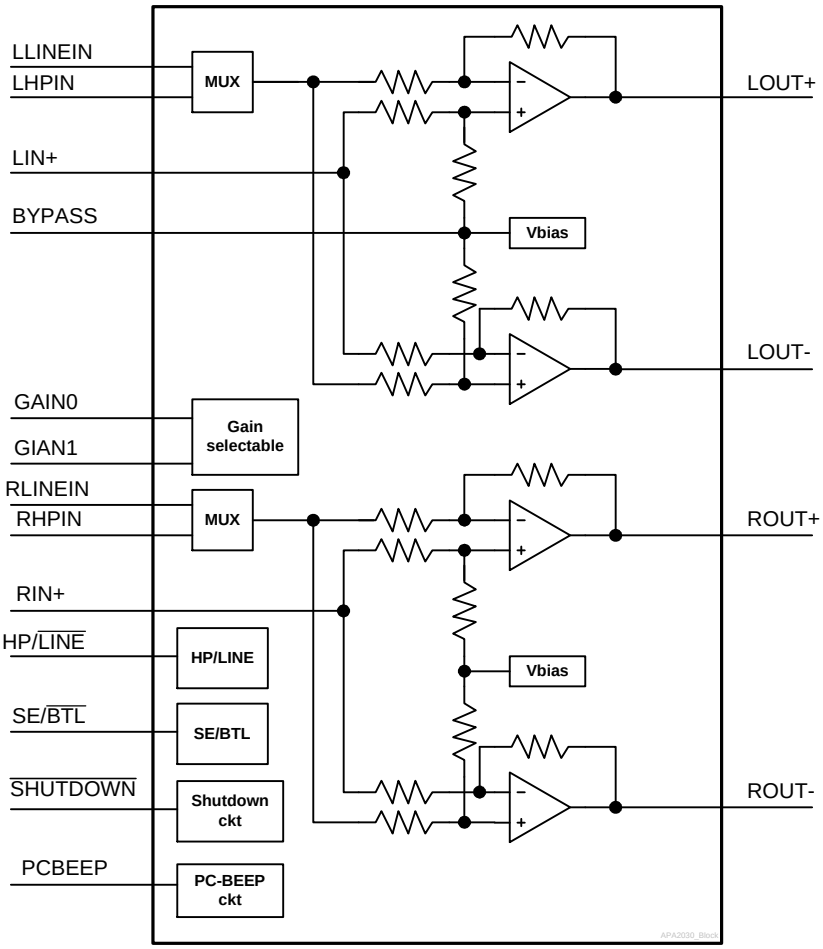
HP/ $\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	PCBEEP	Operating mode
X	X	L	Disable	Shutdown mode
L	L	H	Disable	Line input, BTL out
H	L	H	Disable	HP input, BTL out
L	H	H	Disable	Line input, SE out
H	H	H	Disable	HP input, SE out
X	X	X	Enable	PC-BEEP input, BTL out

Gain Setting Table (for both APA2030 and APA2031)

GAIN0	GAIN1	R_i	R_f	A_V
0	0	90kΩ	90kΩ	6dB
0	1	69kΩ	111kΩ	10dB
1	0	42kΩ	138kΩ	15.6dB
1	1	25.7kΩ	154.3kΩ	21.6dB

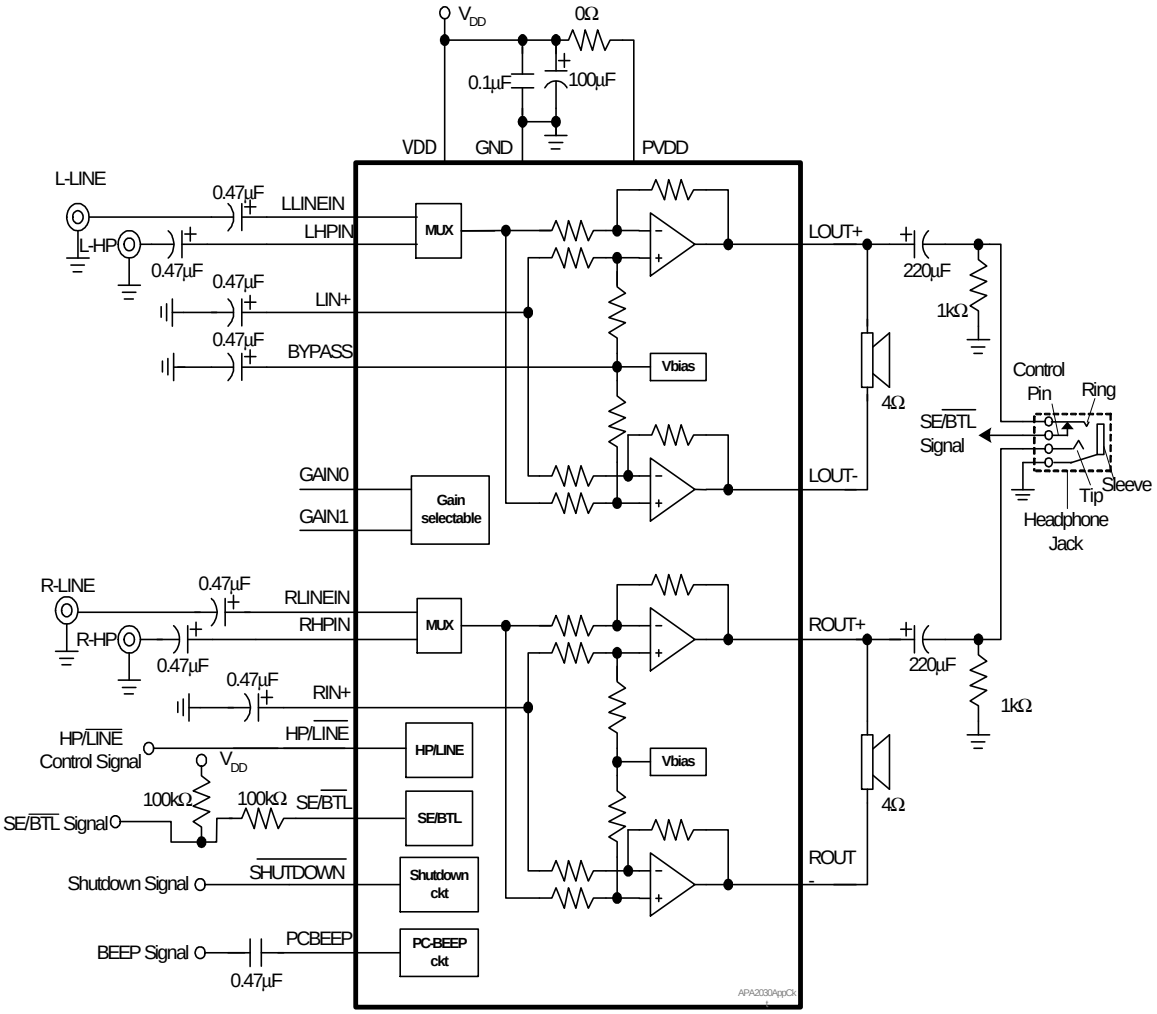
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Block Diagram



Typical Application Circuit

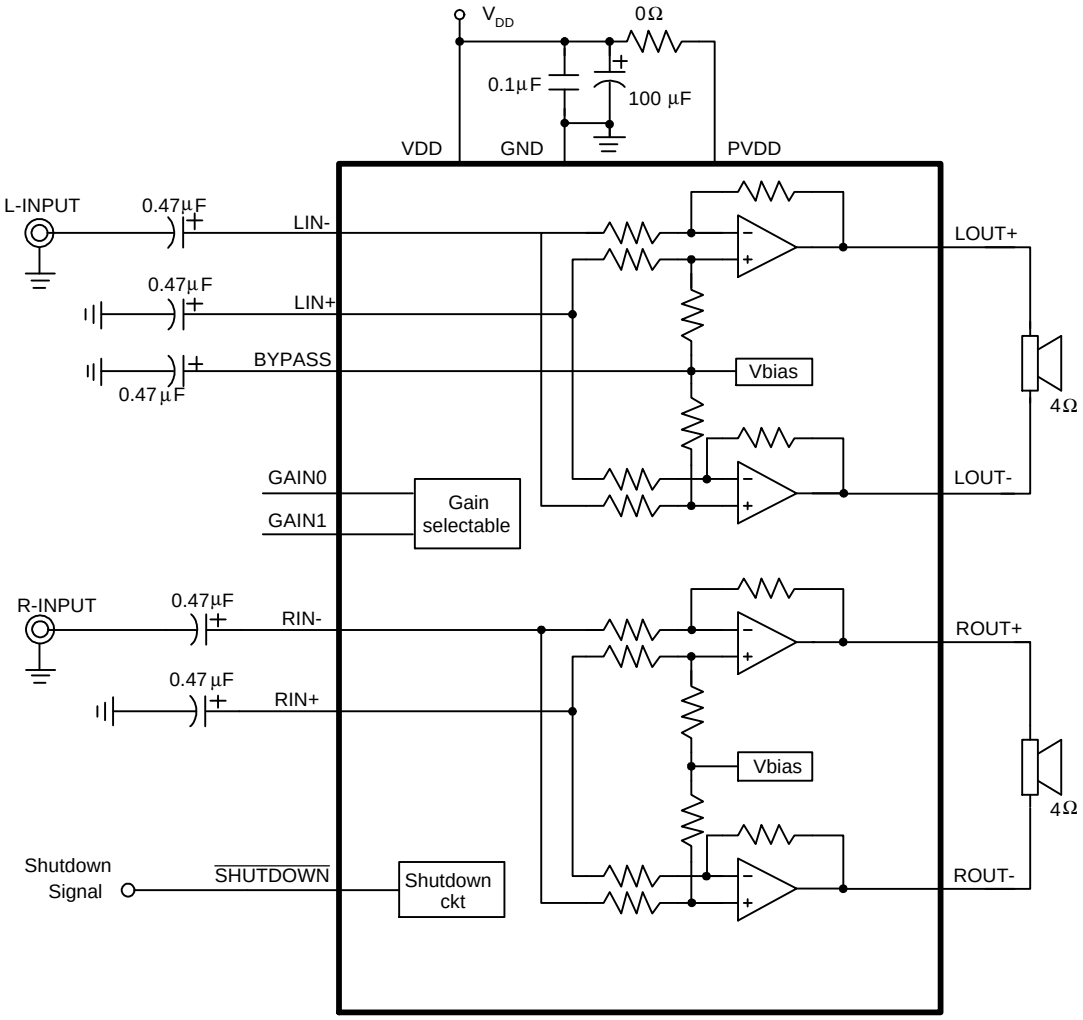
(for APA2030 using SE input signal)



APA2030

Typical Application Circuit (Cont.)

(for APA2031 using SE input signal)



APA2031

Application Information

BTL Operation

The APA2030/1 has two pairs of operational amplifiers internally, which allows for different amplifier configurations.

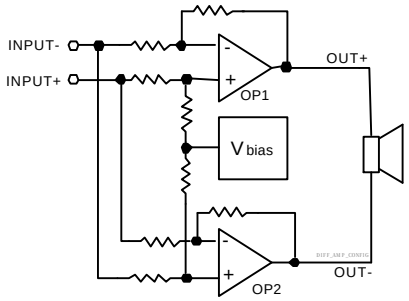


Figure 1: APA2030 Internal Configuration (each channel)

The OP1 and OP2 are all differential drive configurations. The differential driver configurates doubling voltage swing on the load. Compare with the single-ending configuration, the differential gain for each channel is 2X (Gain of SE mode).

By driving the load differentially through outputs OUT+ and OUT-, an amplifier configuration which is commonly referred to bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to the ground.

A BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus, doubling the output swing for a specified supply voltage. When placed under the same conditions, a BTL amplifier has four times the output power of a SE amplifier. A BTL configuration, such as the one used in APA2030/1, also creates a second advantage over SE amplifiers. Since the differential outputs, ROUT+, ROUT-, LOUT+, and LOUT-, are biased at half-supply, it's not necessary for DC voltage to be across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Single-Ended Operation (for APA2030 only)

Consider the single-supply SE configuration shown Application Circuit. A coupling capacitor is required to block the DC offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system (refer to the Output Coupling Capacitor).

The rules described should be following the relationship:

$$\frac{1}{C_{bypass} \times 250k\Omega} \leq \frac{1}{R_i C_i} \leq \frac{1}{R_L C_C} \quad \text{.....(1)}$$

Output SE/$\overline{\text{BTL}}$ Operation (for APA2030 only)

The best cost saving feature of APA2030 is that it can be switched easily between BTL and SE modes. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated.

The APA2030 has two separated amplifiers drive OUT+ and OUT- (See Figure 1). The SE/$\overline{\text{BTL}}$ input controls the operation of the amplifier that drives LOUT- and ROUT-.

- When SE/$\overline{\text{BTL}}$ is held low, the OP2 is actived and the APA2030 is in the BTL mode.
- When SE/$\overline{\text{BTL}}$ is held high, the OP2 is in a high output impedance state, which configures the APA2030 as SE driver from OUT+. I_{DD} is reduced by approximately one-half in SE mode.

The SE/$\overline{\text{BTL}}$ input can be a logic-level TTL source, a resistor divider network or the stereo headphone jack with switch pin as shown in the Application Circuit.

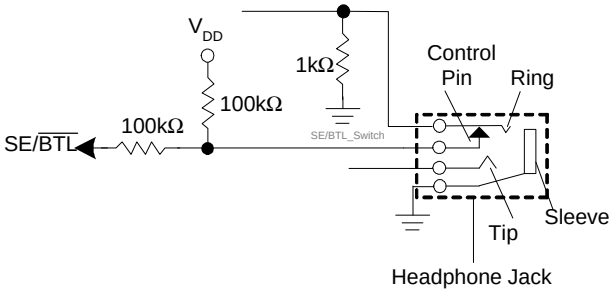


Figure 2: SE/$\overline{\text{BTL}}$ input selection by phonejack plug

In Figure 2, input SE/$\overline{\text{BTL}}$ operates as below:

When the phone jack plug is inserted, the 1kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high and enables the SE mode. When the input goes high level,

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Application Information (Cont.)

Output SE/$\overline{\text{BTL}}$ Operation (for APA2030 only) (Cont.)

the OUT- amplifier is shutdown and causes the speaker to mute. And then, the OUT+ amplifier drives through the output capacitor (CO) into the headphone jack.

When there is no headphone plugged into the system, the contact pin of the headphone jack is connected from the signal pin, the voltage divider is set up by resistors 100kΩ and 1kΩ. Resistor 1kΩ then pulls low the SE/$\overline{\text{BTL}}$ pin, enabling the BTL function.

Input HP/$\overline{\text{LINE}}$ Operation (for APA2030 only)

APA2030 amplifier has two separated inputs for each of the left and right stereo channels. An internal multiplexer selects which input will be connected to the amplifier based on the state of the HP/$\overline{\text{LINE}}$ pin on the IC.

- To select the line inputs, set HP/$\overline{\text{LINE}}$ pin tied to low level
- To enable the headphone inputs, set HP/ $\overline{\text{LINE}}$ pin tied to high level

Refer to the application circuit, the voltage divider of 100kΩ and 1kΩ sets the voltage at the HP/$\overline{\text{LINE}}$ pin to be approximately 50mV when there are no headphones plugged into the system. This logic low voltage at the HP/$\overline{\text{LINE}}$ pin enables the APA2030 and places it LINE input mode operation.

When a set of headphones is plugged into the system, the contact pin of the headphone jack is disconnected from the signal pin, interrupting the voltage divider set up by resistors 100kΩ. Resistor 100kΩ then pulls-up the HP/$\overline{\text{LINE}}$ pin, enabling the headphone input function.

Differential Input Operation

The APA2030/1 can accept the differential input signal and improve the CMRR (Common Mode Rejection Ratio). For example, when applying differential input signals to APA2031, connect positive input signals to the IN+ (LIN+ and RIN+) of APA2031 and negative input signals to the IN- (LIN- and RIN-) of APA2031.

When input signals are single-end, just connect IN+ (LIN+ and RIN+) to ground via a capacitor.

Input Resistance, R_i

The APA2030/1 provides four gain setting decided by GAIN0 and GAIN1 input pins in differential mode and it becomes 4.1dB fixed gain when SE mode is selected (for APA2030). In Table 1, according to the BTL operation, internal resistors R_i and R_f set the gain for each audio input of the APA2030/1.

GAIN0	GAIN1	R_i	R_f	SE/$\overline{\text{BTL}}$	A_V
0	0	90kΩ	90kΩ	0	6dB
0	1	69kΩ	111kΩ	0	10dB
1	0	42kΩ	138kΩ	0	15.6dB
1	1	25.7kΩ	154.3kΩ	0	21.6dB
X	X	69kΩ	111kΩ	1	4.1dB

Table 1: The close loop gain setting resistance R_i/R_f

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. The input resistance has wide variation (+/-10%) caused by manufacturing.

Input Capacitor, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance R_i form a high-pass filter with the corner frequency determined in the following equation:

$$f_{c(highpass)} = \frac{1}{2\pi R_{i(min)} \times C_i} \quad \text{.....(2)}$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Consider the example where R_i is 90kΩ when 6dB gain is set and the specification calls for a flat bass response down to 40Hz. The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_c} \quad \text{.....(3)}$$

When the variation of input resistance (R_i) is considered, the value of C_i is 0.04µF. Therefore, a value in the range from 0.1µF to 1.0µF would be chosen.

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Application Information (Cont.)

Input Capacitor, C_i (Cont.)

A further consideration for this capacitor is the leakage path from the input source through the input network (R_i+R_f, C_i) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifiers' input in most applications becasue the DC level of the amplifiers' inputs is held at V_{DD}/2. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, C_{bypass}

As to any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitor located on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger half supply bypass capacitor improves PSRR due to increased half-supply stability. Typical applications employ a 5V regulator with 1.0µF and a 0.1µF bypass capacitors which aid in supply filtering. This does not eliminate the need for bypassing the supply nodes of the APA2030/1. The selection of bypass capacitors, especially C_B, is thus dependent upon desired PSRR requirements, click and pop performance.

To avoid the start-up pop noise occurred, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation should be maintained.

$$\frac{1}{C_{bypass} \times 250k\Omega} << \frac{1}{C_i \times 180k\Omega} \quad \text{.....(4)}$$

The capacitor is fed from a 250kΩ source inside the amplifier. Bypass capacitor, C_B, values of 3.3µF to 10µF ceramic or tantalum low-ESR capacitors are recommended for the best THD+N and noise performance.

The bypass capacitance also affects the start-up time. It is determined in the following equation:

$$T_{Startup} = 5 \times (C_{bypass} \times 250k\Omega) \quad \text{.....(5)}$$

Output Coupling Capacitor, C_c (for APA2030 only)

In the typical single-supply SE configuration, an output coupling capacitor (C_c) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by the following equation.

$$f_{c(highpass)} = \frac{1}{2\pi R_L C_c} \quad \text{.....(6)}$$

For example, a 330µF capacitor with an 8Ω speaker would attenuate low frequencies below 60.6Hz. Large values of C_C are required to pass low frequencies into the load.

Power Supply Decoupling, C_S

The APA2030/1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible.

Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that targets on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device VDD lead works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Shutdown Function

In order to reduce power consumption when not in use, the APA2030/1 contains a shutdown pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the $\overline{\text{SHUTDOWN}}$ pin. The trigger point between a logic high and logic low level is typically 2.0V. It is better to switch between the ground and the supply V_{DD} to provide maximum device performance.

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Application Information (Cont.)

Shutdown Function (Cont.)

By switching the $\overline{\text{SHUTDOWN}}$ pin to low, the amplifier enters a low-current state, I_{DD}<50mA. The APA2030 is in shutdown mode, except PC-BEEP detect circuit. On normal operating, $\overline{\text{SHUTDOWN}}$ pin is pulled to high level to keep the IC out of the shutdown mode. The $\overline{\text{SHUTDOWN}}$ pin should be tied to a definite voltage to avoid unwanted state changing.

PC-BEEP Detection (for APA2030 only)

The APA2030 integrates a PC-BEEP detect circuit for NOTEBOOK PC using. Over 1Vpp amplitude PC-BEEP signal with the rising time/falling time under 1μs/V should be provided to trigger the APA2030 into PC-BEEP mode. The input impedance is 100kΩ and the bias voltage on PC-BEEP input pin is 2.5V. Therefore, the voltage level of PC-BEEP signal should be higher than 3V and lower than 2V to into PCBEEP mode correctly.

When PC-BEEP signal drives to PC-BEEP input pin, the PC-BEEP mode will be active. When chip in the PC-BEEP mode, the APA2030 will be forced to be in BTL mode and the internal gain is fixed as -10dB. The PC-BEEP signal turns to be the amplifier input signal and plays on the speaker without coupling capacitor. If the amplifier is in the shutdown mode, it will be out of shutdown mode whenever PC-BEEP mode enabled. The APA2030 will return to previous setting when it is out of PC-BEEP mode.

Optimizing Depop Circuitry

Circuitry has been included in the APA2030/1 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry. The value of C_i will also affect turn-on pops. (Refer to Effective Bypass Capacitance) The bypass voltage should rise slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of C_B can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of C_B, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of C_B and the turn-on time.

In a SE (for APA2030) configuration, the output coupling capacitor, C_C, is of particular concern. This capacitor discharges through the internal 10kΩ resistors. Depending on the size of C_C, the time constant can be relatively large. To reduce transients in SE mode, an external 1kΩ resistor can be placed in parallel with the internal 10kΩ resistor. The tradeoff for using this resistor is an increase in quiescent current.

In the cases, choosing a small value of C_i in the range of 0.33μF to 1μF, C_B being equal to 0.47μF and an external 1kΩ resistor should be placed in parallel with the internal 10kΩ resistor, and it should produce a virtually clickless and popless turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. Hence, it is advantageous to use low-gain configurations.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \quad \text{.....(7)}$$

Where

$$P_O = \frac{V_O\text{rms} \times V_O\text{rms}}{R_L} = \frac{V_P \times V_P}{2R_L}$$

$$V_O\text{rms} = \frac{V_P}{\sqrt{2}} \quad \text{.....(8)}$$

$$P_{SUP} = V_{DD} \times I_{DD(AVG)} = V_{DD} \times \frac{2V_P}{\pi R_L} \quad \text{.....(9)}$$

Efficiency of a BTL configuration

$$\frac{P_O}{P_{SUP}} = \frac{\left(\frac{V_P \times V_P}{2R_L}\right)}{V_{DD} \times \frac{2V_P}{\pi R_L}} = \frac{\pi V_P}{4V_{DD}} \quad \text{.....(10)}$$

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Application Information (Cont.)

BTL Amplifier Efficiency (Cont.)

Table 2 calculates efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 3W.

Po (W)	Efficiency (%)	I_{DD}(A)	V_{PP}(V)	P_D (W)
0.25	31.25	0.16	2.00	0.55
0.50	47.62	0.21	2.83	0.55
1.00	66.67	0.30	4.00	0.5
1.25	78.13	0.32	4.47	0.35

**High peak voltages cause the THD+N to increase.

Table 2: Efficiency vs. Output Power in 5V/8W BTL Systems

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to the utmost advantage when possible. Note that in equation, V_{DD} is in the dominator. This indicates that as V_{DD} goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. In equation11, it states that the maximum power dissipation point for a SE mode operates at a given supply voltage and drives a specified load.

$$\text{SE mode}: P_{D.MAX} = \frac{V_{DD}^2}{2\pi^2 R_L} \quad \text{.....(11)}$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus, the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BLT mode}: P_{D.MAX} = \frac{4V_{DD}^2}{2\pi^2 R_L} \quad \text{.....(12)}$$

Since the APA2030/1 is a dual channel power amplifier, the maximum internal power dissipation is 2 times that both of equations depending on the mode of operation. Even with this substantial increase in power dissipation, the APA2030/1 does not require extra heatsink. The power dissipation from equation12, assuming a 5V-power supply and an 8W load, must not be greater than the power dissipation that results from the equation 13:

$$P_{D.MAX} = \frac{T_{J.MAX} - T_A}{\theta_{JA}} \quad \text{.....(13)}$$

For TSSOP-24P (APA2030), TSSOP-20P and TQFN3x3-16 (APA2031) packages with and without thermal pad, the thermal resistance (θ_{JA}) is equal to 45°C/W, 48°C/W and 55°C/W respectively.

Since the maximum junction temperature ($T_{J,MAX}$) of APA2030/1 is 150°C and the ambient temperature (T_A) is defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation12. Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Thermal Pad Consideration

The thermal pad must be connected to the ground. The package with thermal pad of the APA2030/1 requires special attention on thermal design. If the thermal design issues are not properly addressed, the APA2030/1 4Ω will go into thermal shutdown when driving a 4Ω load.

The thermal pad on the bottom of the APA2030/1 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 10 vias of 13 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane. For good thermal conduction, the vias must be plated through and solder filled. The copper plane is used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the APA2030/1 junction temperature below the thermal shutdown temperature (150°C).

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Application Information (Cont.)

Thermal Pad Consideration (Cont.)

In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.

Thermal Consideration

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. To calculate maximum ambient temperatures, first consideration is that the numbers from the **Power Dissipation vs. Output Power** graphs (Page 9 and 10) are per channel values, so the dissipation of the IC heat needs to be doubled for two-channel operation. Given θ_{JA}, the maximum allowable junction temperature ($T_{J,MAX}$), and the total internal dissipation (P_D), the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the APA2030/1 is 150°C. The internal dissipation figures are taken from the **Power Dissipation vs. Output Power** graphs. (Page 9 and 10)

$$T_{A.MAX} = T_{J.MAX} - \theta_{JA} P_D \quad \text{.....(14)}$$

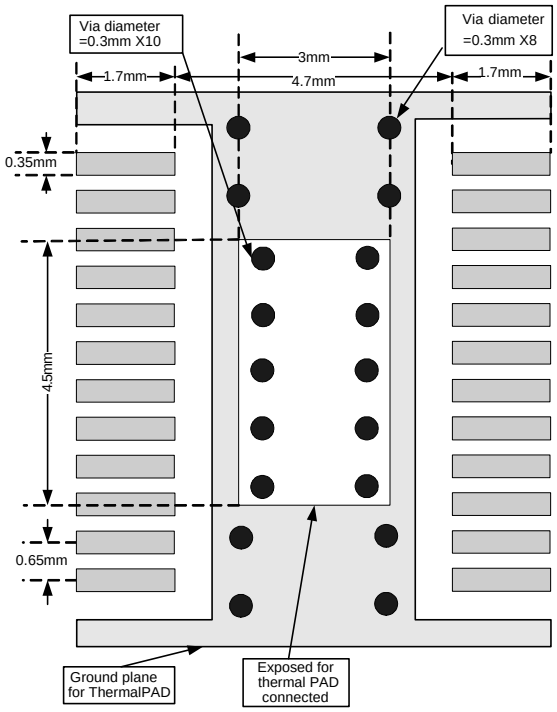
150 - 45(0.8x2) = 78°C (TSSOP-24P)

150 - 48(0.8x2) = 73.2°C (TSSOP-20P)

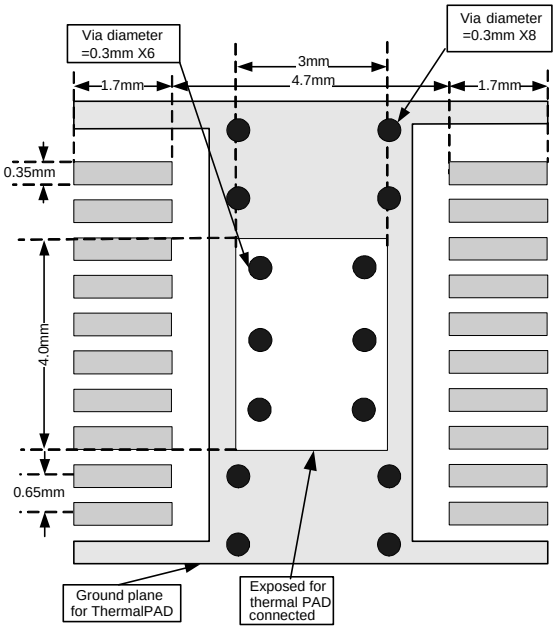
150 - 55(0.8x2) = 62°C (TQFN3x3-16)

The APA2030/1 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent the IC from damages.

Recommended Minimum Footprint



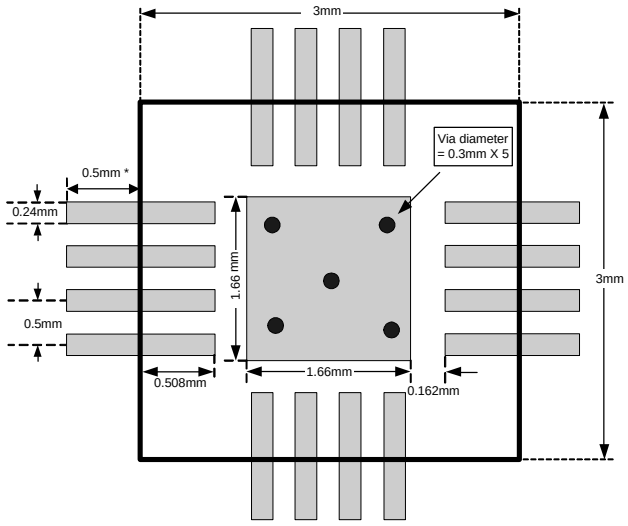
TSSOP-24P



TSSOP-20P

Application Information (Cont.)

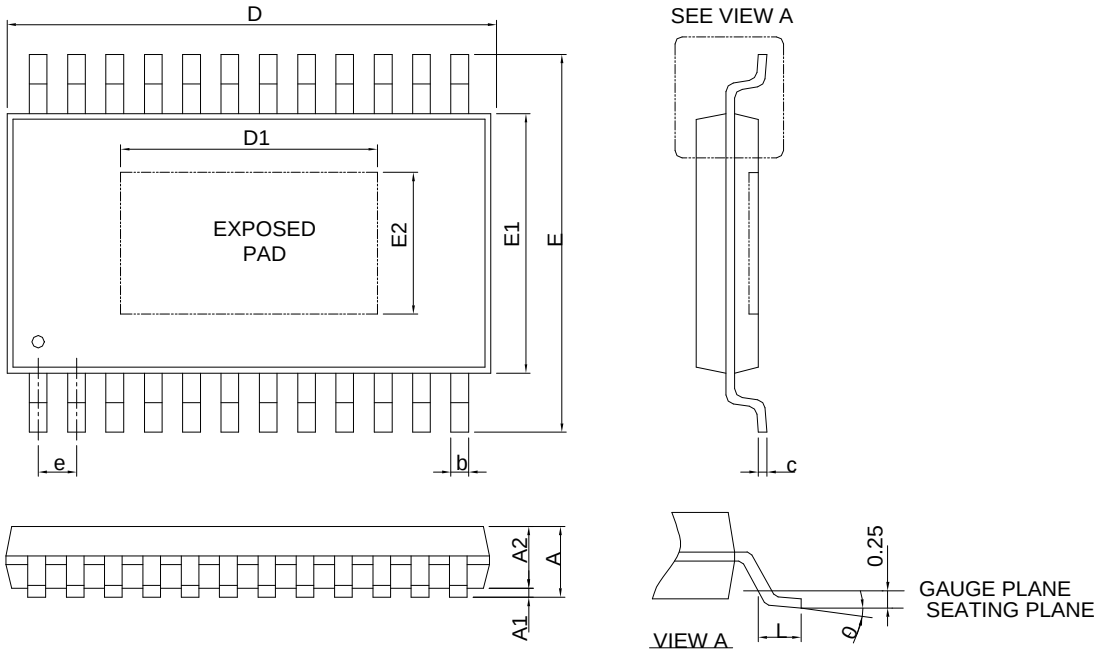
Recommended Minimum Footprint



* Just Recommend

Package Information

TSSOP-24P (APA2030)



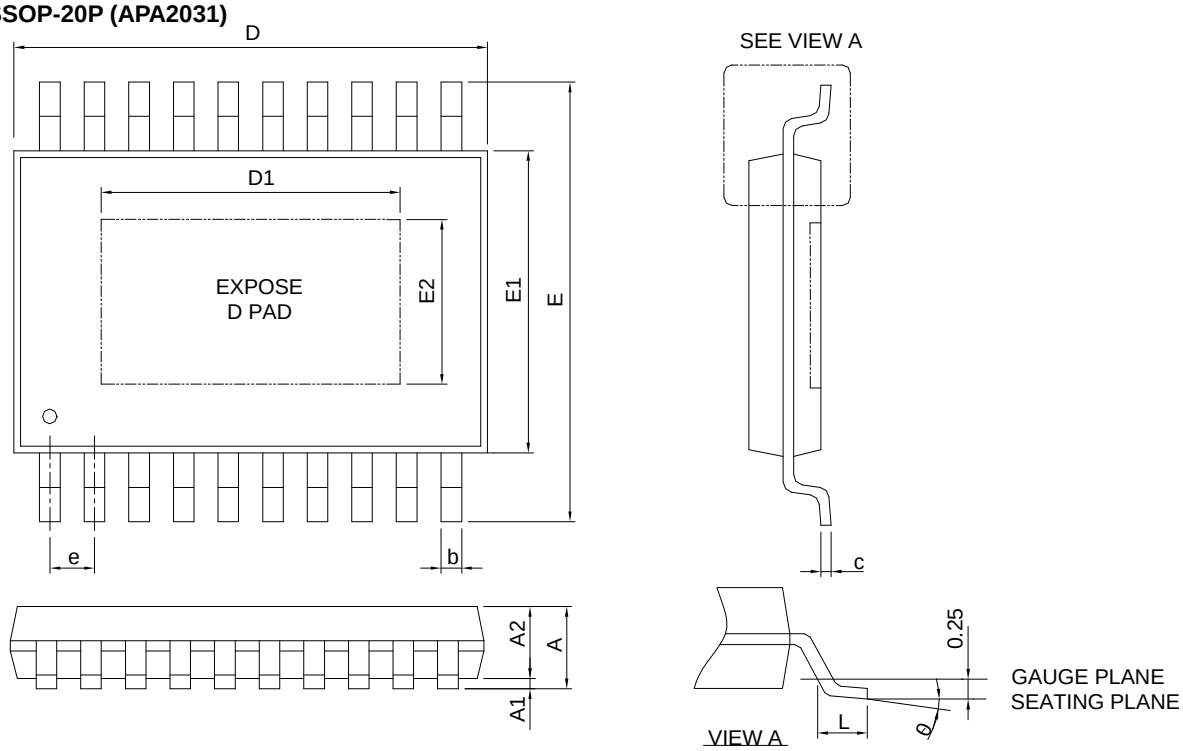
SYMBOL	TSSOP-24P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	7.70	7.90	0.303	0.311
D1	3.50	5.00	0.138	0.197
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
E2	2.50	3.50	0.098	0.138
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°

Note : 1. Followed from JEDEC MO-153 ADT.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

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Package Information

TSSOP-20P (APA2031)



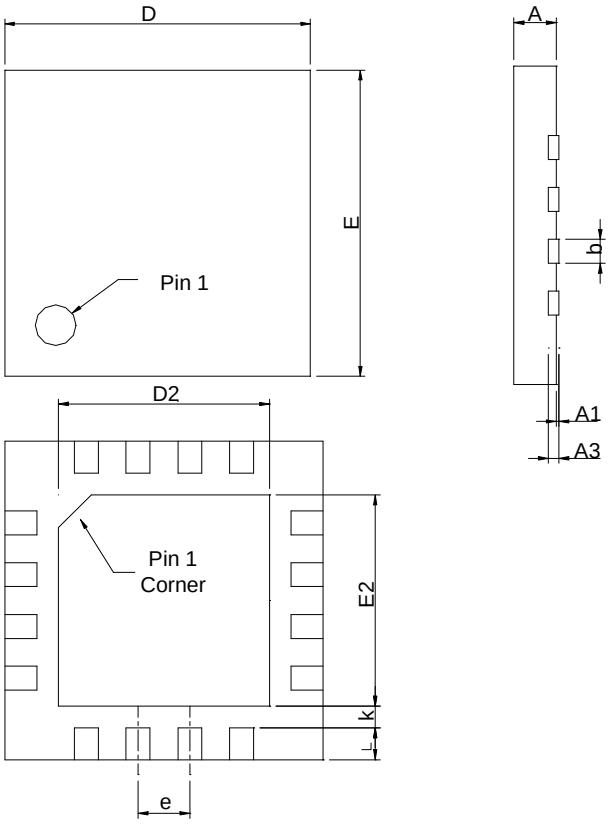
SYMBOL	TSSOP-20P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	6.40	6.60	0.252	0.260
D1	3.00	4.50	0.118	0.177
E	6.20	6.40	0.244	0.260
E1	4.30	4.50	0.169	0.177
E2	2.50	3.50	0.098	0.138
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC MO-153 ACT.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

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Package Information

TQFN3x3-16 (APA2031)

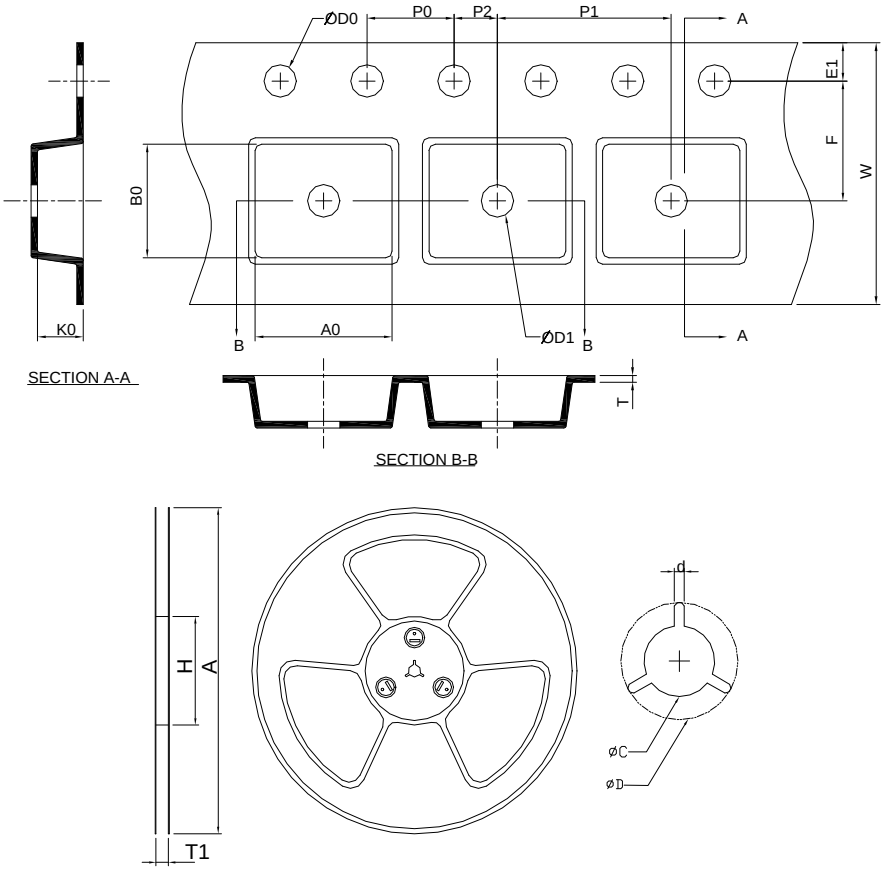


SYMBOL	TQFN3x3-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : Follow JEDEC MO-220 WEED-4.

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Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TSSOP-24P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.9±0.20	8.30.±0.20	1.50±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TSSOP-20P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.10	1.5+0.10 -0.00	1.5 MIN.	0.30±0.05	6.9±0.20	6.90±0.20	1.60±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TQFN3x3-16	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

(mm)

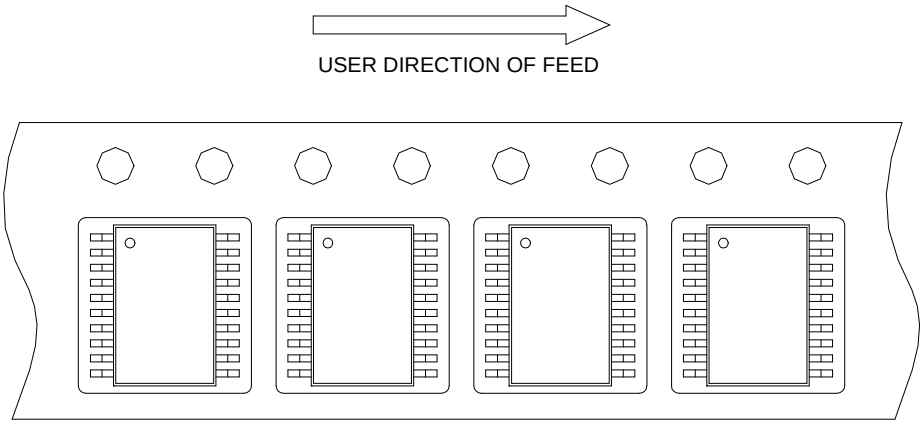
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Devices Per Unit

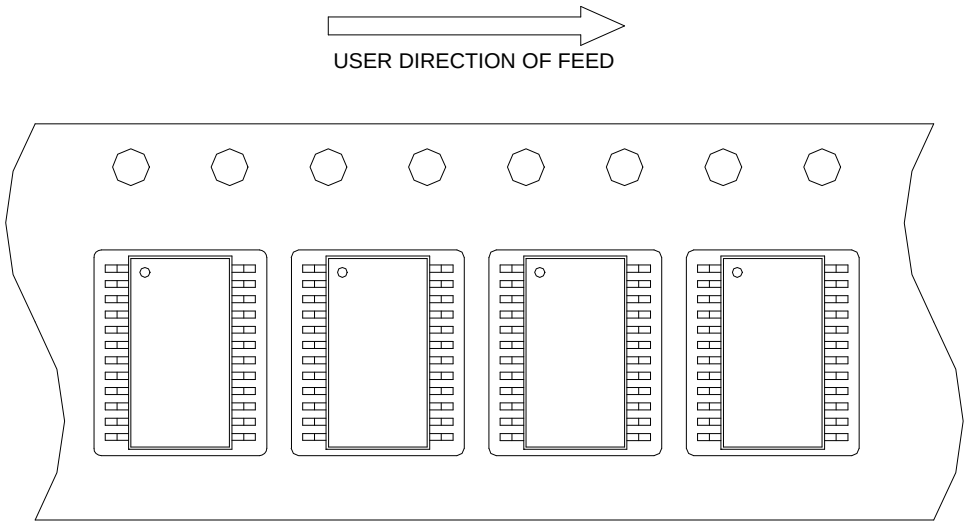
Package Type	Unit	Quantity
TSSOP-24P	Tape & Reel	2000
TSSOP-20P	Tape & Reel	2000
TQFN3x3-16	Tape & Reel	3000

Taping Direction Information

TSSOP-20P

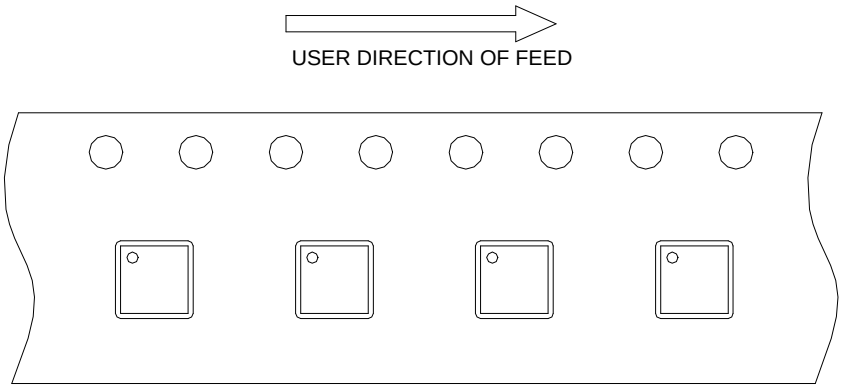


TSSOP-24P

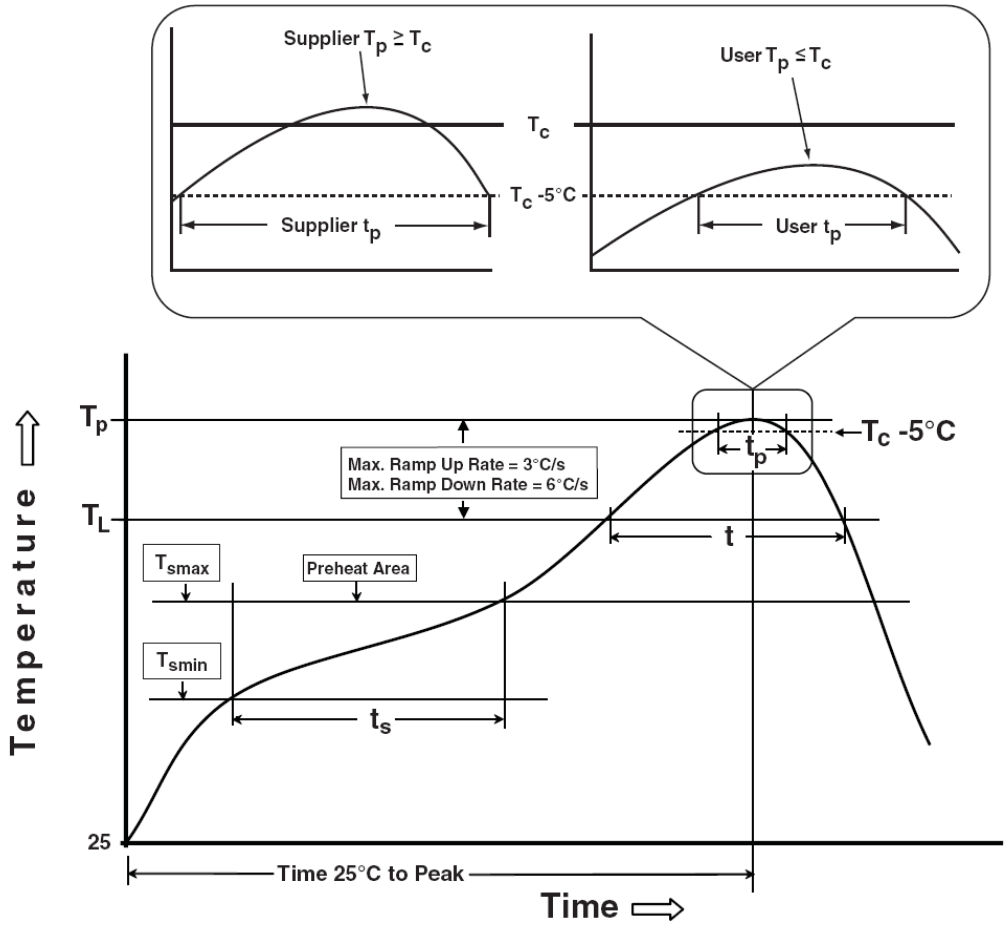


Taping Direction Information

TQFN3x3-16



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 3350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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