SCOPE: IMPROVED, DUAL, HIGH-SPEED CHANNEL ANALOG SWITCHES

Device Type	Generic Number
01	DG401A(x)/883B
02	DG403A(x)/883B
03	DG405A(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
K	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
Z	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

Voltage Referenced to V^-

V^+ to V^- 44V
V^+ to GND 25V
V_L ..... (GND-0.3V) to (V^+ +0.3V)
Digital Inputs, V_S, V_D 1/ ..... .(V^- -2V) to (V^+ +2V)
or 20mA whichever occurs first.
Continuous Current, Any terminal except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% duty cycle max) 100mA
Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
16 lead CERDIP(derate 10.0mW/°C above +70°C) 800mW
20 lead LCC (derate 9.1 mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
Case Outline 16 lead CERDIP..... 50°C/W
Case Outline 20 lead LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
Case Outline 16 lead CERDIP..... 100°C/W
Case Outline 20 lead LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Positive Supply Voltage (V^+) ..... +15V
Negative Supply Voltage (V^-) ..... -15V
V_{INL} (max) 0.8V
V_{INH} (min) 2.4V
Logic Supply Voltage (V_L) ..... +5V
Low Charge Injection 15pC
Crosstalk (channel-to-channel) 2/ 90dB

1/ Signals on S_X, D_X or IN_X exceeding V^+ or V^- are clamped by internal diodes. Limit forward current to maximum current ratings.
2/ Crosstalk performance is improved with case outline for 20LCC.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{INH}=2.4V, V_{INL}=0.8V, V_L=5V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 3/	Limits Max 3/	Units
SWITCH							
Analog-Signal Range	V_{ANALOG}	4/	1,2,3	All	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	V^+=+13.5V, V^-=-13.5V, I_S=-10mA, V_D=±10V, V_{INH}=2.4V, V_{INL}=0.8V	1 2,3	All		30 45	Ω
Drain-Source ON Resistance Matching between Channels 5/	Δr_{DS} (ON)	V^+=+15V, V^-=-15V, I_S=-10mA, V_D=±10V	1 2,3	All		2.0 3.0	Ω
On-Resistance Flatness 5/	$r_{FLAT(ON)}$	V^+=+15V, V^-=-15V, I_S=-10mA, V_D=±5V, 0V	1 2,3	All		3.0 6.0	Ω
Source-OFF Leakage Current	$I_{S(OFF)}$	V^+=+16.5V, V^-=-16.5V, V_D=±15.5V, V_S=±15.5V	1 2	All	-0.25 -10	0.25 10	nA
Drain-OFF Leakage Current	$I_{D(OFF)}$	V^+=+16.5V, V^-=-16.5V, V_D=±15.5V, V_S=±15.5V	1 2,3	All	-0.25 -10	0.25 10	nA
Drain-ON Leakage Current	$I_{D(ON)}$ or $I_{S(ON)}$	V^+=+16.5V, V^-=-16.5V, V_D=±15.5V, V_S=±15.5V	1 2,3	All	-0.4 -20	0.4 20	nA
INPUT							
Input Current/Voltage High	I_{INH}	V_{IN}= 2.4V, all others = 0.8V	1,2,3	All	-1.0	1.0	µA
Input Current/Voltage Low	I_{INL}	V_{IN}= 0.8V, all others = 2.4V	1,2,3	All	-1.0	1.0	µA
SUPPLY							
Power-Supply Range					±4.5	±20	V
Positive Supply Current	I+	All channels on or off, V^+=+16.5V, V^-=-16.5V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
Negative Supply Current	I-	All channels on or off, V^+=+16.5V, V^-=-16.5V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
Logic Supply Current	I_L	All channels on or off, V^+=+16.5V, V^-=-16.5V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA
Ground Current	I_{GND}	All channels on or off, V^+=+16.5V, V^-=-16.5V, V_{IN}=0V or 5V	1 2,3	All	-1.0 -5.0	1.0 5.0	µA

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C V^+=+15V, V^-=-15V, GND=0V V_{INH}=2.4V, V_{INL}=0.8V, V_L=5V Unless otherwise specified	Group A Subgroup	Device type	Limits Min 3/	Limits Max 3/	Units
DYNAMIC							
Turn-On Time	t_{ON}	Figure 2	9	All		150	ns
Turn-Off Time	t_{OFF}	Figure 2	9	All		100	ns
Break-Before-Make Delay 4/	t_D	DG403 only, Figure 3	9	02	10		ns
Charge Injection 4/	Q	C_L=1.0nF, V_{GEN}=0V, R_{GEN}=0Ω Figure 4	9	All		15	pC

NOTE 3: This data sheet uses the algebraic convention, where the most negative value is a minimum and the most positive value is a maximum.

NOTE 4: Guaranteed by design.

NOTE 5: $\Delta r_{ON}=\Delta r_{ON}(max)-\Delta r_{ON}(min)$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

FIGURE 1: SWITCHING TIME TEST CIRCUIT: See Commercial Data Sheet
FIGURE 2: SWITCHING TIME TEST CIRCUIT: See Commercial Data Sheet
FIGURE 3: BREAK-BEFORE-MAKE INTERVAL: See Commercial Data Sheet
FIGURE 4: CHARGE INJECTION: See Commercial Data Sheet

ORDERING INFORMATION:	
DG401AK/883B 16 CDIP	DG403AZ/883B 20 LCC
DG401AZ/883B 20 LCC	DG405AK/883B 16 CDIP
DG403AK/883B 16 CDIP	DG405AZ/883B 20 LCC

TRUTH TABLES:

DG401 LOGIC	DG401 SWITCH	DG403 LOGIC	DG403 SWITCHES 1, 2	DG403 SWITCHES 3,4	DG405 LOGIC	DG405 SWITCH
0	OFF	0	OFF	ON	0	OFF
1	ON	1	ON	OFF	1	ON

TERMINAL CONNECTIONS:

	DG401	DG401	DG403	DG403	DG405	DG405
	J16	LCC20	J16	LCC20	J16	LCC20
1	D1	NC	D1	NC	D1	NC
2	NC	D1	NC	D1	NC	D1
3	NC	NC	D3	NC	D3	NC
4	NC	NC	S3	D3	S3	D3
5	NC	NC	S4	S3	S4	S3
6	NC	NC	D4	NC	D4	NC
7	NC	NC	NC	S4	NC	S4
8	D2	NC	D2	D4	D2	D4
9	S2	NC	S2	NC	S2	NC
10	IN2	D2	IN2	D2	IN2	D2
11	V+	NC	V+	NC	V+	NC
12	V_L	S2	V_L	S2	V_L	S2
13	GND	IN2	GND	IN2	GND	IN2
14	V-	V+	V-	V+	V-	V+
15	IN1	V_L	IN1	V_L	IN1	V_L
16	S1	NC	S1	NC	S1	NC
17		GND		GND		GND
18		V-		V-		V-
19		IN1		IN1		IN1
20		S1		S1		S1

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 9
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Subgroups 10 and 11, if not tested shall be guaranteed to the limits of Table 1.