PWM Power Control with Automatic Duty Cycle Reduction

Description

The U6084B is a bipolar technology PWM-IC designed for the control of an N-channel power MOSFET used as a high-side switch. The IC is ideal for use in the brightness control (dimming) of lamps such as, in dashboard applications. For a constant brightness the preselected duty cycle can be reduced automatically as a function of the supply voltage.

Features

- Pulse width modulation up to 2 kHz clock frequency
- Protection against short circuit, load-dump overvoltage and reverse V_S
- Duty cycle 0 to 100 % continuously
- Output stage for power MOSFET
- Interference and damage protection according to VDE 0839 and ISO/TR 7637/1.
- Charge pump noise suppressed
- Ground wire breakage protection

Ordering Information

Extended Type Number	Package	Remarks
U6084B–FP	SO16	

Block Diagram

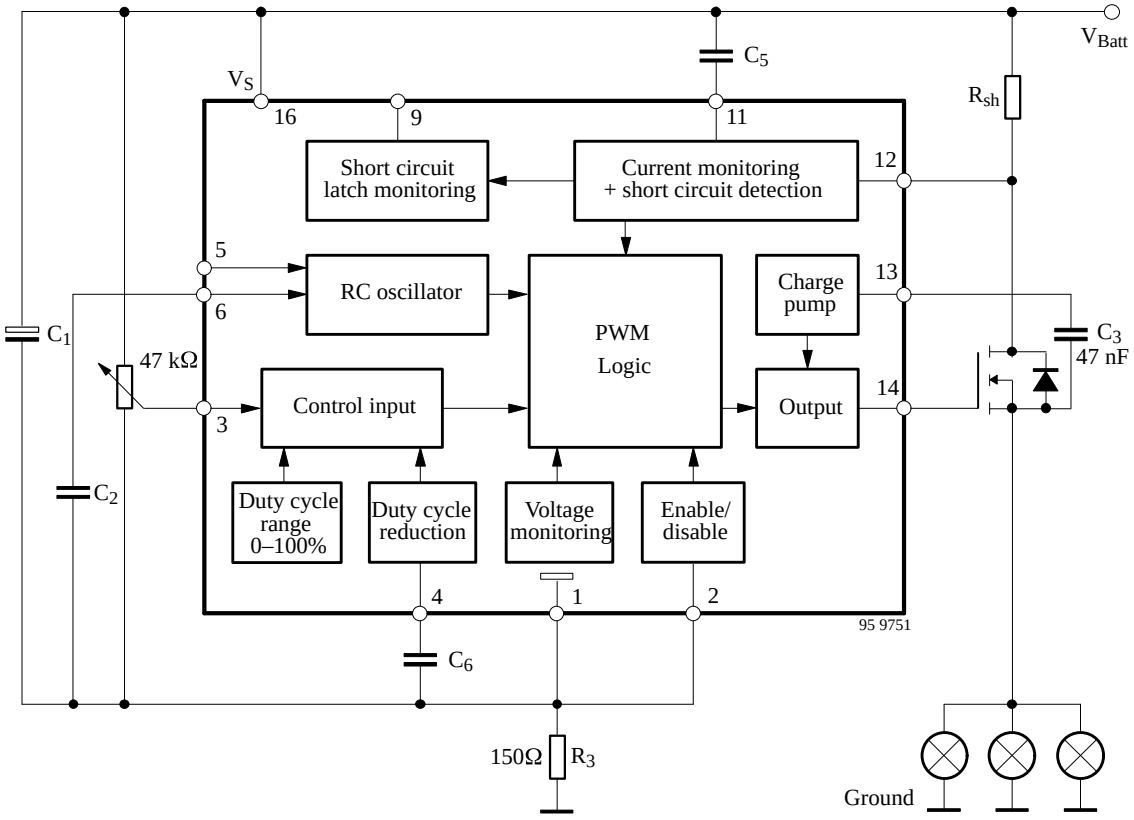
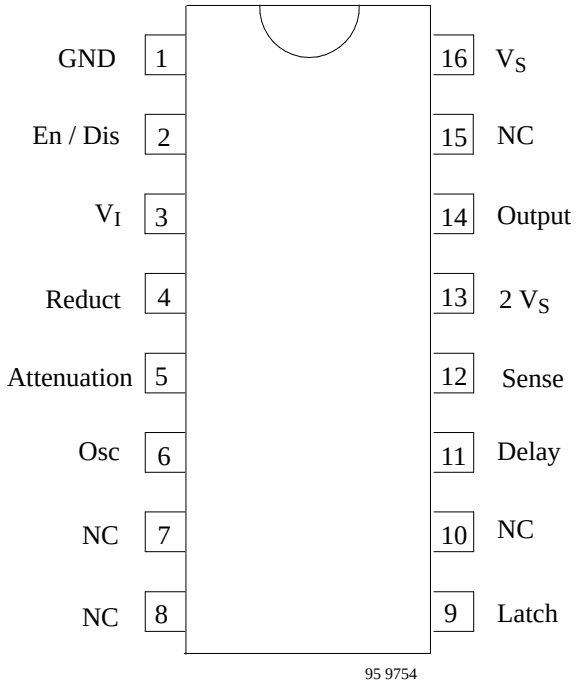


Figure 1. Block diagram with external circuit

Pin Description



Pin	Symbol	Function
1	GND	IC ground
2	En / Dis	Enable/disable
3	V_I	Control input (duty cycle)
4	Reduct	Duty cycle reduction
5	NC	Attenuation
6	Osc	Oscillator
7	NC	Not connected
8	NC	Not connected
9	Latch	Status short circuit latch
10	NC	Not connected
11	Delay	Short circuit protection delay
12	Sense	Current sensing
13	$2V_S$	Voltage doubler
14	Output	Output
15	NC	Not connected
16	V_S	Supply voltage V_S

Functional Description

Pin1, GND

Ground-Wire Breakage

To protect the FET in the case of ground-wire breakage, a 820 kΩ resistor between gate and source it is recommended to provide proper switch-off conditions.

Pin 2, Enable/Disable

The dimmer can be switched on or off with pin 2 independently of the set duty cycle.

V_2	Function
Approx. >0.7 V or open	Disable
< 0.7 V or connected to Pin 1	Enable

Pin 3, Control Input

The pulse width is controlled by means of an external potentiometer (47 kΩ). The characteristic (angle of rotation/duty cycle) is linear. The duty cycle can be varied from 0 to 100%. It is possible to further restrict the duty cycle with the resistors R_1 and R_2 (see figure 2).
Pin 3 is protected against short-circuit to V_{Batt} and ground GND ($V_{Batt} \leqq 16.5$ V).

Pin 4, Duty Cycle Reduction

With Pin 4 connected according to figure 2, the set duty cycle is reduced as from $V_{Batt} \approx 12.5$ V. This causes a power reduction in the FET and in the lamps. In addition, the brightness of the lamps is largely independent of the supply voltage range, V_{Batt} = 12.5 to 16 V.

Output Slope Control

The rise and fall time (t_r, t_f) of the lamp voltage can be limited to reduce radio interference. This is done with an integrator which controls a power MOSFET as source follower. The slope time is controlled by an external capacitor C4 and the oscillator current (see figure 2).

Calculation:

$$t_f = t_r = V_{Batt} \times \frac{C_4}{I_{osc}}$$

With V_{Batt} = 12 V, C_4 = 470 pF and I_{osc} = 40 µA,we thus obtain a controlled slope of

$$t_f = t_r = 12\ V \times \frac{470\ pF}{40\ \mu A} = 141\ \mu s$$

Pin 5, Attenuation

Capacitor C_4 connected to Pin 5 damps oscillation tendencies.

Pin 6, Oscillator

The oscillator determines the frequency of the output voltage. This is defined by an external capacitor, C_2. It is

charged with a constant current, I, until the upper switching threshold is reached. A second current source is then activated which taps a double current, $2 \times I$, from the charging current. The capacitor, C_2, is thus discharged by the current, I, until the lower switching threshold is reached. The second source is then switched off again and the procedure starts once more.

Example for Oscillator Frequency Calculation

$$V_{T100} = V_S \times \alpha_1 = (V_{Batt} - I_S \times R_3) \times \alpha_1$$

$$V_{T<100} = V_S \times \alpha_2 = (V_{Batt} - I_S \times R_3) \times \alpha_2$$

$$V_{TL} = V_S \times \alpha_3 = (V_{Batt} - I_S \times R_3) \times \alpha_3$$

where

V_{T100} = High switching threshold (100% duty cycle)

$V_{T<100}$ = High switching threshold (< 100% duty cycle)

V_{TL} = Low switching threshold

α_1, α_2 and α_3 are fixed constant.

The above mentioned threshold voltages are calculated for the following values given in the data sheet.

V_{Batt} = 12 V, I_S = 4 mA, R_3 = 150 Ω ,
α_1 = 0.7, α_2 = 0.67 and α_3 = 0.28.

$$V_{T100} = (12\ V - 4\ mA \times 150\ \Omega) \times 0.7 \approx 8\ V$$

$$V_{T<100} = 11.4\ V \times 0.67 = 7.6\ V$$

$$V_{TL} = 11.4\ V \times 0.28 = 3.2\ V$$

For a duty cycle of 100%, an oscillator frequency, f, is as follows:

$$f = \frac{I_{osc}}{2 \times (V_{T100} - V_{TL}) \times C_2}\ ,\ \text{where } C_2 = 22\ nF \text{ and } I_{osc} = 40\ \mu A$$

Therefore:

$$f = \frac{40\ \mu A}{2 \times (8\ V - 3.2\ V) \times 22\ nF} = 189\ Hz$$

For a duty cycle of less than 100%, the oscillator frequency, f, is as follows:

$$f = \frac{I_{osc}}{2 \times (V_{T<100} - V_{TL}) \times C_2 + 4 \times V_{Batt} \times C_4}$$

whereas C_4 = 470 pF

$$= \frac{40\ \mu A}{2 \times (7.6\ V - 3.2\ V) \times 22\ nF + 4 \times 12\ V \times 470\ pF}$$

$$= 185\ Hz$$

A selection of different values of C_2 and C_4, provides a range of oscillator frequency, f, from 10 to 2000 Hz.

Pins 7, 8, 10 and 15

Not connected.

Pin 9, Status Short Circuit Latch

The status of the short-circuit latch can be monitored via Pin 9 (open collector output).

Pin 9	Function
L	Short-circuit detected
H	No short-circuit detected

Pins 11 and 12, Short-Circuit Protection and Current Sensing

1. Short-Circuit Detection and Time Delay, t_d

The lamp current is monitored by means of an external shunt resistor. If the lamp current exceeds the threshold for the short-circuit detection circuit ($V_{T2} \approx 90$ mV), the duty cycle is switched over to 100% and the capacitor C_5 is charged by a current source of 20 µA ($I_{ch} - I_{dis}$). The external FET is switched off after the cut-off threshold (V_{T11}) is reached. Renewed switching on the FET is possible only after a power-on reset. The current source, I_{dis}, ensures that the capacitor C_5 is not charged by parasitic currents. The capacitor C_5 is discharged by I_{dis} to typ. 0.7 V.

Time delay, t_d, is as follows:

$$t_d = C_5 \cdot (V_{T11} - 0.7\ V)/(I_{ch} - I_{dis})$$

With C_5 = 330 nF and V_{Batt} = 12 V, we have

$$t_d = 330\ nF \cdot (9.8\ V - 0.7\ V)/20\ \mu A$$

$$= 150\ ms.$$

2. Current Limitation

The lamp current is limited by a control amplifier that protects the external power transistor. The voltage drop across an external shunt resistor acts as the measured variable. Current limitation takes place for a voltage drop of $V_{T1} \approx 100$ mV. Owing to the difference $V_{T1}–V_{T2} \approx 10$ mV, current limitation occurs only when the short-circuit detection circuit has responded.
After a power-on reset, the output is inactive for half an oscillator cycle. During this time , the supply voltage capacitor can be charged so that current limitation is guaranteed in the event of a short circuit when the IC is switched on for the first time.

Pins 13 and 14, Charge Pump and Output

Output, Pin 14, is suitable for controlling a power MOSFET. During the active integration phase, the supply current of the operational amplifier is mainly supplied by the capacitor C_3 (bootstrapping). Additionally, a trickle charge is generated by an integrated oscillator ($f_{13} \approx 400$ kHz) and a voltage doubler circuit. This permits a gate voltage supply at a duty cycle of 100%.

Pin 16, Supply Voltage, V_S or V_{Batt}

Undervoltage Detection:

In the event of voltages of approx. $V_{Batt} < 5.0$ V, the external FET is switched off and the latch for short-circuit detection is reset.

A hysteresis ensures that the FET is switched on again at approximately $V_{Batt} \geq 5.4$ V.

Overvoltage Detection

Stage 1

If overvoltages $V_{Batt} > 20$ V (typ.) occur, the external transistor is switched off and switched on again at $V_{Batt} < 18.5$ V (hysteresis).

Stage 2

If $V_{Batt} > 28.5$ V (typ.), the voltage limitation of the IC is reduced from 26 V to 20 V. The gate of the external transistor remains at the potential of the IC ground, thus producing voltage sharing between FET and lamps in the event of overvoltage pulses occuring (e.g., load-dump). The short-circuit protection is not in operation. At $V_{Batt} < 23$ V, the overvoltage detection stage 2 is switched off.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Junction temperature	T_j	150	°C
Ambient temperature range	T_{amb}	–40 to +110	°C
Storage temperature range	T_{stg}	–55 to +125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	120	K/W

Electrical Characteristics

T_{amb} = –40 to +110°C, V_{Batt} = 9 to 16.5 V, (basic function is guaranteed between 6.0 V to 9.0 V) reference point ground, unless otherwise specified (see figure 1). All other values refer to Pin GND (Pin 1).

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Current consumption	Pin 16	I_S			6.8	mA
Supply voltage	Overvoltage detection, stage 1	V_{Batt}			25	V
Stabilized voltage	I_S = 10 mA Pin 16	V_S	24.5		27.0	V
Battery undervoltage detection	– on – off	V_{Batt}	4.4 4.8	5.0 5.4	5.6 6.0	V

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Battery overvoltage detection	Pin 2					
Stage 1:	– on – off	V_{Batt}	18.3 16.7	20.0 18.5	21.7 20.3	V
Stage 2:	– on – off	V_{Batt}	25.5 19.5	28.5 23.0	32.5 26.5	V
Stabilized voltage	I_S = 30 mA Pin 16	V_Z	18.5	20.0	21.5	V
Short-circuit protection	Pin 12					
Short-circuit current limitation	$V_{T1} = V_S - V_{12}$	V_{T1}	85	100	120	mV
Short-circuit detection	$V_{T2} = V_S - V_{12}$	V_{T2}	75	90	105	mV
		$V_{T1} - V_{T2}$	3	10	30	mV
Delay timer short circuit detection	Pin 11					
Switched off threshold	$V_{T11} = V_S - V_{11}$	V_{T11}	9.5	9.8	10.1	V
Charge current		I_{ch}		23		µA
Dicharge current		I_{dis}		3		µA
Capacitance current	$I_5 = I_{ch} - I_{dis}$	I_5	13	20	27	mA
Output short-circuit latch	Pin 9					
Saturation voltage	I_9 = 100 µA	V_{sat}		150	350	mV
Voltage doubler	Pin 13					
Voltage	Duty cycle 100%	V_{13}	2 V_S			
Oscillator frequency		f_{13}	280	400	520	kHz
Internal voltage limitation	I_{13} = 5 mA	V_{13}	26	27.5	30.0	V
	(whichever is lower)	V_{13}	(V_{S+14})	(V_{S+15})	(V_{S+16})	
Gate output	Pin 14					
Voltage	Low level	V_{14}	0.35	0.70	0.95	V
	V_{Batt} = 16.5 V, T_{amb} = 110 °C, R_3 = 150 Ω				1.5 *)	
	High level, duty cycle 100%	V_{14}		V_{13}		
Current	V_{14} = Low level	I_{14}	1.0			mA
	V_{14} = High level, $I_{13} > \lvert I_{14} \rvert$		–1.0			
Enable/ Disable	Pin 2					
Current	V_2 = 0 V	I_2	–20	–40	–60	µA
Duty cycle reduction	Pin 4					
Z-voltage	I_4 = 500 µA	V_4	6.9	7.4	8.0	V
Oscillator						
Frequency	Pin6	f	10		2000	Hz
Threshold cycle Upper	V_{14} = High, $\alpha_1 = \frac{V_{T100}}{V_S}$	α_1	0.68	0.7	0.72	
	V_{14} = Low, $\alpha_2 = \frac{V_{T<100}}{V_S}$	α_2	0.65	0.67	0.69	
Lower	$\alpha_3 = \frac{V_{TL}}{V_S}$	α_3	0.26	0.28	0.3	
Oscillator current	V_{Batt} = 12 V	$\pm I_{osc}$	26	40	54	µA
Frequency tolerance	C_4 open, C_2 = 470 nF, duty cycle = 50%	f	6.0	9.9	13.5	Hz

*) Reference point is battery ground.

Application

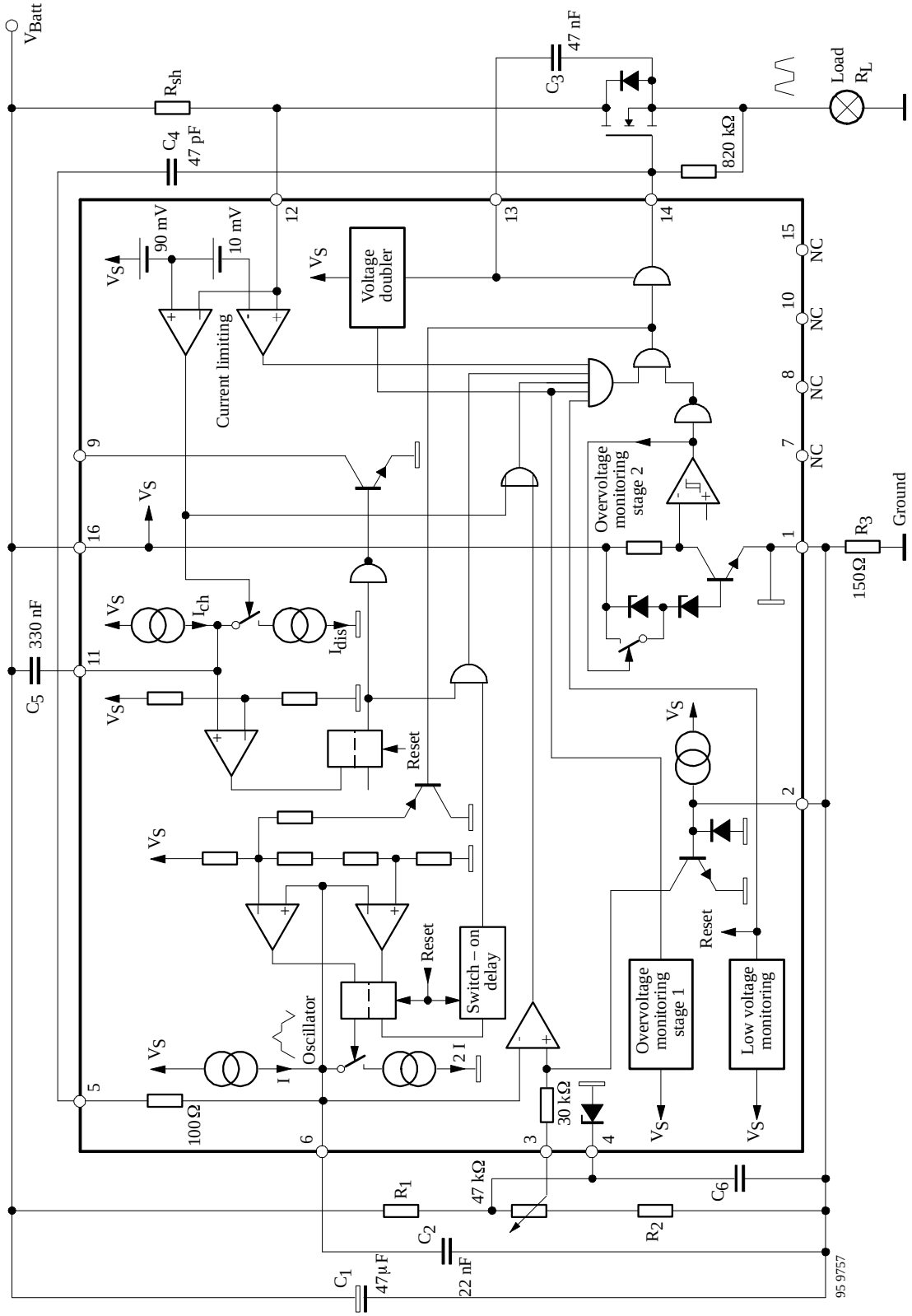
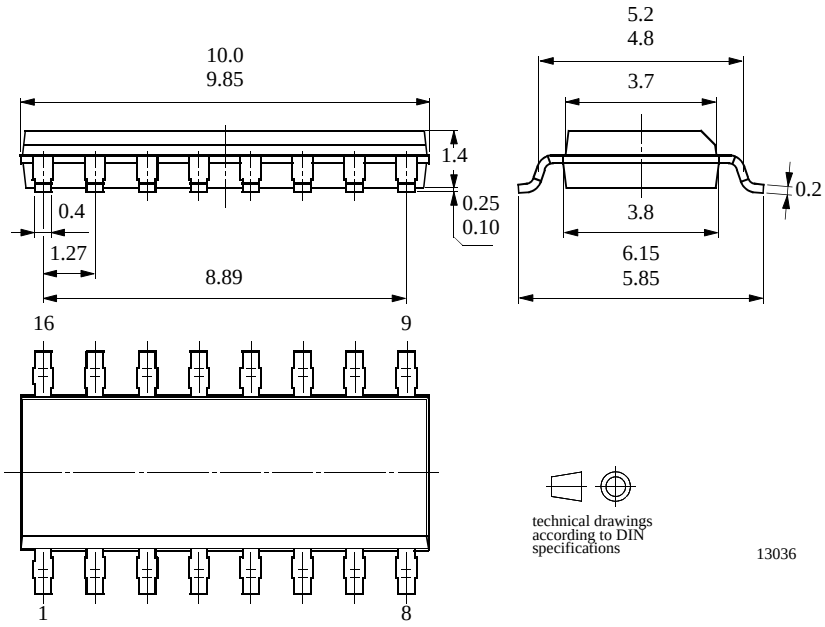


Figure 2.

Dimensions in mm

Package SO16
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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