MIC4421A/22A

9A Peak Low-Side MOSFET Drivers

Features

- High Output Current: 9A Peak (Typical)
- Wide Operating Range: 4.5V to 18V (Typical)
- Minimum Pulse Width: 50 ns
- Latch-Up Proof: Fully Isolated Process is Inherently Immune to Any Latch-Up
- Input Will Withstand Negative Swing of Up to 5V
- High Capacitive Load Drive: 47,000 pF
- Low Delay Time: 15 ns (Typical)
- Logic High Input for Any Voltage from 2.4V to V_S
- Low Equivalent Input Capacitance: 7 pF (typical)
- Low Supply Current: 500 µA (Typical)
- Output Voltage Swing to Within 25 mV of GND or V_S

Applications

- Switch Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class-D Switching Amplifiers
- Line Drivers
- Driving MOSFET or IGBT Parallel Chip Modules
- Local Power On/Off Switch
- Pulse Generators

General Description

The MIC4421A and MIC4422A MOSFET drivers are rugged, efficient, and easy to use. The MIC4421A is an inverting driver, while the MIC4422A is a non-inverting driver.

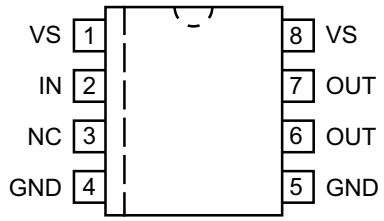
Both versions are capable of 9A (peak) output and can drive the largest MOSFETs with an improved safe operating margin. The MIC4421A/4422A accepts any logic input from 2.4V to V_S without external speed-up capacitors or resistor networks. Proprietary circuits allow the input to swing negative by as much as 5V without damaging the part. Additional circuits protect against damage from electrostatic discharge.

MIC4421A/22A drivers can replace three or more discrete components, reducing PCB area requirements, simplifying product design, and reducing assembly cost.

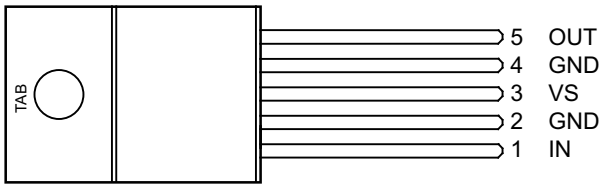
Modern Bipolar/CMOS/DMOS construction guarantees freedom from latch-up. The rail-to-rail swing capability of CMOS/DMOS ensures adequate gate voltage to the MOSFET during power up/down sequencing. Because these devices are fabricated on a self-aligned process, they have very low crossover current, run cool, use little power, and are easy to drive.

Package Types

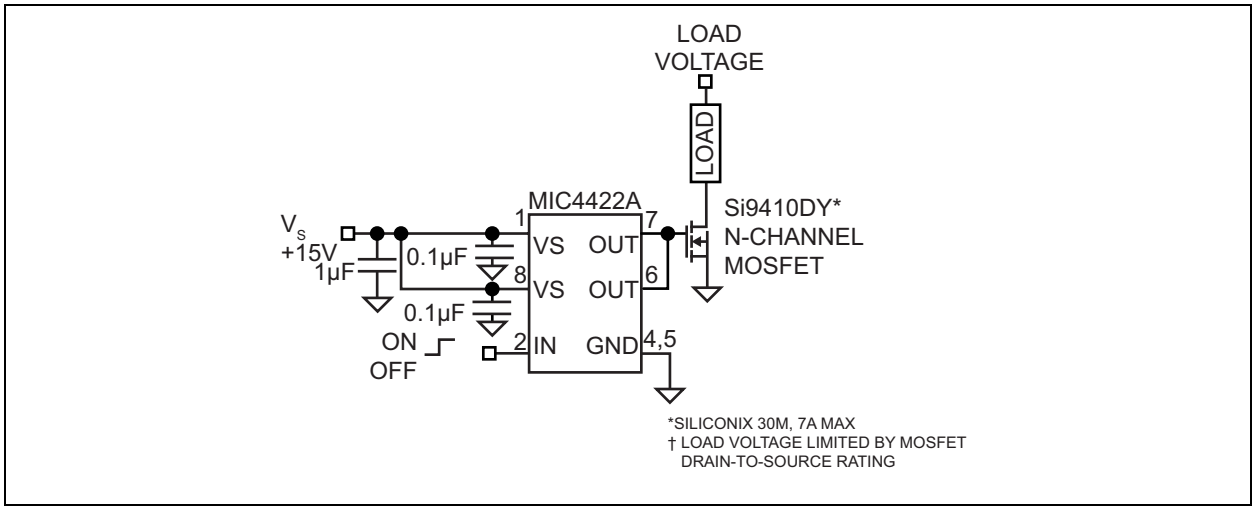
MIC4421A/22A
SOIC-8 (M)
PDIP-8 (N)
(Top View)



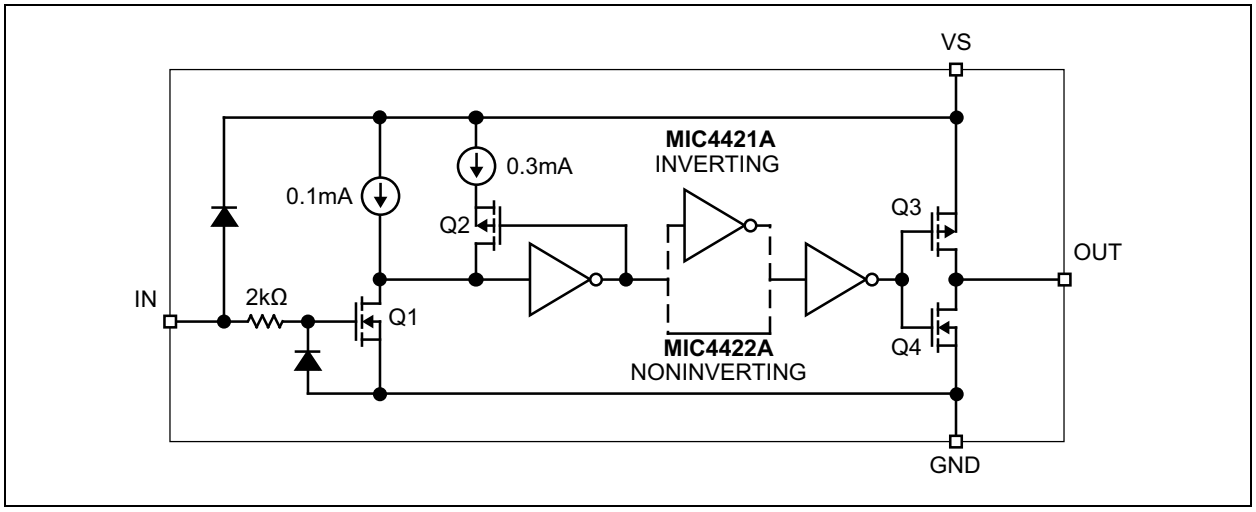
MIC4421A/22A
5-Lead TO-220 (T)
(Top View)



Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_S) ..... +20V
Control Input Voltage (V_{IN}) ..... V_S + 0.3V to GND – 5V
Control Input Current ($V_{IN} > V_S$) ..... 50 mA
Power Dissipation ($T_A \leq +25°C$, Note 1)
PDIP (θ_{JA}) ..... 1478 mW
SOIC (θ_{JA}) ..... 767 mW
TO-220 (θ_{JA}) 1756W
ESD Rating (Note 2) ..... 2 kV

Operating Ratings ††

Supply Voltage (V_S) ..... +4.5V to +18V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Minimum footprint.

2: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $T_A = +25°C$ with $4.5V \leq V_S \leq 18V$, **bold** values valid for X Version: $–55°C \leq T_A \leq +125°C$, for Y Version: $–40°C \leq T_A \leq +85°C$, and for Z Version: $0°C \leq T_A \leq +70°C$, unless noted.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply						
Operating Input Voltage	V_S	**4.5**	—	**18**	V	—
High Output Quiescent Current	I_S	—	0.5	1.5	mA	V_{IN} = 3V (MIC4422A), V_{IN} = 0 (MIC4421A)
		—	—	**3**		
Low Output Quiescent Current		—	50	150	µA	V_{IN} = 0V (MIC4422A), V_{IN} = 3V (MIC4421A)
		—	—	**200**		
Input						
Logic 1 Input Voltage	V_{IH}	**3.0**	2.1	—	V	See Figure 1-3
Logic 0 Input Voltage	V_{IL}	—	1.5	**0.8**	V	See Figure 1-3
Input Voltage Range	V_{IN}	**–5**	—	**V_S + 0.3**	V	—
Input Current	I_{IN}	**–10**	—	**10**	µA	$0V \leq V_{IN} \leq V_S$
Output						
High Output Voltage	V_{OH}	**V_S + .025**	—	—	V	See Figure 1-1
Low Output Voltage	V_{OL}	—	—	**0.025**	V	See Figure 1-1
Output Resistance, Output High	R_O	—	0.6	1.0	Ω	I_{OUT} = 10 mA, V_S = 18V
		—	—	**3.6**		
Output Resistance, Output Low		—	0.8	1.7	Ω	I_{OUT} = 10 mA, V_S = 18V
		—	—	**2.7**		

Note 1: Guaranteed by design.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: T_A = +25°C with 4.5V ≤ V_S ≤ 18V, **bold** values valid for X Version: –55°C ≤ T_A ≤ +125°C, for Y Version: –40°C ≤ T_A ≤ +85°C, and for Z Version: 0°C ≤ T_A ≤ +70°C, unless noted.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Peak Output Current	I_{PK}	—	9	—	A	V_S = 18V, See Figure 5-2
Continuous Output Current	I_{DC}	—	2	—	A	—
Latch-Up Protection Withstand Reverse Current	I_R	>1500	—	—	mA	Duty Cycle ≤ 2%, t ≤ 300 µs, Note 1
Switching Time, Note 1						
Rise Time	t_r	—	20	75	ns	Figure 1-1, C_L = 10,000 pF
		—	—	**120**		
Fall Time	t_f	—	24	75	ns	Figure 1-1, C_L = 10,000 pF
		—	—	**120**		
Delay Time	t_{D1}	—	15	68	ns	Figure 1-1
		—	—	**80**		
	t_{D2}	—	35	60	ns	Figure 1-1
		—	—	**80**		
Minimum Input Pulse Width	t_{PW}	—	50	—	ns	See Figure 1-1 and Figure 1-2.
Maximum Input Frequency	f_{MAX}	—	1	—	MHz	See Figure 1-1 and Figure 1-2.

Note 1: Guaranteed by design.

Test Circuits

Note that the output pulse width may increase with input pulse widths less than 50 ns.

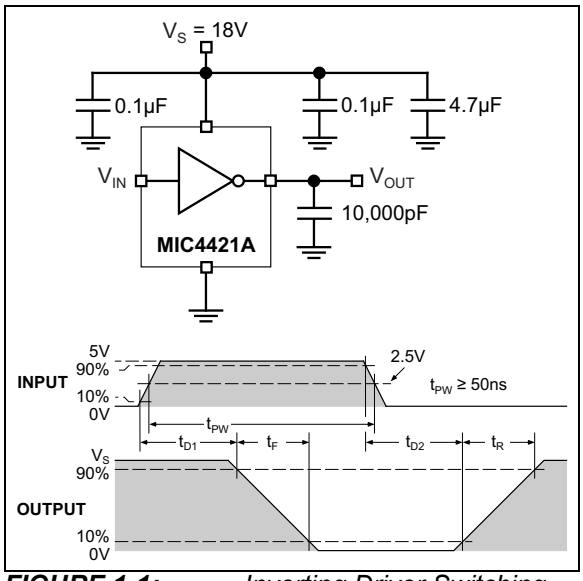


FIGURE 1-1: *Inverting Driver Switching Time.*

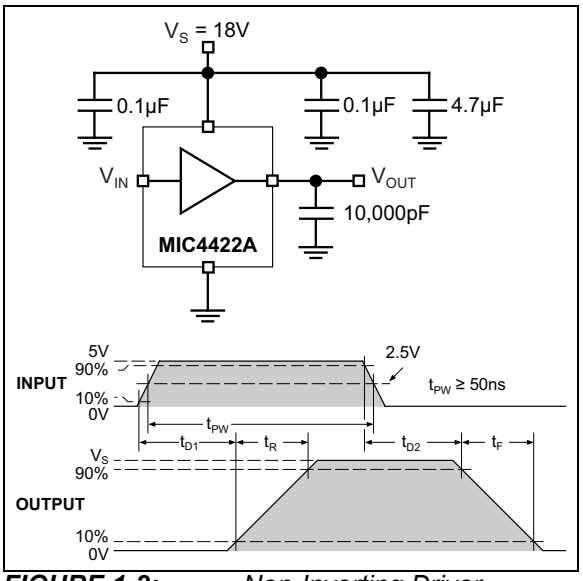


FIGURE 1-2: *Non-Inverting Driver Switching Time.*

Control Input Behavior

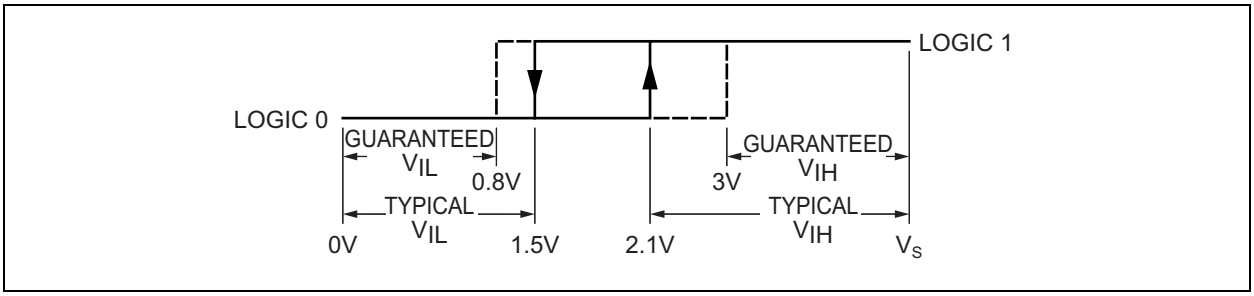


FIGURE 1-3: *Input Hysteresis.*

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+300	°C	Soldering, 10 sec.
Ambient Operating Temperature Range	T_A	0	—	+70	°C	Z option
		–40	—	+85	°C	Y option
		–55	—	+125		X option
Package Thermal Resistances						
Thermal Resistance, PDIP 8-Ld	θ_{JA}	—	84.6	—	°C/W	—
Thermal Resistance, SOIC 8-Ld	θ_{JA}	—	163	—	°C/W	—
Thermal Resistance, TO-220 5-Ld	θ_{JA}	—	71.2	—	°C/W	—
Thermal Resistance, PDIP 8-Ld	θ_{JC}	—	41.2	—	°C/W	—
Thermal Resistance, SOIC 8-Ld	θ_{JC}	—	38.8	—	°C/W	—
Thermal Resistance, TO-220 5-Ld	θ_{JC}	—	6.5	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

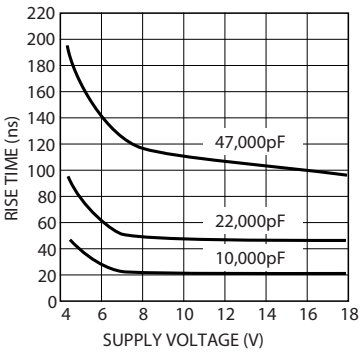


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

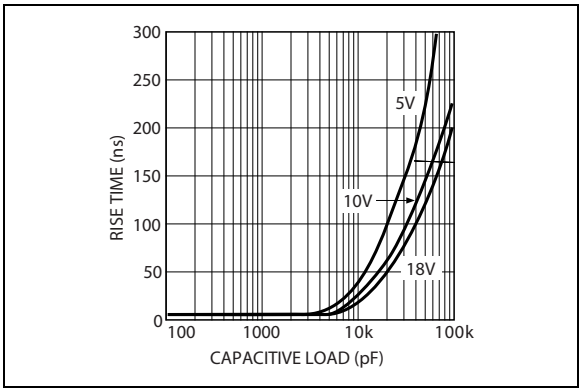


FIGURE 2-4: *Rise Time vs. Capacitive Load.*

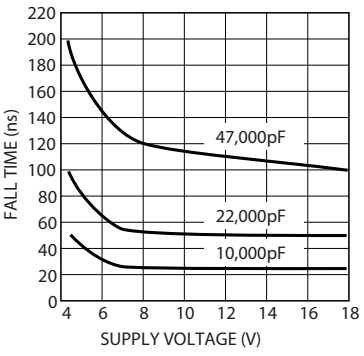


FIGURE 2-2: *Fall Time vs. Supply Voltage.*

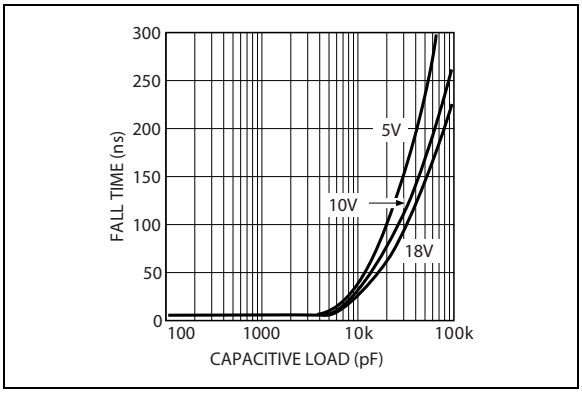


FIGURE 2-5: *Fall Time vs. Capacitive Load.*

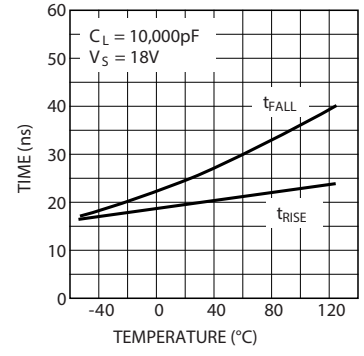


FIGURE 2-3: *Rise and Fall Times vs. Temperature.*

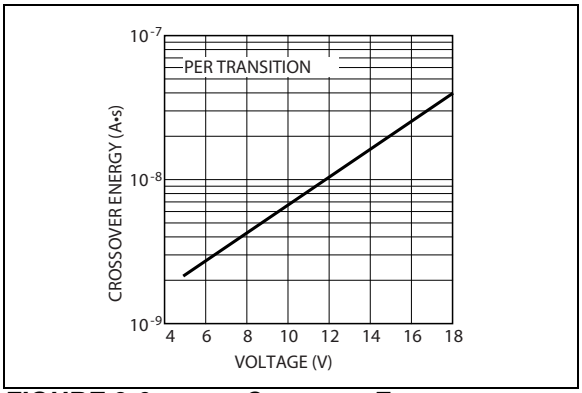


FIGURE 2-6: *Crossover Energy vs. Supply Voltage.*

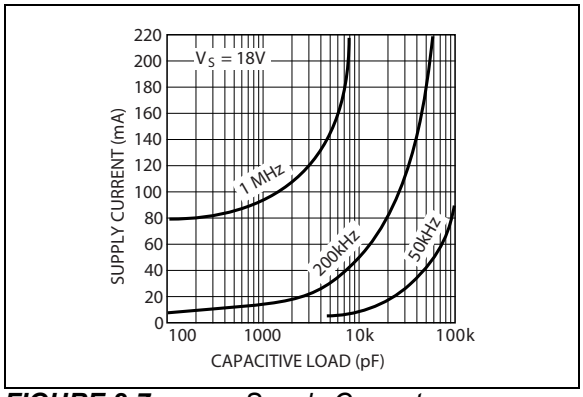


FIGURE 2-7: *Supply Current vs. Capacitive Load (V_S = 18V).*

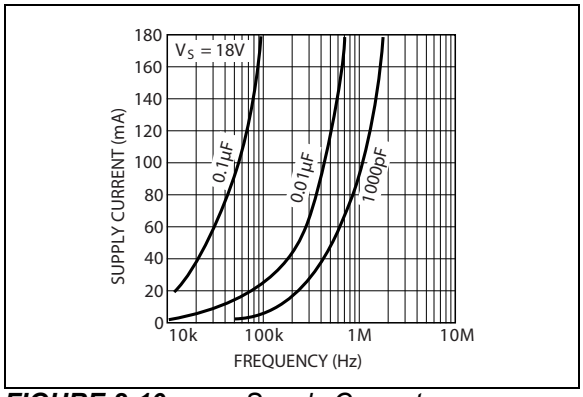


FIGURE 2-10: *Supply Current vs. Frequency (V_S = 18V).*

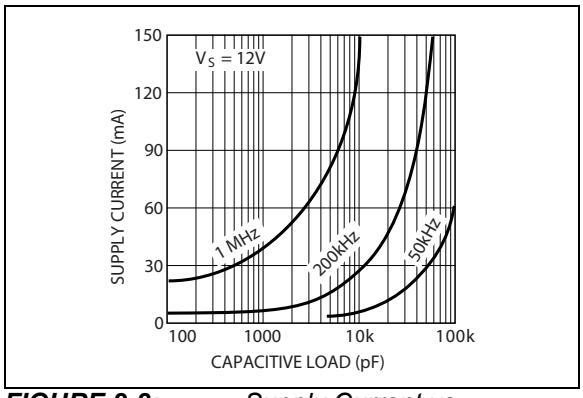


FIGURE 2-8: *Supply Current vs. Capacitive Load (V_S = 12V).*

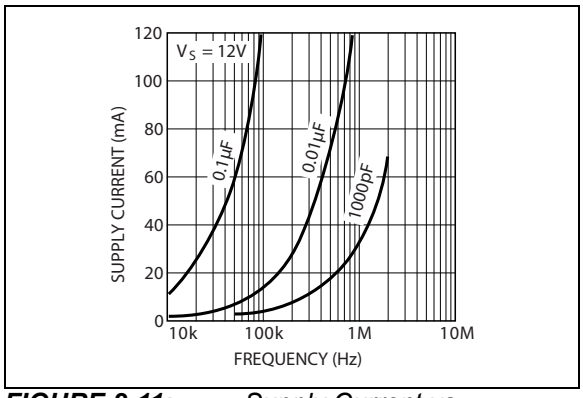


FIGURE 2-11: *Supply Current vs. Frequency (V_S = 12V).*

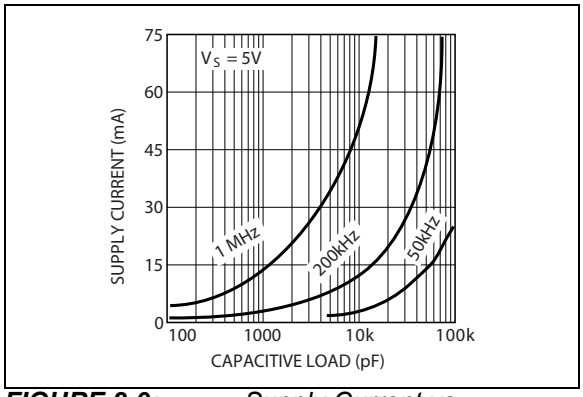


FIGURE 2-9: *Supply Current vs. Capacitive Load (V_S = 5V)*

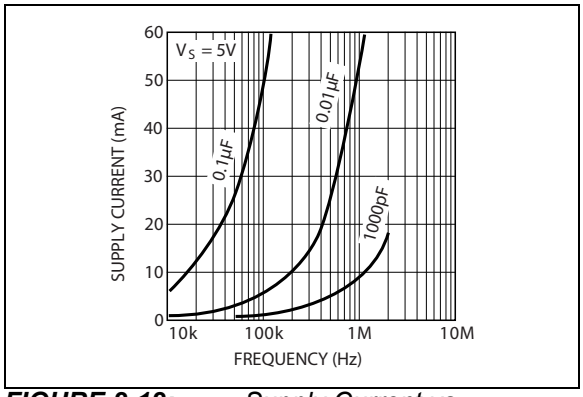


FIGURE 2-12: *Supply Current vs. Frequency (V_S = 5V).*

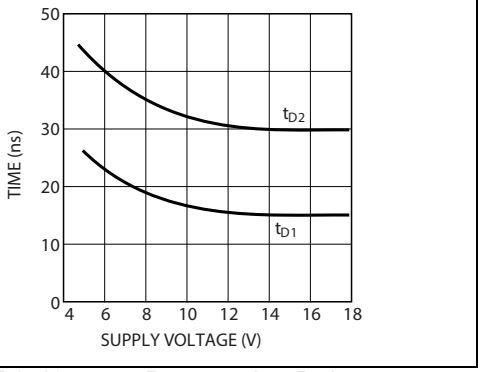


FIGURE 2-13: *Propagation Delay vs. Supply Voltage.*

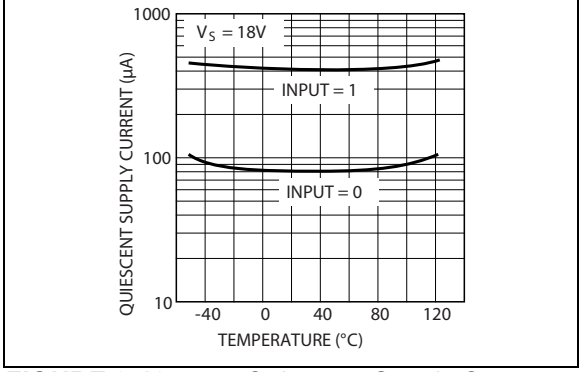


FIGURE 2-16: *Quiescent Supply Current vs. Temperature.*

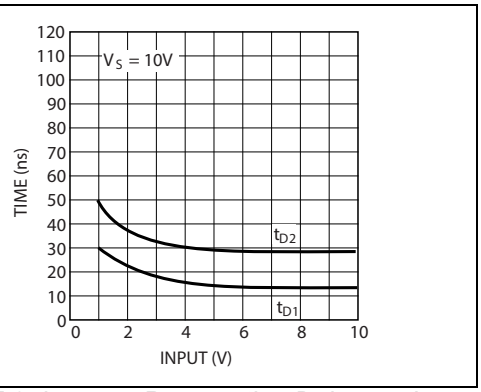


FIGURE 2-14: *Propagation Delay vs. Input Amplitude.*

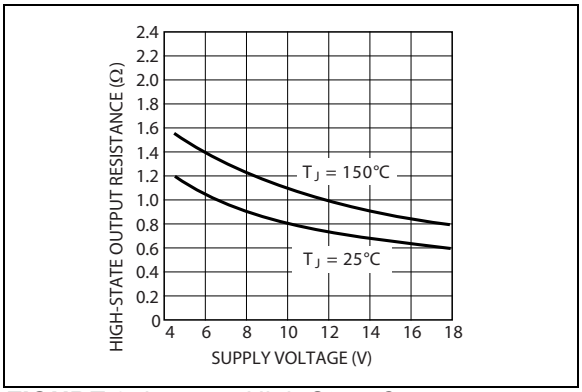


FIGURE 2-17: *High-State Output Resistance vs. Supply Voltage.*

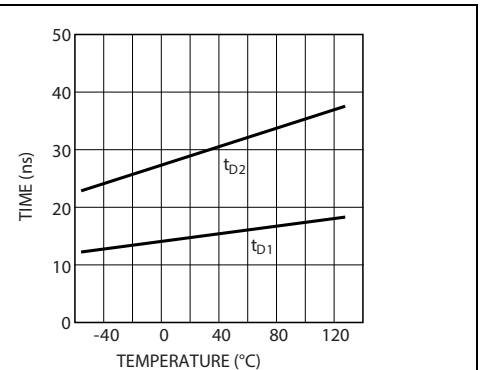


FIGURE 2-15: *Propagation Delay vs. Temperature.*

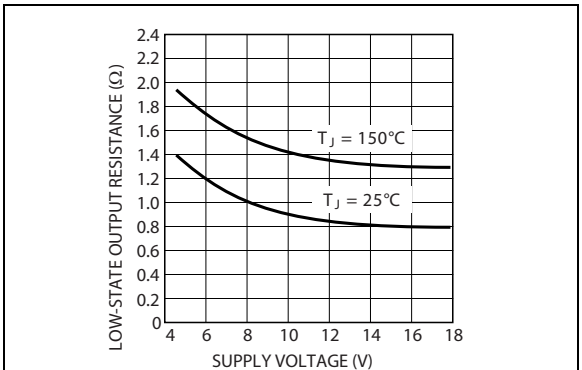


FIGURE 2-18: *Low-State Output Resistance vs. Supply Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number PDIP/SOIC	Pin Number TO-220	Pin Name	Description
2	1	IN	Control Input.
4, 5	2, 4	GND	Ground: Duplicate pins must be externally connected.
1, 8	3, TAB	VS	Supply Input: Duplicate pins must be externally connected.
6, 7	5	OUT	Output: Duplicate pins must be externally connected.
3	—	NC	Not connected.

4.0 FUNCTIONAL DESCRIPTION

Refer to the Functional Block Diagram.

The MIC4422A is a non-inverting driver. A logic high on the IN produces gate drive output. The MIC4421A is an inverting driver. A logic low on the IN produces gate drive output. The output is used to turn on an external N-channel MOSFET.

4.1 Supply

VS (supply) is rated for +4.5V to +18V. External capacitors are recommended to decouple noise.

4.2 Input

IN (control) is a TTL-compatible input. IN must be forced high or low by an external signal. A floating input will cause unpredictable operation.

A high input turns on Q1, which sinks the output of the 0.1 mA and the 0.3 mA current source, forcing the input of the first inverter low.

4.3 Hysteresis

The control threshold voltage, when IN is rising, is slightly higher than the control threshold voltage when CTL is falling.

When IN is low, Q2 is on, which applies the additional 0.3 mA current source to Q1. Forcing IN high turns on Q1 which must sink 0.4 mA from the two current sources. The higher current through Q1 causes a larger drain-to-source voltage drop across Q1. A slightly higher control voltage is required to pull the input of the first inverter down to its threshold.

Q2 turns off after the first inverter output goes high. This reduces the current through Q1 to 0.1 mA. The lower current reduces the drain-to-source voltage drop across Q1. A slightly lower control voltage will pull the input of the first inverter up to its threshold.

4.4 Drivers

The second (optional) inverter permits the driver to be manufactured in inverting and non-inverting versions.

The last inverter functions as a driver for the output MOSFETs Q3 and Q4.

4.5 Output

OUT is designed to drive a capacitive load. V_{OUT} (output voltage) is either approximately the supply voltage or approximately ground, depending on the logic state applied to IN.

If IN is high, and V_S (supply) drops to zero, the output will be floating (unpredictable).

5.0 APPLICATION INFORMATION

5.1 Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 10,000 pF load to 18V in 50 ns requires 3.6A.

The MIC4421A/22A has double bonding on the supply pins, the ground pins, and output pins. This reduces parasitic lead inductance. Low inductance enables large currents to be switched rapidly. It also reduces internal ringing that can cause voltage breakdown when the driver is operated at or near the maximum rated voltage.

Internal ringing can also cause output oscillation due to feedback. This feedback is added to the input signal because it is referenced to the same ground.

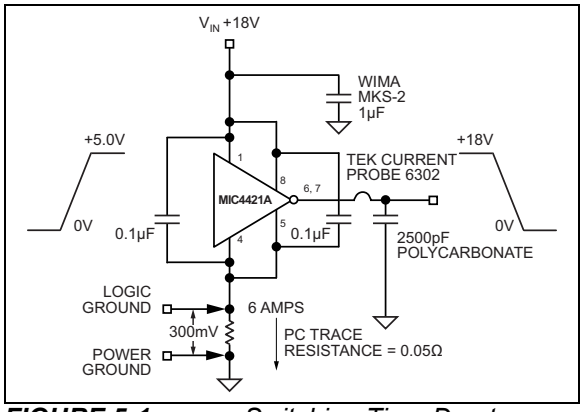


FIGURE 5-1: *Switching Time Due to Negative Feedback.*

TABLE 5-1: MIC4421A MAX. OPERATING FREQUENCY

V_S	Maximum Frequency
18V	220 kHz
15V	300 kHz
10V	640 kHz
5V	2 MHz
Conditions: θ_{JA} = 150°C/W, T_A = 25°C, C_L = 10,000 pF.	

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitor with short lead lengths (<0.5 inch) should be used. A 1 µF low-ESR film capacitor in parallel with two 0.1 µF low-ESR ceramic capacitors, (such as AVX RAM Guard®), provides adequate bypassing. Connect one ceramic capacitor directly between pins 1 and 4. Connect the second ceramic capacitor directly between pins 8 and 5.

5.2 Grounding

The high current capability of the MIC4421A/22A demands careful PCB layout for best performance. Because the MIC4421A is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. Feedback is especially noticeable with slow rise time inputs. The MIC4421A input structure includes about 600 mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 5-1 shows the feedback effect in detail. As the MIC4421A input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the MIC4421A ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillation may result.

To ensure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the MIC4421A GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the MIC4421A GND pins should, however, still be connected to power ground.

5.3 Input Stage

The input voltage level of the MIC4421A changes the quiescent supply current. The N-Channel MOSFET input stage transistor drives a 320 µA current source load. With a logic “1” input, the quiescent supply current is typically 500 µA. Logic “0” input level signals reduce quiescent current to 80 µA typical.

The MIC4421A/22A input is designed to provide 600 mV of hysteresis. This provides clean transitions, reduces noise sensitivity, and minimizes output stage current spiking when changing states. Input voltage threshold level is approximately 1.5V, making the device TTL-compatible over the full temperature and operating supply voltage ranges. Input current is less than ±10 µA.

The MIC4421A can be directly driven by the TL494, SG1526/1527, SG1524, TSC170, MIC38C42, and similar switch mode power supply integrated circuits. By off-loading the power-driving duties to the MIC4421A/22A, the power supply controller can operate at lower dissipation. This can improve performance and reliability.

The input can be greater than the V_S supply, however, current will flow into the input lead. The input currents can be as high as 30 mA_{PP} (6.4 mA_{RMS}) with the input. No damage will occur to the MIC4421A/22A, however, and it will not latch.

The input appears as a 7 pF capacitance and does not change even if the input is driven from an AC source.

5.4 Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 and 74C have outputs that can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The MIC4421A/22A on the other hand, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

The supply current vs. frequency and supply current vs. capacitive load characteristic curves aid in determining power dissipation calculations. Table 5-1 lists the maximum safe operating frequency for several power supply voltages when driving a 10,000 pF load. More accurate power dissipation figures can be obtained by summing the three dissipation sources.

Given the power dissipation in the device and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-lead plastic DIP package, from the data sheet, is 84.6°C/W. In a 25°C ambient, then, using a maximum junction temperature of 150°C, this package will dissipate 1478 mW.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load Power Dissipation (PL)
- Quiescent power dissipation (PQ)
- Transition power dissipation (PT)

Calculation of load power dissipation differs depending on whether the load is capacitive, resistive or inductive.

5.5 Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

EQUATION 5-1:

$$P_L = I^2 \times R_O \times D$$

Where:
I = The current drawn by the load.
R_O = The output resistance of the driver when the output is high, at the power supply voltage used.
D = Fraction of time the load is conducting (duty cycle).

5.6 Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

EQUATION 5-2:

$$E = 1/2 \times C \times V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations, the 1/2 is removed. This equation also shows that it is good practice not to place more voltage in the capacitor than is necessary, because dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

EQUATION 5-3:

$$P_L = f \times C \times V_S^2$$

Where:
f = Operating frequency.
C = Load capacitance.
V_S = Driver supply voltage.

5.7 Inductive Load Power Dissipation

For inductive loads, the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

EQUATION 5-4:

$$P_{L1} = I^2 \times R_O \times D$$

However, in this instance, the R_O required may be either the on-resistance of the driver when its output is in the high state, or its on-resistance when the driver is in the low state. This depends on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as:

EQUATION 5-5:

$$P_{L2} = I \times V_D \times (1 - D)$$

Where:
V_D = The forward voltage drop of the clamp diode in the driver (generally around 0.7V).

The two parts of the load dissipation must be summed in to produce P_L:

EQUATION 5-6:

$$P_L = P_{L1} + P_{L2}$$

5.8 Quiescent Power Dissipation

Quiescent power dissipation (P_Q, as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤0.2 mA; logic high will result in a current drain of ≤3.0 mA.

Quiescent power can therefore be found from:

EQUATION 5-7:

$$P_Q = V_S \times (D \times I_H + (1 - D) \times I_L)$$

Where:
I_H = Quiescent current with input high.
I_L = Quiescent current with input low.
D = Fraction of time input is high (duty cycle).
V_S = Power supply voltage.

5.9 Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-Channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V_S to ground. The transition power dissipation is approximately:

EQUATION 5-8:

$$P_T = 2 \times f \times V_S \times (A \bullet s)$$

A•s is a time-current factor derived from the typical operating characteristic curve Figure 2-6.

Total power (P_D) then, as previously described, is just:

EQUATION 5-9:

$$P_D = P_L + P_Q + P_T$$

5.10 Definitions

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

f = Operating Frequency of the driver in Hertz.

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

P_L = Power dissipated in the driver due to the driver's load in Watts.

P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts.

R_O = Output resistance of a driver in Ohms.

V_S = Power supply voltage to the IC in Volts.

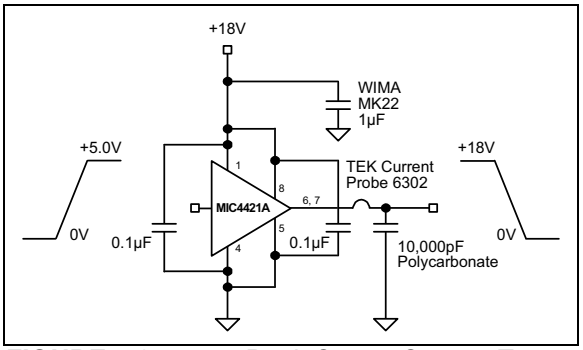
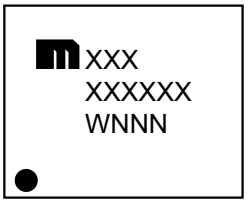


FIGURE 5-2: *Peak Output Current Test Circuit.*

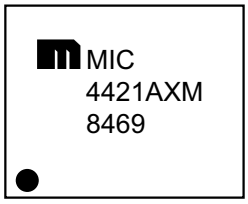
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

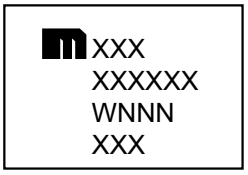
8-Lead SOIC*



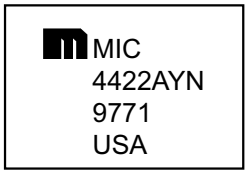
Example



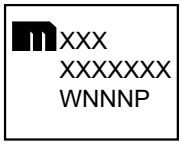
8-Lead PDIP*



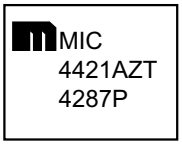
Example



5-Lead TO-220*



Example

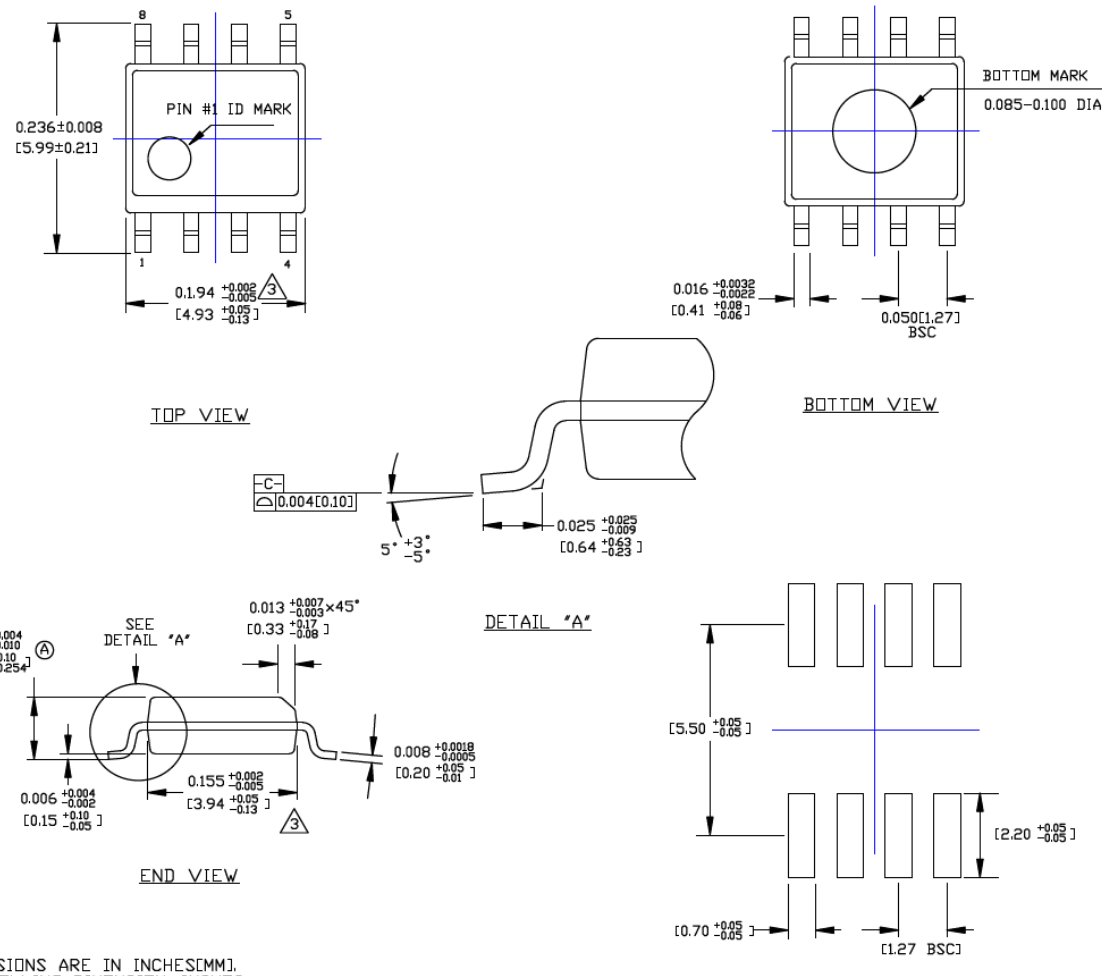


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

8-Lead SOICN Package Outline & Recommended Land Pattern

TITLE
8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOICN-8LD-PL-1	UNIT	INCH [MM]



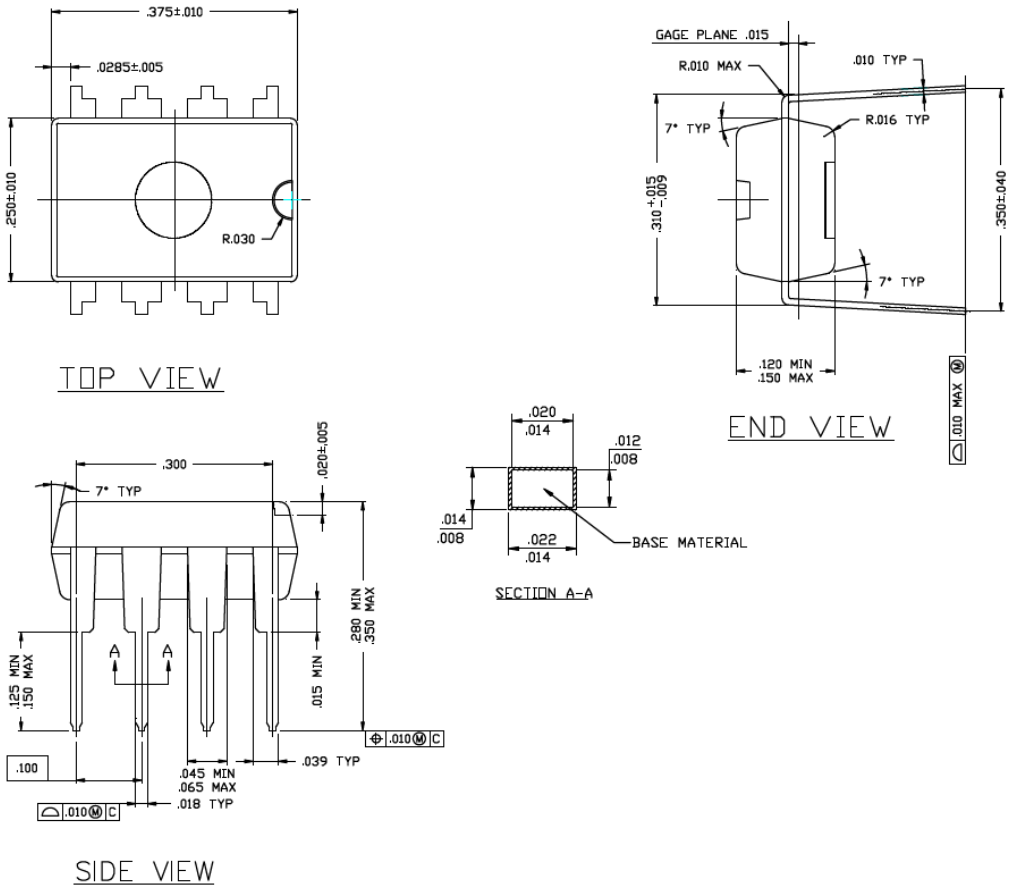
NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

8-Lead PDIP Package Outline and Recommended Land Pattern

TITLE
8 LEAD PDIP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	PDIP-8LD-PL-1	**UNIT**	INCH
Lead Frame	Copper	**Lead Finish**	Matte Tin

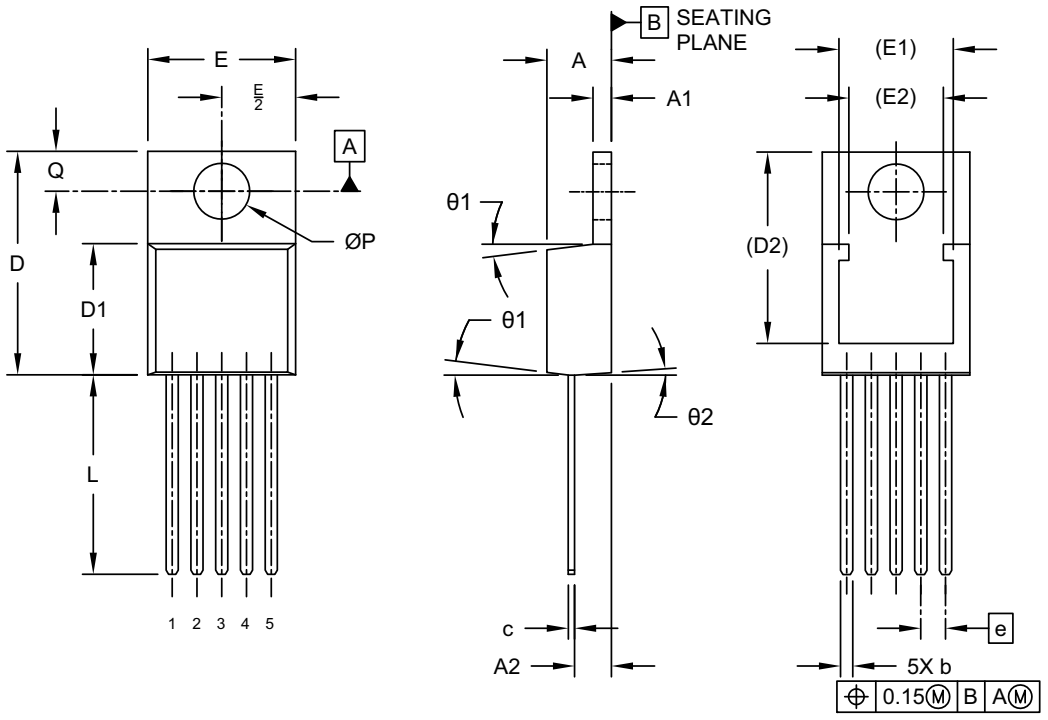


Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

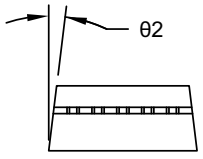
5-Lead TO-220 Package Outline and Recommended Land Pattern

5-Lead Transistor Outline Type LB03 (B8X) - [TO-220]
Micrel Legacy Package TO220-LB03-5LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW SIDE VIEW BOTTOM VIEW

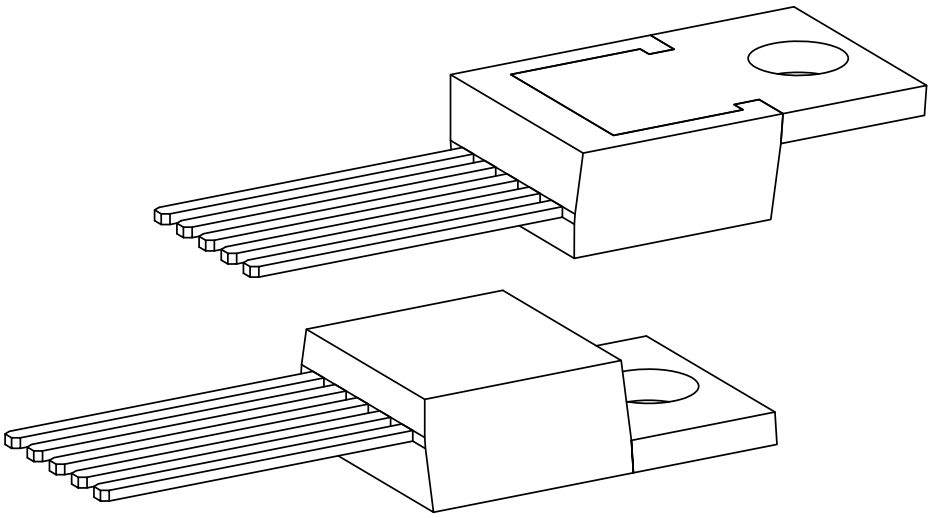


END VIEW

Microchip Technology Drawing C04-036 Rev C Sheet 1 of 2

5-Lead Transistor Outline Type LB03 (B8X) - [TO-220]
Micrel Legacy Package TO220-LB03-5LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		INCHES		
Dimension Limits		Min	Nom	Max
Number of Leads	N		5	
Pitch	e		.067 BSC	
Overall Height	A	.160	.175	.190
Tab Height	A1	.045	.050	.055
Seating Plane to Lead	A2	.080	.098	.115
Lead Width	b	.025	.033	.040
Lead Thickness	c	.012	.016	.020
Lead Length	L	.500	.540	.580
Total Body Length Including Tab	D	.542	.580	.619
Molded Body Length	D1	.348	.354	.360
Total Width	E	.380	.400	.420
Pad Width	E1		0.256 REF	
Pad Length	D2		0.486 REF	
Hole Diameter	ØP	.146	.151	.156
Hole Center to Tab Edge	Q	.103	.108	.113
Molded Body Draft Angle	θ2	3	7	10
Molded Body Draft Angle	θ2	1	4	7

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-036 Rev C Sheet 2 of 2

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2021)

- Converted Micrel document MIC4421A/22A to Microchip data sheet template DS20006511A.
- Minor grammatical text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	X	XX	-XX
Part No.	Junction Temp. Range	Package	Media Type

Device:	MIC4421A:	Inverting, 9A-Peak Low-Side MOSFET Driver
	MIC4422A:	Non-Inverting, 9A-Peak Low-Side MOSFET Driver
Junction Temperature Range:	X =	–55°C to +125°C, RoHS-Compliant
	Y =	–40°C to +85°C, RoHS-Compliant
	Z =	0°C to +70°C, RoHS-Compliant
Package:	N =	8-Lead PDIP
	M =	8-Lead SOIC
	T =	5-Lead TO-220
Media Type:	<blank>=	95/Tube (SOIC only)
	<blank>=	50/Tube (PDIP, TO-220 only)
	TR =	2,500/Reel (SOIC only)

Examples:

a) MIC4421A: Inverting, 9A-Peak Low-Side MOSFET Driver, –55°C to +125°C Temperature Range

MIC4421AXM-TR	8-Lead SOIC	2,500/Reel

b) MIC4421A: Inverting, 9A-Peak Low-Side MOSFET Driver, –40°C to +85°C Temperature Range

MIC4421AYN	8-Lead PDIP	50/Tube
MIC4421AYM	8-Lead SOIC	95/Tube
MIC4421AYM-TR	8-Lead SOIC	2,500/Reel

c) MIC4421A: Inverting, 9A-Peak Low-Side MOSFET Driver, 0°C to +70°C Temperature Range

MIC4421AZN	8-Lead PDIP	50/Tube
MIC4421AZM	8-Lead SOIC	95/Tube
MIC4421AZM-TR	8-Lead SOIC	2,500/Reel
MIC4421AZT	5-Lead TO-220	50/Tube

d) MIC4422A: Non-Inverting, 9A-Peak Low-Side MOSFET Driver, –40°C to +85°C Temperature Range

MIC4422AYN	8-Lead PDIP	50/Tube
MIC4422AYM	8-Lead SOIC	95/Tube
MIC4422AYM-TR	8-Lead SOIC	2,500/Reel

e) MIC4422A: Non-Inverting, 9A-Peak Low-Side MOSFET Driver, 0°C to +70°C Temperature Range

MIC4422AZN	8-Lead PDIP	50/Tube
MIC4422AYM	8-Lead SOIC	95/Tube
MIC4422AYM-TR	8-Lead SOIC	2,500/Reel
MIC4422AYT	5-Lead TO-220	50/Tube

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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