36-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)

Features

- Separate independent read and write data ports
  - Supports concurrent transactions
- 300 MHz to 375 MHz clock for high bandwidth
- 4-Word Burst for reducing address bus frequency
- Double Data Rate (DDR) interfaces on both read and write ports (data transferred at 750 MHz) at 375 MHz
- Read latency of 2.0 clock cycles
- Two input clocks (K and $\overline{K}$) for precise DDR timing
  - SRAM uses rising edges only
- Echo clocks (CQ and $\overline{CQ}$) simplify data capture in high-speed systems
- Single multiplexed address input bus latches address inputs for both read and write ports
- Separate Port Selects for depth expansion
- Data valid pin (QVLD) to indicate valid data on the output
- Synchronous internally self-timed writes
- Available in x8, x9, x18, and x36 configurations
- Full data coherency providing most current data
- Core V_{DD} = 1.8V ± 0.1V; IO V_{DDQ} = 1.4V to V_{DD}[1]
- HSTL inputs and Variable drive HSTL output buffers
- Available in 165-ball FBGA package (15 x 17 x 1.4 mm)
- Offered in both Pb-free and non Pb-free packages
- JTAG 1149.1 compatible test access port
- Delay Lock Loop (DLL) for accurate data placement

Configurations

With Read Cycle Latency of 2.0 cycles:

CY7C1241V18 – 4M x 8
CY7C1256V18 – 4M x 9
CY7C1243V18 – 2M x 18
CY7C1245V18 – 1M x 36

Functional Description

The CY7C1241V18, CY7C1256V18, CY7C1243V18, and CY7C1245V18 are 1.8V Synchronous Pipelined SRAMs, equipped with Quad Data Rate-II+ (QDR-II+) architecture. QDR-II+ architecture consists of two separate ports to access the memory array. The read port has dedicated data outputs to support read operations and the write port has dedicated data inputs to support write operations. QDR-II+ architecture has separate data inputs and data outputs to completely eliminate the need to “turn around” the data bus required with common IO devices. Each port can be accessed through a common address bus. Read and write addresses are latched on alternate rising edges of the input (K) clock. Accesses to the QDR-II+ read and write ports are completely independent of one another. To maximize data throughput, both read and write ports are equipped with Double Data Rate (DDR) interfaces. Each address location is associated with four 8-bit words (CY7C1241V18), 9-bit words (CY7C1256V18), 18-bit words (CY7C1243V18), or 36-bit words (CY7C1245V18), that burst sequentially into or out of the device. Because data can be transferred into and out of the device on every rising edge of both input clocks (K and $\overline{K}$), memory bandwidth is maximized while simplifying system design by eliminating bus “turn-arounds”.

Depth expansion is accomplished with Port Selects for each port. Port selects enable each port to operate independently.

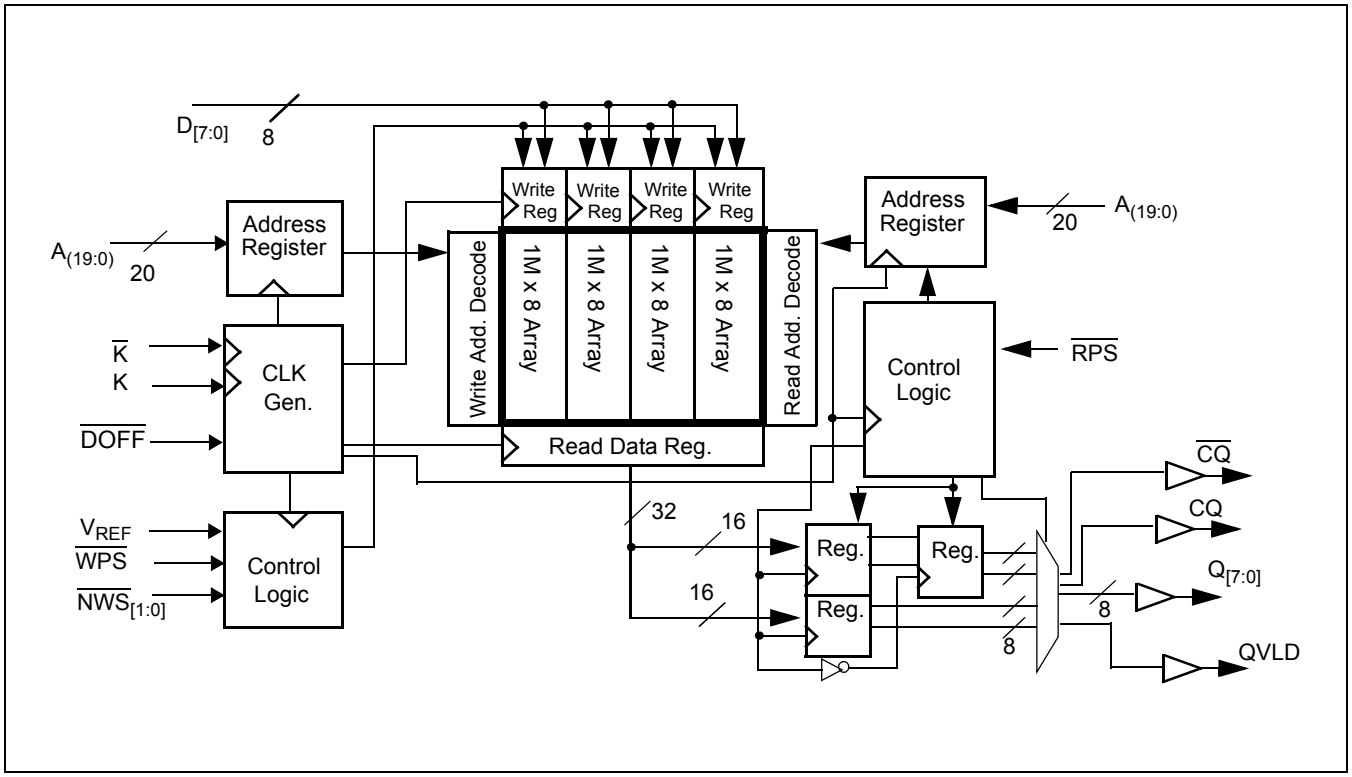
All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the K or $\overline{K}$ input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

Selection Guide

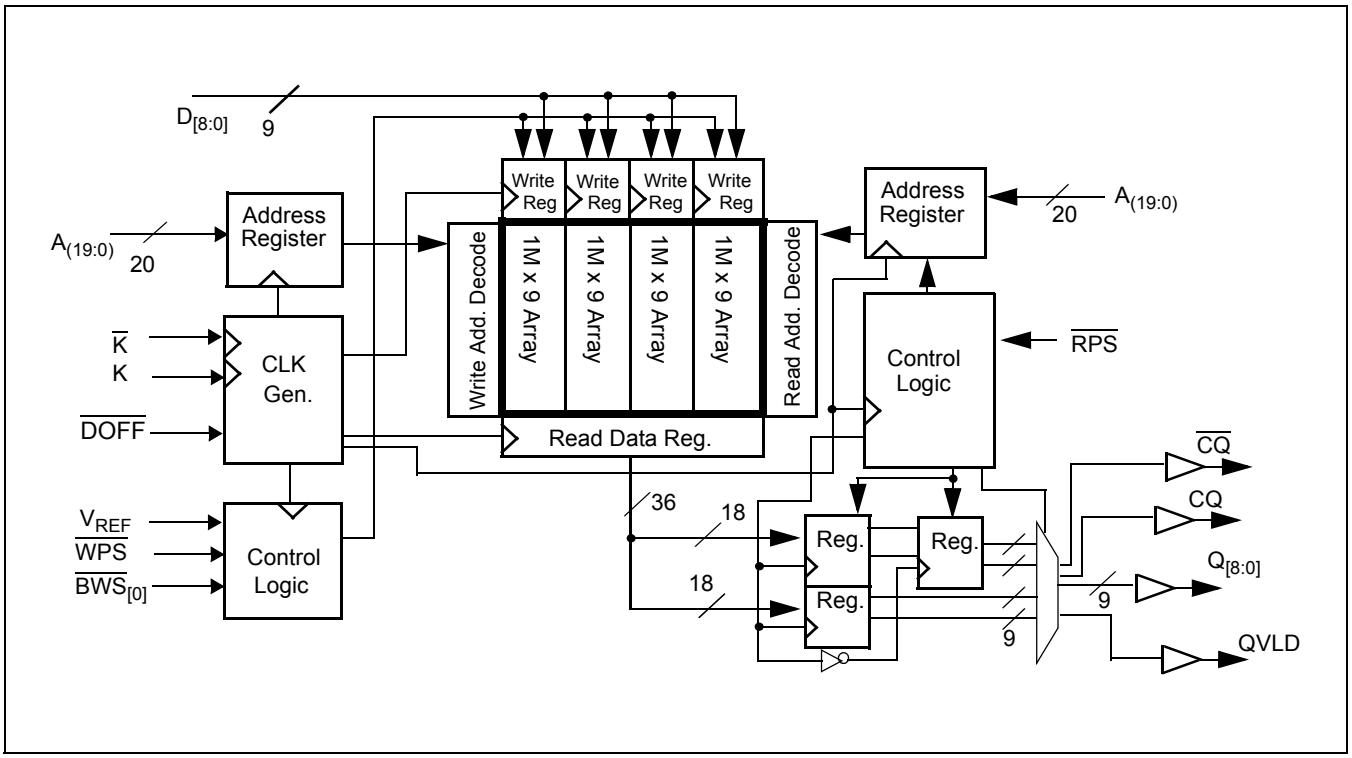
	375 MHz	333 MHz	300 MHz	Unit
Maximum Operating Frequency	375	333	300	MHz
Maximum Operating Current	1240	1120	1040	mA

Note
1. The QDR consortium specification for V_{DDQ} is 1.5V ± 0.1V. The Cypress QDR devices exceed the QDR consortium specification and are capable of supporting V_{DDQ} = 1.4V to V_{DD}.

Logic Block Diagram (CY7C1241V18)

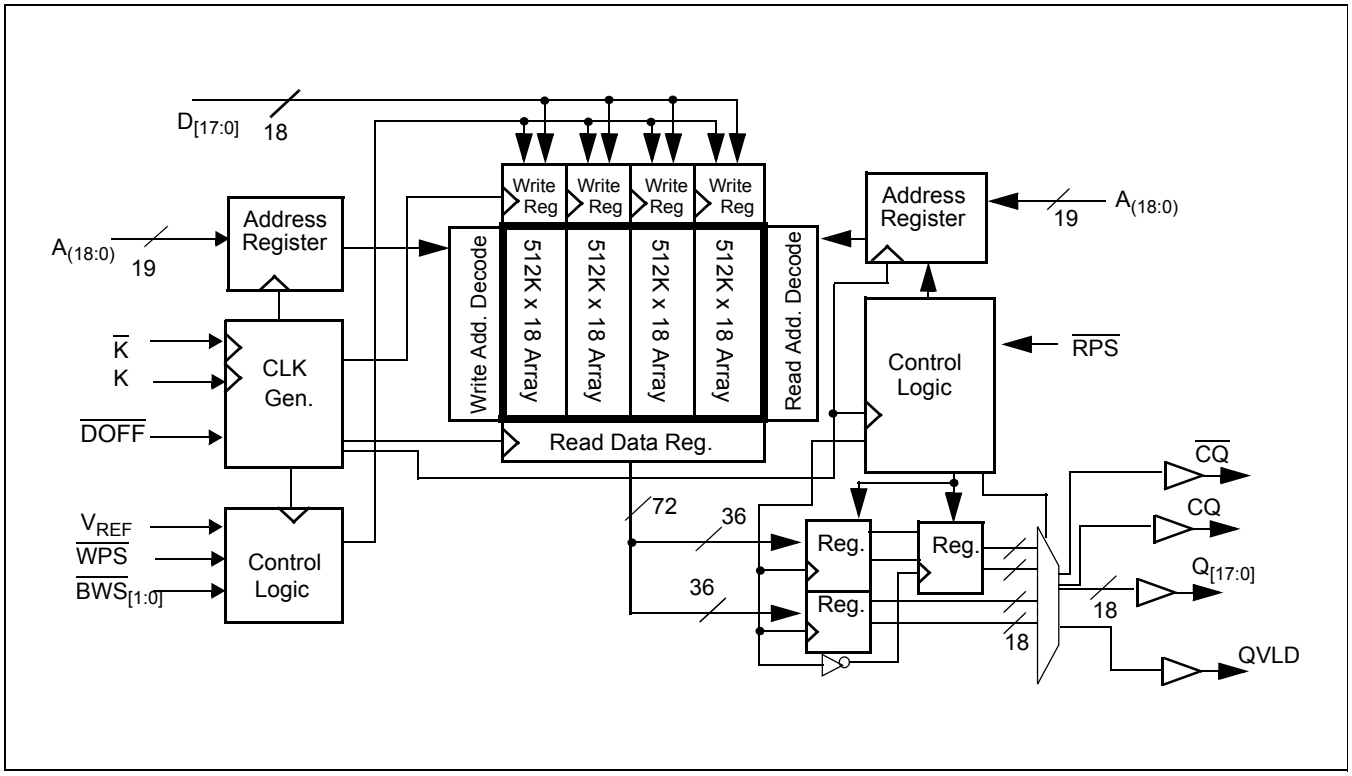


Logic Block Diagram (CY7C1256V18)

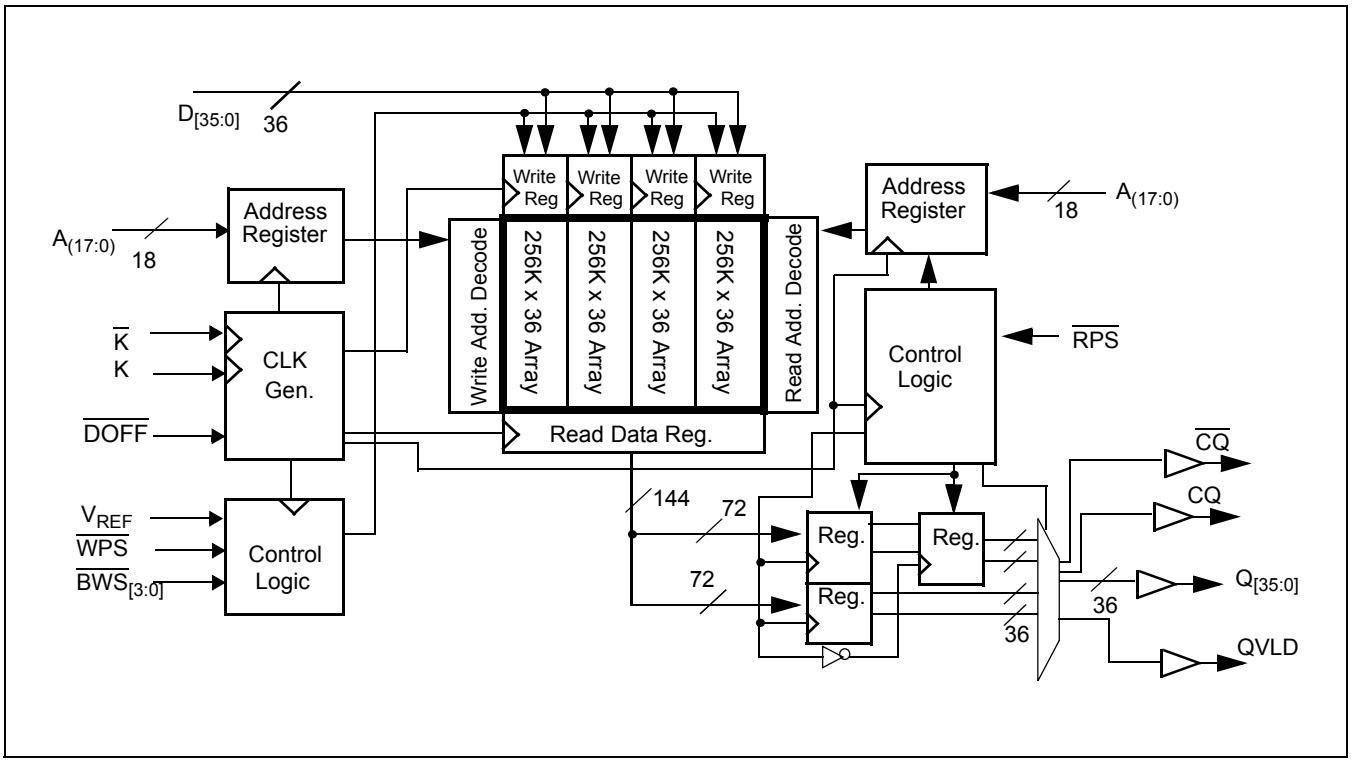


[+] Feedback

Logic Block Diagram (CY7C1243V18)



Logic Block Diagram (CY7C1245V18)



[+] Feedback

Pin Configurations

165-Ball FBGA (15 x 17 x 1.4 mm) Pinout

CY7C1241V18 (4M x 8)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	$\overline{WPS}$	$\overline{NWS_1}$	$\overline{K}$	NC/144M	$\overline{RPS}$	A	A	CQ
B	NC	NC	NC	A	NC/288M	K	$\overline{NWS_0}$	A	NC	NC	Q3
C	NC	NC	NC	V_{SS}	A	NC	A	V_{SS}	NC	NC	D3
D	NC	D4	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	Q4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D2	Q2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	D5	Q5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q1	D1
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	Q6	D6	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D0
N	NC	D7	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	Q7	A	A	QVLD	A	A	NC	NC	NC
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

CY7C1256V18 (4M x 9)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	$\overline{WPS}$	NC	$\overline{K}$	NC/144M	$\overline{RPS}$	A	A	CQ
B	NC	NC	NC	A	NC/288M	K	$\overline{BWS_0}$	A	**NC**	NC	Q4
C	NC	NC	NC	V_{SS}	A	NC	A	V_{SS}	NC	NC	D4
D	NC	D5	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	Q5	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D3	Q3
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	D6	Q6	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q2	D2
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	Q7	D7	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q1
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D1
N	NC	D8	NC	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	Q8	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

[+] Feedback

Pin Configurations (continued)

165-Ball FBGA (15 x 17 x 1.4 mm) Pinout

CY7C1243V18 (2M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	A	$\overline{WPS}$	$\overline{BWS_1}$	$\overline{K}$	NC/288M	$\overline{RPS}$	A	NC/72M	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	NC	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

CY7C1245V18 (1M x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/288M	NC/72M	$\overline{WPS}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{RPS}$	A	NC/144M	CQ
B	Q27	Q18	D18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	A	NC	A	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	A	A	A	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	A	A	QVLD	A	A	Q9	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

[+] Feedback

Pin Definitions

Pin Name	IO	Pin Description
$D_{[x:0]}$	Input-Synchronous	**Data Input Signals**. Sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations. CY7C1241V18 – $D_{[7:0]}$ CY7C1256V18 – $D_{[8:0]}$ CY7C1243V18 – $D_{[17:0]}$ CY7C1245V18 – $D_{[35:0]}$
$\overline{WPS}$	Input-Synchronous	**Write Port Select, Active LOW**. Sampled on the rising edge of the K clock. When asserted active, a Write operation is initiated. Deasserting deselects the write port. Deselecting the write port causes $D_{[x:0]}$ to be ignored.
$\overline{NWS_0}$, $\overline{NWS_1}$,	Input-Synchronous	**Nibble Write Select 0, 1, Active LOW (CY7C1241V18 Only)**. Sampled on the rising edge of the K and $\overline{K}$ clocks when write operations are active. Used to select which nibble is written into the device during the current portion of the write operations. $\overline{NWS_0}$ controls $D_{[3:0]}$ and $\overline{NWS_1}$ controls $D_{[7:4]}$. All the nibble Write Selects are sampled on the same edge as the data. The corresponding nibble of data is ignored by deselecting a nibble write select and is not written into the device.
$\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$	Input-Synchronous	**Byte Write Select 0, 1, 2, and 3, Active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Selects which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. CY7C1256V18 – $\overline{BWS_0}$ controls $D_{[8:0]}$ CY7C1243V18 – $\overline{BWS_0}$ controls $D_{[8:0]}$ and $\overline{BWS_1}$ controls $D_{[17:9]}$. CY7C1245V18 – $\overline{BWS_0}$ controls $D_{[8:0]}$, $\overline{BWS_1}$ controls $D_{[17:9]}$, $\overline{BWS_2}$ controls $D_{[26:18]}$, and $\overline{BWS_3}$ controls $D_{[35:27]}$. All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select causes the corresponding byte of data to be ignored and not written into the device.
A	Input-Synchronous	**Address Inputs**. Sampled on the rising edge of the K clock during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 4M x 8 (4 arrays each of 1M x 8) for CY7C1241V18, 4M x 9 (4 arrays each of 1M x 9) for CY7C1256V18, 2M x 18 (4 arrays each of 512K x 18) for CY7C1243V18 and 1M x 36 (4 arrays each of 256K x 36) for CY7C1245V18. Therefore, only 20 address inputs are needed to access the entire memory array of CY7C1241V18 and CY7C1256V18, 19 address inputs for CY7C1243V18, and 18 address inputs for CY7C1245V18. These inputs are ignored when the appropriate port is deselected.
$Q_{[x:0]}$	Outputs-Synchronous	**Data Output Signals**. These pins drive out the requested data during a read operation. Valid data is driven out on the rising edge of both the K and $\overline{K}$ clocks during read operations. When the read port is deselected, $Q_{[x:0]}$ are automatically tri-stated. CY7C1241V18 – $Q_{[7:0]}$ CY7C1256V18 – $Q_{[8:0]}$ CY7C1243V18 – $Q_{[17:0]}$ CY7C1245V18 – $Q_{[35:0]}$
$\overline{RPS}$	Input-Synchronous	**Read Port Select, Active LOW**. Sampled on the rising edge of Positive Input Clock (K). When active, a read operation is initiated. Deasserting causes the read port to be deselected. When deselected, the pending access is allowed to complete and the output drivers are automatically tri-stated following the next rising edge of the K clock. Each read access consists of a burst of four sequential transfers.
QVLD	Valid output indicator	**Valid Output Indicator**. The Q Valid indicates valid output data. QVLD is edge aligned with CQ and $\overline{CQ}$.
K	Input-Clock	**Positive Input Clock Input**. The rising edge of K captures synchronous inputs to the device and drives out data through $Q_{[x:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input-Clock	**Negative Input Clock Input**. $\overline{K}$ captures synchronous inputs being presented to the device and drives out data through $Q_{[x:0]}$ when in single clock mode.
CQ	Echo Clock	**Synchronous Echo Clock Outputs**. This is a free running clock and is synchronized to the input clock (K) of the QDR-II+. The timing for the echo clocks is shown in "Switching Characteristics" on page 23.

[+] Feedback

Pin Definitions (continued)

Pin Name	IO	Pin Description
$\overline{CQ}$	Echo Clock	**Synchronous Echo Clock Outputs**. This is a free running clock and is synchronized to the input clock ($\overline{K}$) of the QDR-II+. The timing for the echo clocks is shown in "Switching Characteristics" on page 23.
ZQ	Input	**Output Impedance Matching Input**. This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
$\overline{DOFF}$	Input	**DLL Turn Off, Active LOW**. Connecting this pin to ground turns off the DLL inside the device. The timing in the DLL turned off operation is different from that listed in this data sheet. For normal operation, this pin can be connected to a pull up through a 10 Kohm or less pull up resistor. The device behaves in QDR-I mode when the DLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with QDR-I timing.
TDO	Output	**TDO for JTAG**.
TCK	Input	**TCK pin for JTAG**.
TDI	Input	**TDI pin for JTAG**.
TMS	Input	**TMS pin for JTAG**.
NC	N/A	**Not connected to the die**. Can be tied to any voltage level.
NC/72M	N/A	**Not connected to the die**. Can be tied to any voltage level.
NC/144M	N/A	**Not connected to the die**. Can be tied to any voltage level.
NC/288M	N/A	**Not connected to the die**. Can be tied to any voltage level.
V_{REF}	Input-Reference	**Reference Voltage Input**. Static input used to set the reference level for HSTL inputs, outputs, and AC measurement points.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the device**.
V_{DDQ}	Power Supply	**Power supply inputs for the outputs of the device**.

[+] Feedback

Functional Overview

The CY7C1241V18, CY7C1256V18, CY7C1243V18, and CY7C1245V18 are synchronous pipelined Burst SRAMs equipped with a read and a write port. The read port is dedicated to read operations and the write port is dedicated to write operations. Data flows into the SRAM through the write port and out through the read port. These devices multiplex the address inputs to minimize the number of address pins required. By having separate read and write ports, the QDR-II+ completely eliminates the need to “turn around” the data bus and avoids any possible data contention, thereby simplifying system design. Each access consists of four 8-bit data transfers in the case of CY7C1241V18, four 9-bit data transfers in the case of CY7C1256V18, four 18-bit data transfers in the case of CY7C1243V18, and four 36-bit data transfers in the case of CY7C1245V18, in two clock cycles.

Accesses for both ports are initiated on the Positive Input Clock (K). All synchronous input and output timing refer to the rising edge of the input clocks (K/$\overline{K}$).

All synchronous data inputs ($D_{[x:0]}$) inputs pass through input registers controlled by the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) outputs pass through output registers controlled by the rising edge of the Input clocks (K and $\overline{K}$).

All synchronous control ($\overline{RPS}$, $\overline{WPS}$, $\overline{BWS}_{[x:0]}$) inputs pass through input registers controlled by the rising edge of the input clocks (K/$\overline{K}$).

CY7C1243V18 is described in the following sections. The same basic descriptions apply to CY7C1241V18, CY7C1256V18, and CY7C1245V18.

Read Operations

The CY7C1243V18 is organized internally as 4 arrays of 512K x 18. Accesses are completed in a burst of four sequential 18-bit data words. Read operations are initiated by asserting $\overline{RPS}$ active at the rising edge of the Positive Input Clock (K). The addresses presented to Address inputs are stored in the Read address register. Following the next two K clock rising edges, the corresponding lowest order 18-bit word of data is driven onto the $Q_{[17:0]}$ using K as the output timing reference. On the subsequent rising edge of K the next 18-bit data word is driven onto the $Q_{[17:0]}$. This process continues until all four 18-bit data words have been driven out onto $Q_{[17:0]}$. The requested data is valid 0.45 ns from the rising edge of the input clock (K or $\overline{K}$). To maintain the internal logic, each read access must be allowed to complete. Each read access consists of four 18-bit data words and takes two clock cycles to complete. Therefore, read accesses to the device cannot be initiated on two consecutive K clock rises. The internal logic of the device ignores the second read request. Read accesses can be initiated on every other K clock rise. Doing so pipelines the data flow such that data is transferred out of the device on every rising edge of the input clocks (K and $\overline{K}$).

When the read port is deselected, the CY7C1243V18 first completes the pending Read transactions. Synchronous internal circuitry automatically tri-states the outputs following the next rising edge of the Positive Input Clock (K). This enables a seamless transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting $\overline{WPS}$ active at the rising edge of the Positive Input Clock (K). On the following K clock rise, the data presented to $D_{[17:0]}$ is latched and stored into the lower 18-bit Write Data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the Negative Input Clock ($\overline{K}$), the information presented to $D_{[17:0]}$ is also stored into the Write Data register, provided $\overline{BWS}_{[1:0]}$ are both asserted active. This process continues for one more cycle until four 18-bit words (a total of 72 bits) of data are stored in the SRAM. The 72 bits of data are then written into the memory array at the specified location. Therefore, write accesses to the device cannot be initiated on two consecutive K clock rises. The internal logic of the device ignores the second write request. Write accesses can be initiated on every other rising edge of the Positive Input Clock (K). Doing so pipelines the data flow such that 18 bits of data can be transferred into the device on every rising edge of the input clocks (K and $\overline{K}$).

When deselected, the write port ignores all inputs after the pending write operations have been completed.

Byte Write Operations

Byte Write operations are supported by the CY7C1243V18. A Write operation is initiated as described in the Write Operations section. The bytes that are written are determined by $\overline{BWS}_0$ and $\overline{BWS}_1$, which are sampled with each set of 18-bit data words. Asserting the appropriate Byte Write Select input during the data portion of a write enables the data being presented to be latched and written into the device. Deasserting the Byte Write Select input during the data portion of a write allows the data stored in the device for that byte to remain unaltered. This feature can be used to simplify read/modify/write operations to a Byte Write operation.

Concurrent Transactions

The read and write ports on the CY7C1243V18 operate completely independently of one another. Since each port latches the address inputs on different clock edges, you can read or write to any location, regardless of the transaction on the other port. If the ports access the same location when a read follows a write in successive clock cycles, the SRAM delivers the most recent information associated with the specified address location. This includes forwarding data from a write cycle that was initiated on the previous K clock rise.

Read accesses and write access must be scheduled such that one transaction is initiated on any clock cycle. If both ports are selected on the same K clock rise, the arbitration depends on the previous state of the SRAM. If both ports were deselected, the read port takes priority. If a read was initiated on the previous cycle, the write port assumes priority (because read operations cannot be initiated on consecutive cycles). If a write was initiated on the previous cycle, the Read port assumes priority (because write operations cannot be initiated on consecutive cycles). Therefore, asserting both port selects active from a deselected state results in alternating read/write operations being initiated, with the first access being a read.

Depth Expansion

The CY7C1243V18 has a Port Select input for each port. This enables easy depth expansion. Both Port Selects are sampled

[+] Feedback

on the rising edge of the Positive Input Clock only (K). Each port select input can deselect the specified port. Deselecting a port does not affect the other port. All pending transactions (read and write) are completed before the device is deselected.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to enable the SRAM to adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of ±15% is between 175Ω and 350Ω, with V_{DDQ} = 1.5V. The output impedance is adjusted every 1024 cycles upon power up to account for drifts in supply voltage and temperature.

Echo Clocks

Echo clocks are provided on the QDR-II+ to simplify data capture on high speed systems. Two echo clocks are generated by the QDR-II+. CQ is referenced with respect to K and CQ is referenced with respect to K. These are free running clocks and are synchronized to the input clock of the QDR-II+. The timing for the echo clocks is shown in "Switching Characteristics" on page 23.

Valid Data Indicator (QVLD)

QVLD is provided on the QDR-II+ to simplify data capture on high speed systems. The QVLD is generated by the QDR-II+ device along with data output. This signal is also edge-aligned with the echo clock and follows the timing of any data pin. This signal is asserted half a cycle before valid data arrives.

Delay Lock Loop (DLL)

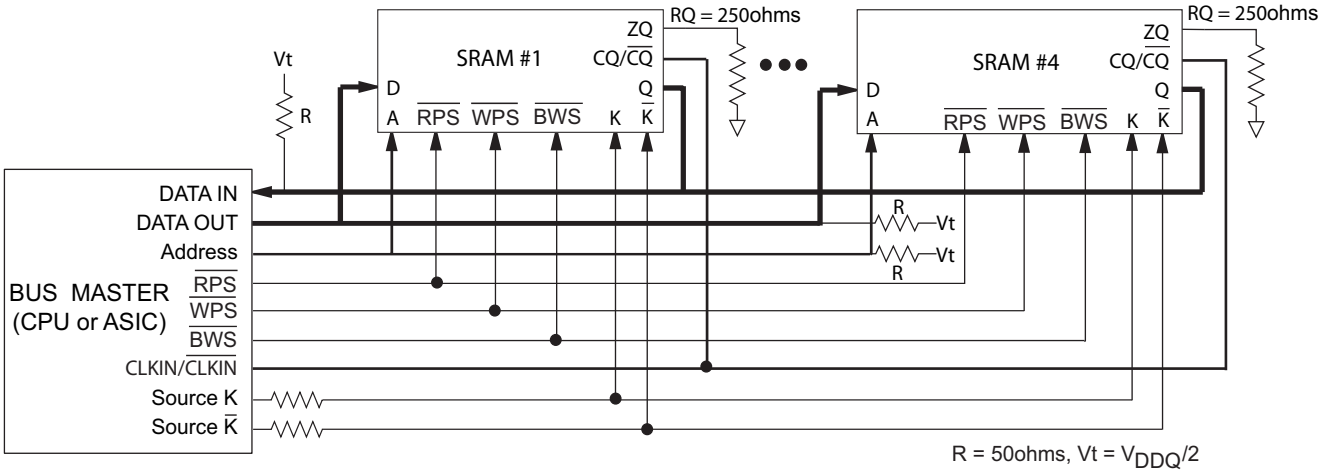
These chips use a DLL that is designed to function between 120 MHz and the specified maximum clock frequency. The DLL may be disabled by applying ground to the DOFF pin. When the DLL is turned off, the device behaves in QDR-I mode (with 1.0 cycle latency and a longer access time). For more information, refer to the application note, *DLL Considerations in QDRII/DDRII/QDRII+/DDRII+*. The DLL can also be reset by slowing or stopping the input clocks K and K for a minimum of 30 ns. However, it is not necessary for the DLL to be reset to lock to the desired frequency. During power up, when the DOFF is tied HIGH, the DLL is locked after 2048 cycles of stable clock.

[+] Feedback

Application Example

Figure 1 shows the use of 4 QDR-II+ SRAMs in an application.

Figure 1. Application Example



Truth Table

The truth table for the CY7C1241V18, CY7C1256V18, CY7C1243V18, and CY7C1245V18 follows.[2, 3, 4, 5, 6, 7]

Operation	K	$\overline{RPS}$	$\overline{WPS}$	DQ	DQ	DQ	DQ
Write Cycle: Load address on the rising edge of K; input write data on two consecutive K and $\overline{K}$ rising edges.	L-H	H[8]	L[9]	D(A) at K(t + 1) ↑	D(A + 1) at $\overline{K}$(t +1) ↑	D(A + 2) at K(t + 2) ↑	D(A + 3) at $\overline{K}$(t + 2) ↑
Read Cycle: (2.0 cycle Latency) Load address on the rising edge of K; wait two cycle; read data on two consecutive K and $\overline{K}$ rising edges.	L-H	L[9]	X	Q(A) at K(t + 2) ↑	Q(A + 1) at $\overline{K}$(t + 2) ↑	Q(A + 2) at K(t + 3) ↑	Q(A + 3) at $\overline{K}$(t + 3) ↑
NOP: No Operation	L-H	H	H	D = X Q = High-Z	D = X Q = High-Z	D = X Q = High-Z	D = X Q = High-Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State	Previous State	Previous State

Notes

2. X = "Don't Care," H = Logic HIGH, L = Logic LOW, ↑ represents rising edge.
3. Device will power-up deselected and the outputs in a tri-state condition.
4. "A" represents address location latched by the devices when transaction was initiated. A + 1, A + 2, and A + 3 represents the address sequence in the burst.
5. "t" represents the cycle at which a Read/write operation is started. t + 1, t + 2, and t + 3 are the first, second and third clock cycles respectively succeeding the "t" clock cycle.
6. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on K and $\overline{K}$ rising edges.
7. It is recommended that K = $\overline{K}$ = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
8. If this signal was LOW to initiate the previous cycle, this signal becomes a "Don't Care" for this operation.
9. This signal was HIGH on previous K clock rise. Initiating consecutive Read or Write operations on consecutive K clock rises is not permitted. The device will ignore the second Read or Write request.

[+] Feedback

Write Cycle Descriptions

The write cycle description table for CY7C1241V18 and CY7C1243V18 follows.[2, 10]

$\overline{BWS_0}$/ $\overline{NWS_0}$	$\overline{BWS_1}$/ $\overline{NWS_1}$	K	$\overline{K}$	Comments
L	L	L–H	–	During the data portion of a write sequence : CY7C1241V18 – both nibbles ($D_{[7:0]}$) are written into the device, CY7C1243V18 – both bytes ($D_{[17:0]}$) are written into the device.
L	L	–	L-H	During the data portion of a write sequence : CY7C1241V18 – both nibbles ($D_{[7:0]}$) are written into the device, CY7C1243V18 – both bytes ($D_{[17:0]}$) are written into the device.
L	H	L–H	–	During the data portion of a write sequence : CY7C1241V18 – only the lower nibble ($D_{[3:0]}$) is written into the device, $D_{[7:4]}$ remains unaltered. CY7C1243V18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
L	H	–	L–H	During the data portion of a write sequence : CY7C1241V18 – only the lower nibble ($D_{[3:0]}$) is written into the device, $D_{[7:4]}$ remains unaltered. CY7C1243V18 – only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9]}$ remains unaltered.
H	L	L–H	–	During the data portion of a write sequence : CY7C1241V18 – only the upper nibble ($D_{[7:4]}$) is written into the device, $D_{[3:0]}$ remains unaltered. CY7C1243V18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	L	–	L–H	During the data portion of a write sequence : CY7C1241V18 – only the upper nibble ($D_{[7:4]}$) is written into the device, $D_{[3:0]}$ remains unaltered. CY7C1243V18 – only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0]}$ remains unaltered.
H	H	L–H	–	No data is written into the devices during this portion of a write operation.
H	H	–	L–H	No data is written into the devices during this portion of a write operation.

Write Cycle Descriptions

The write cycle description table for CY7C1256V18 follows.[2, 10]

$\overline{BWS_0}$	K	$\overline{K}$	Comments
L	L–H	–	During the data portion of a write sequence, the single byte ($D_{[8:0]}$) is written into the device.
L	–	L–H	During the data portion of a write sequence, the single byte ($D_{[8:0]}$) is written into the device.
H	L–H	–	No data is written into the device during this portion of a write operation.
H	–	L–H	No data is written into the device during this portion of a write operation.

Note
10. Assumes a write cycle was initiated per the Write Cycle Description Table. $\overline{NWS_0}$, $\overline{NWS_1}$, $\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, and $\overline{BWS_3}$ can be altered in different portions of a write cycle, as long as the setup and hold requirements are met.

Write Cycle Descriptions

The write cycle description table for CY7C1245V18 follows.[2, 10]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L–H	–	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	–	L–H	During the data portion of a write sequence, all four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L–H	–	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	–	L–H	During the data portion of a write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remain unaltered.
H	L	H	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remain unaltered.
H	H	L	H	L–H	–	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remain unaltered.
H	H	L	H	–	L–H	During the data portion of a write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remain unaltered.
H	H	H	L	L–H	–	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	–	L–H	During the data portion of a write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L–H	–	No data is written into the device during this portion of a write operation.
H	H	H	H	–	L–H	No data is written into the device during this portion of a write operation.

IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan test access port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1-2001. The TAP operates using JEDEC standard 1.8V IO logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, tie TCK LOW (V_{SS}) to prevent device clocking. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. Upon power up, the device comes up in a reset state which does not interfere with the operation of the device.

Test Access Port – Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the "TAP Controller State Diagram" on page 15. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. Whether the output is active depends upon the current state of the TAP state machine (see "Instruction Codes" on page 18). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and enable data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in "TAP Controller Block Diagram" on page 16. Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture IR state, the two least significant bits are loaded with a binary '01' pattern to enable fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the input and output ring.

"Boundary Scan Order" on page 19 shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in "Identification Register Definitions" on page 18.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in "Instruction Codes" on page 18. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

[+] Feedback

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power up or whenever the TAP controller is in a Test-Logic-Reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High-Z state until the next command is issued during the Update-IR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

Be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, although the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output may undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD enables an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required — that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the Shift-DR controller state.

EXTEST OUTPUT BUS TRI-STATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

The boundary scan register has a special bit located at bit #108. When this scan cell, called the “extest output bus tri-state,” is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High-Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

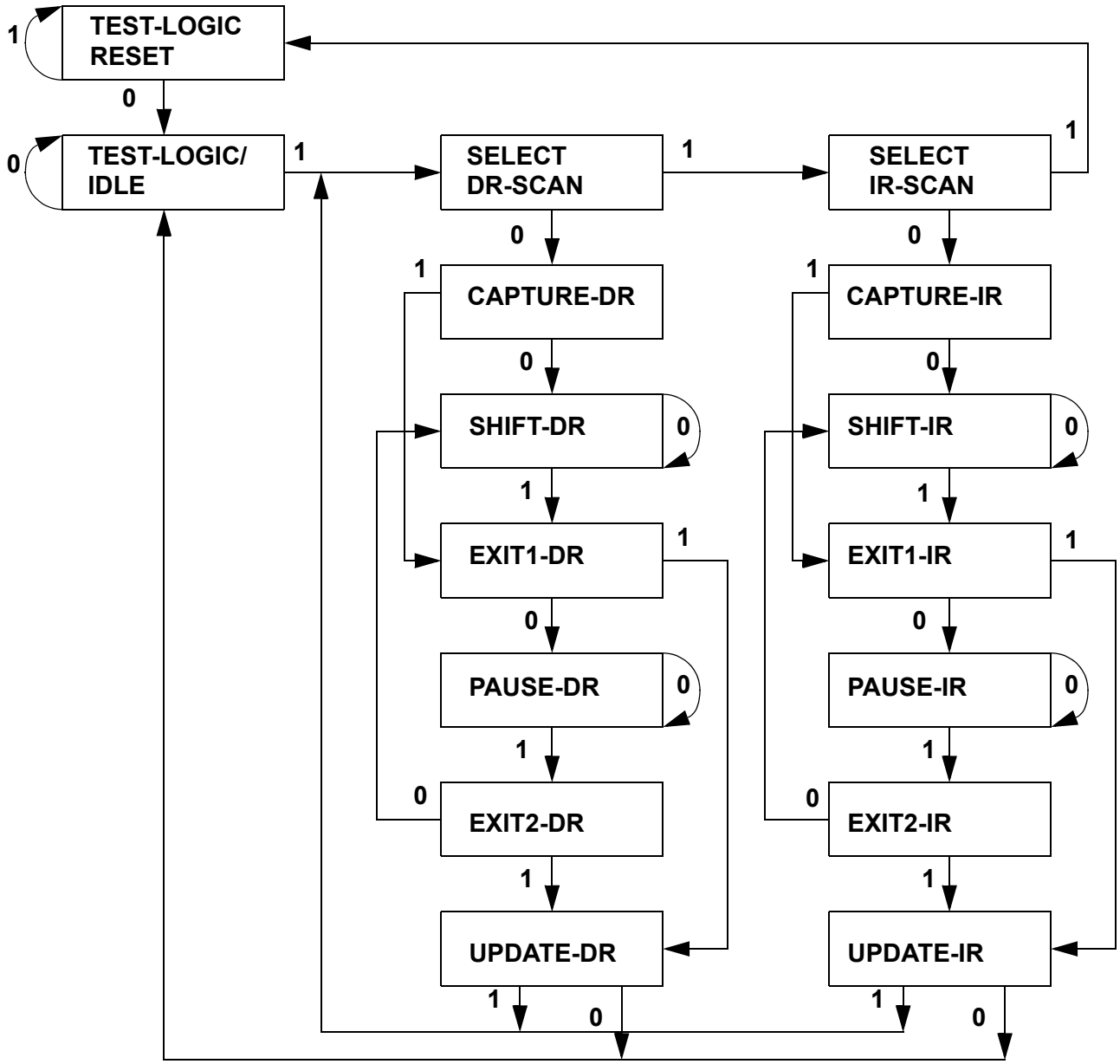
Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

[+] Feedback

TAP Controller State Diagram

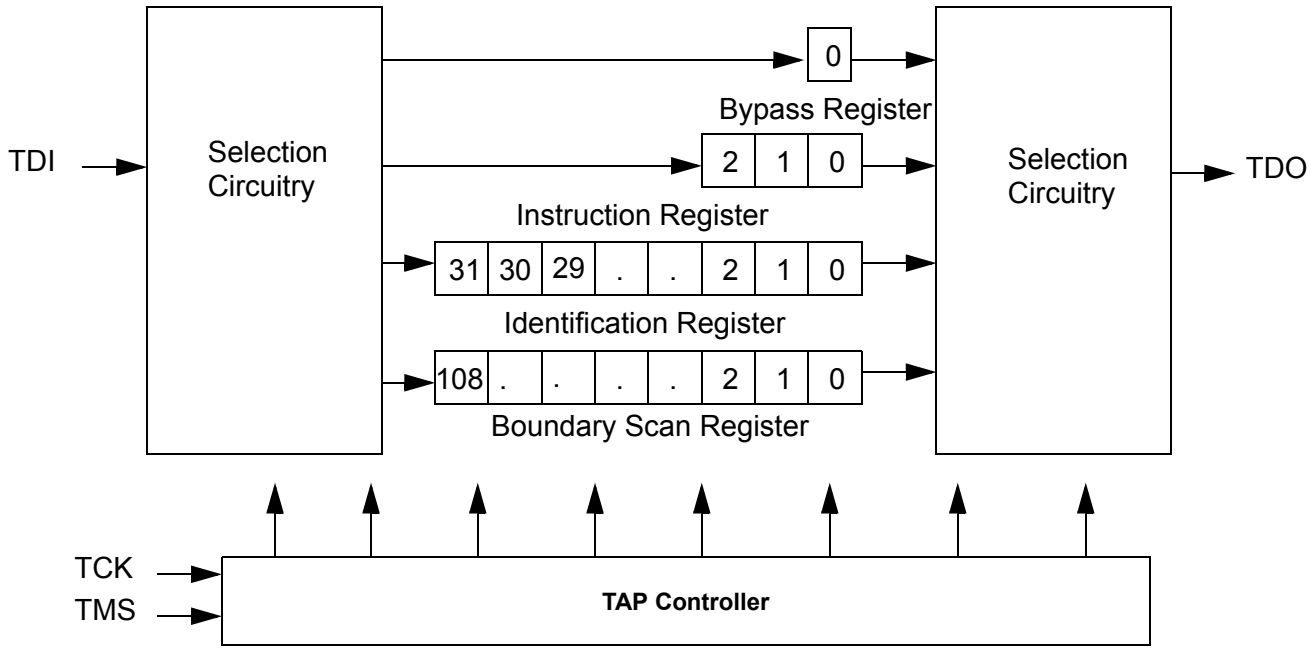
The state diagram for the CY7C1241V18, CY7C1256V18, CY7C1243V18, and CY7C1245V18 follows.[11]



Note
11. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

[+] Feedback

TAP Controller Block Diagram



TAP Electrical Characteristics

Over the Operating Range[12, 13, 14]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –2.0 mA	1.4		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	1.6		V
V_{OL1}	Output LOW Voltage	I_{OL} = 2.0 mA		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage		0.65V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.35V_{DD}	V
I_X	Input and Output Load Current	GND ≤ V_I ≤ V_{DD}	–5	5	µA

Notes
12. These characteristics apply to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in "Electrical Characteristics" on page 21.
13. Overshoot: $V_{IH}(AC) \leq V_{DDQ} + 0.3V$ (pulse width less than $t_{CYC}/2$). Undershoot: $V_{IL}(AC) \geq -0.3V$ (pulse width less than $t_{CYC}/2$).
14. All voltage refers to Ground.

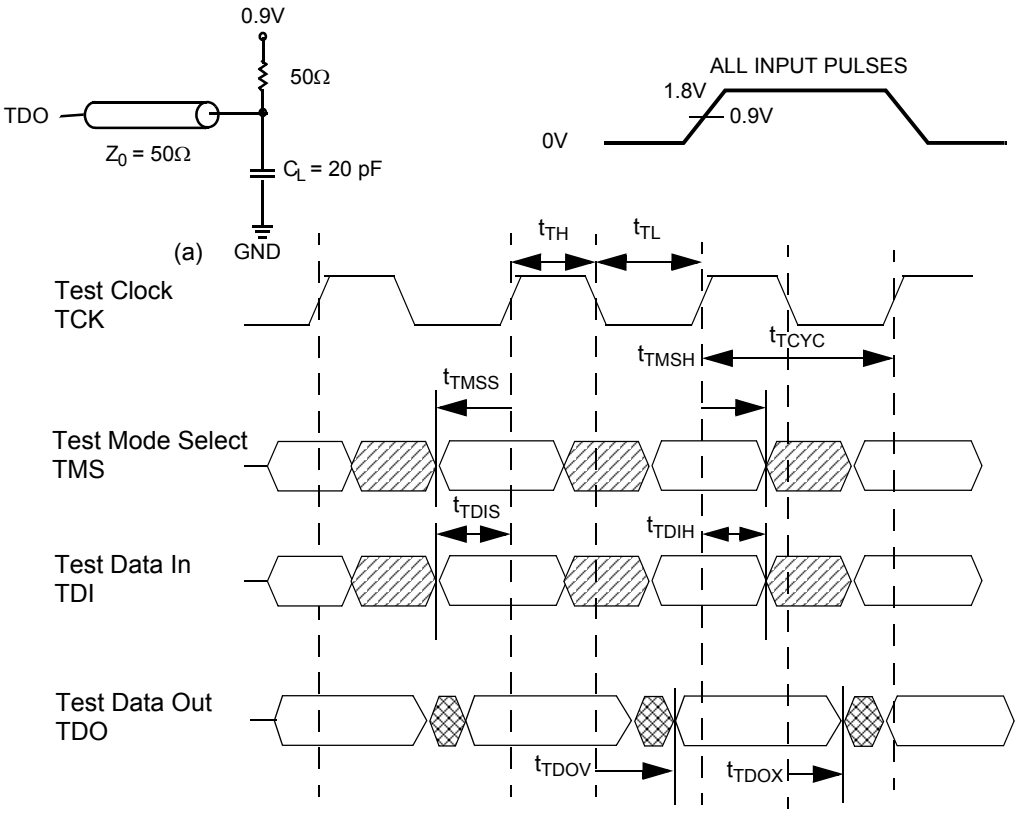
[+] Feedback

TAP AC Switching Characteristics

Over the Operating Range [15, 16]

Parameter	Description	Min	Max	Unit
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH	20		ns
t_{TL}	TCK Clock LOW	20		ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5		ns
t_{CS}	Capture Setup to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

TAP Timing and Test Conditions[16]



Notes

15. t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
16. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

[+] Feedback

Identification Register Definitions

Instruction Field	Value				Description
	CY7C1241V18	CY7C1256V18	CY7C1243V18	CY7C1245V18	
Revision Number (31:29)	000	000	000	000	Version number.
Cypress Device ID (28:12)	11010010101000111	11010010101001111	11010010101010111	11010010101100111	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	00000110100	00000110100	Enables unique identification of SRAM vendor.
ID Register Presence (0)	1	1	1	1	Indicates the presence of an ID register.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	109

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input/output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input/output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input/output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

[+] Feedback

Boundary Scan Order

Bit #	Bump ID
0	6R
1	6P
2	6N
3	7P
4	7N
5	7R
6	8R
7	8P
8	9R
9	11P
10	10P
11	10N
12	9P
13	10M
14	11N
15	9M
16	9N
17	11L
18	11M
19	9L
20	10L
21	11K
22	10K
23	9J
24	9K
25	10J
26	11J
27	11H

Bit #	Bump ID
28	10G
29	9G
30	11F
31	11G
32	9F
33	10F
34	11E
35	10E
36	10D
37	9E
38	10C
39	11D
40	9C
41	9D
42	11B
43	11C
44	9B
45	10B
46	11A
47	10A
48	9A
49	8B
50	7C
51	6C
52	8A
53	7A
54	7B
55	6B

Bit #	Bump ID
56	6A
57	5B
58	5A
59	4A
60	5C
61	4B
62	3A
63	2A
64	1A
65	2B
66	3B
67	1C
68	1B
69	3D
70	3C
71	1D
72	2C
73	3E
74	2D
75	2E
76	1E
77	2F
78	3F
79	1G
80	1F
81	3G
82	2G
83	1H

Bit #	Bump ID
84	1J
85	2J
86	3K
87	3J
88	2K
89	1K
90	2L
91	3L
92	1M
93	1L
94	3N
95	3M
96	1N
97	2M
98	3P
99	2N
100	2P
101	1P
102	3R
103	4R
104	4P
105	5P
106	5N
107	5R
108	Internal

Power Up Sequence in QDR-II+ SRAM

QDR-II+ SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations. During power up, when the DOFF is tied HIGH, the DLL is locked after 2048 cycles of stable clock.

Power Up Sequence

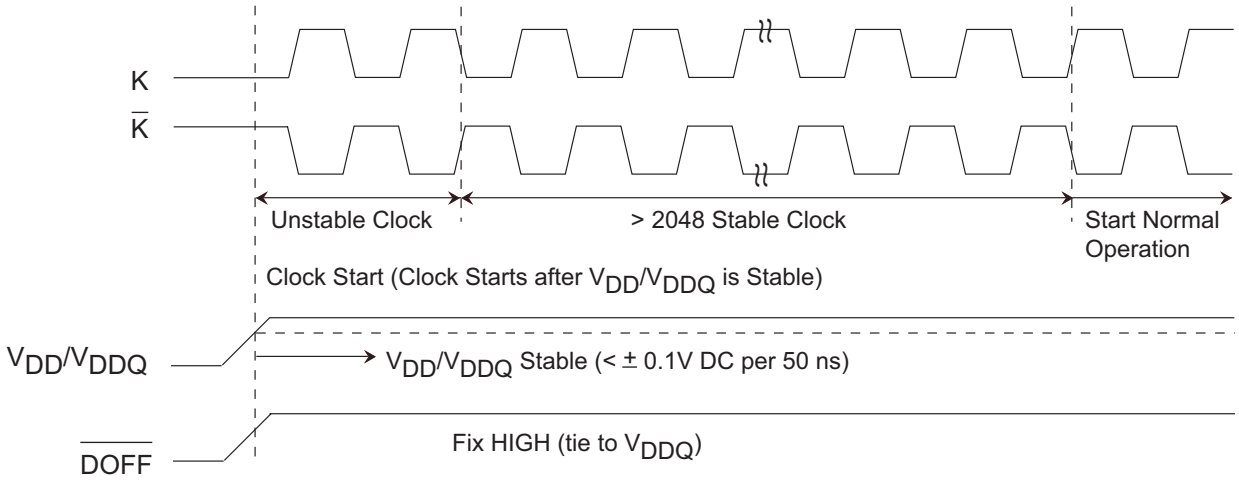
- Apply power with $\overline{DOFF}$ tied HIGH (All other inputs can be HIGH or LOW)
  - Apply V_{DD} before V_{DDQ}
  - Apply V_{DDQ} before V_{REF} or at the same time as V_{REF}
  - Provide stable power and clock (K, $\overline{K}$) for 2048 cycles to lock the DLL.

DLL Constraints

- DLL uses K clock as its synchronizing input. The input must have low phase jitter, which is specified as $t_{KC\ Var}$.
- The DLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the DLL is enabled, then the DLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 2048 cycles stable clock to relock to the clock frequency you want.

Power Up Waveforms

Figure 2. Power Up Waveforms



[+] Feedback

Maximum Ratings

Exceeding maximum ratings may shorten the battery life of the device. User guidelines are not tested.

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied ..–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND..... –0.5V to +2.9V

Supply Voltage on V_{DDQ} Relative to GND .....–0.5V to + V_{DD}

DC Applied to Outputs in High-Z .....–0.5V to V_{DDQ} + 0.3V

DC Input Voltage[13] .....–0.5V to V_{DD} + 0.3V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage (MIL-STD-883, M. 3015)... >2001V

Latch Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}[17]	V_{DDQ}[17]
Com'l	0°C to +70°C	1.8 ± 0.1V	1.4V to V_{DD}
Ind'l	–40°C to +85°C		

Electrical Characteristics

Over the Operating Range [14]

DC Electrical Characteristics

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage			1.7	1.8	1.9	V
V_{DDQ}	I/O Supply Voltage			1.4	1.5	V_{DD}	V
V_{OH}	Output HIGH Voltage	Note 18		$V_{DDQ}/2 – 0.12$		$V_{DDQ}/2 + 0.12$	V
V_{OL}	Output LOW Voltage	Note 19		$V_{DDQ}/2 – 0.12$		$V_{DDQ}/2 + 0.12$	V
$V_{OH(LOW)}$	Output HIGH Voltage	I_{OH} = –0.1 mA, Nominal Impedance		$V_{DDQ} – 0.2$		V_{DDQ}	V
$V_{OL(LOW)}$	Output LOW Voltage	I_{OL} = 0.1 mA, Nominal Impedance		V_{SS}		0.2	V
V_{IH}	Input HIGH Voltage			$V_{REF} + 0.1$		$V_{DDQ} + 0.15$	V
V_{IL}	Input LOW Voltage			–0.15		$V_{REF} – 0.1$	V
I_X	Input Leakage Current	$GND \le V_I \le V_{DDQ}$		–2		2	µA
I_{OZ}	Output Leakage Current	$GND \le V_I \le V_{DDQ}$, Output Disabled		–2		2	µA
V_{REF}	Input Reference Voltage[20]	Typical Value = 0.75V		0.68	0.75	0.95	V
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0mA, $f = f_{MAX} = 1/t_{CYC}$	300 MHz			1040	mA
			333 MHz			1120	mA
			375 MHz			1240	mA
I_{SB1}	Automatic Power down Current	Max. V_{DD}, Both Ports Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, $f = f_{MAX} = 1/t_{CYC}$, Inputs Static	300 MHz			280	mA
			333 MHz			300	mA
			375 MHz			310	mA

AC Electrical Characteristics

Over the Operating Range [13]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage		$V_{REF} + 0.2$	–	$V_{DDQ} + 0.24$	V
V_{IL}	Input LOW Voltage		–0.24	–	$V_{REF} – 0.2$	V

Notes

17. Power-up: Assumes a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
18. Outputs are impedance controlled. $I_{OH} = –(V_{DDQ}/2)/(RQ/5)$ for values of 175Ω <= RQ <= 350Ωs.
19. Outputs are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175Ω <= RQ <= 350Ωs.
20. V_{REF} (min) = 0.68V or 0.46V_{DDQ}, whichever is larger; V_{REF} (max) = 0.95V or 0.54V_{DDQ}, whichever is smaller.

[+] Feedback

Capacitance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 1.8V V_{DDQ} = 1.5V	5	pF
C_{CLK}	Clock Input Capacitance		4	pF
C_O	Output Capacitance		5	pF

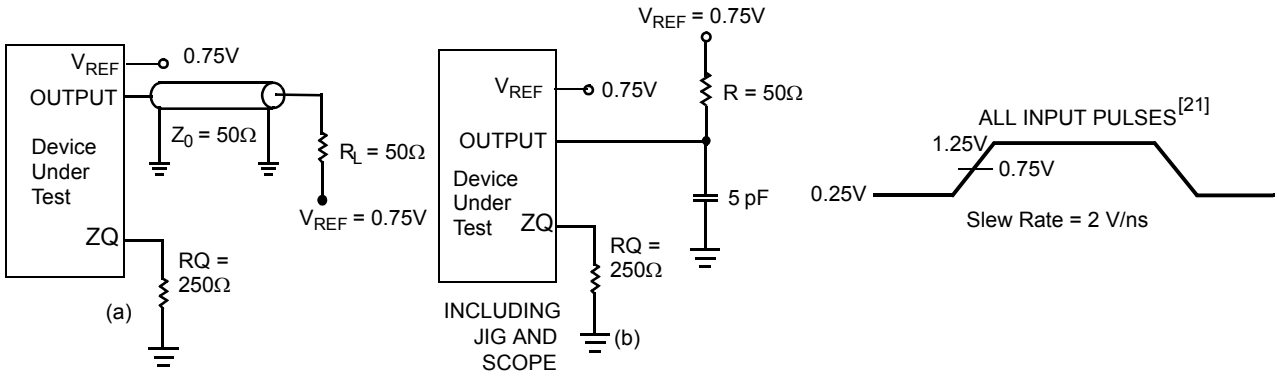
Thermal Resistance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	165 FBGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	16.25	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		2.91	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Note

21. Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75V, V_{REF} = 0.75V, RQ = 250Ω, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of AC Test Loads and Waveforms.

[+] Feedback

Switching Characteristics

Over the Operating Range[21, 22]

Cypress Parameter	Consortium Parameter	Description	375 MHz		333 MHz		300 MHz		Unit
			Min	Max	Min	Max	Min	Max	
t_{POWER}		V_{DD}(Typical) to the First Access[23]	1	–	1	–	1	–	ms
t_{CYC}	t_{KHKH}	K Clock Cycle Time	2.66	8.4	3.0	8.4	3.3	8.4	ns
t_{KH}	t_{KHKL}	Input Clock (K/$\overline{K}$) HIGH	0.4	–	0.4	–	0.4	–	t_{CYC}
t_{KL}	t_{KLKH}	Input Clock (K/$\overline{K}$) LOW	0.4	–	0.4	–	0.4	–	t_{CYC}
$t_{KH\overline{K}H}$	$t_{KH\overline{K}H}$	K Clock Rise to $\overline{K}$ Clock Rise (rising edge to rising edge)	1.13	–	1.28	–	1.40	–	ns
Set-up Times									
t_{SA}	t_{AVKH}	Address Set-up to K Clock Rise	0.4	–	0.4	–	0.4	–	ns
t_{SC}	t_{IVKH}	Control Set-up to K Clock Rise ($\overline{RPS}$, $\overline{WPS}$)	0.4	–	0.4	–	0.4	–	ns
t_{SCDDR}	t_{IVKH}	Double Data Rate Control Set-up to Clock (K, $\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.28	–	0.28	–	0.28	–	ns
t_{SD}	t_{DVKH}	$D_{[X:0]}$ Set-up to Clock (K/$\overline{K}$) Rise	0.28	–	0.28	–	0.28	–	ns
Hold Times									
t_{HA}	t_{KHAX}	Address Hold after K Clock Rise	0.4	–	0.4	–	0.4	–	ns
t_{HC}	t_{KHIX}	Control Hold after K Clock Rise ($\overline{RPS}$, $\overline{WPS}$)	0.4	–	0.4	–	0.4	–	ns
t_{HCDDR}	t_{KHIX}	Double Data Rate Control Hold after Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$, $\overline{BWS_3}$)	0.28	–	0.28	–	0.28	–	ns
t_{HD}	t_{KHDX}	$D_{[X:0]}$ Hold after Clock (K/$\overline{K}$) Rise	0.28	–	0.28	–	0.28	–	ns
Output Times									
t_{CO}	t_{CHQV}	K/$\overline{K}$ Clock Rise to Data Valid	–	0.45	–	0.45	–	0.45	ns
t_{DOH}	t_{CHQX}	Data Output Hold after Output K/$\overline{K}$ Clock Rise (Active to Active)	–0.45	–	–0.45	–	–0.45	–	ns
t_{CCQO}	t_{CHCQV}	K/$\overline{K}$ Clock Rise to Echo Clock Valid	–	0.45	–	0.45	–	0.45	ns
t_{CQOH}	t_{CHCQX}	Echo Clock Hold after K/$\overline{K}$ Clock Rise	–0.45	–	–0.45	–	–0.45	–	ns
t_{CQD}	t_{CQHQV}	Echo Clock High to Data Valid		0.2		0.2		0.2	ns
t_{CQDOH}	t_{CQHQX}	Echo Clock High to Data Invalid	–0.2	–	–0.2	–	–0.2	–	ns
t_{CQH}	t_{CQHCQL}	Output Clock (CQ/$\overline{CQ}$) HIGH[24]	0.88	–	1.03	–	1.15	–	ns
$t_{CQH\overline{CQ}H}$	$t_{CQH\overline{CQ}H}$	CQ Clock Rise to $\overline{CQ}$ Clock Rise[24] (rising edge to rising edge)	0.88	–	1.03	–	1.15	–	ns
t_{CHZ}	t_{CHQZ}	Clock (K/$\overline{K}$) Rise to High-Z (Active to High-Z)[25, 26]	–	0.45	–	0.45	–	0.45	ns
t_{CLZ}	t_{CHQX1}	Clock (K/$\overline{K}$) Rise to Low-Z[25, 26]	–0.45	–	–0.45	–	–0.45	–	ns
t_{QVLD}	$t_{CQHQVLD}$	Echo Clock High to QVLD Valid[27]	–0.20	0.20	–0.20	0.20	–0.20	0.20	ns
DLL Timing									
$t_{KC\ Var}$	$t_{KC\ Var}$	Clock Phase Jitter	–	0.20	–	0.20	–	0.20	ns
$t_{KC\ lock}$	$t_{KC\ lock}$	DLL Lock Time (K)	2048	–	2048	–	2048	–	Cycles
$t_{KC\ Reset}$	$t_{KC\ Reset}$	K Static to DLL Reset[28]	30	–	30	–	30	–	ns

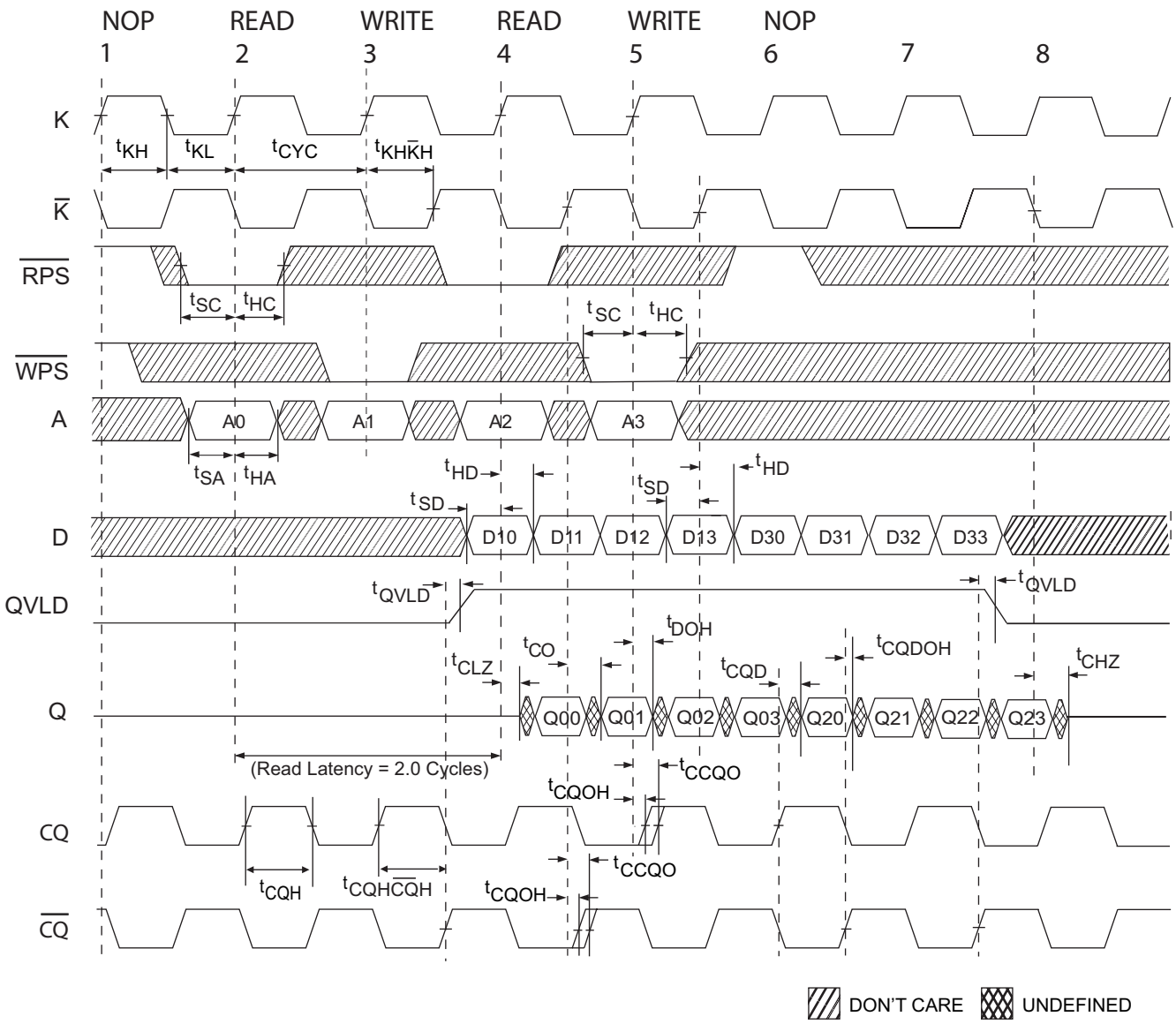
Notes

22. When a part with a maximum frequency above 300 MHz is operating at a lower clock frequency, it requires the input timings of the frequency range in which it is being operated and will output data with the output timing of that frequency range.
23. This part has an internal voltage regulator; t_{POWER} is the time that the power needs to be supplied above V_{DD} minimum initially before a read or write operation can be initiated.
24. These parameters are extrapolated from the input timing parameters ($t_{KH\overline{K}H}$ – 250 ps, where 250 ps is the internal jitter. An input jitter of 200 ps ($t_{KC\ Var}$) is already included in the $t_{KH\overline{K}H}$). These parameters are only guaranteed by design and are not tested in production.
25. t_{CHZ}, t_{CLZ} are specified with a load capacitance of 5 pF as in part (b) of "AC Test Loads and Waveforms" on page 22. Transition is measured ±100 mV from steady-state voltage.
26. At any voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} less than t_{CO}.
27. t_{QVLD} spec is applicable for both rising and falling edges of QVLD signal.
28. Hold to $>V_{IH}$ or $<V_{IL}$.

[+] Feedback

Switching Waveforms

Figure 4. Read/Write/Deselect Sequence waveform for 2.0 Cycle Read Latency[29, 30, 31]



Notes
29. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0+1.
30. Outputs are disabled (High-Z) one clock cycle after a NOP.
31. In this example, if address A2 = A1, then data Q20 = D10 and Q21 = D11. Write data is forwarded immediately as read results. This note applies to the whole diagram.

[+] Feedback

Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
375	CY7C1241V18-375BZC	51-85195	165-ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Commercial
	CY7C1256V18-375BZC			
	CY7C1243V18-375BZC			
	CY7C1245V18-375BZC			
	CY7C1241V18-375BZXC	51-85195	165-ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1256V18-375BZXC			
	CY7C1243V18-375BZXC			
	CY7C1245V18-375BZXC			
	CY7C1241V18-375BZI	51-85195	165-ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Industrial
	CY7C1256V18-375BZI			
	CY7C1243V18-375BZI			
	CY7C1245V18-375BZI			
	CY7C1241V18-375BZXI	51-85195	165-ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1256V18-375BZXI			
	CY7C1243V18-375BZXI			
	CY7C1245V18-375BZXI			
333	CY7C1241V18-333BZC	51-85195	165-ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Commercial
	CY7C1256V18-333BZC			
	CY7C1243V18-333BZC			
	CY7C1245V18-333BZC			
	CY7C1241V18-333BZXC	51-85195	165-ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1256V18-333BZXC			
	CY7C1243V18-333BZXC			
	CY7C1245V18-333BZXC			
	CY7C1241V18-333BZI	51-85195	165-ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Industrial
	CY7C1256V18-333BZI			
	CY7C1243V18-333BZI			
	CY7C1245V18-333BZI			
	CY7C1241V18-333BZXI	51-85195	165-ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1256V18-333BZXI			
	CY7C1243V18-333BZXI			
	CY7C1245V18-333BZXI			

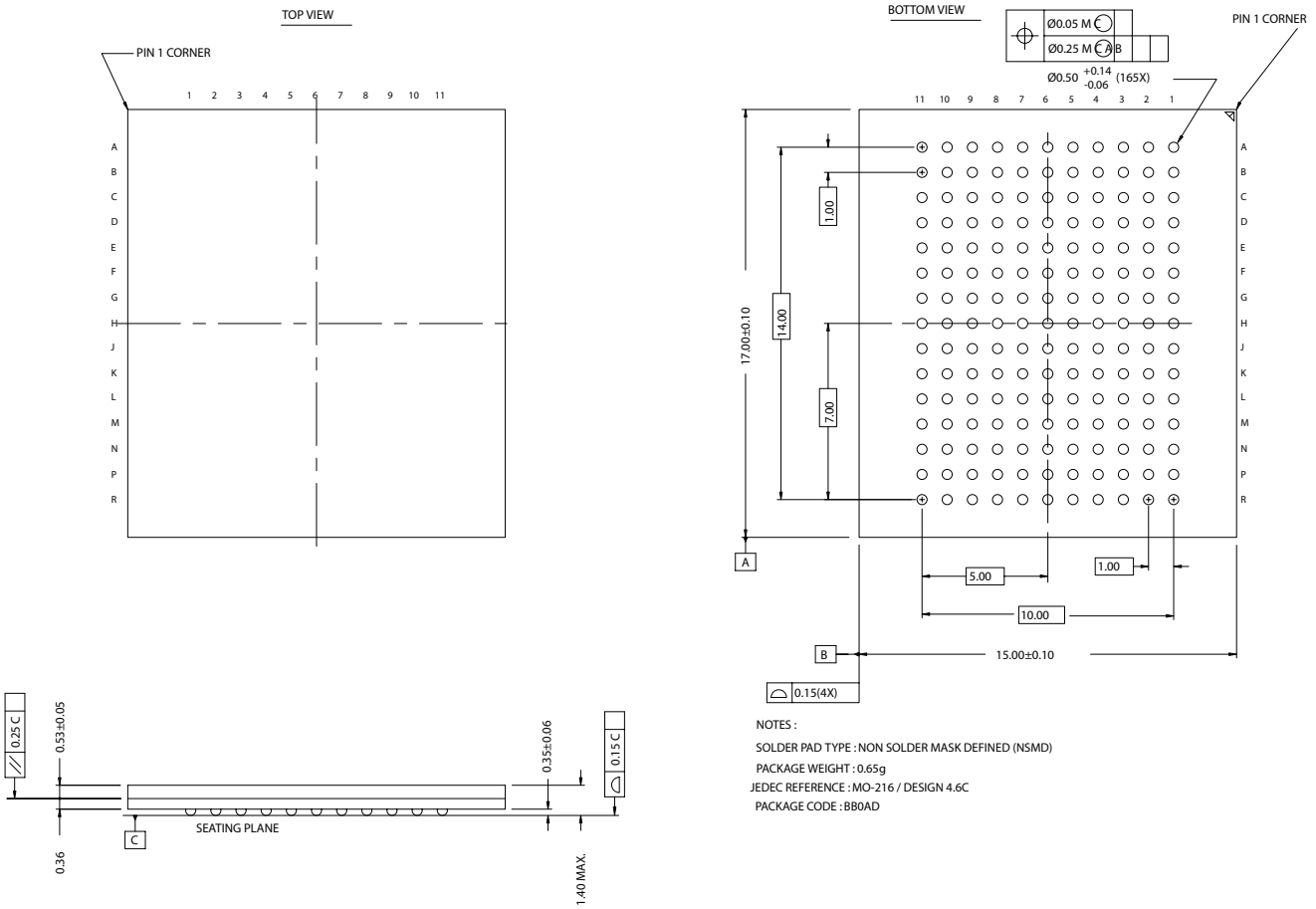
Ordering Information (continued)

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
300	CY7C1241V18-300BZC	51-85195	165-ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Commercial
	CY7C1256V18-300BZC			
	CY7C1243V18-300BZC			
	CY7C1245V18-300BZC			
	CY7C1241V18-300BZXC	51-85195	165-ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1256V18-300BZXC			
	CY7C1243V18-300BZXC			
	CY7C1245V18-300BZXC			
	CY7C1241V18-300BZI	51-85195	165-ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm)	Industrial
	CY7C1256V18-300BZI			
	CY7C1243V18-300BZI			
	CY7C1245V18-300BZI			
	CY7C1241V18-300BZXI	51-85195	165-ball Fine Pitch Ball Grid Array (15 x 17 x 1.4 mm) Lead-Free	
	CY7C1256V18-300BZXI			
	CY7C1243V18-300BZXI			
	CY7C1245V18-300BZXI			

Package Diagram

Figure 5. 165-ball FBGA (15 x 17 x 1.40 mm), 51-85195



51-85195-*A

© Cypress Semiconductor Corporation, 2006-2007. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

QDR RAMs and Quad Data Rate RAMs comprise a new family of products developed by Cypress, IDT, NEC, Renesas, andSamsung. All other trademarks or registered trademarks referenced herein are property of the respective corporations.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Document History Page

Document Title: CY7C1241V18/CY7C1256V18/CY7C1243V18/CY7C1245V18, 36-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency) Document Number: 001-06365				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	425689	See ECN	NXR	New Data Sheet
*A	461639	See ECN	NXR	Revised the MPNs from CY7C1256AV18 to CY7C1256V18 CY7C1243AV18 to CY7C1243V18 CY7C1245AV18 to CY7C1245V18 Changed t_{TH} and t_{TL} from 40 ns to 20 ns, changed t_{TMSS}, t_{TDIS}, t_{CS}, t_{TMSH}, t_{TDIH}, t_{CH} from 10 ns to 5 ns and changed t_{TDOV} from 20 ns to 10 ns in TAP AC Switching Characteristics table Modified Power-Up waveform
*B	497628	See ECN	NXR	Changed the V_{DDQ} operating voltage to 1.4V to V_{DD} in the Features section, in Operating Range table and in the DC Electrical Characteristics table Added foot note in page# 1 Changed the Maximum rating of Ambient Temperature with Power Applied from –10°C to +85°C to –55°C to +125°C Changed V_{REF} (Max.) spec from 0.85V to 0.95V in the DC Electrical Characteristics table and in the note below the table Updated footnote #20 to specify Overshoot and Undershoot Spec Updated Θ_{JA} and Θ_{JC} values Removed x9 part and its related information Updated footnote #25
*C	1072841	See ECN	VKN/KKVTMP	Converted from preliminary to final Added x8 and x9 parts Changed I_{DD} values from 950 mA to 1240 mA for 375 MHz, 850 mA to 1120 mA for 333 MHz, 800 mA to 1040 mA for 300 MHz Changed I_{SB} values from 300 mA to 310 mA for 375 MHz, 275 mA to 300 mA for 333 MHz, 250 mA to 280 mA for 300 MHz Changed t_{CYC} max spec to 8.4 ns for all speed bins Changed Θ_{JA} value from 12.43 °C/W to 16.25 °C/W Updated Ordering Information table

[+] Feedback