

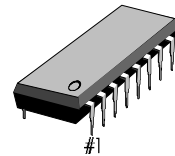
INTRODUCTION

The S5T8554B03 consists of on-chip PCM encoders, decoders (PCM CODECs) and PCM line filter. This device provides all the functions required to interface a full-duplex voice telephone circuit, digital answering phone. This device is designed to perform the transmit encoding and receive decoding as well as the transmit and receive filtering function in PCM system. Also it is intended to be used at the analog termination of a PCM line / trunk. This device provide the Band pass filtering of the analog signals prior to encoding and after decoding. This combination device performs the encoding and decoding of voice and call progress tones as well as the signaling and supervision information.

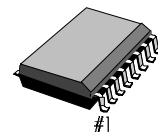
FEATURES

- Complete CODEC and filtering system
- Encoding / Decoding : 8 bits μ -law PCM
- On-chip auto zero, sample and hold, and precision voltage references
- Low power dissipation : 60mW (operating)
3mW (standby)
- $\pm 5V$ operation
- TTL or CMOS compatible
- Automatic power down

16-DIP-300



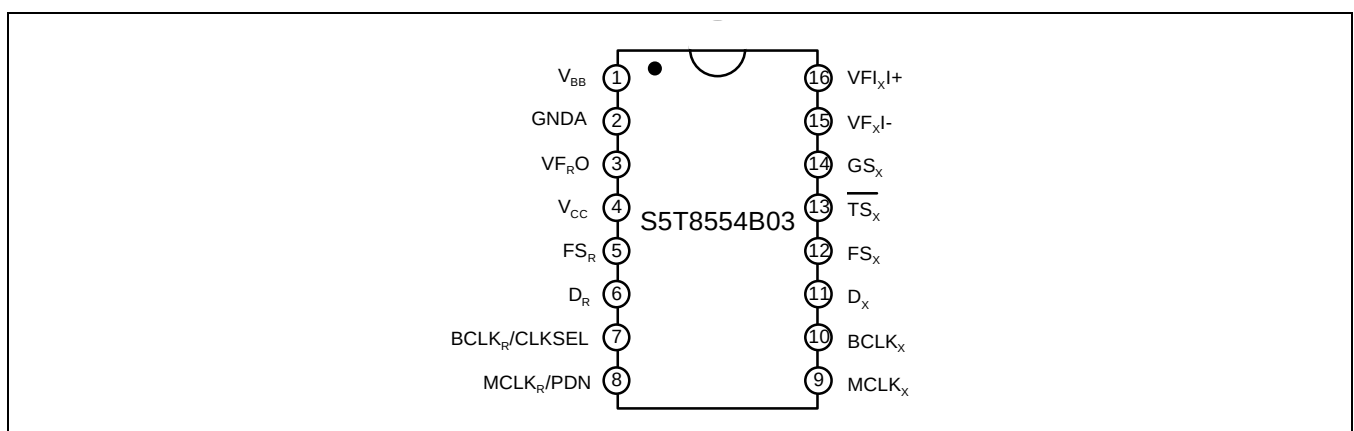
16-SOP-BD300



ORDERING INFORMATION

Device	Package	Operating Temperature
S5T8554B03-D0B0	16-DIP-300	0 ~ + 70°C
S5T8554B03-S0B0	16-SOP-BD300	

PIN CONFIGURATION



BLOCK DIAGRAM

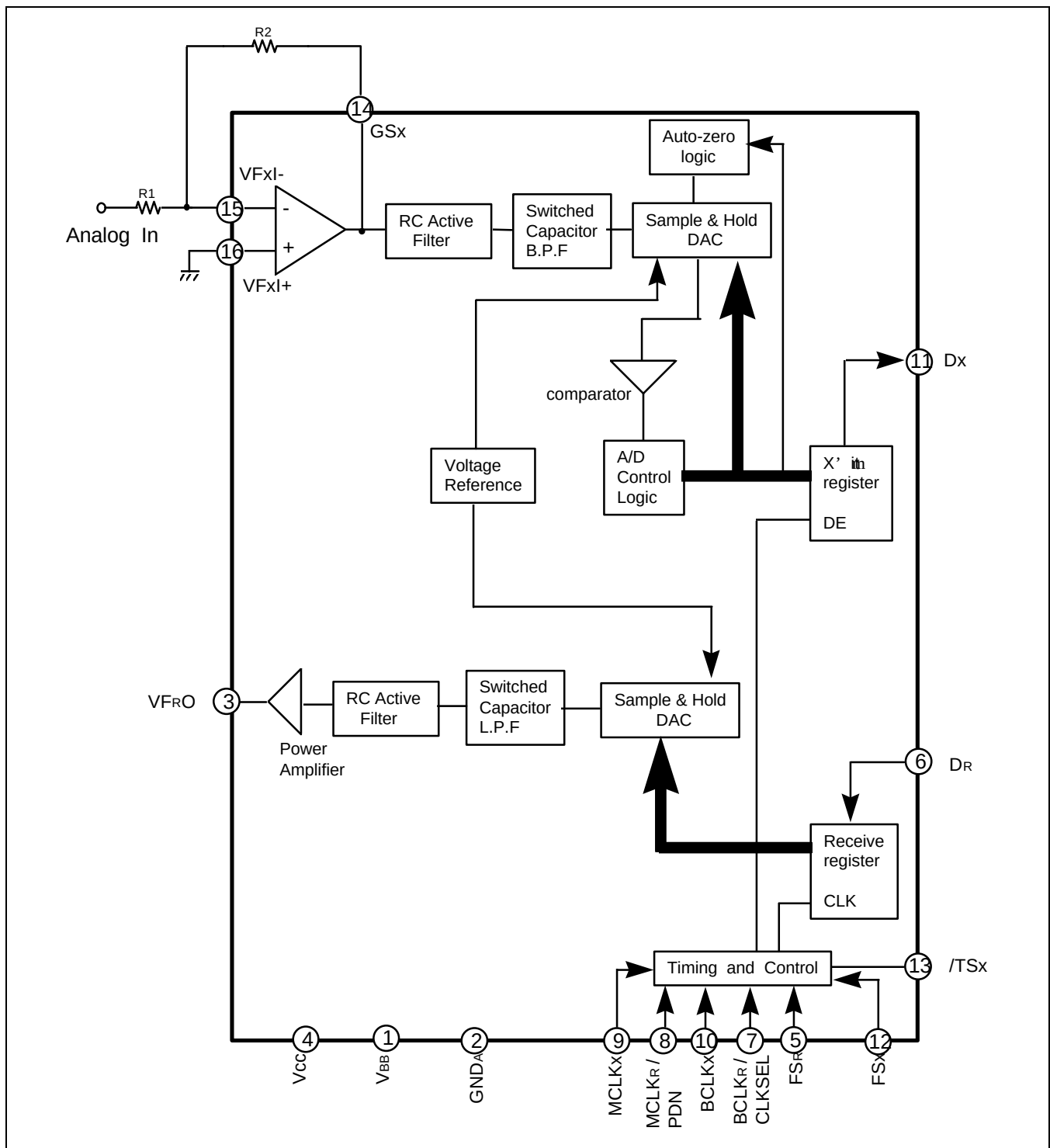


Figure 1.

PIN DESCRIPTION

Pin No	Symbol	Description
1	V _{BB}	V _{BB} = -5V ± 5%
2	GNDA	Analog ground
3	VF _{RO}	Analog output of the receiver filter
4	V _{CC}	V _{CC} = + 5V ± 5%
5	FS _R	Receive frame sync pulse. 8kHz pulse train.
6	D _R	PCM data input
7	BCLK _R / CLKSEL	Logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in normal operation and BCLKx is used for both TX and RX directions. Alternately direct clock input available, vary from 64kHz to 2.048MHz.
8	MCLK _R / PDN	When MCLK _R is connected continuously high, the device goes powered down . Normally connected continuously low, MCLKx is selected for all DAC timing. Alternately direct 1.536MHz/1.544MHz or 2.048MHz clock input is available.
9	MCLK _{Xn}	1.536MHz/1.544MHz or 2.048MHz clock input is available
10	BCLK _X	May be vary from 64kHz 2.048MHz, but BCLKx is externally tied with MCLKx in normal operation.
11	D _X	PCM data output.
12	FS _X	TX frame sync pulse. 8kHz pulse train.
13	TS _X	Changed from high to low during the encoder timeslot. Open drain output.
14	GS _X	Analog output of the TX input amplifier. Used to set gain through external resistor between pin 14 to pin 15.
15	VF _{XI-}	Inverting input stage of the TX analog signal.
16	VF _{XI+}	Non-inverting input stage of the TX analog signal.e

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V _{CC}	+7	V
Negative Supply Voltage	V _{BB}	-7	V
Voltage at any Analog Input or Output	V _{I(A)}	V _{CC} + 0.3 to V _{BB} - 0.3	V
Voltage at any Digital Input or Output	V _{I(D)}	V _{CC} + 0.3 to GNDA - 0.3	V
Operating Temperature Range	T _a	0 to 70	°C
Storage Temperature Range	T _{STG}	-65 to +150	°C
Lead Temperature Range (soldering, 10 sec)	T _{LEAD}	300	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified : Ta = 0°C to 70°C , Vcc = 5V ± 5%, VBB = -5V ± 5%, GND_A = 0V)

Characteristic	System	Test Conditions	Min.	Typ.	Max.	Unit
Power Dissipation						
Power down Current	I _{CC (down)}	No Load	–	0.5	3.0	mA
Power down Current	I _{BB (down)}	No Load	–	0.05	1.0	mA
Active Current	I _{CC (A)}	No Load	–	6.0	10	mA
Active Current	I _{BB (A)}	No Load	–	6.0	10	mA
Digital Interface						
Input Low Voltage	V _{IL}	–	–	–	0.6	V
Input High Voltage	V _{IH}	–	2.2	–	–	V
Input Low Current	I _{IL}	GND _A < V _{IN} < V _{IL} , all digital input	–15	–	15	μA
Input High Current	I _{IH}	V _{IH} < V _{IN} < V _{CC}	–15	–	15	μA
Output Low Voltage	V _{OL}	Dx , I _L = 3.2 mA SIG _R , I _L = 1.0 mA /TSx , I _L = 3.2 mA , open drain	–	–	0.4 0.4 0.4	V V V
Output High Voltage	V _{OH}	Dx , I _H = –3.2mA SIG _R , I _H = –1.0mA	2.4 2.4	–	–	V V
Output Current in High impedance state (Tri – state)	I _{OH (HZ)}	Dx , GND _A < V _O < V _{CC8}	–15	–	15	μA
Analog Interface with Receiver Filter						
Output Resistance	R _O	pin V _{FR0}	–	1	3	Ω
Load Resistance	R _L	V _{FR0} = ± 2.5V	600	–	–	Ω
Load Capacitance	C _L	–	–	–	500	pF
Output Capacitance	C _L	–	–200	–	200	mV
Analog Interface with Transmit input Amp						
Input Leakage Current	I _{LKG}	–2.5V < V < +2.5V, V _{Fxl+} or V _{Fxl-}	–200	–	200	nA
Input Resistance	R _I	–2.5V < V < +2.5V, V _{Fxl+} or V _{Fxl-}	10	–	–	MΩ
Output Resistance	R _O	closed loop , unity gain	–	1	3	Ω
Load Resistance	R _L	GSx	10	–	–	kΩ
Load Capacitance	C _L	GSx	–	–	50	pF
Output Dynamic Range	V _{OD(TX)}	GSx , R _L < 10kΩ	± 2.8	–	–	V
Voltage Gain	G _V	V _{Fxl+} to GSx	5000	–	–	V/V
Unity Gain bandwidth	B _W	–	1	2	–	MHz
Offset Voltage	V _{IO(TX)}	–	–20	–	20	mV
Common - mode Voltage	V _{CM(TX)}	CMRR _{xA} > 60dB	–2.5	–	2.5	V
Common mode rejection ratio	CMRR	DC test	55	–	–	dB
Power supply rejection ratio	PSRR	DC test	55	–	–	dB

TIMING CHARACTERISTICS(Unless otherwise specified : Ta = 0°C to 70°C, Vcc = 5V ± 5%, VBB = -5V ± 5%, GND_A = 0V)

Characteristic	System	Test Conditions	Min.	Typ.	Max.	Unit
Frequency of Master Clock	f _{MCK}	Depends on the device used and the BCLK _R /CLKSEL pin. MCLK _X and MCLK	–	1.536	–	MHz
			–	1.544	–	
			–	2.048	–	
Rise time of Bit Clock	t _R (BCK)	t _{PB} = 488ns	–	–	50	nS
Fall Time of Bit Clock	t _F (BCK)	t _{PB} = 488ns	–	–	50	nS
Hold Time for Bit Clock low to Frame sync	t _H (LFS)	Long Frame only	0	–	–	nS
Hold Time for Bit Clock High to Frame sync	t _H (HFS)	Short Frame only	0	–	–	nS
Set-up Time from Frame sync to Bit Clock low	t _{SU} (FBCL)	Long Frame only	80	–	–	nS
Delay time from BCLK _X High to data valid	t _D (HDV)	Load = 150pF + 2 LSTTL loads	0	–	180	nS
Delay time to /TS _X low	t _D (TSXL)	Load = 150pF + 2 LSTTL loads	–	–	140	nS
Delay time from BCLK _X low to data output disable	t _D (LDD)		50	–	165	nS
Delay Time to valid data from FS _X or BCLK _X	t _D (VD)	CL = 0 pF to 150 pF Whichever comes later.	20	–	165	nS
Set-up Time from DR valid to BCLK _{X/R} low	t _{SU} (DRBL)	–	50	–	–	nS
Hold time from BCLK _{X/R} low to DR invalid	t _H (BLDR)	–	50	–	–	nS
Set-up time from FS _{X/R} to BCLK _{X/R} low	t _{SU} (FBLS)	Short Frame sync pulse (1 or 2 bit clock periods long) : note1	50	–	–	nS
Width of master clock High	t _W (MCKH)	MCLK _X and MCLK _R	160	–	–	nS
Width of master clock Low	t _W (MCKL)	MCLK _X and MCLK _R	160	–	–	nS
Rise Time of Master clock	t _R (MCK)	MCLK _X and MCLK _R	–	–	50	nS
Fall Time of Master clock	t _F (MCK)	MCLK _X and MCLK _R	–	–	50	nS
Set-up time from BCLK _X High (FS _X in Long Frame Sync mode) to MCLK _X falling edge	t _{SU} (BHMF)	1'st bit clock after the leading edge of FS _X	50	–	–	nS
Period of Bit Clock	t _{CK}	–	485	488	15.725	nS
Width of Bit clock High	t _W (BCKH)	V _{IH} = 2.2V	160	–	–	nS
Width of Bit clock Low	t _W (BCKL)	V _{IL} = 0.6V	160	–	–	nS
Hold time from BCLK _{X/R} to FS _{X/R} low	t _H (BLFL)	Short Frame sync pulse (1 or 2 bit clock periods long) : note1	100	–	–	nS

TIMING DIAGRAM

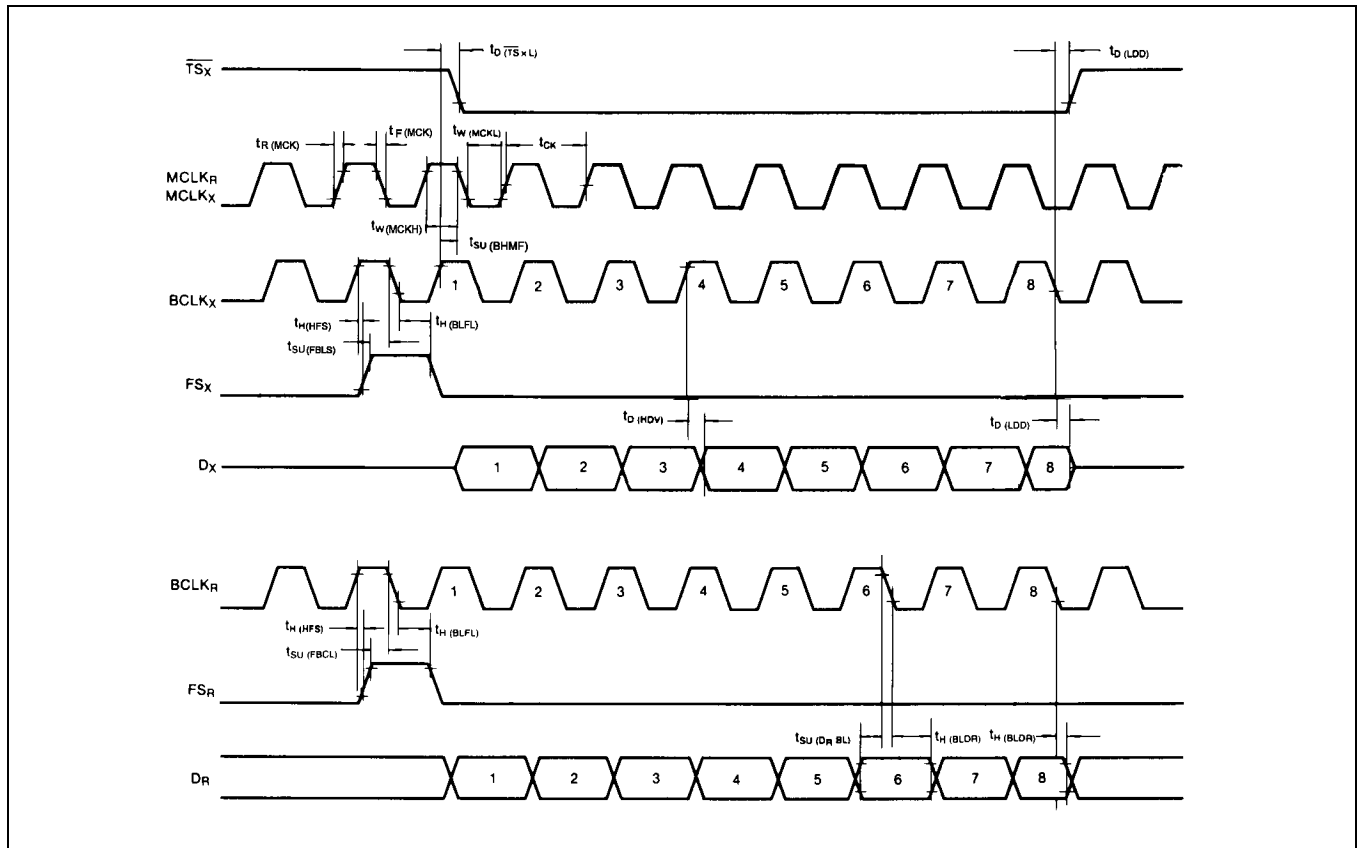


Figure 2. Short Frame SYNC Timing

TIMING DIAGRAM (Continued)

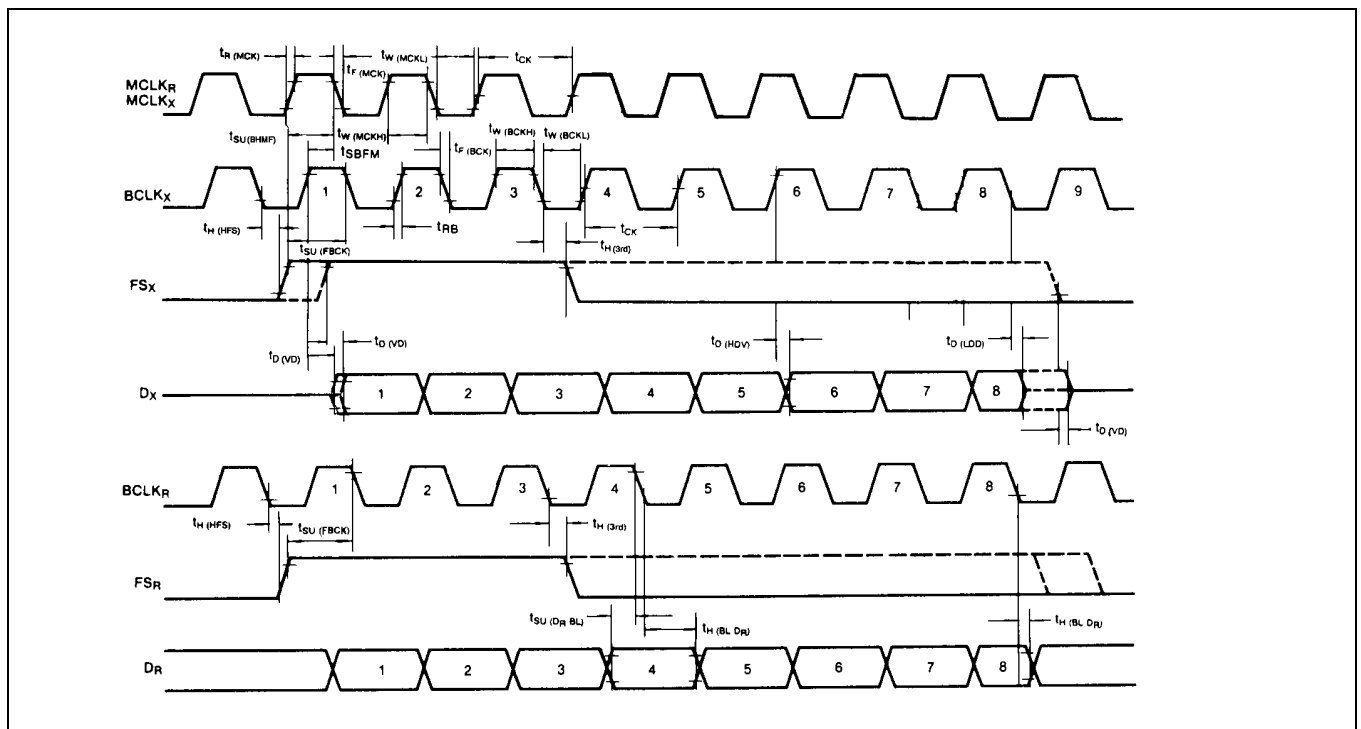


Figure 3.

NOTE: 1. For Short Frame Sync timing, FSX and FSR must go high while their respective bit clocks has high level

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: $T_a = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$, $V_{BB} = -5\text{V} \pm 5\%$, $GND_A = 0\text{V}$, $f = 1.02\text{kHz}$, $V_{in} = 0\text{dBm0}$, transmit input amplifier connected for unity-gain, non-inverting)

Characteristic	System	Test Conditions	Min.	Typ.	Max.	Unit
Amplitude Response						
Receive Gain, Absolute	$G_{V(ARX)}$	$T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $V_{BB} = -5\text{V}$ Input = Digital code sequence for 0dBm0 signal at 1020Hz	-1.5	—	1.5	dB
Receive Gain, Relative to $G_{V(RRX)}$	$G_{V(RRX)}$	$f = 0\text{Hz}$ to 3000Hz $f = 3300\text{Hz}$ $f = 3400\text{Hz}$	-0.6 -0.55 -1.5	—	0.5 0.5 1.5	dB
Absolute Receive Gain Variations with temperature	$\Delta G_{V(ARX)} / \Delta T$	$T_a = 0^\circ\text{C}$ to 70°C	—	—	± 0.1	dB

TRANSMISSION CHARACTERISTICS (Continued)

(Unless otherwise specified: $T_a = 0^{\circ}\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$, $V_{BB} = -5\text{V} \pm 5\%$, $G_{ND A} = 0\text{V}$, $f = 1.02\text{kHz}$
 $V_{in} = 0\text{dBm0}$, transmit input amplifier connected for unity-gain, non-inverting)

Characteristic	System	Test Conditions	Min.	Typ.	Max.	Unit
Receive Gain Variations with level	$\Delta G_{V(RXL)}$	Sinusoidal test method; reference input PCM code correspond to an ideally encoded -10dBm0 signal PCM level = -40dBm0 to $+3\text{dBm0}$ PCM level = -50dBm0 to -40dBm0	-0.4 -0.8	—	0.4 0.8	dB
Receive output drive level		$R_L = 600\Omega$	-2.5	—	2.5	V
Absolute level	$V_{O(RX)}$ V_{AL}	Norminal 0dBm0 level is same as 4--dBm (600Ω)	—	1.2276	—	V _{rms}
Max overload level	$V_{OL(MAX)}$	Max overload level (3.17dBm0)	—	2.501	—	V _{PK}
Transmit gain, absolute	$G_{V(ATX)}$	$T_a = 25^{\circ}\text{C}$, $V_{CC} = 5\text{V}$, $V_{BB} = -5\text{V}$ Input at $G_{Sx} = 0\text{dBm0}$ at 1020Hz	-1.5	—	1.5	dB
Transmit gain, relative to $G_{V(ATX)}$	$G_{V(RTX)}$	$f = 16\text{Hz}$ $f = 50\text{Hz}$ $f = 60\text{Hz}$ $f = 200\text{Hz}$ $f = 300\text{Hz} - 3000\text{Hz}$ $f = 3300\text{Hz}$ $f = 3400\text{Hz}$ $f = 4000\text{Hz}$ $f = 4600\text{Hz}$ and above, measure response from 0Hz to 4kHz	-2 -0.5 -0.55 -1.5	—	-35 -25 -21 -0.5 0.5 0.5 -0.5 -10 -25	dB
Absolute transmit gain variations with temperature	$\Delta G_{V(ATX)} / \Delta T$	$T_a = 0^{\circ}\text{C}$ to 70°C	—	—	± 0.1	dB
Transmit gain variations with level	$\Delta G_{V(TXL)}$	Sinusoidal test method ; Reference level = -10dBm0 $V_{F_{X1}} = -40\text{dBm0}$ to $+3\text{dB0}$ $V_{F_{X1}} = -50\text{dBm0}$ to -40dB0	-0.4 -0.8	—	0.4 0.8	dB
Envelope Delay Distortion with Frequency						
Receive Delay, Absolute	$t_{D(ARX)}$	$f = 1600\text{Hz}$	—	—	200	μs
Receive Delay, Relative to $t_{D(ARX)}$	$t_{D(RRX)}$	$f = 500\text{Hz} - 1000\text{Hz}$ $f = 1000\text{Hz} - 1600\text{Hz}$ $f = 1600\text{Hz} - 2600\text{Hz}$ $f = 2600\text{Hz} - 2800\text{Hz}$ $f = 2800\text{Hz} - 3000\text{Hz}$	-40 -30	—	90 125 175	μs
Transmit Delay, Absolute	$t_{D(ATX)}$	$f = 1600\text{Hz}$	—	—	315	μs

TRANSMISSION CHARACTERISTICS (Continued)

(Unless otherwise specified: $T_a = 0^{\circ}\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$, $V_{BB} = -5\text{V} \pm 5\%$, $GND_A = 0\text{V}$, $f = 1.02\text{kHz}$, $V_{in} = 0\text{dBm0}$, transmit input amplifier connected for unity-gain, non-inverting)

Characteristic	System	Test Conditions	Min.	Typ.	Max.	Unit
Transmit Delay, Relative to $t_{D(ATX)}$	$t_{D(RTX)}$	$f = 500\text{Hz} - 600\text{Hz}$ $f = 600\text{Hz} - 800\text{Hz}$ $f = 800\text{Hz} - 1000\text{Hz}$ $f = 1000\text{Hz} - 1600\text{Hz}$ $f = 1600\text{Hz} - 2600\text{Hz}$ $f = 2600\text{Hz} - 2800\text{Hz}$ $f = 2800\text{Hz} - 3000\text{Hz}$	–	–	220 145 75 40 75 105 155	μs
Noise						
Receive Noise, C Message Weighted	N_{RXC}	PCM code equals alternating positive and negative zero, S5T8554B03	–	–	18	dBrnC0
Transmit Noise, C Message Weighted	N_{TXC}	S5T8554B03	–	–	15	dBrnC0
Noise, Single Frequency	NSF	$f = 0\text{kHz}$ to 100kHz , loop around measurement, $V_{FXI+} = 0\text{Vrms}$	–	–	–53	dBrnC0
Positive Power Supply Rejection, Transmit	$PSRR_{(PTX)}$	$V_{FXI+} = 0\text{Vrms}$, $V_{CC} = 5.0\text{VDC} + 100\text{mVms}$ $f = 0\text{kHz} - 50\text{kHz}$	25	–	–	dB
Negative Power Supply Rejection, Transmit	$PSRR_{(NTX)}$	$V_{FXI+} = 0\text{Vrms}$, $V_{BB} = -5.0\text{VDC} + 100\text{mVrms}$ $f = 0\text{kHz} - 50\text{kHz}$	25	–	–	dB
Positive Power Supply Rejection, Receive	$PSRR_{(PRX)}$	PCM code equals positive zero $V_{CC} = 5.0\text{VDC} + 100\text{mVrms}$ $f = 0\text{Hz} - 4000\text{Hz}$ $f = 4\text{kHz} - 25\text{kHz}$	25 25	–	–	dB
Negative Power Supply Rejection, Receive	$PSRR_{(NRX)}$	PCM code equals positive zero $V_{BB} = -5.0\text{VDC} + 100\text{mVrms}$ $f = 0\text{Hz} - 4000\text{Hz}$ $f = 4\text{kHz} - 25\text{kHz}$	25 25	–	–	dB
Spurious Out-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0 , $300\text{Hz} - 3400\text{Hz}$ input PCM applied to DR, Measure individual image signals at VFRO $4600\text{Hz} - 7600\text{Hz}$ $7600\text{Hz} - 100,000\text{Hz}$	–	–	–28 –35	dB
Distortion						
Signal to Total Distortion Transmit or Receive Half-Channel	THD_{TX} THD_{RXa}	Sinusoidal test method; level = 3.0dBm0 = 0dBm0 to 30dBm0 = -40dBm0 XMT RCV	28 30 25 25	–	–	dB

TRANSMISSION CHARACTERISTICS (Continued)

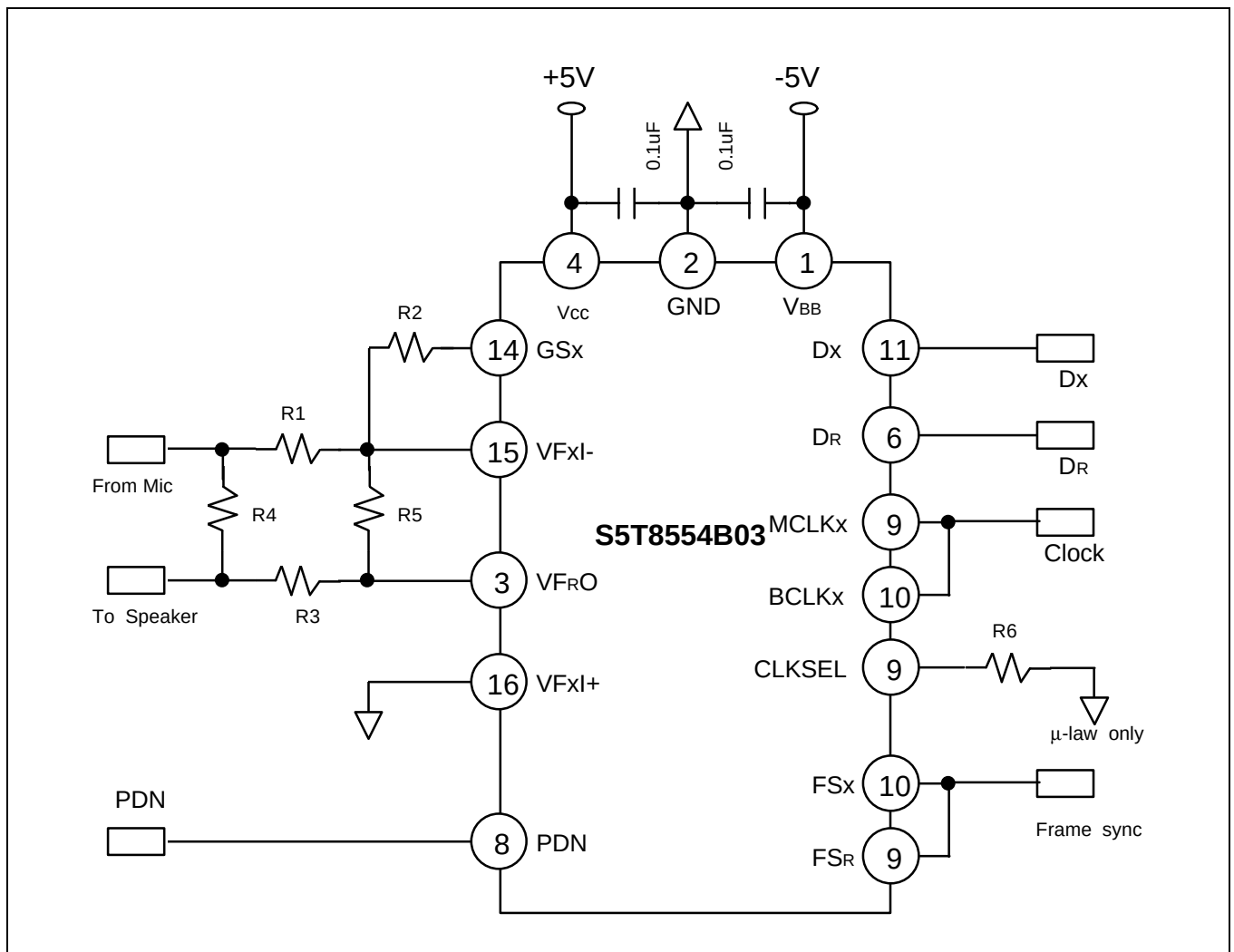
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Characteristic	System	Test Conditions	Min.	Typ.	Max.	Unit
Single Frequency Distortion, Transmit	$\text{THD}_{\text{SF(TX)}}$	–	–	–	–41	–dB
Single Frequency Distortion, Receive	$\text{THD}_{\text{SF(RX)}}$	–	–	–	–41	–dB
Intermodulation Distortion	THD_{IMD}	Loop around measurement, $\text{VFXI+} = -4\text{dBm0}$ to -21dBm0 , two frequencies in the range 300Hz – 3400Hz	–	–	–35	–dB
Crosstalk						
Transmit to Receive Crosstalk, 0dBm0 Transmit level	$\text{CT}_{(\text{TX-RX})}$	$f = 300\text{Hz} - 3400\text{Hz}$ $D_R = \text{Steady PCM code}$	–	–90	–75	dB
Receive to Transmit Crosstalk, 0dBm0 Receive level	$\text{CT}_{(\text{RX-TX})}$	$f = 300\text{Hz} - 3400\text{Hz}$, $\text{VFXI} = 0\text{V}$	–	–90	–70 (note 1)	dB

NOTE: $\text{CT}_{(\text{RX-TX})}$ is measured with a -40dBm0 activating signal applied at VFXI+

	m-Law PCM : S5T8554B03
VIN (at GSX) = + Full Scale	1 0 0 0 0 0 0 0
VIN (at GSx) = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
VIN (at GSx) = – Full Scale	0 0 0 0 0 0 0 0

APPLICATION CIRCUIT



NOTES:

1. Supposing desired Line Termination Impedance $R_L = 600\Omega$
It is 0 dBm - 0.77459 Vrms
2. Tx Gain = $20 \log (R_2 / R_1)$, $R_1 + R_2 < 100k\Omega$
or The Correspondence of 0 dBm0 = 4 dBm

Selection of Master Clock Frequency

BCLKR / CLKSEL	Master Clock Frequency
Clocked	1.536 / 1.544MHz
0	2.048MHz
1(or Open)	1.536 / 1.544MHz

NOTES