DATA SHEET

DIGITAL dcc COMPACT CASSETTE

SAA3323
Drive processor for DCC systems

Preliminary specification
File under Integrated Circuits, IC01

May 1994

Philips Semiconductors

PHILIPS

Drive processor for DCC systems SAA3323

FEATURES

- Operating supply voltage: 2.7 to 3.6 V
- Low power dissipation: 84 mW (typ)
- Single chip digital equalizer, tape formatting and error correction
- 8-bit flash analog-to-digital converter (ADC) for low symbol error rate
- Two switchable Infinite Impulse-Response (IIR) filter sections
- 10-tap Finite Impulse-Response (FIR) filter per main data channel, with 8 bit coefficients, identical for all main channels
- 10-tap FIR filter for the AUX channel
- Analog and digital eye outputs
- Interrupt line triggered by internal auxiliary envelope processing e.g. label, counter, and others
- Robust programmable digital PLL clock extraction unit
- Low power SLEEP mode
- Slew rate limited Electromagnetic Compatibility (EMC) friendly output
- Digital Compact Cassette (DCC) optimized error correction
- Programmable symbol synchronization strategy for tape input data
- Microcontroller control of capstan servo possible during playback and recording



- Frequency and phase regulation of capstan servo during playback
- Choice of Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM) types for system Random Access Memory (RAM)
- Scratch pad RAM for microcontroller in system RAM
- Integrated interface for Precision Adaptive Sub-band Coding (PASC) data bus
- Three wire microcontroller ‘L3’ interface
- Protection against invalid auxiliary data
- Seamless joins between recordings.

GENERAL DESCRIPTION

The SAA3323 performs the drive processor function in the DCC system. This function is built up of digital equalizer, error correction and tape formatting functions. The digital equalizer is intended for use with DCC read amplifiers TDA1318 or TDA1380. The tape formatting and error correction circuit is intended for use with PASC ICs SAA2003 and SAA2013, and write amplifiers TDA1319 or TDA1381.

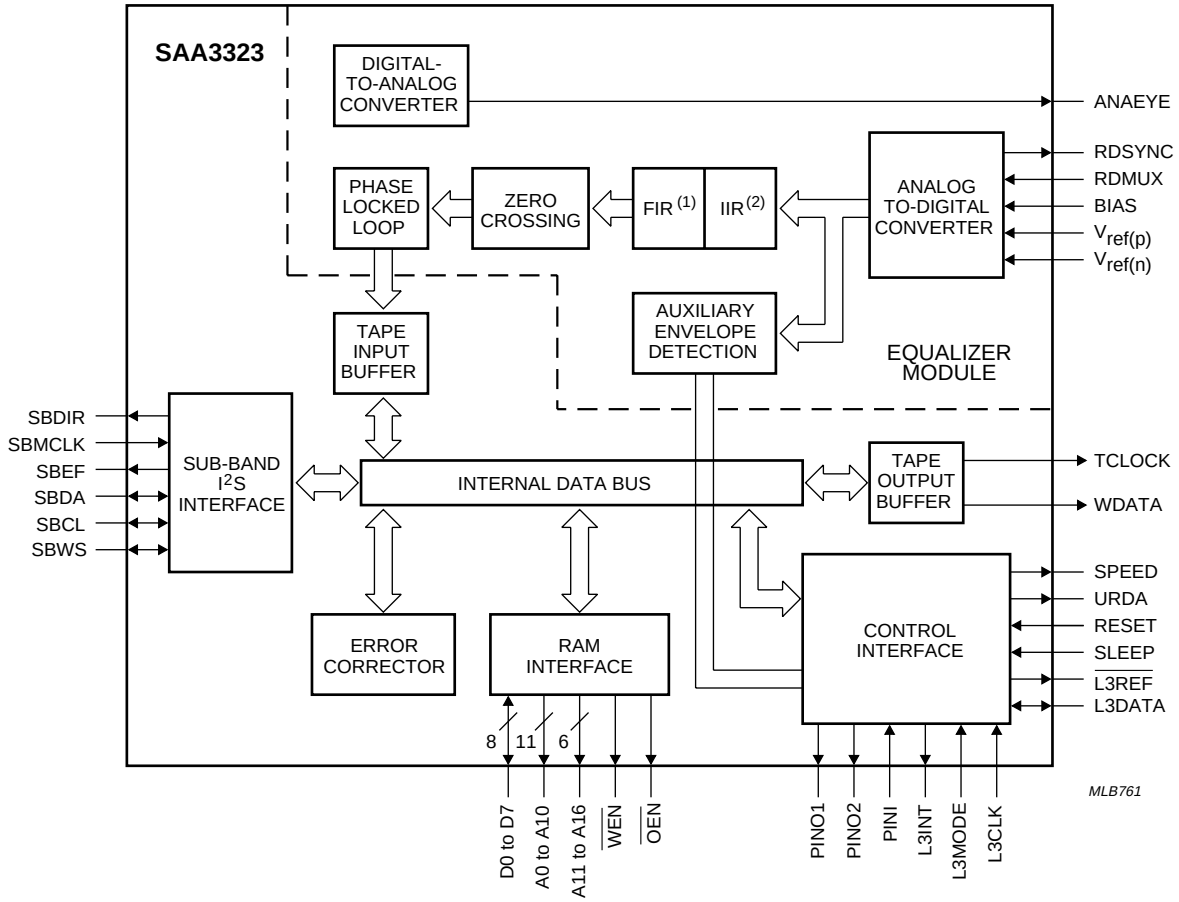
ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA3323H	80	TQFP80[1]	plastic	SOT315-1
SAA3323GP	80	QFP80[1]	plastic	SOT318-2

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *“Quality Reference Pocketbook”* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM



(1) FIR = Finite Impulse-Response.

(2) IIR = Infinite Impulse-Response.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
SBWS	1	79	word select for sub-band PASC interface	I/O (1 mA)
SBCL	2	80	bit clock for sub-band PASC interface	I/O (1 mA)
SBDA	3	1	data line for sub-band PASC interface	I/O (1 mA)
SBDIR	4	2	direction line for sub-band PASC interface	O (1 mA)
SBMCLK	5	3	master clock for sub-band PASC interface	I
URDA	6	4	unreliable data	O (1 mA)
L3MODE	7	5	mode line for L3 interface	I
L3CLK	8	6	bit clock line for L3 interface	I
L3DATA	9	7	serial data line for L3 interface	I/O (2 mA)
L3INT	10	8	L3 interrupt output	O (1 mA)
V_{DD1}	11	9	digital supply voltage	S
V_{SS1}	12	10	digital ground	S
$\overline{\text{L3REF}}$	13	11	L3 bus timing reference	O (1 mA)
RESET	14	12	reset SAA3323	I
SLEEP	15	13	sleep mode selection of SAA3323	I
CLK24	16	14	24.576 MHz clock input	I
AZCHK	17	15	channel 0 and channel 7 azimuth monitor	O (1 mA)
MCLK	18	16	6.144 MHz clock output	O (1 mA)
TEST3	19	17	TEST3 output; do not connect	O (1 mA)
ERCOSTAT	20	18	ERCO status, for symbol error rate measurements	O (1 mA)
$\overline{\text{OEN}}$	21	19	output enable for RAM	O (2 mA)
A10/$\overline{\text{RAS}}$	22	20	address SRAM; $\overline{\text{RAS}}$ DRAM	O (2 mA)
V_{DD2}	23	21	digital supply voltage	S
V_{SS2}	24	22	digital ground	S
D7	25	23	data SRAM	I/O (4 mA)
D6	26	24	data SRAM	I/O (4 mA)
D5	27	25	data SRAM	I/O (4 mA)
D4	28	26	data SRAM	I/O (4 mA)
D3	29	27	data SRAM; data DRAM	I/O (4 mA)
D2	30	28	data SRAM; data DRAM	I/O (4 mA)
D1	31	29	data SRAM; data DRAM	I/O (4 mA)
V_{DD7}	32	30	digital supply voltage for RAM	S
V_{SS7}	33	31	digital ground for RAM	S
D0	34	32	data SRAM; data DRAM	I/O (4 mA)
A0	35	33	address SRAM; address DRAM	O (2 mA)
A1	36	34	address SRAM; address DRAM	O (2 mA)
A2	37	35	address SRAM; address DRAM	O (2 mA)
A3	38	36	address SRAM; address DRAM	O (2 mA)

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
A4	39	37	address SRAM; address DRAM	O (2 mA)
V_{SS3}	40	38	digital ground	S
V_{DD3}	41	39	digital supply voltage	S
A5	42	40	address SRAM; address DRAM	O (2 mA)
A6	43	41	address SRAM; address DRAM	O (2 mA)
A7	44	42	address SRAM; address DRAM	O (2 mA)
A12/PINO5	45	43	address SRAM; Port expander output 5	O (2 mA)
A14/PINO1	46	44	address SRAM; Port expander output 1	O (2 mA)
A16/PINO3	47	45	address SRAM; Port expander output 3	O (2 mA)
A15/PINO4	48	46	address SRAM; Port expander output 4	O (2 mA)
$\overline{WEN}$	49	47	write enable for RAM	O (2 mA)
A13/PINO2	50	48	address SRAM; Port expander output 2	O (2 mA)
A8	51	49	address SRAM; address DRAM	O (2 mA)
V_{DD4}	52	50	digital supply voltage	S
V_{SS4}	53	51	digital ground	S
A9/$\overline{CAS}$	54	52	address SRAM; $\overline{CAS}$ for DRAM	O (2 mA)
A11	55	53	address SRAM	O (2 mA)
SPEED	56	54	Pulse Width Modulation (PWM) capstan control output for deck	O_t (1 mA)
PINO2	57	55	Port expander output 2	O_t (1 mA)
WDATA	58	56	serial output to write amplifier	O (1 mA)
TCLOCK	59	57	3.072 MHz clock output for tape I/O	O (1 mA)
V_{SS5}	60	58	digital ground	S
V_{DD5}	61	59	digital supply voltage	S
TEST2	62	60	TEST mode select; do not connect	I_{pd}
RDMUX	63	61	analog multiplexed input from read amplifier	I_A
$V_{ref(p)}$	64	62	ADC positive reference voltage	I_A
$V_{ref(n)}$	65	63	ADC negative reference voltage	I_A
SUBSTR	66	64	substrate connection	I_A
BIAS	67	65	bias current for ADC	I_A
V_{SSA}	68	66	analog ground	S
V_{DDA}	69	67	analog supply voltage	S
ANAEYE	70	68	analog eye pattern output	O_A
RDSYNC	71	69	synchronization output for read amplifier	O (1 mA)
V_{DD6}	72	70	digital supply voltage	S
V_{SS6}	73	71	digital ground	S
CHTST1	74	72	channel test pin 1	O (1 mA)
CHTST2	75	73	channel test pin 2	O (1 mA)
TEST0	76	74	TEST mode select; do not connect	I_{pd}
TEST1	77	75	TEST mode select; do not connect	I_{pd}

SYMBOL	PIN		DESCRIPTION	TYPE(1)
	QFP80	TQFP80		
PINI	78	76	Port expander input	I
PINO1	79	77	Port expander output 1	O (1 mA)
SBEF	80	78	sub-band PASC error flag line	O (1 mA)

Note

1. I = input; I_A = analog input; I_{pd} = input with pull-down resistance; I/O = bidirectional; O = output; O_A = analog output; O_t = 3-state output; S = supply.

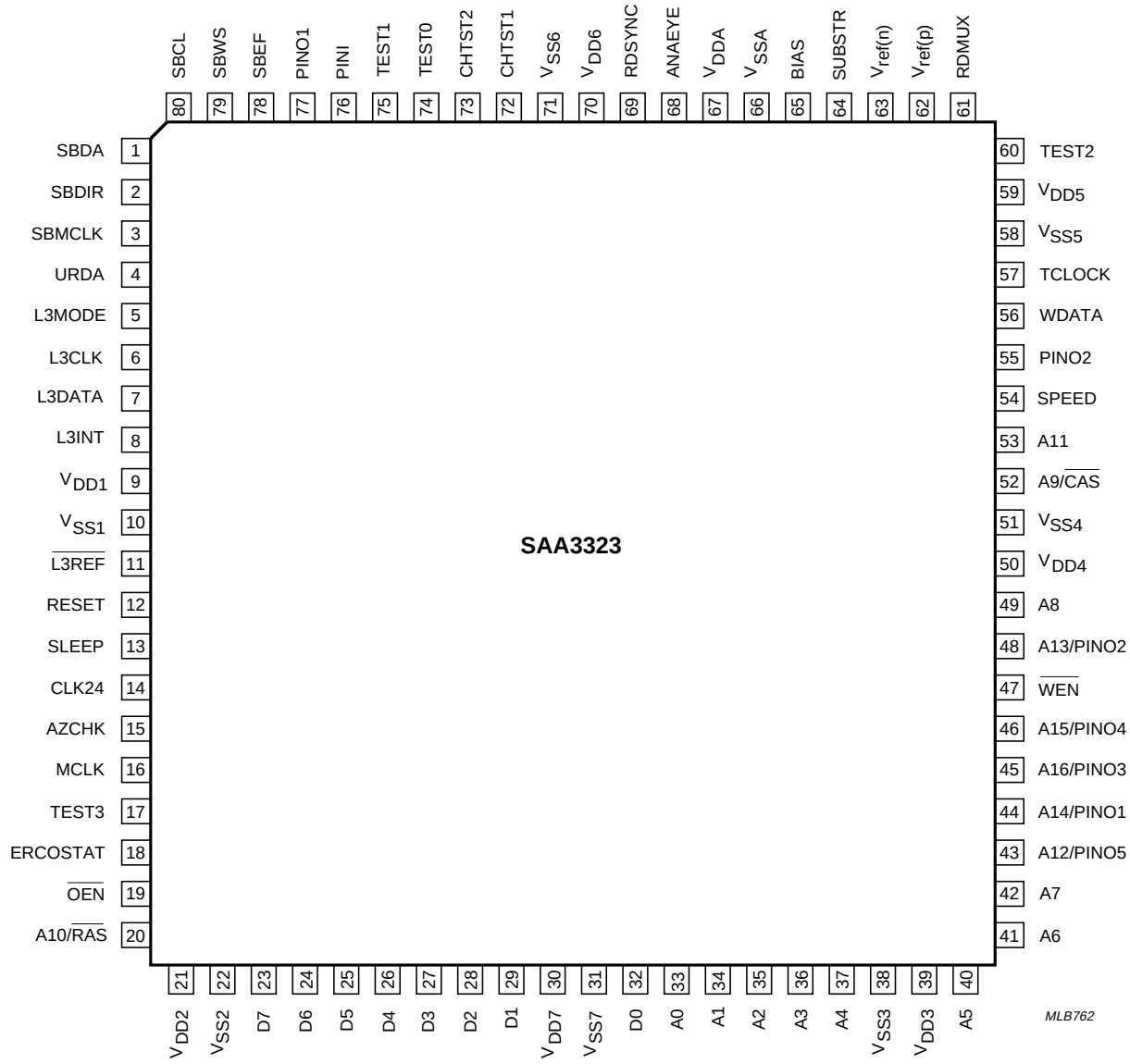


Fig.2 Pin configuration (SOT315-1; TQFP80).

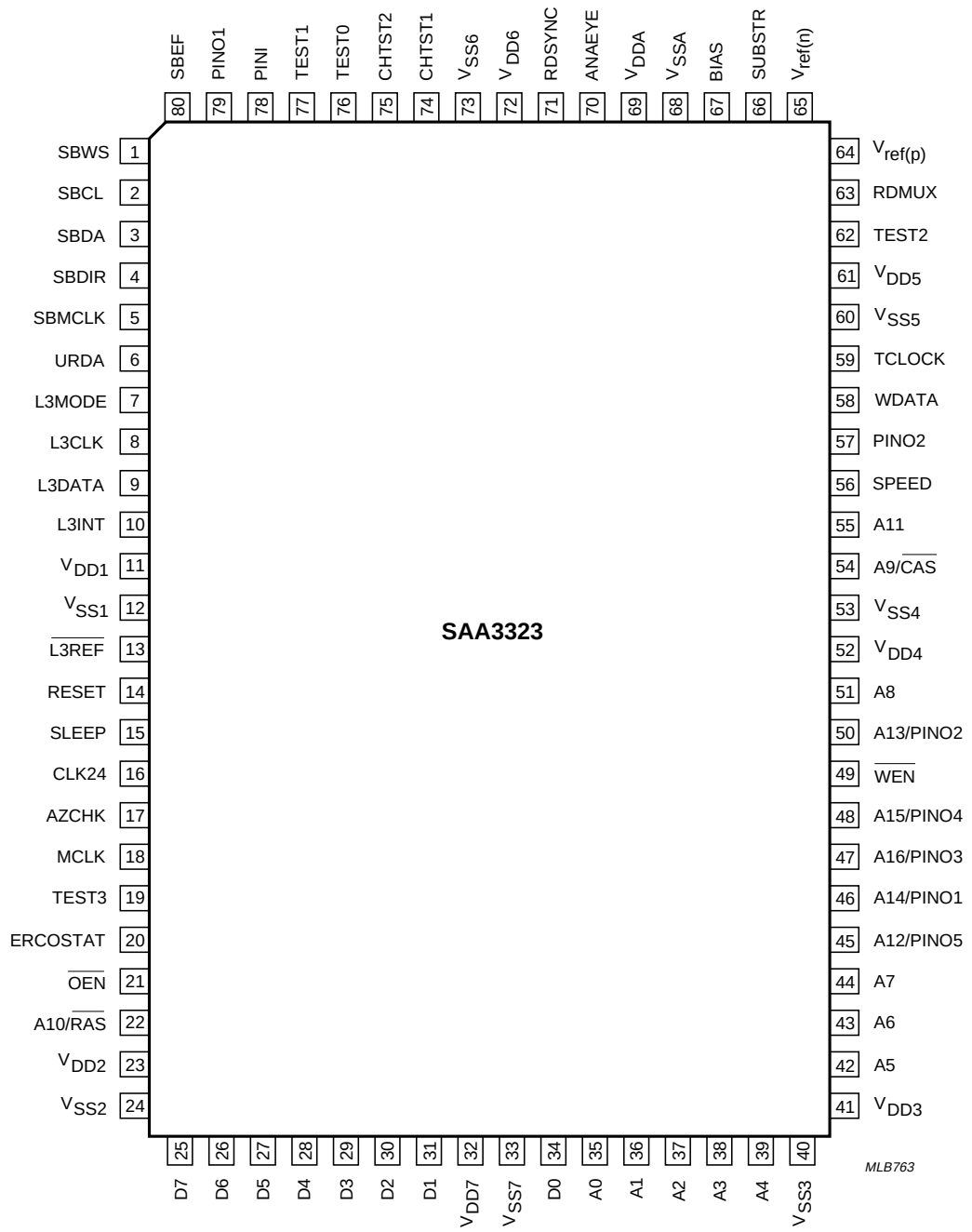


Fig.3 Pin configuration (SOT318-2; QFP80).

FUNCTIONAL DESCRIPTION

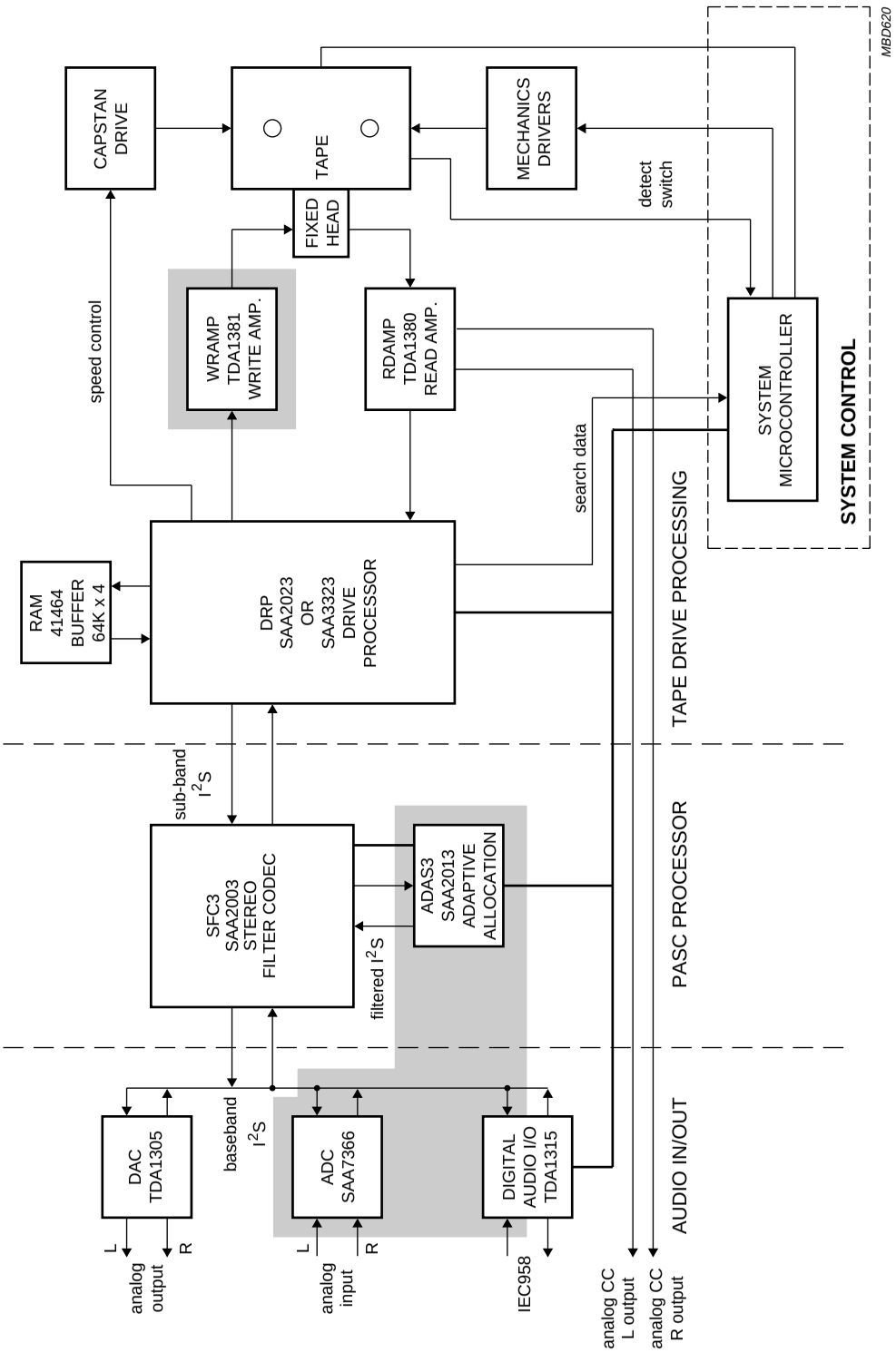


Fig.4 DCC system block diagram.

A simplified block diagram of the SAA3323 is shown in Fig.1.

DCC drive processing

The SAA3323 provides the following functions for the DCC drive processing.

PLAYBACK MODES

- Analog-to-digital conversion
- Tape channel equalization
- Tape channel data and clock recovery
- 10-to-8 demodulation
- Data placement in system RAM
- C1 and C2 error correction decoding
- Interfacing to sub-band serial PASC interface
- Interfacing to microcontroller for SYSINFO and AUX data
- Capstan control for tape deck.

RECORD MODES

- Interfacing to sub-band serial PASC interface
- C1 and C2 error correction encoding
- Formatting for tape transfer
- 8-to-10 modulation
- Interfacing to microcontroller for SYSINFO and AUX data
- Capstan control for tape deck, programmable by microcontroller.

SEARCH MODE

- Detection and interpretation of AUX envelope information
- AUX envelope counting
- Search speed estimation.

Tape Formatting and Error (TFE) correction module

The TFE module has 3 basic modes of operation as shown in Table 1.

Table 1 Basic modes of TFE module.

MODE	EXPLANATION
DPAP	audio and SYSINFO (main data) play; AUX play
DPAR	audio and SYSINFO (main data) play; AUX record
DRAR	audio and SYSINFO (main data) record; AUX record

TFE REGISTERS

The TFE module has 8 writable and 5 readable registers that are accessible via the L3 interface, one write register (CMD) and four read registers (STATUS0 to STATUS3) which are directly addressable, the other registers are indirectly addressable via commands sent to the CMD register. The registers are named as shown in Table 2.

Table 2 TFE register names.

REGISTER NAME	READ/WRITE
CMD	W
STATUS0	R
STATUS1	R
STATUS2	R
STATUS3	R
SET0	W
SET1	W
SET2	W
SET3[1]	W
SPDDTY	W
BYTCNT	W
RACCNT	W
SPEED	R

Note

1. The 4 LSBs of register ‘SET3’ set RAM type (RType) and RAM timing (RTim). See Table 3.

   For normal operation the 4 MSBs of register ‘SET3’ should be logic 0.

Table 3 RAM settings by register SET3.

RAM	REGISTER SET3
RTYPE 0	bit 0
RTYPE 1	bit 1
RTim 0	bit 2
RTim 1	bit 3

TFE DATA STREAMS

The TFE module has three read/write data streams that are accessible via the L3 interface and they are shown in Table 4.

Table 4 TFE data streams.

DATA STREAM NAME	READ/WRITE
SYSINFO	R/W
AUXINFO	R/W
Scratch pad RAM	R/W

TFE 'COMMANDS'

These are the commands that need to be sent to the TFE in order to access the indirectly accessible registers and the data streams, see Table 5.

Table 5 TFE commands.

NAME	COMMAND BYTE								EXPLANATION
	7	6	5	4	3	2	1	0	
RDSPEED	0	0	0	0	0	0	0	0	read SPEED register
LDSET0	0	0	0	1	0	0	0	0	load new TFE settings register 0
LDSET1	0	0	0	1	0	0	0	1	load new TFE settings register 1
LDSET2	0	0	0	1	0	0	1	0	load new TFE settings register 2
LDSET3	0	0	0	1	0	0	1	1	load new TFE settings register 3
LDSPDDTY	0	0	0	1	0	1	0	1	load SPDDTY register
LDBYTCNT	0	0	0	1	0	1	1	1	load BYTCNT register
LDRACCNT	0	0	0	1	1	0	0	0	load RACCNT register
RDAUX	0	0	1	0	0	0	0	0	read AUXILIARY information
RDSYS	0	0	1	0	0	0	0	1	read SYSINFO
RDDRAC	Y	Z	1	0	0	0	1	0	read RAM data bytes (8 bits) from quarter YZ
RDWDRAC	Y	Z	1	0	0	0	1	1	read RAM data words (12 bits) from quarter YZ
WRAUX	0	0	1	1	0	0	0	0	write AUXILIARY information
WRSYS	0	0	1	1	0	0	0	1	write SYSINFO
WRDRAC	Y	Z	1	1	0	0	1	0	write RAM data bytes (8 bits) to quarter YZ
WRWDRAC	Y	Z	1	1	0	0	1	1	write RAM data words (12 bits) to quarter YZ

Digital equalizer module

The digital equalizer module has 2 basic modes of operation as shown in Table 6.

Table 6 Basic modes of equalizer module.

MODE	EXPLANATION
Play	main data and AUX channels are equalized
Search	only AUX channel is processed; AUX envelope information is processed

DIGITAL EQUALIZER REGISTERS

The digital equalizer module has 9 write only, 3 read only and 1 read/write register(s) that are accessible via the L3 interface, one write register (CMD) and 2 read registers (STATUS0 and STATUS1) which are directly addressable, the other registers are indirectly addressable via commands sent to the CMD register. The registers are named as shown in Table 7.

Table 7 Digital equalizer register names.

REGISTER NAME	READ/WRITE
CMD	W
STATUS0	R
STATUS1	R
COEFCNT	W
FCTRL	W
CHT1SEL	W
CHT2SEL	W
ANAEYE	W
AEC	R/W
SSPD	R
INTMASK	W
DEQ2SET	W
CLKSET	W

DATA STREAMS

The digital equalizer module has one write only and one read only data stream that are accessible via the L3 interface and they are shown in Table 8.

Table 8 Digital equalizer data streams.

DATA STREAM NAME	READ/WRITE
FIR coefficients to buffer bank	W
FIR coefficients from active bank	W

DIGITAL EQUALIZER "COMMANDS"

These are the commands that need to be sent to the digital equalizer in order to access the indirectly accessible registers and the data streams.

Table 9 Digital equalizer commands.

NAME	COMMAND BYTE								EXPLANATION
	7	6	5	4	3	2	1	0	
WRCOEF	0	0	1	1	0	0	0	0	write FIR coefficients to the digital equalizer buffer bank
RDCOEF	0	0	1	0	0	0	0	0	read FIR coefficients from the digital equalizer active bank
LDCOEFCNT	0	0	0	1	0	0	1	1	load FIR coefficient counter
LDFCTRL	0	0	0	1	0	1	0	0	load filter control register
LDT1SEL	0	0	0	1	0	1	1	0	load CHTST1 pin selection register
LDT2SEL	0	0	0	1	0	1	1	1	load CHTST2 pin selection register
LDTAEYE	0	0	0	1	1	0	0	0	load ANAEYE channel selection register
LDAEC	0	0	0	1	1	0	0	1	load AEC counter
RDAEC	0	0	1	0	0	0	1	0	read AEC counter
RDSSPD	0	0	1	0	0	1	0	0	read SEARCH speed register
LDINTMSK	0	0	0	1	0	0	1	0	load interrupt mask register
LDDEQ3SET	0	0	0	1	0	0	0	0	load digital equalizer settings register
LDCLKSET	0	0	0	1	0	0	0	1	load PLL clock extraction settings register

Table 10 Filter control register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	µCS[1]	SH1	SH0	Reserved	
Default	0	0	0	0	1	0	1	1

Note

1. µCS is a microcontroller controlled coefficient bank switch. This causes the filter coefficients to be activated at a time that is safe for the digital equalizer, i.e. at the end of the FIR program and that the complete value of coefficient number 9 has been received.

Table 11 SH1 and SH2 (FIR output scaling).

SH		EFFECT ON FIR OUTPUT
1	**0**	
0	0	FIR mod 256
0	1	$\frac{FIR}{2}$ mod 256
1	0	$\frac{FIR}{4}$ mod 256
1	1	$\frac{FIR}{8}$ mod 256

Transfer of FIR coefficients

For the main data channels (tracks 0 to 7) there are 10 coefficients (taps) each of 8 bits, where all of the data channels make use of the same coefficients. The addresses for the main data coefficients 0 to 9 are 0 to 9_{dec} respectively.

There are ten coefficients (taps) each of 8 bits for the aux channel (CHAUX). The addresses for the auxiliary coefficients 0 to 9 are 16 to 25_{dec} respectively.

There are 2 banks of coefficients for both the aux and the main data channels, namely the ‘buffer’, and the ‘active’ banks. The microcontroller writes only to the ‘buffer’ banks, and reads only from the ‘active’ banks.

The microcontroller can poll the digital equalizer status bit BKSW to see when the switch occurs. BKSW starts life LOW, goes HIGH as a result of the bank switching and goes LOW as result of the complete value of a main data coefficient being received by the digital equalizer.

The microcontroller sets μCS HIGH before sending the new set of aux or main data coefficients, the digital equalizer resets it once the bank switch occurs.

The actual FIR coefficients that are used are a function of the tape head, read amplifier and type of tape (i.e. pre-recorded or own recorded) used, such information is outside of the scope of this data sheet.

Coefficient address counter (COEFCNT)

This 5 bit counter is used to point to the FIR coefficient to be transferred to or from the digital equalizer.

Table 12 Coefficient address counter.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	CC4	CC3	CC2	CC1	CC0
Default	0	0	0	0	0	0	0	0

Pin explanations and interfacing to other hardware

RESET

This is an active HIGH input which resets the SAA3323 and brings it into its default mode, DPAP. This reset does not affect the contents of the FIR filter coefficients in the digital equalizer. This should be connected to the system reset, which can be driven by the microcontroller. The duration of the reset pulse should be at least 15 μs.

SLEEP

This pin is an active HIGH input which puts the SAA3323 in a low power consumption SLEEP mode. This pin should be connected to the DCC SLEEP signal, which can be driven by the microcontroller. The CLK24 clock may be stopped and the VREFP and VREFN inputs brought to ground while the SAA3323 is in ‘sleep’ mode to further reduce power consumption. When recovering from sleep mode, the SLEEP pin should be taken LOW and the SAA3323 reset.

CLK24

This is the 24.576 MHz clock input and should be connected directly to the SAA2003 (pin CLK24).

Sub-band serial PASC interface connections

The timing for the sub-band serial PASC interface is given in Figs 5 to 7.

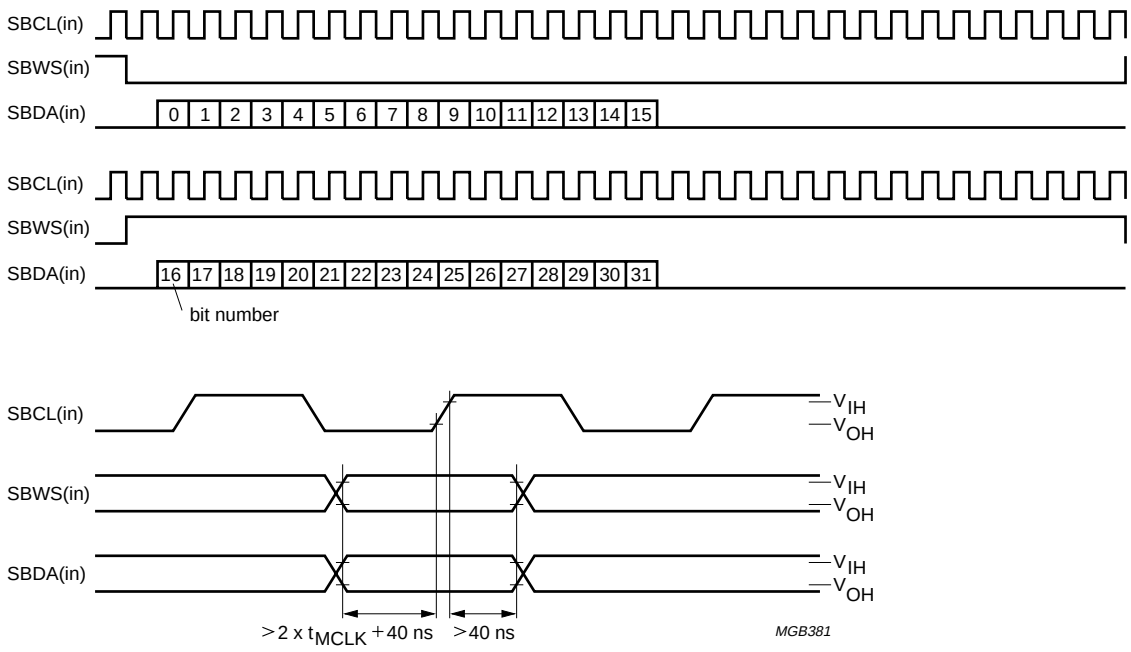


Fig.5 Sub-band serial PASC interface timing; DRAR mode.

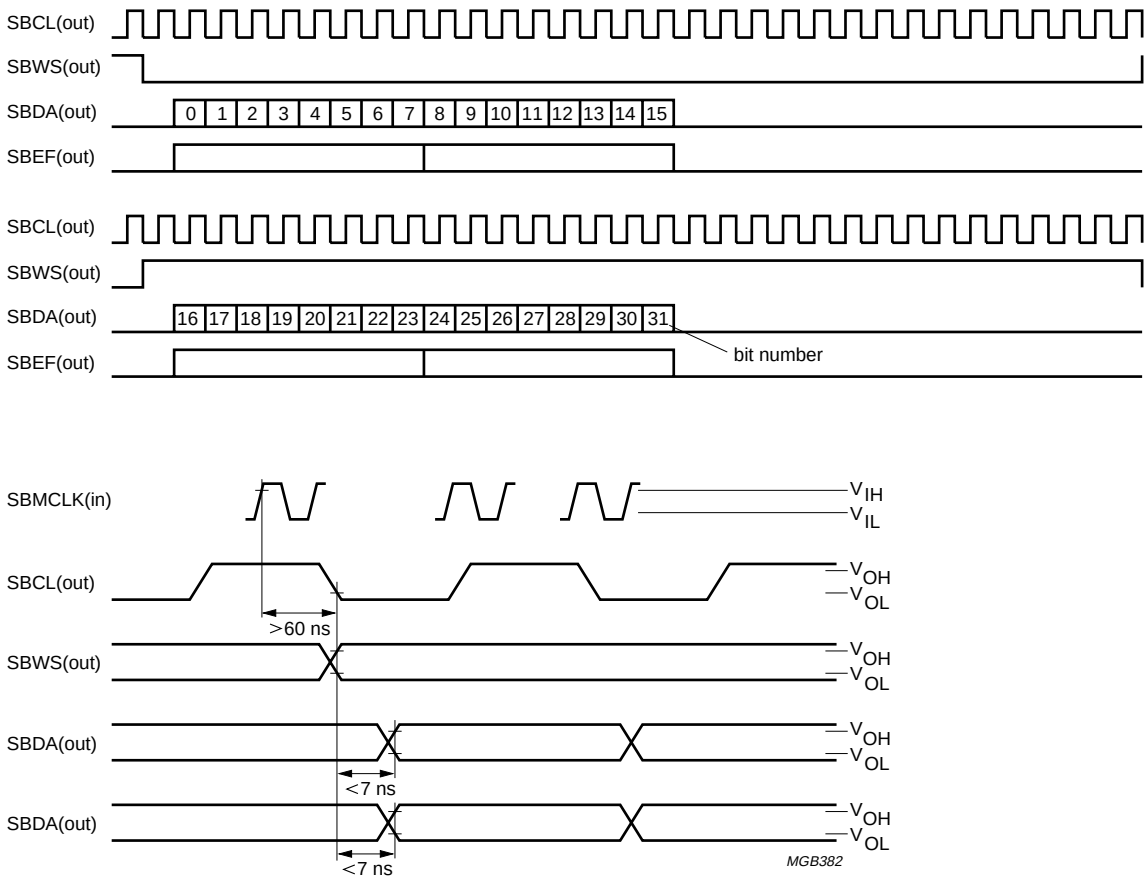


Fig.6 Sub-band serial PASC interface timing in play modes; DRPMAS = logic 1.

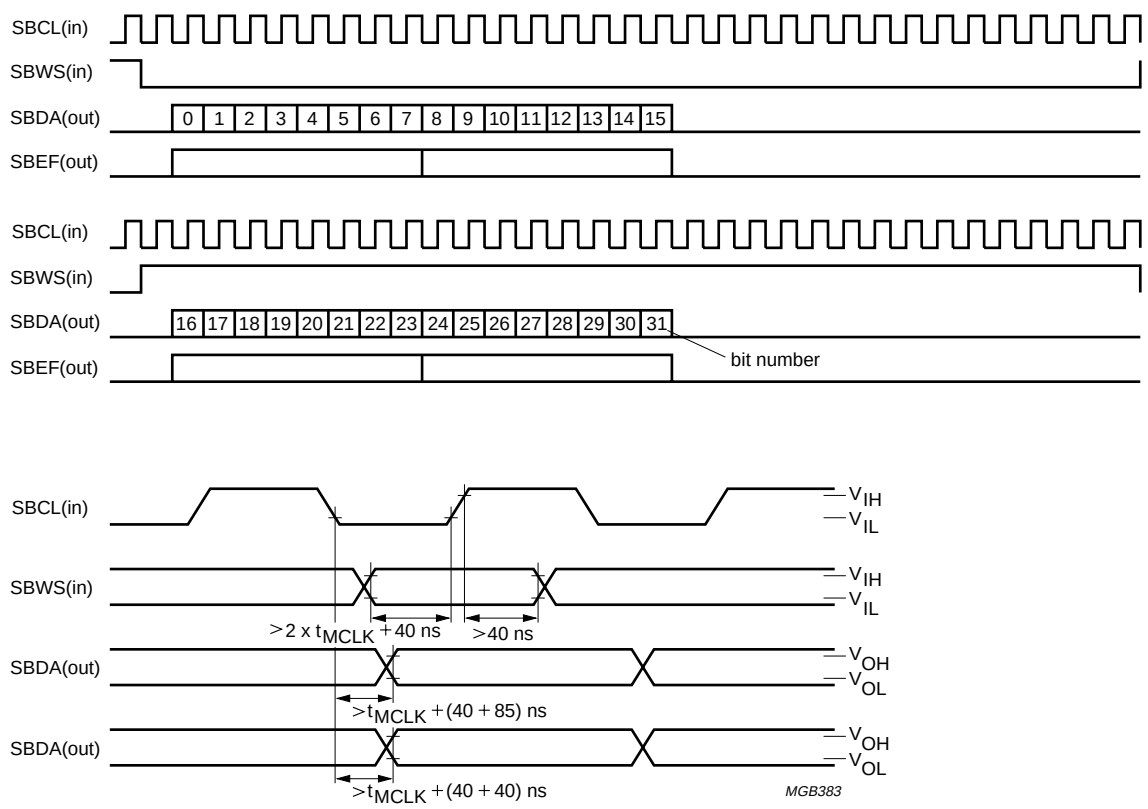


Fig.7 Sub-band serial PASC interface timing in play modes; DRPMAS = logic 0.

SBMCLK

This is the sub-band master clock input for the sub-band serial PASC interface. The frequency of this signal is nominally 6.144 MHz. When the SAA3323 is used with SAA2003 this pin is tied to ground, and the TFE settings bit 'DRPMAS' set to logic 1.

SBDIR

This output pin is the sub-band serial PASC bus direction signal, it indicates the direction of transfer on the sub-band serial PASC bus. This pin connects directly to the SBDIR pin on the SAA2003. The transfer directions are shown in Table 13.

Table 13 PASC bus transfer directions.

SBDIR	DIRECTION
1	SAA3323 to SAA2003 transfer (audio play)
0	SAA2003 to SAA3323 transfer (audio record)

SBCL

This input/output pin is the bit clock line for the sub-band serial PASC interface to the SAA2003. When used with SAA2003 this pin is input only. It has a nominal frequency of 768 kHz.

SBWS

This input/output pin is the word select line for the sub-band serial PASC interface to the SAA2003. When used with SAA2003 this pin is input only. It has a nominal frequency of 12 kHz.

SBDA

This input/output pin is the serial data line for the sub-band serial PASC interface to the SAA2003.

SBEF

This active HIGH output pin is the error-per-byte line for the sub-band serial PASC interface to the SAA2003.

URDA

This active HIGH output pin indicates that the main data (audio), the SYSINFO and the AUXILIARY data are NOT usable, regardless of the state of the corresponding reliability flags. The state of this pin is reflected in the URDA bit of STATUS byte 0, which can be read by the microcontroller. This pin should be connected directly to the URDA pin of the SAA2003. URDA goes active as a result of a reset, a mode change from mode DRAR to DPAP, or if the SAA3323 has had to re-synchronize with the incoming data from tape.

The position of the first sub-band serial PASC bytes in a tape frame is shown in Figs 8 and 9.

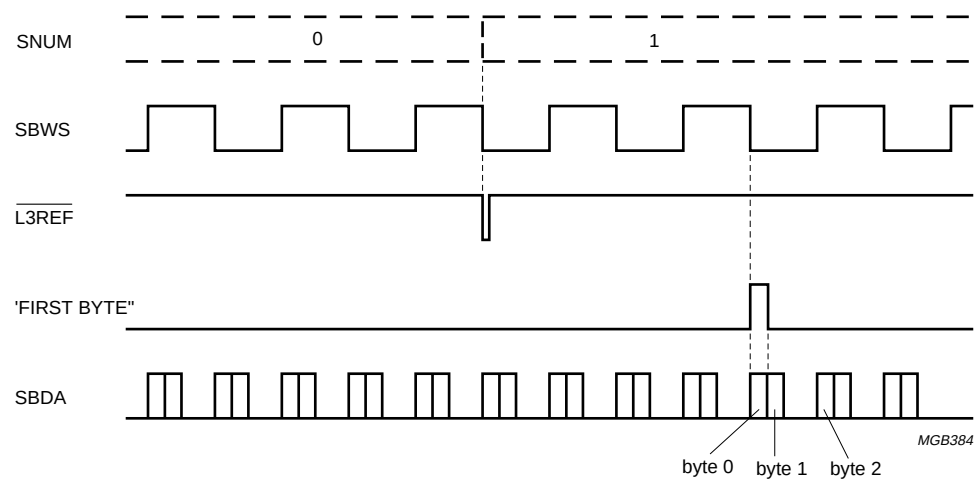


Fig.8 Position of first sub-band serial PASC bytes in a tape frame in DPAP/DPAR mode.

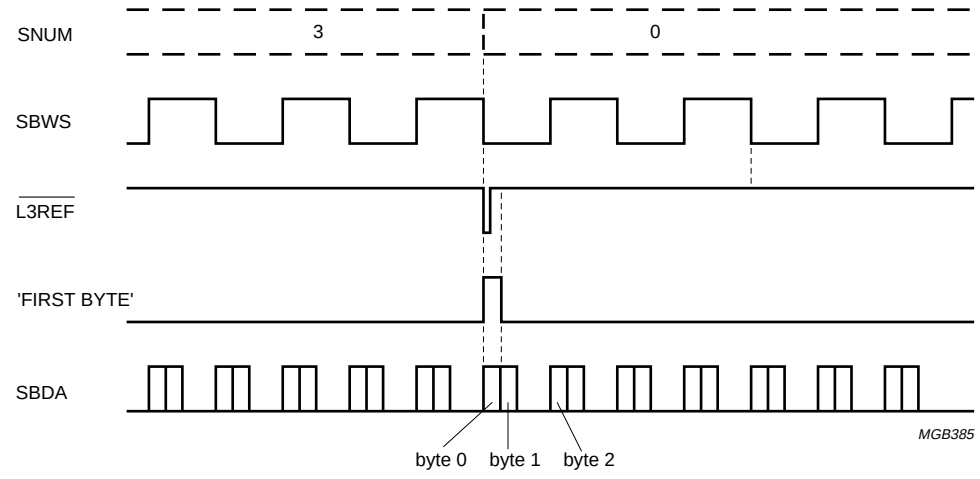


Fig.9 Position of first sub-band serial PASC bytes in a tape frame in DRAR mode.

RAM connections

The SAA3323 has been designed to operate with DRAMs and SRAMs. Suitable DRAMs are 64K × 4-bit or 256K × 4-bit configurations operating in page mode, with an access time of 80 to 100 ns. The timing for read, write and refresh cycles for DRAMs is shown in Figs 10 to 12. The timing for SRAMs is shown in Figs 13 to 19.

For fast SRAMs: (these values are subject to verification during characterization in). The conditions (most critical at the required V_{DD}) are shown in Table 14.

Table 14 Fast SRAM conditions.

CONDITION(1)	TIME
Write pulse duration	$t_W \leq 140$ ns
Data set-up to rising $\overline{WEN}$	$t_{su} \leq 72$ ns
Write cycle time	$T_{cy} \leq 200$ ns
Read access time	$t_{ACC} \leq 240$ ns

Note

1. The SAA3323 should work in: RType = ‘01’; RTim = ‘00’ mode.

A9/$\overline{CAS}$

When SAA3323 is used with SRAM this output pin is Address line 9, and should be connected directly to the corresponding address pin on the SRAM. When SAA3323 is used with DRAM this output pin is the column address strobe (active LOW), it connects directly to the column address strobe pin of the DRAM.

A10/$\overline{RAS}$

When SAA3323 is used with SRAM this output pin is Address line 10, and should be connected to the corresponding address pin of the SRAM. When SAA3323 is used with DRAM this output pin is the row address strobe (active LOW), it connects directly to the row address strobe pin of the DRAM.

$\overline{OEN}$

This output pin is the output enable (active LOW) for the RAM, it connects directly to the output enable pin of the RAM.

$\overline{WEN}$

This output pin is the write enable (active LOW) for the RAM, it connects directly to the write enable pin of the RAM.

A0 TO A8

When SAA3323 is used with DRAM these output pins are the multiplexed column and row address lines. When the 64K × 4-bit DRAM is used, pins A0 to A7 should be connected to the DRAM address input pins, and pin A8 should be left unconnected. When using the 256K × 4-bit DRAM the address pins A0 to A8 should be connected to the address input pins of the DRAM.

When SAA3323 is used with SRAM these are the lower address pins and should be connected directly to the SRAM address pins.

A11

This output pin is the an address pin for the SRAM and when SRAM is used they should be connected directly to the address pins of the SRAM. When DRAM is used this pin should not be connected.

A10 AND A12 TO A16

These output pins are the upper address pins for the SRAM and when SRAM is used they should be connected directly to the address pins of the SRAM. When DRAM is used or when the small SRAM is used all or some of these pins become available as Port expander outputs.

Table 15 Port expander outputs.

PIN NAME	PIN		PORT EXPANDER OUTPUT	CONDITIONS
	QFP80	TQFP80		
A14/PINO1	46	44	PINO1	RType = 00
A13/PINO2	50	48	PINO2	RType = 00
A16/PINO3	47	45	PINO3	RType = 00 or RType = 01
A15/PINO4	48	46	PINO4	RType = 00 or RType = 01
A12/PINO5	45	43	PINO5	RType = 00

D0 TO D3

When SAA3323 is used with SRAM these I/O pins form the lower nibble of the data bus connection to the RAM, and should be connected to the corresponding data I/O pins of the SRAM. When SAA3323 is used with DRAM these input/output pins are the data lines for the RAM, they should be connected directly to the DRAM data I/O pins.

D4 TO D7

These input/output pins are the upper nibble of the data bus for use with SRAM, and when SRAM is being used they should be connected directly to the corresponding SRAM I/O pins.

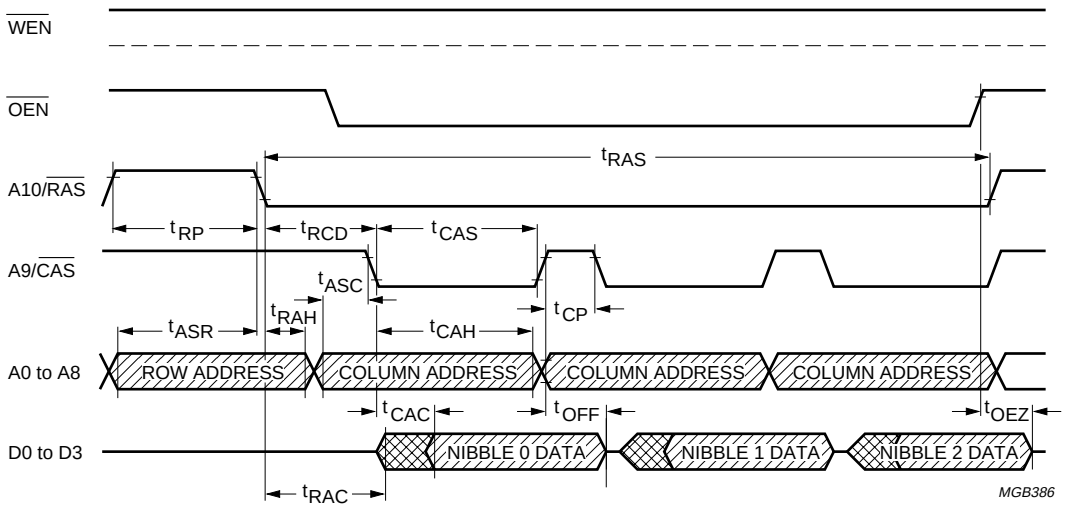


Fig.10 DRAM read cycle timing.

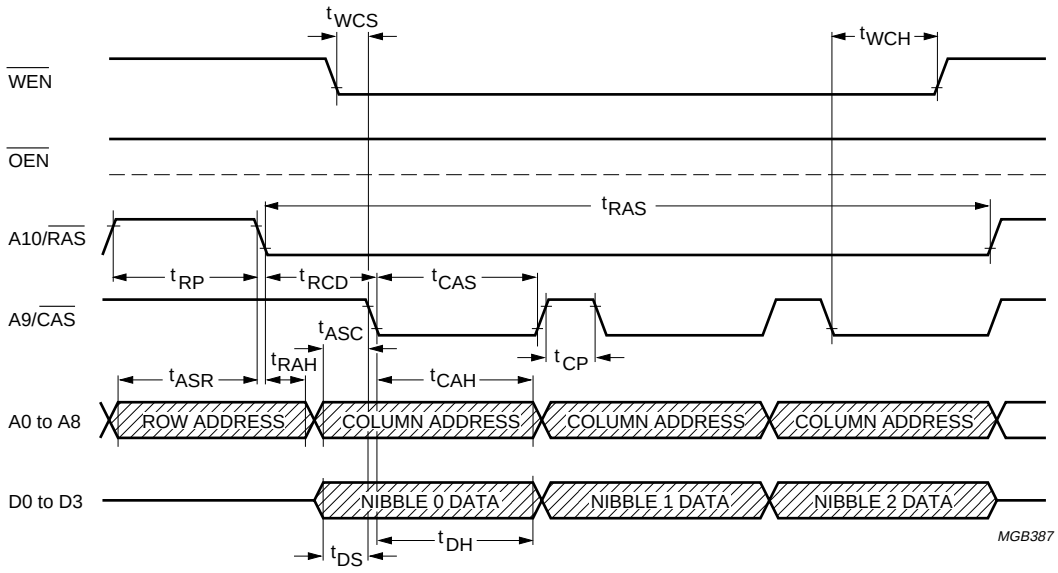


Fig.11 DRAM write cycle timing.

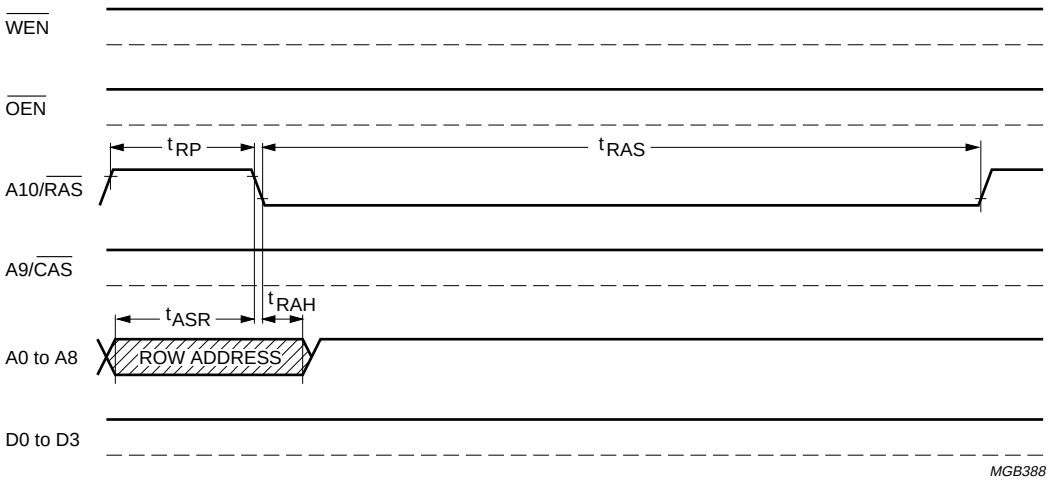


Fig.12 DRAM refresh cycle timing.

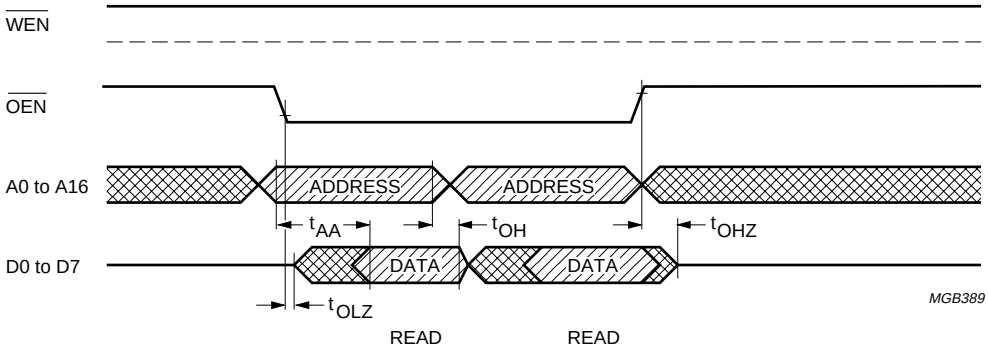


Fig.13 Fast SRAM read cycle timing.

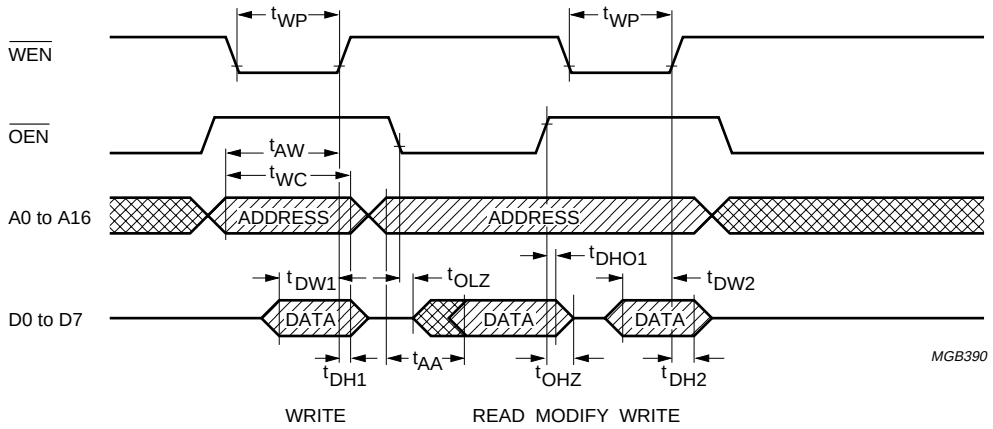


Fig.14 Fast SRAM write cycle timing; RTim = “00”.

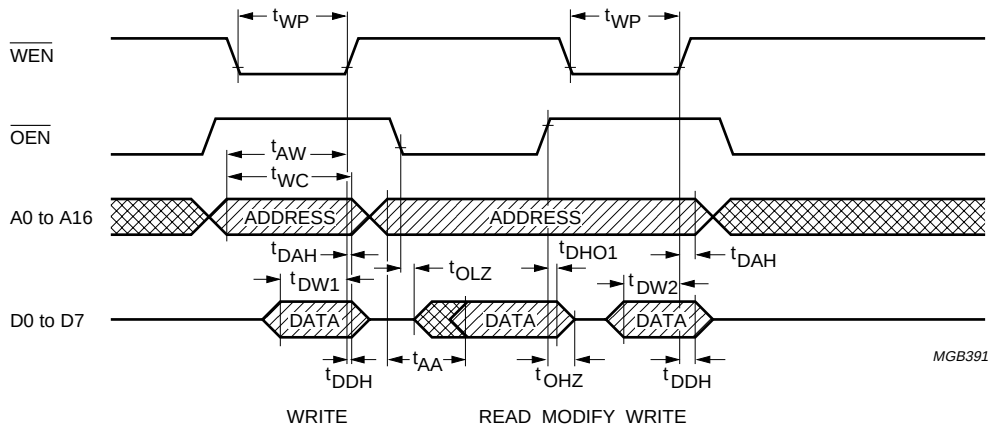


Fig.15 Fast SRAM write cycle timing; RTim = “01”.

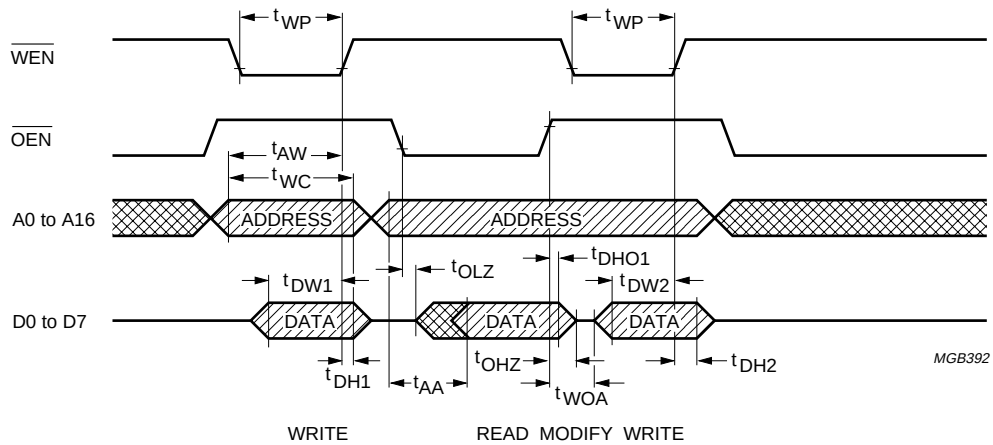


Fig.16 Fast SRAM write cycle timing; RTim = “10”.

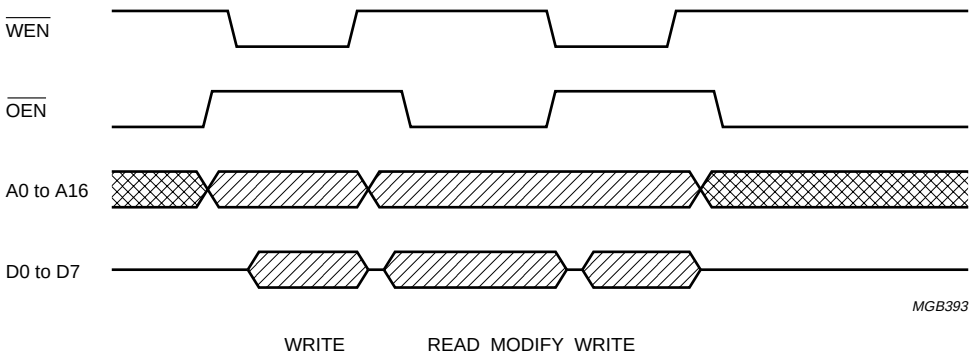


Fig.17 Fast SRAM write cycle timing; RTim = “11”.

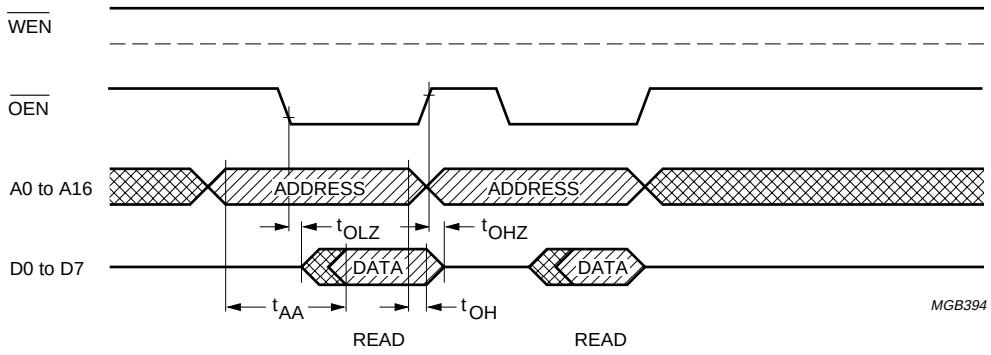


Fig.18 Slow SRAM read cycle timing.

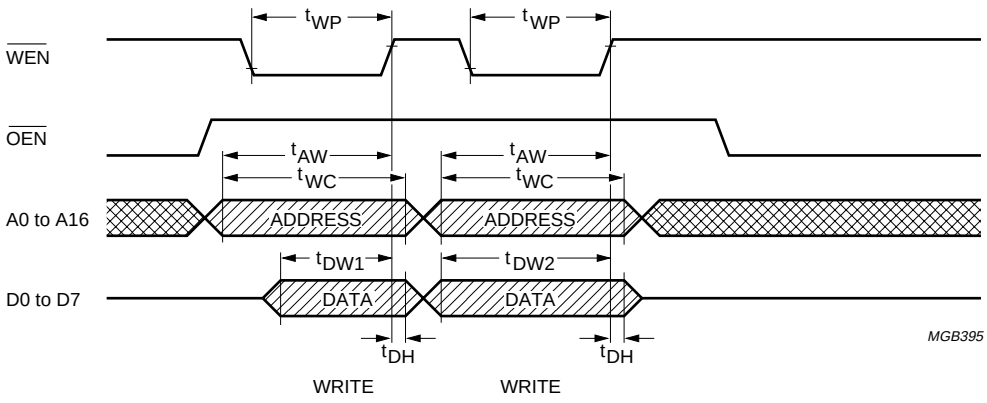


Fig.19 Slow SRAM write cycle timing.

Table 16 Timing values for Figs 10 to 12.

SYMBOL	VALUE (ns)
t_{RP}	≥110
t_{RAS}	≥510
t_{RCD}	≥70
t_{CP}	≥30
t_{CAS}	≥100
t_{ASR}	≥100
t_{RAH}	≥25
t_{ASC}	≥30
t_{CAM}	≥100
t_{DS}	≥25
t_{DH}	≥100
t_{WCS}	≥30
t_{WCH}	≥100
t_{RAC}	≤160
t_{CAC}	≤80

Table 17 Timing values for Figs 13 to 17.

SYMBOL	VALUE (ns)
t_{WP}	≥140
t_{AW}	≥180
t_{WC}	≥200
t_{DW}	≥72
t_{DM}	≥25
t_{AA}	≤240
t_{HC}	≥250

Table 18 Timing values for Figs 18 and 19.

SYMBOL	VALUE (ns)
t_{WP}	≥225
t_{AW}	≥260
t_{WC}	≥300
t_{DW}	≥140
t_{DM}	≥25
t_{AA}	≤280

Read/write connections

TCLOCK

This output pin is the 3.072 MHz clock output for the read and write amplifiers, it should be connected directly to the WCLOCK pin of the write amplifier and to the RDCLK pin of the read amplifier.

RDMUX

This input pin carries the time multiplexed analog tape channel signals from the read amplifier.

$V_{ref(n)}$ AND $V_{ref(p)}$

These are the lower and upper voltage reference inputs for the ADC in the digital equalizer part of SAA3323.

BIAS

This pin defines a bias current for the ADC. It should be connected to the analog supply voltage V_{DDA} via a 47 kΩ resistor.

RDSYNC

This output line provides synchronization information for the read Amplifier data transfers. The relationship between TCLOCK, RDSYNC and the channel information carried by the RDMUX line is given in Fig.20. This pin should be connected directly to the RDSYNC pin of the read amplifier. When the digital equalizer in SAA3323 is in search mode this pin will be HIGH ensuring that only the AUX channel is processed by the SAA3323.

WDATA

This output pin is the multiplexed data and control line for the write amplifier. Figure 21 shows the manner in which this information is multiplexed onto WDATA. The WDATA pin should be connected directly to the WDATA pin of the write amplifier.

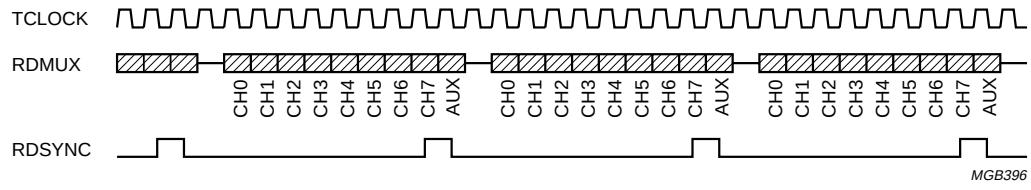


Fig.20 RDMUX, RDSYNC and TCLOCK timing.

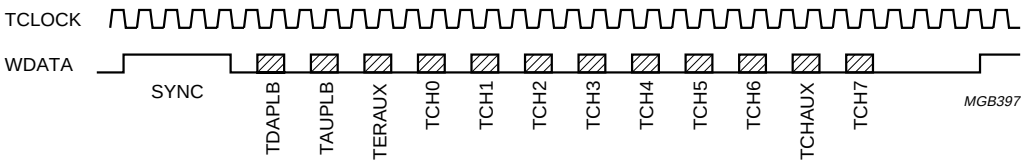


Fig.21 WDATA and TCLOCK timing.

Tape deck capstan control connections

SPEED

This pin outputs a pulse width modulated signal that may be used for controlling the tape capstan of the deck.

Operation of the SPEED control signal

Table 19 gives the sources that determine the duty factor of the SPEED signal. Note that the 3-state SPEED output may be put into high-impedance state by programming the TFE setting by bit HiZSpd.

Table 19 SPEED signal duty factor.

MODE	µCSPD	SOURCE FOR SPEED DUTY FACTOR
DPAP	0	tape(1)
DPAP	1	µC(2)
DPAR	0	tape(1)
DPAR	1	µC(2)
DRAR	0	50%(3)
DRAR	1	µC(2)

Notes

1. “Tape” means that the duty factor has been calculated from the played back main data tape signal. When tape is the source for the duty factor of the SPEED signal, the type of regulation can be chosen with the TFE settings bits EnFReg and SeINBand.
2. “µC” means that the microcontroller programs the duty factor via the SPDDTY register.
3. “50%” means that the duty factor is fixed at 50%.

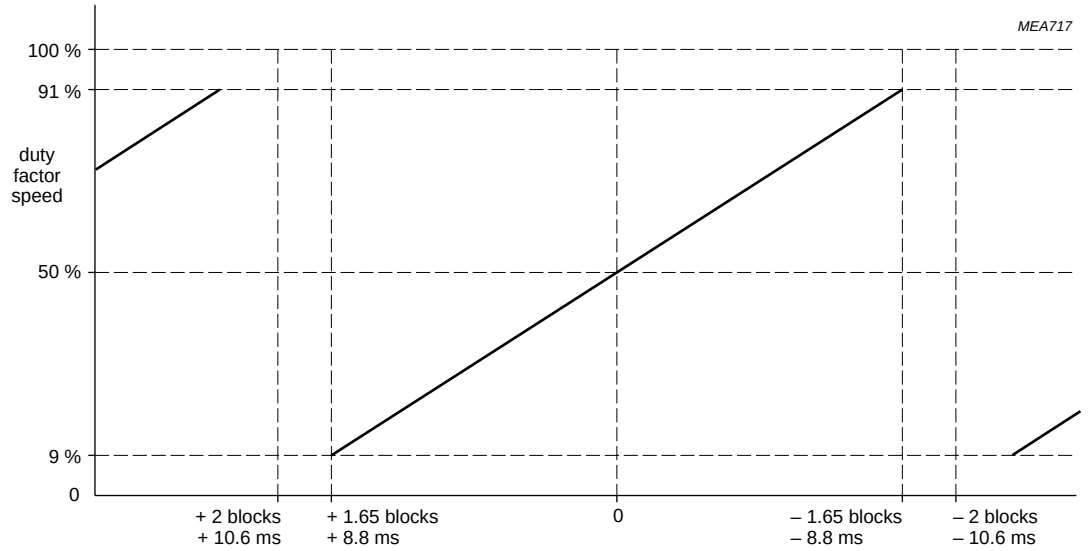


Fig.22 SPEED regulation duty factor as a function of phase characteristic.

If EnFReg is programmed ‘LOW’ then there is phase regulation of the capstan speed. The period of the pulse width modulated SPEED signal is 41.66 µs. The SAA3323 performs a new calculation to determine the duty factor of SPEED once every 21.33 ms, giving a sampling rate of approximately 46.9 Hz. This calculation is basically a phase comparison between the incoming Main Data tape frame and an internally generated reference. The SPEED duty factor as a function of phase characteristic is shown in Fig.22. As shown the duty factor increases monotonously from approximately 9% when the incoming Main Data tape frame is 1.65 tape blocks (8.8 ms) too early up to 91% when it is 1.65 tape blocks (8.8 ms) too late. Outside of a ±2 tape blocks range the pulse width characteristic overflows and repeats itself forming a sawtooth pattern. The SAA3323 has an internal buffer of ±8.8 ms outside of which the phase information is invalid.

If EnFReg is programmed ‘HIGH’ then the above description is over-ridden with frequency information. If the incoming main data bit rate deviation from the nominal 96000 bits/s rate is less than the Phase Only Threshold (POT) then the control is as described above in the phase control description. If the deviation is more than the Frequency Only Threshold (FOT) then the SPEED information is gated with the phase information resulting in the SPEED signal being continuously HIGH or LOW while the condition continues. If the deviation is between the POT and the FOT then the frequency information is gated with the Phase information for 50% of the time.

The deviation thresholds POT and FOT are programmable via the TFE settings bit SeINBand.

Table 20 POT and FOT deviation thresholds.

SeINBand	POT (DEVIATION FROM NOMINAL)	FOT (DEVIATION FROM NOMINAL)
0	±6%	±9%
1	±3%	±4.5%

If SLEEP is 'HIGH' then the state of the SPEED signal will be the state that it was in just before the SAA3323 went into sleep. Thus if SPEED was HIGH just before sleep it will stay HIGH during sleep. The same applies if it was LOW or if it was in 'high-Z' state. Note that a reset of the SAA3323 will take the SPEED signals out of 'high-Z' state.

Microcontroller connections

$\overline{\text{L3REF}}$

This active LOW output pin indicates the start of a time segment, it goes LOW for 5.2 μs once every 42.66 ms approximately and can be used for generating interrups for the microcontroller. If a re-synchronization occurs then the time between the occurrences van vary. This pin can be connected directly to the interrupt input of the microcontroller.

L3CLK

This input pin is the clock line for the microcontroller interface.

L3DATA

This input/output pin is the serial data line for the microcontroller interface.

L3MODE

This input determines the type of transfer that is occurring between the microcontroller and the SAA3323. If L3MODE is LOW then a device address can be sent by the microcontroller. If L3MODE is HIGH then a data transfer may be occurring.

L3INT

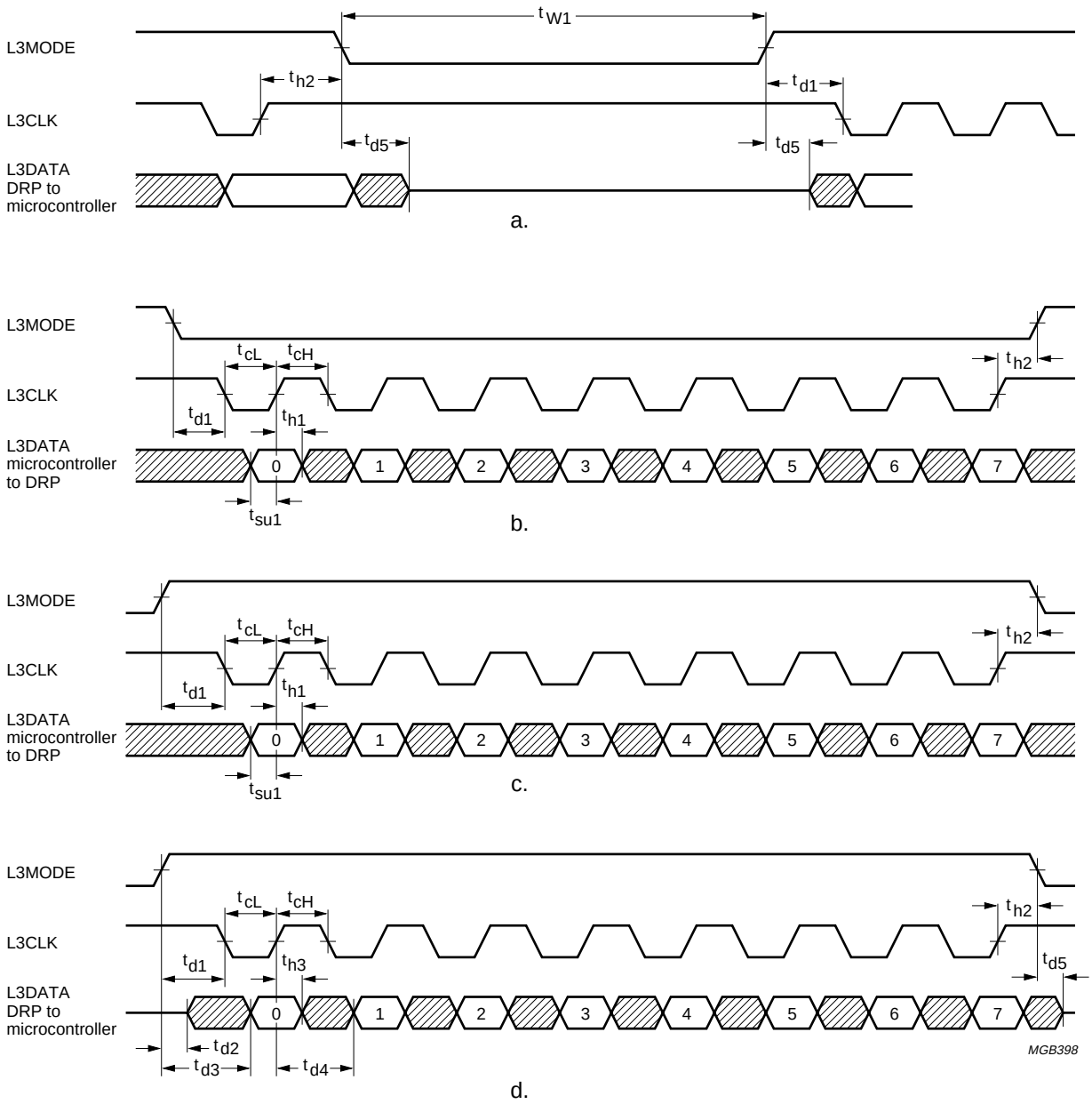
This pin carries interrupts from the digital equalizer module. It can also be programmed to reflect the state of the AENV, LABEL and VIRGIN signals.

Table 21 Timing values for Fig.23.

SYMBOL	TIME[1]
t_{W1}	$T + t_{su\ (L3MODE)} + t_{h\ (L3MODE)}$; $t_{w1} \geq 200$ ns
t_{d1}	$T + t_{su\ (L3MODE)} + t_{h\ (L3CLK)}$; $t_{d1} \geq 200$ ns
t_{h2}	$T + t_{su\ (L3CLK)} + t_{h\ (L3MODE)}$; $t_{h2} \geq 200$ ns
t_{d2}	$T + t_{su\ (L3CLK)} + t_{d\ (L3DATA)}$; $t_{d2} \leq 250$ ns
t_{d5}	$0 \leq t_{d5} \leq 50$ ns
t_{cL}	$T + t_{su\ (L3CLK)} + t_{h\ (L3CLK)}$; $t_{cL} \geq 200$ ns
t_{cH}	$T + t_{su\ (L3CLK)} + t_{h\ (L3CLK)}$; $t_{cH} \geq 200$ ns
t_{su1}	$T + t_{su\ (L3DATA)} + t_{h\ (L3CLK)}$; $t_{su1} \leq 200$ ns
t_{h1}	$T + t_{su\ (L3CLK)} + t_{h\ (L3DATA)}$; $t_{h1} \leq 35$ ns
t_{d3}	$2 \times T + t_{su\ (L3MODE)} + t_{d\ (L3DATA)}$; $t_{d3} \leq 250$ ns
t_{h3}	$T + t_{h\ (L3CLK)} + t_{d\ (L3DATA)}$; $t_{h3} \geq 50$ ns
t_{d4}	$2 \times T + t_{su\ (L3CLK)} + t_{d\ (L3DATA)}$; $t_{d4} \leq 410$ ns
t_{d4}[2]	$3 \times T + t_{su\ (L3CLK)} + t_{d\ (L3DATA)}$; $t_{d4} \leq 575$ ns

Notes

1. T is the period of the master clock on the chip.
2. t_{d4} is the delay time between the last bit of a byte and first bit of the next byte, if no 'halt' is used.



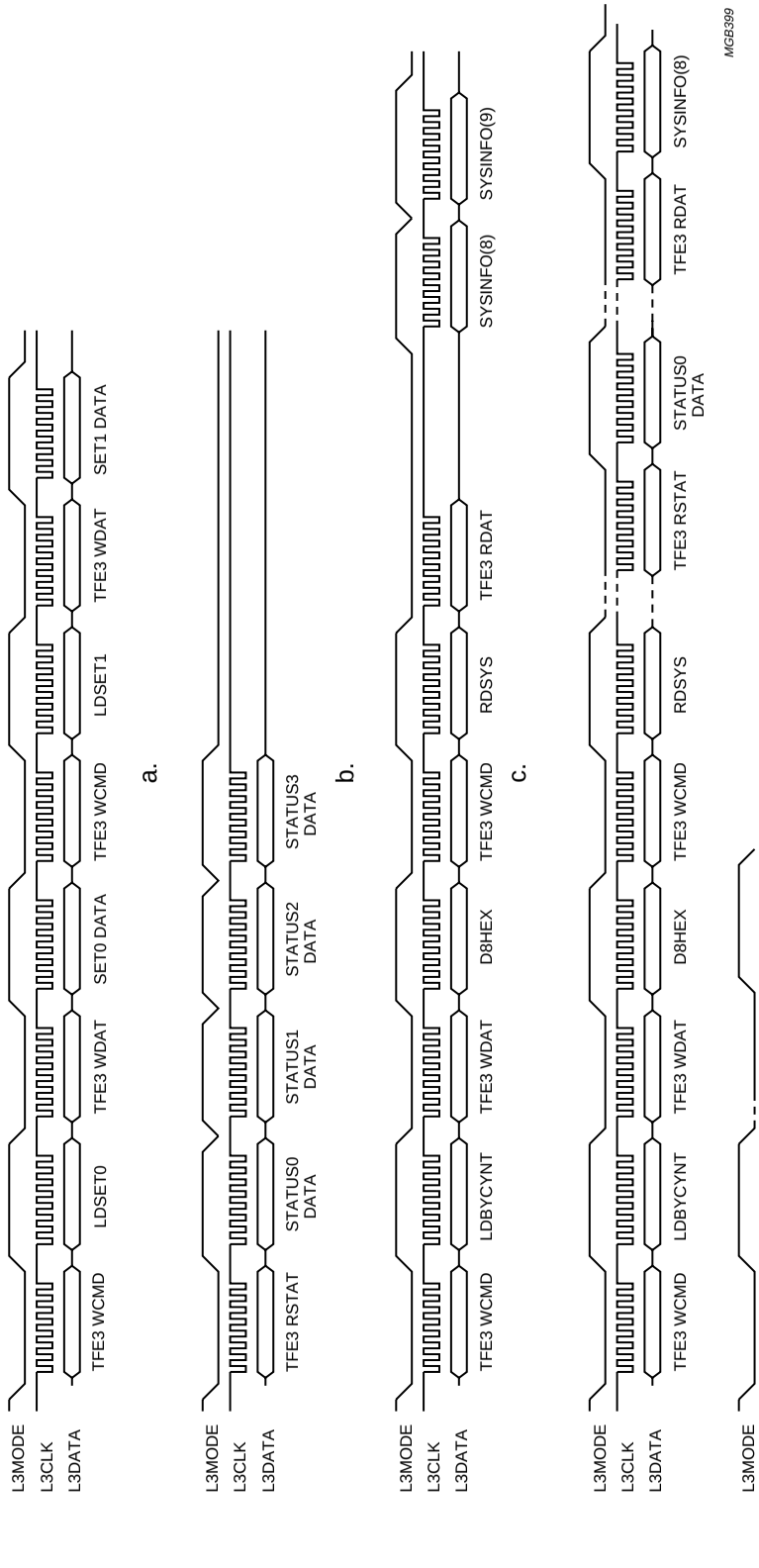
a. Halt mode.

b. Addressing mode.

c. Data mode (transfer from microcontroller to SAA3323).

d. Data mode (transfer from SAA3323 to microcontroller).

Fig.23 L3 interface timing and typical transfers (1).



a. Write settings bytes 0 and 1 to TFE3 part of SAA3323.
b. Read all 4 status bytes from TFE part of SAA3323.
c. Read 2 SYSINFO bytes starting at byte 8 (in high-speed transfer part of program).
d. Read 2 SYSINFO bytes starting at byte 8 (in low-speed transfer part of program).

Fig.24 L3 interface timing and typical transfers (2).

SAA3323 test pins

TEST0 TO TEST3

These input pins are for test only, **do not connect**.

AZCHK

This output pin indicates the occurrence of a tape channel sync symbol on tape channels TCH0 and TCH7, the distance between the pulses for the TCH0 and TCH7 channels gives a measure of the azimuth error between the tape and head alignment. Figure 25 shows the typical timing for this signal.

ERCOSTAT

This output pin can be connected to a symbol error rate measurement system.

Port expansion pins

PINI

This input pin is connected directly to the PINI bit in the status byte 1, it can be read by the microcontroller, and may be used for any CMOS level compatible input signals.

PINO1

This output pin is connected directly to the PINO1 bit of the TFE settings 0 register. The microcontroller can set or reset this pin.

PINO2 TO PINO5

Depending upon the type and the size of system RAM used, some or all of these Port expander output pins may be available, (please see Section “RAM connections” “A10 and A12 to A16” on interfacing to the RAM pins).

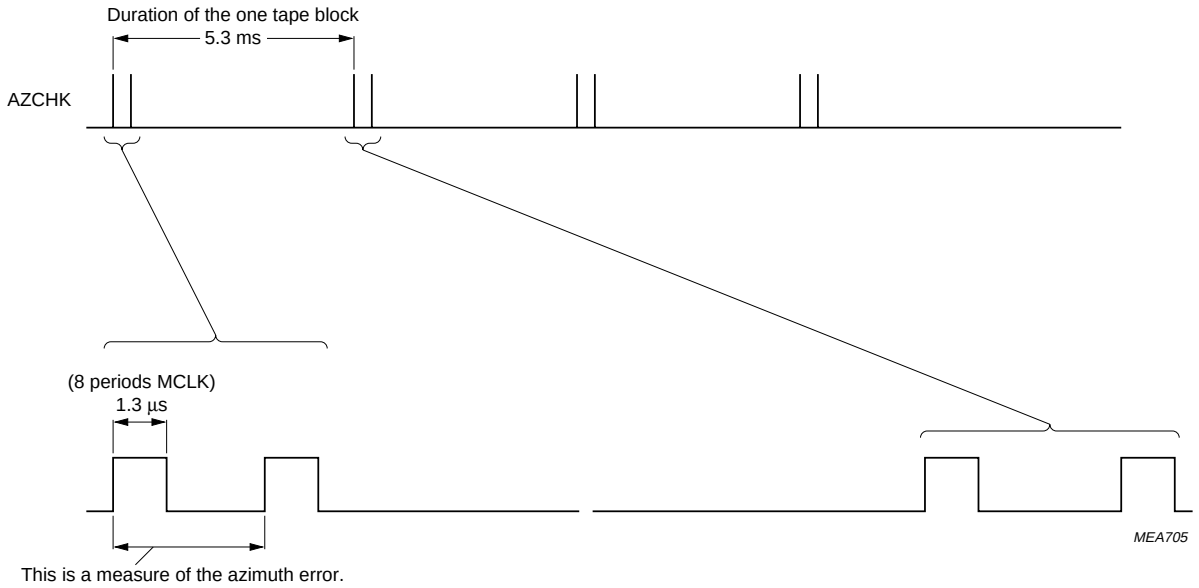
Supply pins

V_{DD1} TO V_{DD6}

These are the supply pins, all of these pins must be connected. We recommend that each power supply pin pair (i.e. V_{DD1} to V_{SS1}, V_{DD2} to V_{SS2}, etc.) be decoupled using a 22 nF capacitor as close as is physically possible to the pins of the SAA3323.

V_{SS1} TO V_{SS6}

These are the supply ground pins, all of which must be connected.



Nominal Inter Frame Gap (IFG) lasts 660 µs.

Fig.25 AZCHK timing.

V_{DD7}

This is the supply pin for the output buffers to the data lines of the system RAM. It should always be connected externally. Decouple this pin with a 22 nF capacitor to the V_{SS7} pin.

V_{SS7}

This is the ground supply pin for the output buffers of the data lines of the system RAM. This pin is connected internally to all the supply ground pins (V_{SS1} to V_{SS6}), however it should always be connected externally.

Auxiliary envelope detection

INTMASK

INTMASK is a interrupt mask register. This register sets the mode of operation for the interrupt interface, and is writable only.

Table 22 Interrupt mask register.

BIT	7	6	5	4	3	2	1	0
Meaning	BP1	BP0	Vup(1)	AEup(2)	AEdn(3)	Lup(4)	Ldn(5)	ECZ(6)
Default	0	0	0	0	0	0	0	0

Notes

1. Vup ≡ rising edge of VIRGIN interrupt.
2. AEup ≡ rising edge of AUX envelope interrupt.
3. AEdn ≡ falling edge of AUX envelope interrupt.
4. Lup ≡ rising edge of LABEL interrupt.
5. Ldn ≡ falling edge of LABEL interrupt.
6. ECZ ≡ AUX envelope counter has just reached zero interrupt.

BP1 AND BP0 (BYPASS)

If any of the bypass bits are HIGH then the interrupts are not passed on to the microcontroller, instead the level of the corresponding signal is available an the interrupt pin.

Table 23 BP1 and BP0.

BP		EFFECT OF BYPASS
1	0	
0	0	no bypass
0	1	LAB on L3INT pin; note 1
1	0	AENV on L3INT pin; note 2
1	1	VIR on L3INT pin; note 3

Notes

1. LAB = LABEL (HIGH if a LABEL condition is detected in the envelope of the AUX channel).
2. AENV = envelope of the AUX channel (1 bit binary).
3. VIR = VIRGIN (indicated by the total [continuous] absence of signal on the AUX channel).

The AUX envelope information is only valid when the digital equalizer is in search mode and when the tape speed is between the values of
3 to 48 × nominal tape speed. The timing relationships between the AUX channel input signal, AENV, LAB and VIR are shown in Figs 26 to 28. The delays t_{d1} and t_{d2} are between 0.25 and $0.5t_{AUX}$ (AUX envelope periods). The delays t_{d3}, t_{d4}, t_{d5} and t_{d6} are between 2 and $6t_{AUX}$ (AUX envelope periods).

When using the digital equalizer in search mode first program the digital equalizer to search mode, then program the INTMASK register.

MASK

If the BP1 and BP0 bits are LOW then the mask bits take effect. Any combination of the mask bits may be HIGH, enabling the corresponding interrupts. The interrupt pin L3INT is active LOW when used for interrupts and active HIGH when used for bypassing. So if it is not in bypass mode and at least one of the interrupts has occurred it will go LOW and stays LOW until DEQ status byte 0 has been read. Extra interrupts that occur after the first interrupt and before the DEQ status byte 0 is read are seen in the status register. Extra interrupts that occur after the status byte

has been read will generate a new interrupt. Interrupts that are already noted in the digital equalizer Status 0 are cleared by reading it.

Table 24 Digital equalizer STATUS0.

BIT	7	6	5	4	3	2	1	0
Meaning	BKSW(1)	TEST	Vup(2)	AEup(3)	AEdn(4)	Lup(5)	Ldn(6)	ECZ(7)

Notes

1. BKSW (filter bank switched) indicates that the last main data coefficients sent to the digital equalizer have been activated.
2. Vup indicates whether an interrupt caused by the rising edge of VIRGIN has occurred.
3. AEup indicates whether an interrupt caused by the rising edge of AUX envelope has occurred.
4. AEdn indicates whether an interrupt caused by the falling edge of AUX envelope has occurred
5. Lup indicates whether an interrupt caused by the rising edge of LABEL has occurred.
6. Ldn indicates whether an interrupt caused by the falling edge of LABEL has occurred.
7. ECZ indicates that the AUX envelope counter has reached zero.

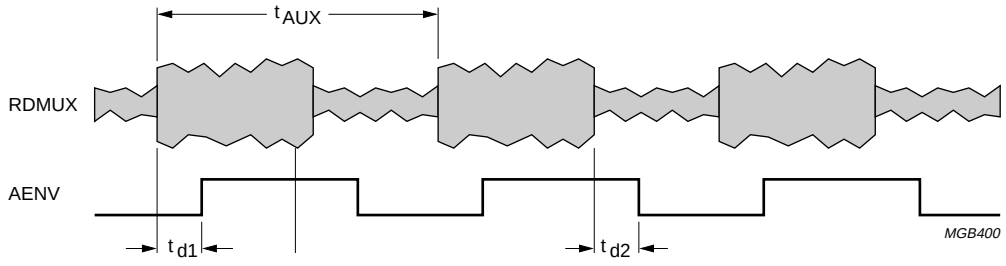


Fig.26 AUX channel envelope to AENV delays.

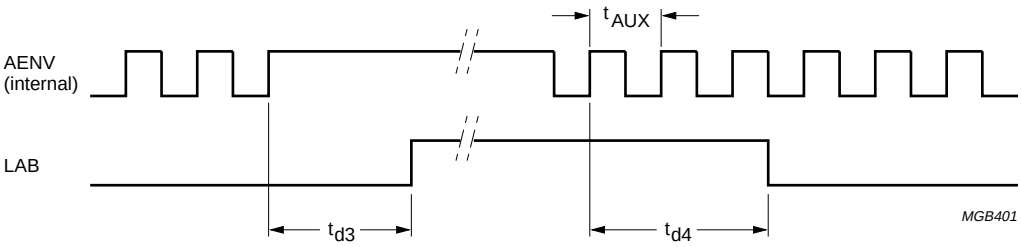


Fig.27 AENV to LAB delays.

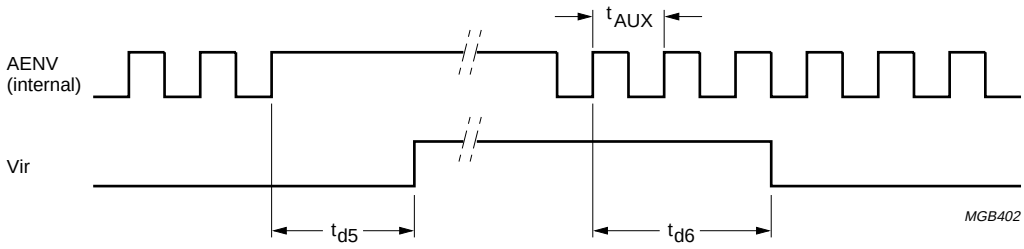


Fig.28 AENV to VIR delays.

Table 25 Digital equalizer STATUS1.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	–	–	VIR(1)	AENV(2)	LAB(3)

Notes

1. VIR gives the state of the VIRGIN signal.
2. AENV represents the state of the AENV signal.
3. LAB gives the state of the LAB signal.

AUX envelope count (AECNT) register

This 16 bit register is used for loading the AUX envelope counter and for reading the state of that counter, it is therefore readable and writable as 2 bytes. Least Significant Byte first.

Table 26 AECNT register.

AECNT	LEAST SIGNIFICANT BYTE								MOST SIGNIFICANT BYTE							
BIT	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Meaning	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8

Search speed (SSPD) register

$$\text{Search speed} = \left(2^{SR}\right) \times \left(\frac{51.2}{SV}\right) \times \text{normal speed}$$

Table 27 Search speed register.

BIT	7	6	5	4	3	2	1	0
Meaning	SVF(1)	SV4(2)	SV3(2)	SV2(2)	SV1(2)	SV0(2)	SR1(3)	SR0(3)

Notes

1. SVF speed validation flag, if HIGH then the search speed measurement is invalid.
2. SV4 to SV0 search speed value.
3. SR1 and SR0 search speed range.

ANAEYE register

Table 28 ANAEYE register analog eye pattern selection register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	AEN[1]	ACHN3[2]	ACHN2[2]	ACHN1[2]	ACHN0[2]
Default	0	0	0	0	0	0	0	0

Notes

1. AEN analog eye pattern output enable. If this bit is LOW the Digital-to-Analog Converter (DAC) is switched off and the output is HIGH.
2. ACHN3 to ACHN0 select channel for analog eye output.

Table 29 ACHN3 to ACHN0 channel selections for analog eye output.

ACHN				CHANNEL ON ANAEYE
3	2	1	0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	AUX

T1sel register

Table 30 T1SEL register CHTST1 pin selection register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	T1F2	T1F1	T1F0	T1C3	T1C2	T1C1	T1C0
Default	0	0	0	0	0	0	0	0

Table 31 T1C3 to T1C0 CHTST1 pin channel selections.

T1C				CHANNEL ON CHTST1
3	2	1	0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	AUX

Table 32 T1F2 to T1F0 CHTST1 pin function selections.

T1F			FUNCTION OF CHTST1 PIN
2	**1**	**0**	
0	0	0	off; logic 0
0	0	1	digital eye pattern
0	1	0	sliced data
0	1	1	bit clock
1	0	0	clock extraction frequency

The digital eye pattern is in 8 bits two's complement notation, the sliced data and the bit clock give the current binary state of the corresponding signals, and the clock extraction frequency output is in 8 bits offset binary format. The timing diagrams for the digital eye pattern output and the clock extraction frequency output are shown in Fig.29.

T2sel register

Table 33 T2SEL register CHTST2 pin selection register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	T2F2	T2F1	T2F0	T2C3	T2C2	T2C1	T2C0
Default	0	0	0	0	0	0	0	0

Table 34 T2C3 to T2C0 CHTST2 pin channel selections.

T2C				CHANNEL ON CHTST2
3	**2**	**1**	**0**	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	AUX

Table 35 T2F2 to T2F0 CHTST2 pin function selections.

T2F			FUNCTION OF CHTST2 PIN
2	**1**	**0**	
0	0	0	off; logic 0
0	0	1	digital eye pattern
0	1	0	sliced data
0	1	1	bit clock
1	0	0	clock extraction frequency

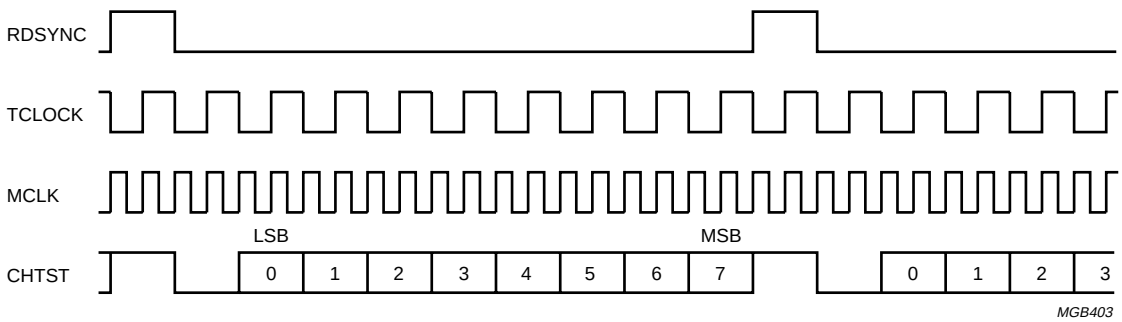


Fig.29 CHTST1 and CHTST2 output timing.

Table 36 DEQSET digital equalizer settings.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	–	–	ACup(1)	DM1	DM0
Default	0	0	0	0	0	0	0	0

Note

1. ACup is the AUX envelope counter direction is up. This setting caused the AUX envelope counter increment or to decrement by 1 every rising edge of the AUX envelope signal AENV.

DM1 and DM0

Table 37 DM1 and DM0 digital equalizer mode of operation.

DM		MODE OF OPERATION OF DIGITAL EQUALIZER
1	0	
0	0	normal(1)
0	1	search(2)
1	0	off(3)
1	1	off(3)

Notes

1. In normal mode the main data channels and the AUX channel are processed (equalized), the AUX channel envelope information is not processed.
2. In search mode only the AUX channel is processed by the digital equalizer.
3. Off means that the digital equalizer is put to sleep (low power), this can be used for example in portable recording equipment. RDSYNC is HIGH if off mode. Also note that the other digital equalizer registers are not addressable while the digital equalizer is in off mode.

CLKSET

Table 38 CLKSET clock extraction settings.

BIT	7	6	5	4	3	2	1	0
Meaning	LEAE[1]	FR1	FR0	GNOR	GE1	GE0	RD1	RD0
Default	1	0	0	1	1	0	1	0

Note

1. LEAE (leakage enable): this setting enables a leakage function in the PLL clock extraction loop filter. This gives a slightly improved performance with high SER tapes at the cost of a slight decrease in dynamic performance. For home (static) applications program this bit to logic 1 and for portable applications to logic 0.

Table 39 FR1 and FR0 clock extraction frequency range control.

FR		EFFECT ON PLL FREQUENCY LOOP
1	0	
0	0	range ±8%
0	1	range ±16%
1	0	range ±22%
1	1	range ±28%

Note that in the (FR = 0) range the clock extraction stays in its normal range only, hence it does not enter the extended range.

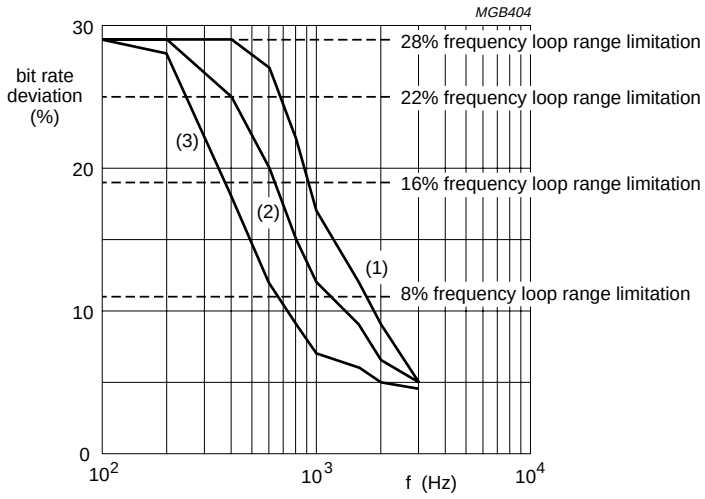
Figure 30 shows the lock characteristic of the clock extraction PLL.

Table 40 GNOR gain in normal frequency range mode of clock extraction.

GNOR	EFFECT ON GAIN IN NORMAL RANGE
0	gain 2; for portable (mobile) applications
1	gain 1; for home (static) applications

Table 41 GE1 and GE0 gain in extended frequency range mode of clock extraction.

GE		EFFECT ON PLL GAIN IN EXTENDED RANGE
1	0	
0	0	gain 2
0	1	gain 3
1	0	gain 4
1	1	gain 5; do not use



(1) Gain 4.
(2) Gain 3.
(3) Gain 2.

Fig.30 Clock extraction PLL lock characteristic.

RD1 and RD0 return delay

This is the delay before returning to normal mode after being in ‘extended range mode’ (i.e. the number of consecutive channel clock bit periods where the bit clock frequency falls within the normal range before the clock extraction returns to normal frequency mode).

Table 42 RD1 and RD0 return delay.

RD		DELAY IN BITS TO RETURN TO NORMAL MODE
1	**0**	
0	0	64
0	1	128
1	0	256
1	1	512

SYSINFO and AUX data offsets in the SAA3323

AUX data consists of 4 blocks of 36 bytes, one block being transferred in each (n) time segment.

The 128 bytes in each tape frame contain SYSINFO. The SYSINFO bytes can for convenience, be considered as being grouped into 4 SYSINFO blocks with:
SYSBLK0 → SI0 to SI31, SYSBLK1 → SI31 to SI63, etc.

In modes DPAP and DRAR SYSINFO transfers may occur in two ways:

1. 4 blocks of 36 bytes, one block being transferred to the SAA3323 in each time segment.
2. 1 block of 128 bytes being transferred in time segment 1.

In mode DRAR SYSINFO must be transferred as 4 blocks of 32 bytes, one block in each segment.

Figures 31 to 34 show the offsets between the SYSINFO and AUX and the time segment counter, for the various modes of operation of the SAA3323.

Table 43 Block offsets with respect to time segment.

MODE	DESCRIPTION
DPAP	SYSBLK = (SNUM + 3) MOD4; or read all 4 SYSINFO blocks when SNUM = logic 0; if AUX and main were recorded simultaneously then AUXBLK = (SNUM + 1) MOD4; else read and interpret 1 AUX block in each time segment.
DRAR	SYSBLK = SNUM; AUXBLK = (SNUM + 1) MOD4
DPAR	SYSBLK = (SNUM + 3) MOD4; or read all 4 SYSINFO blocks when SNUM = logic 0

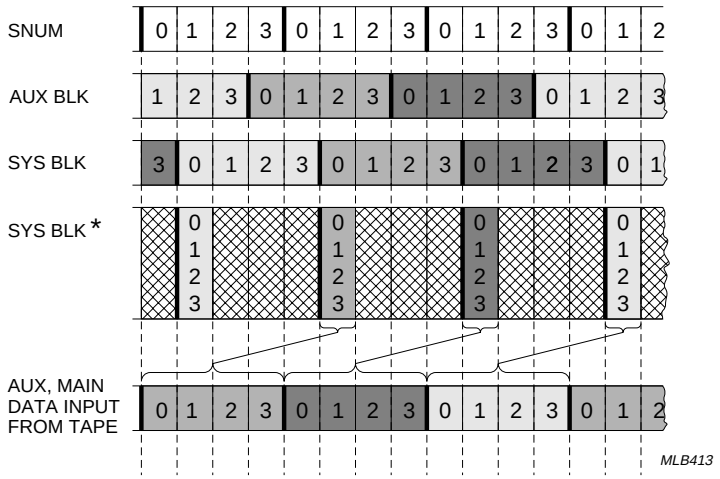


Fig.31 SYSINFO and AUX block delays in DPAP mode; audio and AUX simultaneously recorded.

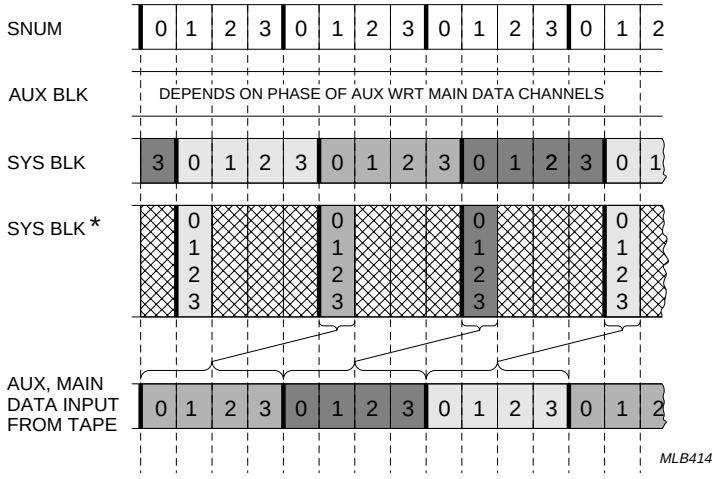


Fig.32 SYSINFO and AUX block delays in DPAP mode; audio and AUX separately recorded.

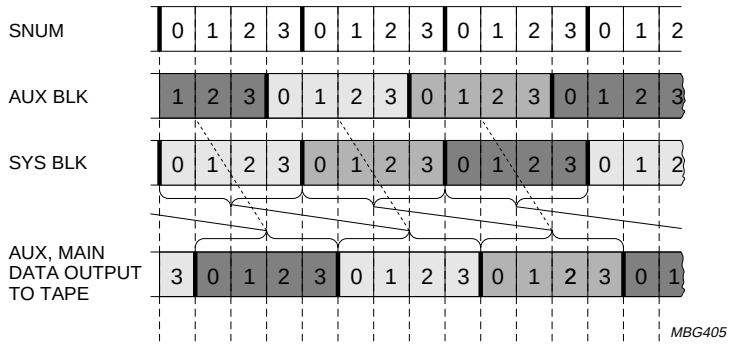


Fig.33 SYSINFO and AUX block delays in DRAR mode.

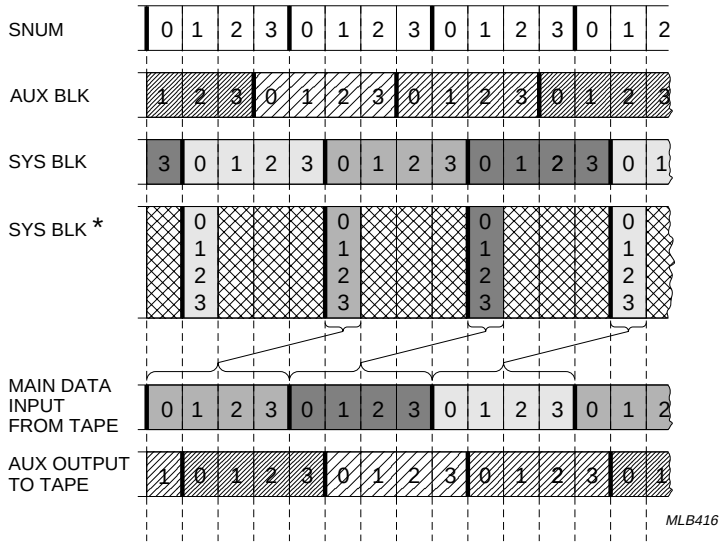


Fig.34 SYSINFO and AUX block delays in DPAR mode.

Scratch pad RAM

The SAA3323 provides the microcontroller with a scratch pad RAM that the microcontroller can use for whatever it likes. The size of the scratch pad depends upon the size and type of RAM used with the SAA3323. The locations in the scratch pad RAM may be written and read in 8 bit or 12 bit units.

The RAM may be viewed as having up to 4 quarters, the availability of these quarters for the scratch pad RAM is given in Table 44.

Table 44 Availability of RAM quarters for the scratch pad RAM.

RTYPE		TYPE OF RAM USED	AVAILABLE RAM QUARTERS YZ[1]
1	**0**		
0	0	DRAM 64K × 4	00
0	0	DRAM 256K × 4	00, 01, 10 and 11
0	1	SRAM 32K × 8 fast	00
1	0	SRAM 128K × 8 fast	00, 01, 10 and 11
1	1	SRAM (2×) 32K × 8 slow	00
1	1	SRAM 128K × 8 slow	00 and 10

Note

1. In RAM quarter YZ = 00, the scratch pad is arranged as 6 pages, where each page consists of 7 columns × 64 rows. The pages are numbered **0 to 5**, the columns **1 to 7** and the rows **0 to 63**. This gives a total of (6 × 7 × 64) 2688 locations.

   In each of the RAM quarters YZ = 01, 10 and 11 the scratch pad is arranged as 6 pages where each page consists of 8 columns × 448 rows. The pages are numbered **0 to 5**, the columns **0 to 7** and the rows **0 to 447**. This gives then a total of (6 × 8 × 448) 21504 locations per RAM quarter YZ.

During communication with the scratch pad RAM, the RAM quarter YZ is chosen when sending the RDDRAC, RDWDRAC, WRDRAC or WRWDRAC commands to the TFE module.

Use of the scratch pad RAM outside the specified ranges is not allowed and it may upset the operation of the SAA3323.

As with SYSINFO and AUX transfers can occur at high speed at all times except the second half of time segment 0, that is when the status bit SLOWTFR is HIGH. When SLOWTFR is HIGH the microcontroller must poll the status bit RFBT to investigate when a transfer can occur.

Two addressing modes are available for the scratch pad, namely random access and auto-increment. For random access mode the address of each location is sent by the microcontroller to the SAA3323 before each location transfer. For auto-increment mode the address of the first location is sent by the microcontroller before the first location transfer, auto-incrementing of the row occurs then for all transfers until the end of the column.

The 8 bit transfers are initiated by the WRDRAC and RDDRAC commands, these transfers are each 1 byte per memory location, therefore the byte counter will increment after each byte transfer.

The 12 bit transfers are initiated by the WRDRAC and RDDRAC commands, these transfers are each 2 bytes per memory location. The first byte contains the 4 Most Significant Bits (MSBs) of the memory location in its 4 Least Significant Bits (LSBs) positions. The other bit positions being ‘don’t care’. The second byte contains the 8 LSBs of the memory location. The byte counter is incremented after the transfer of the second byte.

The RACCNT and BYTCNT registers are used for addressing the scratch pad.

For RAM quarter YZ = 00 the mapping of the scratch pad RAM address onto the RACCNT and BYTCNT registers is shown in Table 45.

Table 45 Mapping of scratch pad RAM address for RAM quarter YZ = 00.

REGISTER	RACCNT							BYTCNT							
BIT	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	P2	P1	P0	C2	C1	C0	1	1	R6	R5	R4	R3	R2	R1	R0

For The other three quarters of the RAM the mapping of the scratch pad RAM address onto the RACCNT and BYTCNT registers is shown in Table 46.

Table 46 Mapping of scratch pad RAM address for RAM quarter YZ = 01, 10 and 11.

REGISTER	RACCNT							BYTCNT							
BIT	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Value	P2	P1	P0	C2	C1	C0	R8	R7	R6	R5	R4	R3	R2	R1	R0

Mode changes

The possible mode changes for the TFE are shown in Table 47.

Table 47 Mode changes.

CURRENT MODE	NEW MODE		
	DPAP	**DRAR**	**DPAR**
DPAP	–	yes	yes
DRAR	yes	–	no
DPAR	yes	no	–

TIMING FOR SAA3323 MODE CHANGES

Mode change DPAP to DRAR

This mode change occurs at the end of the time segment in which the TFE module receives the new settings. Writing of the first Main and AUX data to tape starts at the start of the time segment 1 which occurs 2 ‘end of time segment 3’ s after the mode change. The delay to writing to tape is approximately 222 ms, as shown in Fig.35.

If ‘seamless appending’ is required the new settings should be sent to the TFE module during time segment 2.

Mode change DPAP to DPAR

This mode change occurs at the first end of time segment 2 after the TFE module receives the new settings. Output of AUX to tape begins at the start of the following time segment 1, (i.e. approximately 85.3 ms after the mode change), as shown in Fig.36.

Mode change DRAR to DPAP

This mode change occurs at the first end of time segment 0 after the TFE module receives the new setting. Writing of Main and AUX data stops immediately after the mode change.The time segment jumps back to logic 0, URDA goes HIGH and stays HIGH for 5 time segments (i.e. approximately 213.3 ms) after which it goes LOW, as shown in Fig.37.

Mode change DPAR to DPAP

This mode change occurs at the first end of time segment 0 after the TFE module receives the new setting. The writing of AUX data to tape stops immediately after the mode change. The first AUX read from tape can be expected during the following time segment 0 or 1 (i.e. approximately 128 to 170.67 ms after the mode change), as shown in Fig.38.

Mode change DPAP to search

This mode change occurs almost instantaneously, program the digital equalizer module in SAA3323 to go to search mode, then program the interrupt mask register to select the required type of interrupt.

Mode change search to DPAP

This mode change occurs almost instantaneously, program the interrupt mask register to disable interrupts program the digital equalizer module of SAA3323 to go to normal mode. A re-synchronization will most likely occur when as result of the data being read from tape, thus causing URDA to go HIGH.

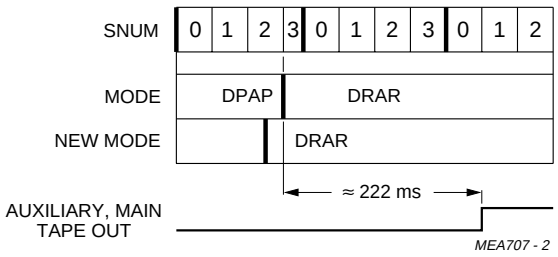


Fig.35 Mode change to DRAR.

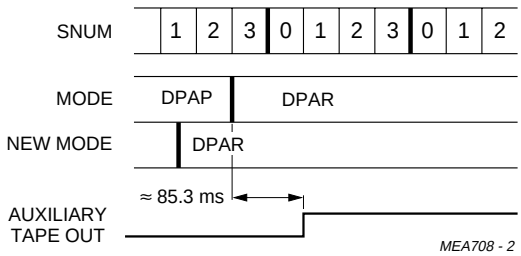


Fig.36 Mode change to DPAR.

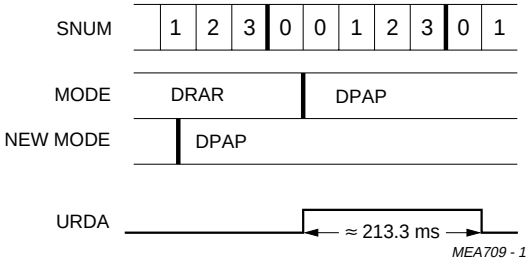


Fig.37 Mode change from DRAR.

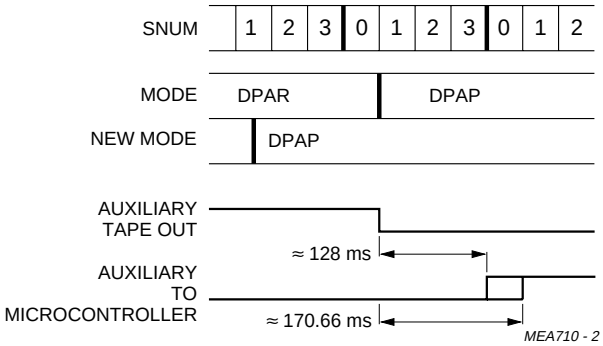


Fig.38 Mode change from DPAR.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		2.7	3.6	V
V_I	input voltage	note 1	–0.5	V_{DD} + 0.5	V
I_I	input current		–10	+10	mA
V_O	output voltage		tbf	tbf	V
I_O	output current		–20	+20	mA
I_{DD}	supply current		–	100	mA
I_{SS}	supply current		–100	–	mA
P_{tot}	total power dissipation		–	500	mW
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{es1}	electrostatic handling	note 2	–2000	+2000	V
V_{es2}	electrostatic handling	note 3	–200	+200	V

Notes

1. The input voltage must not exceed maximum supply voltage unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	tbf	3.6	V
I_{DD}	supply current	digital plus analog; see Fig.39	–	28.1	–	mA
		inputs with internal pull-down to V_{SS}; all other inputs to V_{SS} or V_{DD}	–	–	100	µA
Inputs CLK24, L3CLK, L3MODE, PINI, SLEEP and SBMCLK						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_I	input current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA
Inputs TEST0, TEST1 and TEST2						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_I	input current	$V_I = V_{DD}$; T_{amb} = 25 °C	25	–	400	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input RESET						
V_{tLH}	positive-going threshold		–	–	$0.8V_{DD}$	V
V_{tHL}	negative-going threshold		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis (V_{tLH} to V_{tHL})		–	$0.3V_{DD}$	–	V
Outputs AZCHK, CHTST1, CHTST2, ERCOSTAT, L3INT, $\overline{\text{L3REF}}$, MCLK, PINO3, RDSYNC, SBDIR, SBEF, URDA, TCLOCK and WDATA						
V_{OH}	HIGH level output voltage	I_O = 1 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –1 mA	–	–	0.4	V
Outputs A0 to A8, A9/$\overline{\text{CAS}}$, A10/$\overline{\text{RAS}}$, $\overline{\text{OEN}}$ and $\overline{\text{WEN}}$						
V_{OH}	HIGH level output voltage	I_O = 2 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –2 mA	–	–	0.4	V
Outputs SPEED and PINO2						
V_{OH}	HIGH level output voltage	I_O = 1 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –1 mA	–	–	0.4	V
I_{OZ}	3-state leakage current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA
Inputs/outputs SBCL, SBDA and SBWS						
V_{OH}	HIGH level output voltage	I_O = 1 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –1 mA	–	–	0.4	V
V_{IL}	LOW level input voltage	outputs in 3-state	–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	outputs in 3-state	$0.7V_{DD}$	–	–	V
I_{OZ}	3-state leakage current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA
Inputs/outputs A11 to A16 and L3DATA						
V_{OH}	HIGH level output voltage	I_O = 2 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –2 mA	–	–	0.4	V
V_{IL}	LOW level input voltage	outputs in 3-state	–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	outputs in 3-state	$0.7V_{DD}$	–	–	V
I_{OZ}	3-state leakage current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA
Inputs/outputs D0 to D7						
V_{OH}	HIGH level output voltage	I_O = 4 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_O = –4 mA	–	–	0.4	V
V_{IL}	LOW level input voltage	outputs in 3-state	–	–	0.8	V
V_{IH}	HIGH level input voltage	outputs in 3-state	2	–	–	V
I_{OZ}	3-state leakage current	V_I = 0 V to V_{DD}; T_{amb} = 25 °C	–10	–	+10	µA

Average current consumption

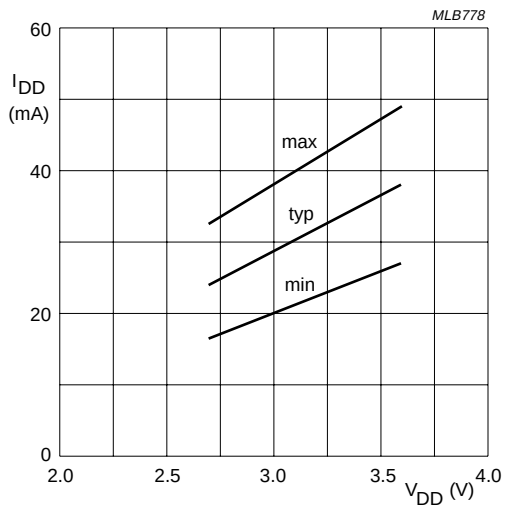


Fig.39 Average current consumption.

AC CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; T_{amb} = –40 to +85 °C; C_L = 10 pF on all outputs; see Fig.40; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock inputs						
C_I	input capacitance		–	–	10	pF
CLK24						
f_{CLK24}	clock frequency		24	24.576	25	MHz
t_{24L}	pulse width LOW		12	–	–	ns
t_{24H}	pulse width HIGH		12	–	–	ns
SBMCLK						
f_{SBMCLK}	clock frequency			6.144	12.5	MHz
t_{SCL}	pulse width LOW		30	–	–	ns
t_{SCH}	pulse width HIGH		30	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock output MCLK						
C_L	load capacitance		–	–	20	pF
t_d	delay time from SLEEP HIGH to SLEEP active		–	20	–	ns
f_{MCLK}	clock frequency			6.144	6.25	MHz
t_{MCL}	MCLK pulse width LOW		50	–	–	ns
t_{MCH}	MCLK pulse width HIGH		50	–	–	ns
t_{pd}	propagation delay time from rising edge of CLK24		–	–	65	ns
Inputs						
C_I	input capacitance		–	–	10	pF
L3CLK, L3MODE AND RESET						
t_{su}	set-up time to rising edge of MCLK		35	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
PINI						
t_{su}	set-up time to rising edge of MCLK		60	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
Outputs						
C_L	load capacitance		–	–	20	pF
A0 TO A8						
t_{pd}	propagation delay time from falling edge of CLK24		–	–	50	ns
A9/$\overline{\text{CAS}}$, A10/$\overline{\text{RAS}}$ AND $\overline{\text{OEN}}$						
t_{pd}	propagation delay time from falling edge of CLK24		–	–	50	ns
t_d	delay time from SLEEP HIGH to SLEEP active		–	20	–	ns
$\overline{\text{WEN}}$						
t_{pd}	propagation delay time					
	from falling edge of CLK24		–	–	50	ns
	from falling edge of $\overline{\text{WEN}}$ to rising edge of CLK24	long write pulse mode	–	–	50	ns
t_d	delay time from SLEEP HIGH to SLEEP active		–	20	–	ns
AZCHK, CHTST1, CHTST2, L3INT, PINO3, RDSYNC, SBEF AND WDATA						
t_{pd}	propagation delay time from rising edge of MCLK		–	–	45	ns
ERCOSTAT, $\overline{\text{L3REF}}$, SBDIR, SPEED, PINO2, URDA AND TCLOK						
t_{pd}	propagation delay time from rising edge of MCLK		–	–	55	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs/outputs						
C_I	input capacitance		–	–	10	pF
C_L	load capacitance		–	–	20	pF
A11 TO A16						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{pd}	propagation delay time from falling edge of CLK24		–	–	55	ns
D0 TO D3						
t_d	delay time from SLEEP HIGH to SLEEP active		–	20	–	ns
t_{su}	set-up time to falling edge of CLK24		5	–	–	ns
t_h	hold time from falling edge of CLK24		15	–	–	ns
t_{pd}	propagation delay time					
	from falling edge of CLK24		–	–	50	ns
	from rising edge of CLK24	early write mode	–	–	50	ns
D4 TO D7						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{su}	set-up time to falling edge of CLK24		5	–	–	ns
t_h	hold time from falling edge of CLK24		15	–	–	ns
t_{pd}	propagation delay time					
	from falling edge of CLK24		–	–	50	ns
	from rising edge of CLK24	early write mode	–	–	50	ns
L3DATA						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{su}	set-up time to rising edge of MCLK		35	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
t_{pd}	propagation delay time					
	from rising edge of MCLK		–	–	50	ns
	from L3MODE		–	–	45	ns
SBCL AND SBWS						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{su}	set-up time to rising edge of MCLK		40	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
t_{pd}	propagation delay time					
	from rising edge of SBMCLK		–	–	60	ns
	from rising edge of MCLK (3-state control)		–	–	55	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SBDA						
t_d	delay time from SLEEP HIGH to SLEEP active		–	25	–	ns
t_{su}	set-up time to rising edge of MCLK		35	–	–	ns
t_h	hold time from rising edge of MCLK		0	–	–	ns
t_{pd}	propagation delay time from rising edge of MCLK		–	–	55	ns

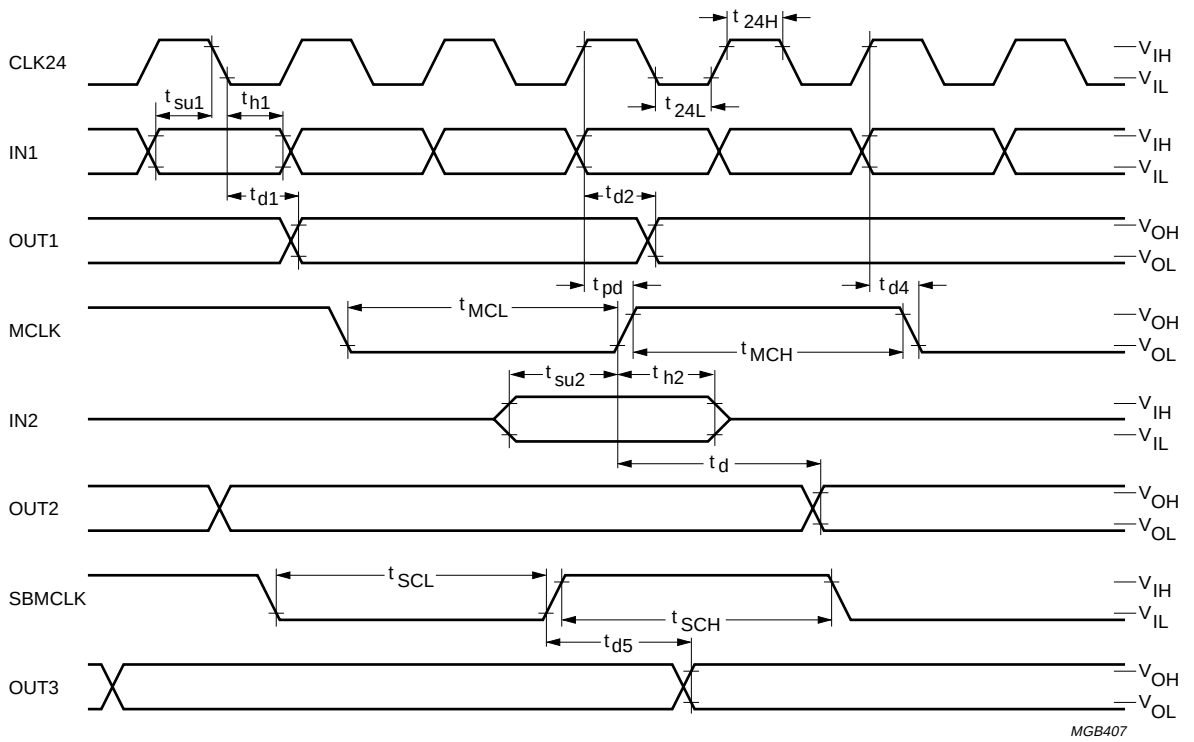


Fig.40 Timing for AC characteristics.

ADC CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; T_{amb} = –40 to +85 °C; C_L = 10 pF on TCLOCK output; see Fig.41; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	AC RDMUX ADC resolution		–	8	–	bits
$V_{ref(p)}$	positive reference voltage		–	–	V_{DD} – 0.5	V
$V_{ref(n)}$	negative reference voltage		0	–	–	V
ΔV_{ref}	$V_{ref(p)}$ to $V_{ref(n)}$		2.0	–	–	V
Z_i	input impedance	$V_{ref(p)}$ to $V_{ref(n)}$	700	1200	1500	Ω
		$V_{ref(n)}$ to V_{SS}	–	650	–	Ω
C_I	input capacitance (RDMUX)		–	–	15	pF
I_I	input current		–	–	90	μA
DNL	differential non-linearity		–	–	±0.99	LSB
S/(THD+N)	signal-to-total harmonic distortion plus noise ratio	–20 dB (FS); 100 to 500 kHz	24	–	–	dB
Timing						
T_{cy}	cycle time of CLK24		40	–	–	ns
t_{d1}	TCLOCK delay time from rising edge of CLK24	C_L = 10 pF	–	–	80	ns
t_{su}	RDMUX set-up time to falling edge of CLK24	Z_{source} < 150 Ω	60	–	–	ns
t_h	RDMUX hold time from falling edge of CLK24		40	–	–	ns

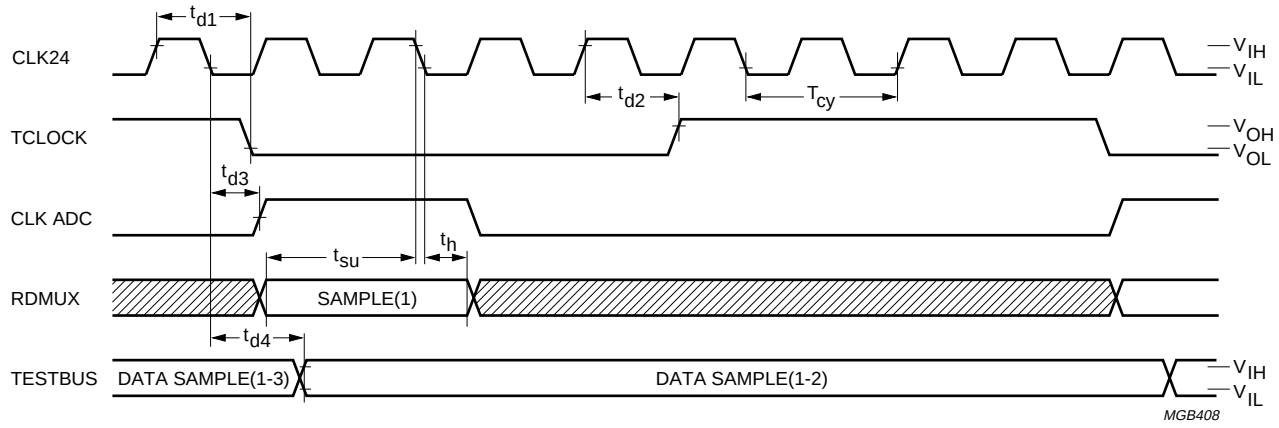


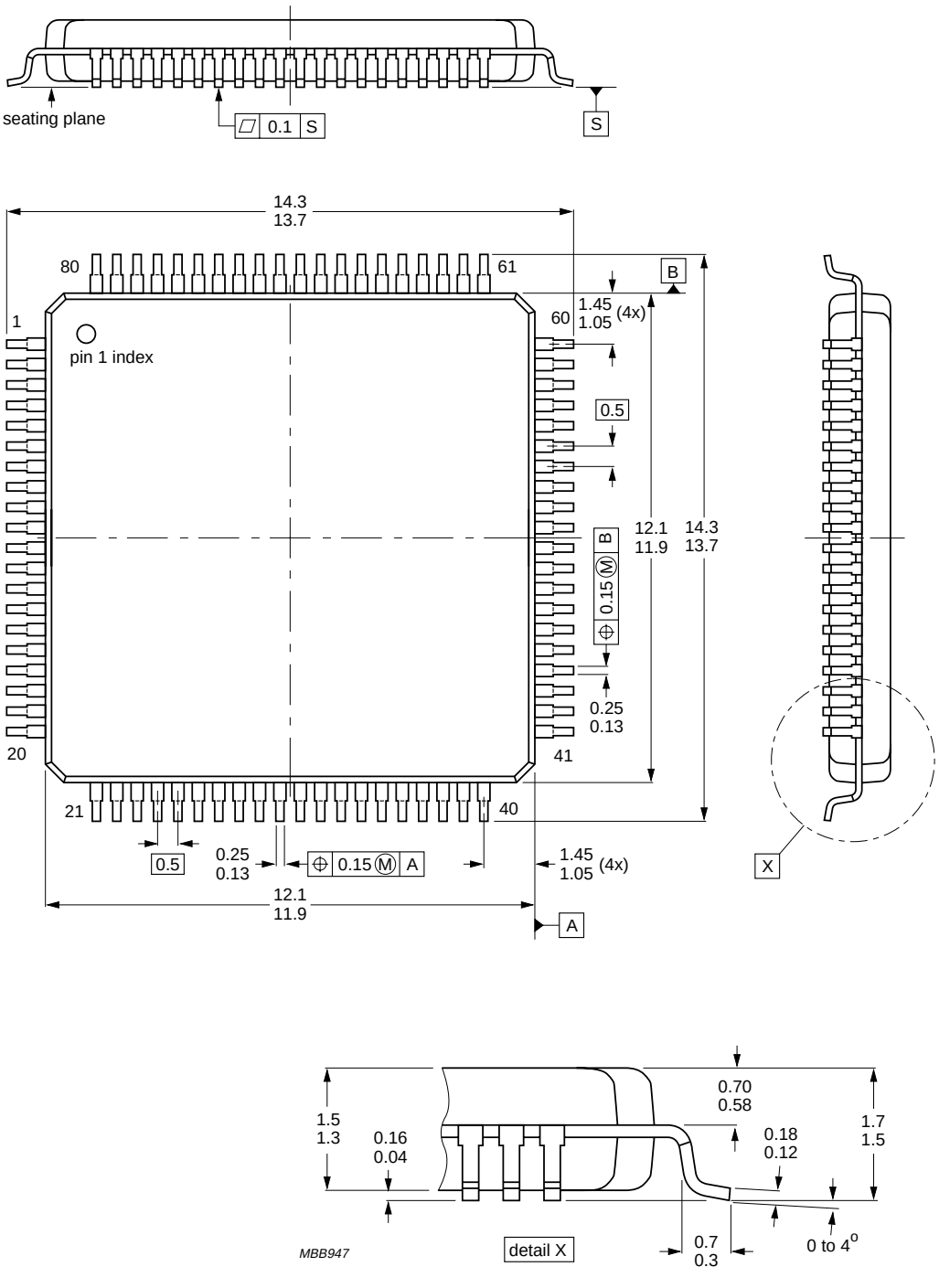
Fig.41 ADC timing.

DAC CHARACTERISTICS

V_{DD} = 2.7 to 3.6 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

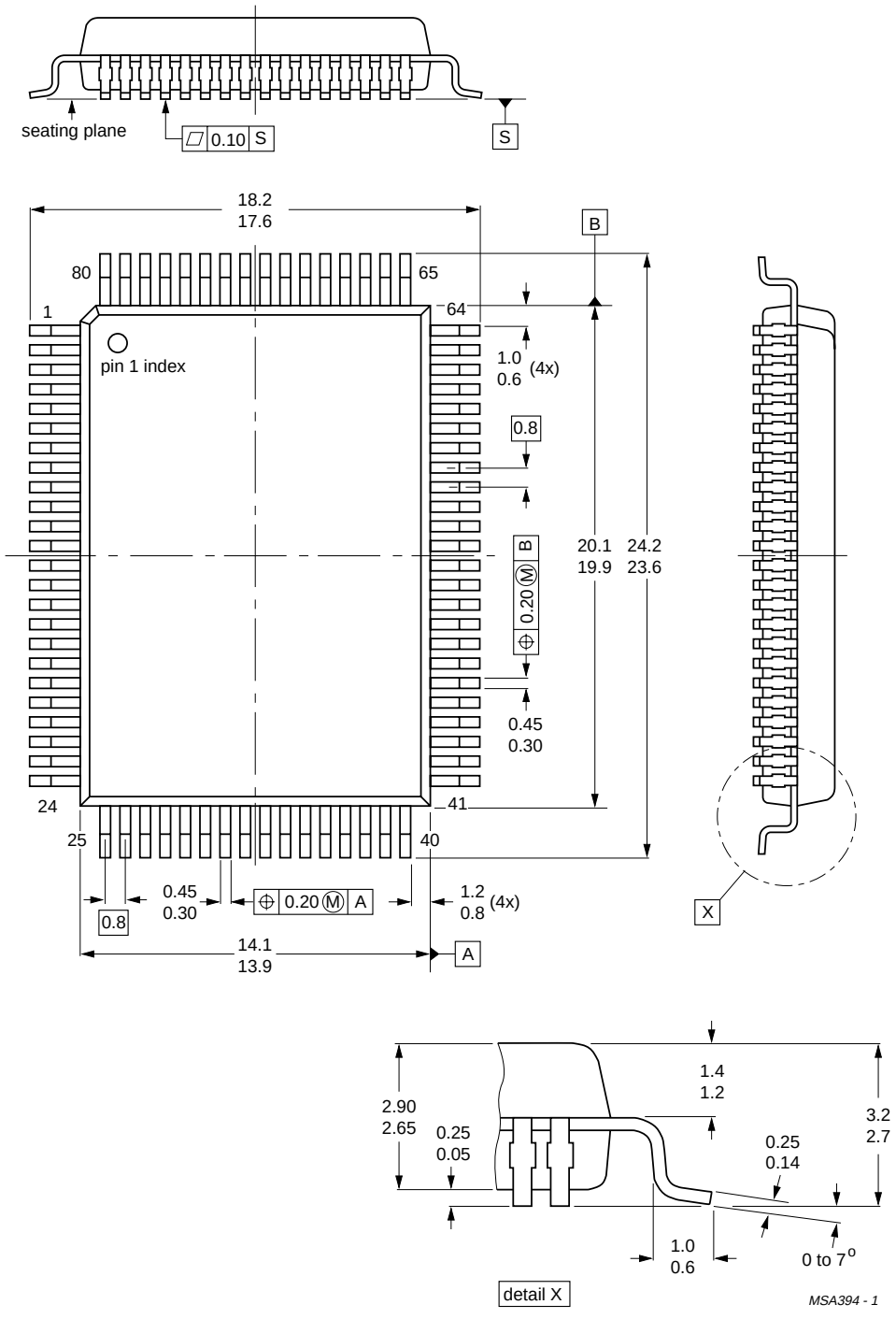
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	DIGEYE/ANAEYE resolution		–	6	–	bits
V_o	ANAEYE output voltage	Z_L > 1 MΩ	–	(V_{DD} – 1.1) to V_{DD}	–	V

PACKAGE OUTLINES



Dimensions in mm.

Fig.42 Plastic thin quad flatpack; 80 leads; body 12 × 12 × 1.4 mm (SOT315-1; TQFP80).



Dimensions in mm.

Fig.43 Plastic quad flatpack; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height (SOT318-2; QFP80).

SOLDERING

Plastic quad flatpacks

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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